

AM335x Starter Kit Hardware

This document provides the design information on the AM335x processor based starter kit (TMDSSK3358).

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1 Introduction

The AM335x Starter Kit (TMDSSK3358) can be used as an evaluation and development platform for low cost AM335x based solutions and networking platforms. The embedded emulation logic allows emulation and debug using standard development tools such as TI's Code Composer Studio by just using the supplied USB cable. It is not intended for use in end products. All of the design information is freely available and can be used as the basis for the development of an AM335x-based product.

2 EVM System View

TMDSSK3358 is partitioned into two different boards: the main board (processor, peripherals and the main power supply) and the LCD Carrier board (LCD and touch screen). The TMDSSK3358 main board and the LCD carrier board mounted are mounted together using 10 mm standoffs. The TMDSSK3358 main board has dimensions of 5.257" x 2.798" and that of the LCD Carrier board is 4.963" x 2.798". The top and the bottom side views of the TMDSSK3358 are shown in [Figure 1](#).

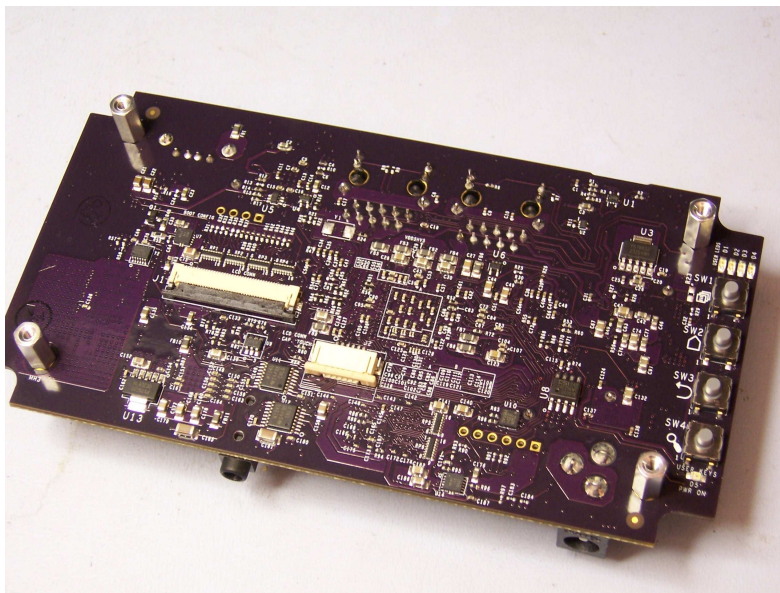


Figure 1. TMDSSK3358 Top View

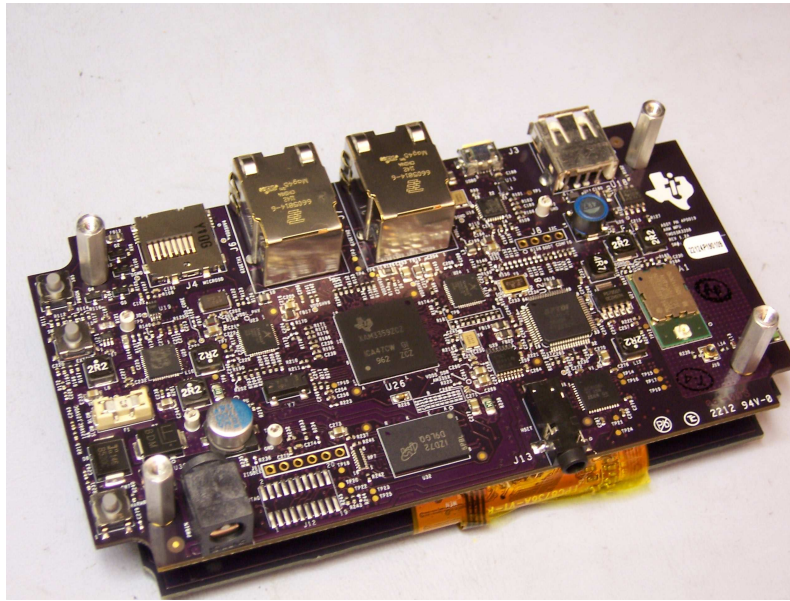


Figure 2. TMDSSK3358 V1.2B Bottom View

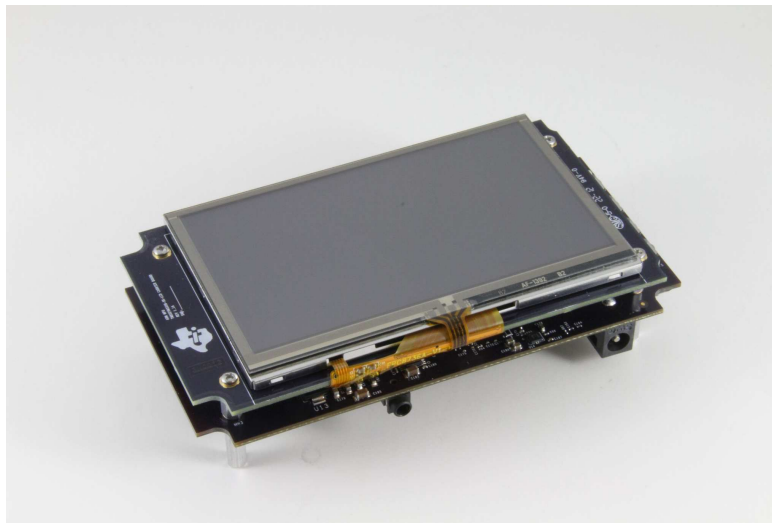


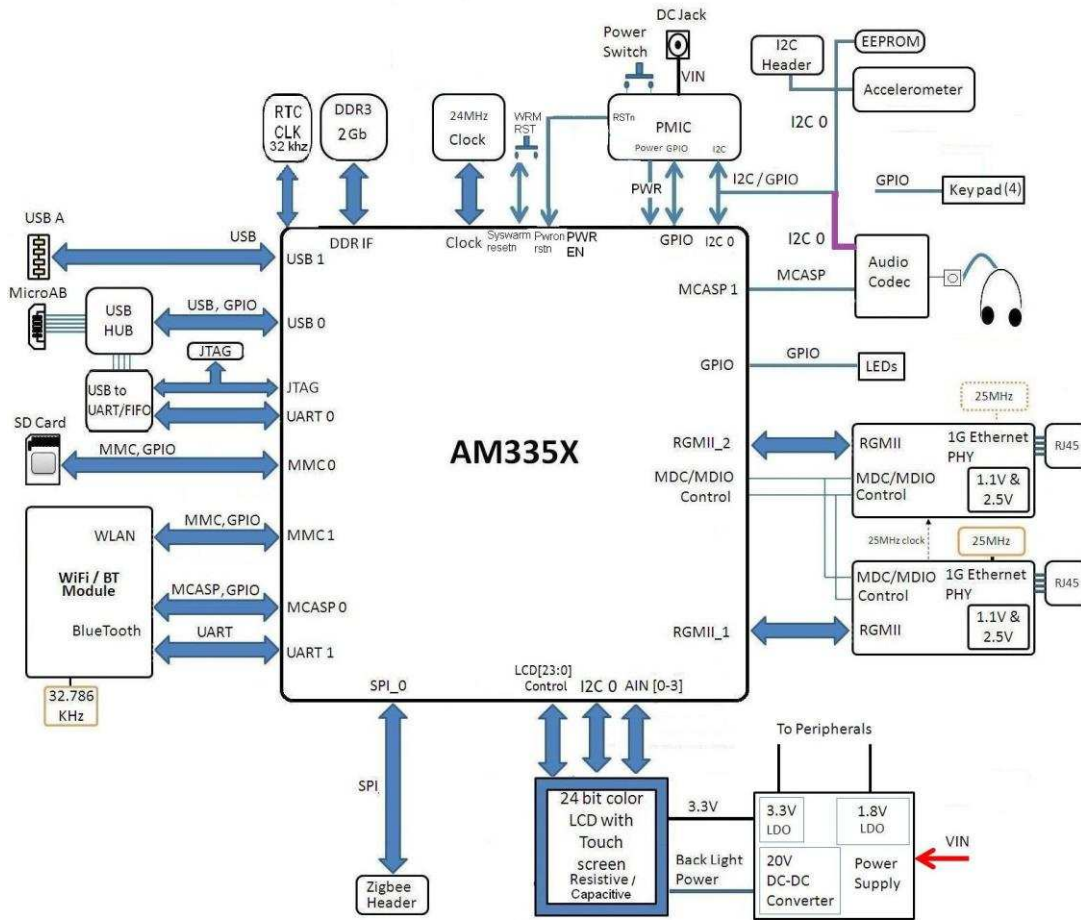
Figure 3. TMDSSK3358 System View

2.1 Schematics/Design Files

Hardware Documentation - Schematics, Design Files, and other related Hardware Documentation

3 Functional Block Diagram

This section describes about the major functional blocks of the TMDSSK3358. The functional block diagram of the TMDSSK3358 design is shown in Figure 4.



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Figure 4. TMDSSK3358 Block Diagram

3.1 Processor

The AM3358ZCZ processor is the central processor for TMDSSK3358. All the resources on the board surround the AM3358 processor to provide development capabilities for hardware and software. See the AM3358 datasheet and TRM for the details about the processor.

There are system configuration signals, SYSBOOT, that can be set on the EVM to define some startup parameters on the AM335x processor. For more details, see Section 3.6.

3.2 Clocks

The main clock for the processor is derived from a 24 MHz crystal. An on-board oscillator in the AM3358 generates the base clock and subsequent module clocks as needed within the AM3358 processor. A 32 kHz clock for the RTC on the AM3358 is derived from a 32 kHz crystal on board.

3.3 Reset Signals

Power On Reset to the AM335x is driven by the PMIC. SYS_WARMRESETn is a signal running to several peripherals and AM335x which performs a reset on those peripherals. SYS_WARMRESETn is asserted by a pushbutton on the main board and is used to force a reset of the AM335x. AM335x can also pull down on the RESET_INOUTn signal to cause the SYS_WARMRESETn line to go active. The RTC_PORZ reset signal for the RTC section is derived using AND Gates.

3.4 Power

The power input to TMDSSK3358 is from a 5V Power Supply. This 5 V power is provided as power input to the Power Manager TPS65910A3. The power requirements of the processor are taken care of by the Power Manager IC TPS65910A3. The Power ON LED "D5" is ON if the PMIC output power VAUX33 is available (to indicate the active status of the PMIC). The power sequencing requirements of the AM335X processor are handled automatically by the TPS65910A3 PMIC. For more information, see [AM335x Sitara™ Processors Data Sheet](#).

NOTE: When powering the TMDSSK3358 EVM, always use the supplied power supply (CUI/V-Infinity Part Number EMSA050300-P6P-SZ, Model 3A-182WP05) or equivalent model having output voltage of +5VDC and output current max 3.0 Amps. A power supply is not included with the kit.

3.5 Power Management IC

TMDSSK3358 uses the TPS65910A3 power management IC. The I2C0 on AM335x is used to control the TPS65910A PMIC.

The PWRON input of PMIC is connected to an external push-button. The built-in debouncing time defines a minimum button press duration that is required for button press detection. Any button press duration which is lower than this value is ignored, considered an accidental touch.

For AM335x, the following power supplies from the TPS65910A are used.

Table 1. Power Supplies to AM335x From TPS65910A3 PMIC

TPS65910 Power Supply/Other Sources	AM335x Power Rail	Voltage
VAUX2 (300 mA)	VDDSHV6 (300mA)	3.3 V
VMMC (300 mA)	VDDSHV2,3,4,5 (300 mA), VDDA3P3V_USB0/1 (10 mA)	3.3 V
VDD2 SMPS (1500 mA)	VDD_CORE (1000 mA)	1.1 V
VDD1 SMPS (1500 mA)	VDD_MPU (1500 mA)	1.2 V
No supply needed	VDD_RTC	1.1 V
VRTC (External LDO)	VDDS_RTC (10 mA)	1.8 V
VIO_SMPS (1000 mA)	VDDS_DDR (200 mA)	1.5 V
VIO_SMPS (1000 mA)	DDR_VREF (10 mA)	0.9 V
VDAC (150 mA)	VDDS (100mA)	1.8 V
VDIG1 (300 mA)	VDDSHV1	1.8 V
VDIG2 (300 mA)	VDDS_SRAM_CORE_BG (40 mA)	1.8 V
VDIG2 (300 mA)	VDDS_SRAM_MPU_BB (40 mA)	1.8 V
VDIG2 (300 mA)	VDDS_PLL_DDR (25 mA)	1.8 V
VDIG2 (300 mA)	VDDS_PLL_CORE_LCD (25 mA)	1.8 V
VDIG2 (300 mA)	VDDS_PLL_MPU (25 mA)	1.8 V
VDIG2 (300 mA)	VDDS_OSC (10 mA)	1.8 V
VAUX1 (300 mA)	VDDA1P8V_USB0/1 (50 mA)	1.8 V
VPLL (50 mA)	VDDA_ADC	1.8 V
VDD3 SMPS (100 mA)	Not Used	-

3.6 Configuration/Setup

3.6.1 Boot Configuration

Various boot configurations can be set using the pull up / down resistor combinations provided on the SYS_BOOT pins (LCD_DATA0..15). Boot configuration pins are latched upon de-assertion of PORz pin.

The default settings for the TMDSSK3358 is 01_00XX_XXXX_XX11_0111b. This corresponds to a boot sequence of:

- MMC0
- SPI0
- UART0
- USB0

For more details, see the TMDSSK3358 schematic. For the definitions of each of the sysboot signals, see the [AM335x Sitara™ Processors Data Sheet](#) and the [AM335x and AMIC110 Sitara™ Processors Technical Reference Manual](#).

3.6.2 I2C Port Address Assignments

Information on I2C address assignments are provided in [Table 2](#).

Table 2. I2C Bus Addresses

AM335x Starter Kit (TMDSSK3358) Function	AM335x I2C Port	Address
Baseboard ID memory	I2C0	0x50
AM335x PMIC Control	I2C0	0x2D
AM335x PMIC Smart Reflex Control	I2C0	0x12
Accelerometer Control	I2C0	0x18
Audio Codec	I2C0	0x1B
Capacitive Touch screen	I2C0	0x38

3.7 Memories Supported

The TMDSSK3358 design supports on-board memories like DDR3 SDRAM and Board ID EEPROM. It also supports an SD card socket.

3.7.1 DDR3 SDRAM

DDR3 SDRAM memory design is provided by using a 2 Gb single chip solution (MT41J128M16JT-125) from Micron. It is internally configured as a 16 Meg x 16 x 8 bank memory. A separate Regulator to supply the DDR reference power to the AM335x and the VTT termination voltage to the termination components is provided in the design. The VIO_SMPS output from the PMIC is programmed to provide the required 1.5 V to the DDR3 SDRAM.

3.7.2 Board Identity Memory

The board contains a serial EEPROM with the board specific data that allows the processor to automatically detect which board is connected and the version of that board. Other hardware specific data can be stored in this memory as well. The part number of the memory device used is CAT24C256WI-GT3. For details on the data in this memory, see [Section 3.6](#).

Table 3. I2C Configuration

Name	Size	Contents
Header	4	MSB 0xEE3355AA LSB
Board Name	8	Name for board in ASCII "A335X_SK" = AM335x TMDSSK3358Board
Version	4	Hardware version code for board in ASCII "1.2B" = rev. 01.2B
Serial Number	12	Serial number of the board. This is a 12 character string which is: WWYY4P19nnnn where: WW = 2 digit week of the year of production YY = 2 digit year of production nnnn = incrementing board number
Configuration Option	32	Codes to show the configuration setup on this board. For the available EVM's supported, the following codes are used: ASCII "SKU#00" = default configuration Remaining 26 bytes are reserved
Available	32720	Available space for other non-volatile codes/data

3.7.3 SD/MMC0

The Micro SD/MMC0 port is provided with a card socket SCHA5B0200. This is a standard Micro SD/MMC Card type of connector which is of the low profile compact type. It is connected to the MMC0 port of the AM335x processor. Check the AM335x data sheet and TRM for supported card types/densities. 8Gb SD cards are tested with this design. The pin assignment is as shown in [Table 4](#).

Table 4. SD/MMC0 Connector Pin Details

Pin Number	Memory Card PIN Number
uSD#1	DAT2
uSD#2	CD/DAT3
uSD #3	CMD
uSD #4	VCC
uSD #5	CLK
uSD #6	GND
uSD #7	DAT0
uSD #8	DAT1
uSD #9	GND
uSD #10	CD

3.8 Ethernet

TMDSSK3358 has two Giga bit Ethernet transceivers. AR8031-AL1A from Atheros is used as a single port, tri speed PHY. A single 3.3 V is enough to power this PHY and the other voltages required were generated internally. Reset for both the chips are driven by the SYS_WARMRESETn signal through a SN74LVC1G07 buffer. Both the PHYs have individual 25 MHz, 50 ppm crystal as their clock source. The 25 MHz Clock out of the EMAC1-PHY port has been connected to the XTLI of the EMAC2-PHY as an optional clock input.

NOTE: The Starter Kit EVM PCB does not support external delay for the clock signals on the RGMII interface. The AR8031A PHY can be setup to use internal clock delay mode once booting is complete. Therefore, there may be problems in function/performance when booting in Gb mode or when running Gb Ethernet Mode before the AR8031A PHY is configured properly. For more information, see [Appendix A](#).

For both the PHYs, mode selection pins MODE [3:0] are set as “0000” to operate it in 1000 BASE-T, RGMII mode. The PHY address for the EMAC1-PHY and EMAC2-PHY are 00100 and 00101 respectively. The interrupts from the both PHYs are connected to both the non maskable interrupt pin and to the processor GPIO pins.

The Wake On LAN interrupts from the both PHYs are connected to the EXT_WAKEUP signal of the processor as an option.

Table 5. 10/100/1000 Ethernet1 Pin Details

Pin Number	Signal Name	Description
1	DGND	Ground
2	NC	No connect
3	ETHER_D3P	MDI 3 POSITIVE
4	ETHER_D3N	MDI 3 NEGATIVE
5	ETHER_D2P	MDI 2 POSITIVE
6	ETHER_D2N	MDI 2 NEGATIVE
7	ETHER_D1P	MDI 1 POSITIVE
8	ETHER_D1N	MDI 1 NEGATIVE
9	ETHER_D0P	MDI 0 POSITIVE
10	ETHER_D0N	MDI 0 NEGATIVE
D1	PHY_LED_ACTn	PHY ACTIVITY LED signal
D2	GND	Ground
D3	GND	Ground
D4	PHY_LED_1000n	1000 Base-T LINK LED signal

3.9 USB

3.9.1 USB to UART/JTAG

Micro AB USB port is provided as an upstream port of the USB HUB USB2412. This is used for USB to JTAG and USB to UART conversion applications through the downstream port 1 of the HUB. FT2232L is used for the USB to UART and JTAG conversion applications. The Downstream port 2 of the Hub is connected to USB port 0 of the AM335x.

The USB to UART/JTAG converter (FT2232L) has 32 configurable multifunction pins. A 16 bit, serial EEPROM 93LC56B from MicroChip is used to store the configuration data. Some of the pins from ADBUS [7:0] and ACBUS [7:0] are configured as JTAG and Reset signals. These JTAG pins from the FT2232 IC are connected to the dedicated processor JTAG pins and as well to the optional JTAG connector.

The Micro AB USB pin out details are provided in [Table 6](#).

Table 6. Micro AB – USB0

Pin Number	Signal Name	Description
1	USB_DC	USB BUS VOLTAGE
2	USBDM_UP	USB DATA MINUS
3	USBDP_UP	USB DATA PLUS
4	NC (USB_ID)	No connect
5	DGND	Ground

3.9.2 USB 1

The USB port1 of the AM335x is connected to the USB type A connector. USB power (5V)is provided to this connector through a buck-boost converter circuit.

Table 7. USB A Type – USB1

Pin Number	Signal Name	Description
1	VUSB_VBUS1	USB BUS VOLTAGE
2	USB1_CONN_DM	USB1 DATA MINUS
3	USB1_CONN_DP	USB1 DATA PLUS
4	DGND	Ground

3.10 Audio Codec

The TLV320AIC3106 is a low-power stereo audio codec with stereo headphone amplifier from TI. CLKOUT1 of the processor is sourcing the master clock of the codec (24 Mhz). The CODEC I2C is capable of supporting both the standard and fast modes. I2C address of the codec is configured as 0011011. MCASP1 interface of the processor is connected to the audio interface of the codec. The stereo audio output is terminated in a stereo headphone Jack. The pinout assignments for the headset jack are provided in [Table 8](#).

Table 8. Headset Jack

Pin Number	Signal	Description
1	AGND_AUD	Analog Ground
3	HS_SPKRP	Headset stereo LOUT
10	NC	No Connect
2	HD_SPKRP	Headset stereo ROUT

3.11 WLAN

WLAN is no longer populated or supported on the AM335x Starter Kit. For TI WLAN support, consider using the AM335x EVM (TMDXEVM3358) along with WiLink8 module (WL1835MODCOM8B) which is sold separately.

3.12 User LEDs

The Four User LEDs implemented are D1-D4 in the user panel area. These are driven by the GPIOs from the AM335x.

All of the user LEDs are green in color.

3.13 User Keys

This design has four user keys (SW1, SW2, SW3 and SW4): three of them connect directly to the GPIO bank2 of the processor (Keys 2,3 and 4) and one of them (Key 1) connects to the GPIO bank0 of the processor.

3.14 Accelerometer

The LIS331DLH is an ultra low-power high performance three axes linear accelerometer used in TMDSSK3358 board. The accelerometer is mounted closer to the center of the board as to allow the most useful/dynamic data. The accelerometer is connected via I2C0 of the processor. The I2C(0) address is 0011000b.

4 Pin Use Description

The Pin use description file provides us the information on the pin functionality mode selected. The pin mux utility file is found here [Pin Mux Data File \[2\]](#)

4.1 GPIO Definitions

See the updated pinmux document [Pin Mux Description \[3\]](#), which shows the use case columns for GPIOs.

5 Board Expansion Connectors

The SPI0 and the I2C0 ports are extended through the connectors J11 and J8, respectively. SPI0 Expansion header pinout is provided in [Table 9](#).

Table 9. SPI0 Expansion Header

Pin Number	Signal	Description
1	V3_3D	Power 3.3V supply
2	AM335X_SPI0_CS0	SPI0 Chip Select 0
3	AM335X_SPI0_D1	SPI0 Data 1
4	DGND	Ground
5	AM335X_SPI0_SCLK	SPI0 Clock
6	AM335X_SPI0_D0	SPI0 Data 0

I2C0 Expansion header is provided in [Table 10](#).

Table 10. I2C0 Expansion Header

Pin Number	Signal	Description
1	DGND	Ground
2	AM335X_I2C0_SDA	I2C0 DATA
3	AM335X_I2C0_SCL	I2C0 Clock
4	V3_3D	Power 3.3V supply

6 LCD

TFT color LCD module from Newhaven Display NHD-4.3-480272MF-ATXI#-T-1 with resistive touch screen should be used as the LCD display for the TMDSSK3358 design. It is 4.3 inches wide and it has a built in driver and no controller is required. It has 480 X 272 pixels and supports up to 16.7M colors. This LCD supports white LED backlight. 24bit RGB signals, control signals and Resistive touch screen signals are terminated in a flex PCB with a 40 pin connector that fits into the TMDSSK3358 main board using a mating connector.

40 pin LCD connector pinout is provided in [Table 11](#).

Table 11. LCD Connector

Pin Number	Signal	Description
1	LED-	Backlight LED power supply GND
2	LED+	Backlight LED power supply voltage
3	DGND	Ground
4	VCC	3.3V LCD Power Supply
5	R0	Red Data0
6	R1	Red Data1
7	R2	Red Data2
8	R3	Red Data3
9	R4	Red Data4
10	R5	Red Data5
11	R6	Red Data6
12	R7	Red Data7
13	G0	Green Data0
14	G1	Green Data1
15	G2	Green Data2
16	G3	Green Data3
17	G4	Green Data4
18	G5	Green Data5
19	G6	Green Data6
20	G7	Green Data7
21	B0	Blue Data0
22	B1	Blue Data1
23	B2	Blue Data2
24	B3	Blue Data3
25	B4	Blue Data4
26	B5	Blue Data5
27	B6	Blue Data6
28	B7	Blue Data7
29	GND	Ground
30	PCLK	Data Sample clock signal
31	DISP	Display ON/OFF signal
32	HSYNC	Line Sync signal
33	VSYNC	Frame Sync signal
34	DE	Data enable
35	AVDD	No connect
36	GND	Ground
37	XR	Touch Panel Right
38	YD	Touch Panel Down
39	XL	Touch Panel Left
40	YU	Touch Panel Up

7 References

1. http://processors.wiki.ti.com/images/f/fe/TMDSSK3358_1_2A_PinMux_data.zip
2. http://processors.wiki.ti.com/images/8/82/TMDSSK3358_1.2A_PinMux_Description.zip
3. *AM335x Sitara™ Processors Data Sheet*
4. *AM335x and AMIC110 Sitara™ Processors Technical Reference Manual*

AM335x Starter Kit EVM Errata

This section contains the known exceptions and usage notes to the functional specifications for the AM335x Starter Kit EVM.

A.1 Revision 1.2 Usage Notes and Known Design Exceptions

Usage notes highlight and describe particular situations where the device's behavior may not match presumed or documented behavior. This may include behaviors that affect device performance or functional correctness. These notes may be incorporated into future documentation updates for the device (such as the device-specific data manual), and the behaviors they describe may or may not be altered in future device revisions.

Advisory numbers are used to describe known design exceptions and may not be sequential. Some advisory numbers may be moved to the next revision and others may have been removed because the design exception was fixed or documented in the device-specific data manual or peripheral user's guide. When items are moved or deleted, the remaining numbers remain the same and are not re-sequenced.

A.2 Revision 1.2B Usage Notes

None

A.3 Revision 1.2 Known Design Exceptions to Functional Specifications

Table 12 lists known design exceptions to functional specifications for General Purpose EVM revision 1.2. Advisories are numbered in the order in which they were added to this document. If the design exceptions are still applicable, the advisories move up to the latest EVM revision section. If the design exceptions are no longer applicable or if the information has been documented elsewhere, those advisories are removed. Therefore, advisory numbering in this section may not be sequential.

Table 12. Summary of Instructions

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Advisory 2.2.2 Oscillator Power Supply Decoupling Capacitor —	14
Advisory 2.2.3 CLKOUT Used as Source Clock —	14

Advisory 2.2.1 RGMII Ethernet Operation

Revision(s) Affected: 1.2B/1.2C

Details While the AM335x Starter Kit EVM has 2 Gb Ethernet PHY's, AR8031A's, on the board, the PCB was designed to use internal clock delay mode of the RGMII interface and the AM335x does not support the internal clock delay mode. Therefore, if operating the Ethernet in Gb mode, there may be problems with the performance/function due to this. The AR8031A PHY supports internal delay mode. This can be enabled by software to guarantee Gb operation. However, this cannot be done to enable internal delay mode for Ethernet booting.

Workaround Enable the internal clock delay mode in the AR8031A PHY using software after boot occurs.

Advisory 2.2.2 Oscillator Power Supply Decoupling Capacitor

Revision(s) Affected 1.2B/1.2C

Details The AM335x Starter Kit EVM has a decoupling capacitor that is connected to the oscillator power supply on the board. This capacitor is connected to the incorrect ground. Instead of GND_OSC0 (local crystal ground), it should be connected to the main power ground DGND.

Workaround Remove capacitor C95 and replace it so that it is connected to VDDS_OSC and DGND.

Advisory 2.2.3 CLKOUT Used as Source Clock

Revision(s) Affected 1.2B/1.2C

Details The AM335x GP EVM uses a CLKOUT1 signal from the AM335x device to source the input clock for the audio CODEC. The CLKOUT signals from the AM335x should not be used for input clock sources that have stringent jitter requirements.

Workaround Remove resistor R1528 on the board and connect an external 12MHz clock oscillator as an input to U37.

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1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an "EVM" or "EVMs") to the User ("User") in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.
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 - 2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.
3. *Regulatory Notices:*
 - 3.1 *United States*
 - 3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.
 - 3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

3.3 Japan

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_02.page
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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive):*

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

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8. *Limitations on Damages and Liability:*

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10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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