EVM User's Guide: AM263P1, AM263P1-Q1, AM263P2, AM263P2-Q1, AM263P4, AM263P4-Q1

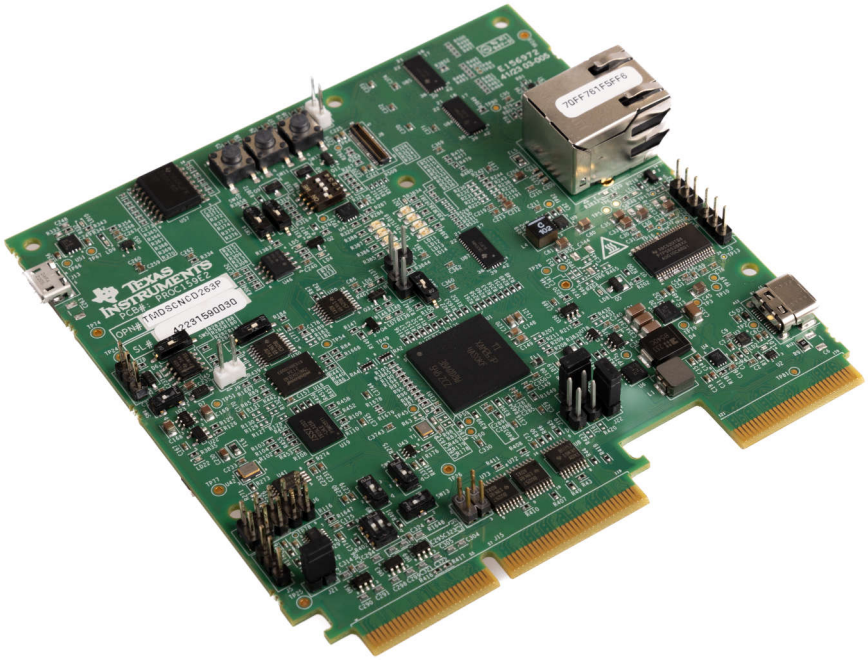
AM263Px Control Card Evaluation Module

Description

The AM263Px Control Card Evaluation Module (EVM) is an evaluation and development board for the Texas Instruments Sitara™ AM263Px series of microcontrollers (MCUs). This EVM provides an easy way to start developing on the AM263Px MCUs with on-board emulation for programming and debugging as well as buttons and LED for a simple user interface. The control card also enables header pin access to key signals through the use of a high speed edge connector (HSEC) baseboard docking station for rapid prototyping.

Features

- Powered through 5 V, 3 A USB type-C input
- Multirail power supply designed for safety-relevant applications
- One RJ45 Ethernet ports with on-board Industrial Ethernet PHY
- Additional Ethernet add-on board connector for an automotive or industrial Ethernet PHY
- On-board XDS110 debug probe
- 180 pin HSEC interface for rapid prototyping
- Three push buttons:
  - PORz
  - User interrupt
  - RESETz
- LEDs for:
  - Power status
  - User testing
  - Ethernet connection
  - I2C driven array
- CAN connectivity with on-board CAN transceiver
- Hardware resolver for accelerated motor position sensing with two additional SAR ADC's
- Dedicated FSI connector
- TI test automation header
- MMC interface to micro SD card connector
- On-board memory
  - 1 GB QSPI NAND flash
  - 256 MB OSPI NOR flash
  - 1 MB I2C EEPROM



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1 Evaluation Module Overview

1.1 Introduction

The AM263Px Control Card was developed to enable easy and rapid prototyping of the AM263Px and all of the peripherals. There are several on-board transceiver and PHYs to enable the many interfaces of the AM263Px SoC (System on a Chip). This user's guide details the design of the EVM and how to properly use each interface. The user's guide also details many important aspects of the board including but not limited to pin header descriptions, test points, and mux/switch signal routing.

Preface: Read This First

1.1.1.1 Sitara MCU+ Academy

Texas Instruments offers the *MCU+ Academy* as a resource for designing with the MCU+ software and tools on supported devices. The MCU+ Academy features easy-to-use training modules that range from the basics of getting started to advanced development topics.

1.1.1.2 Important Usage Notes

Note

The E1 version of the AM263Px Control Card only includes signal routing for the PRU-ICSS MDIO. To make use of the CPSW MDIO, blue-wire modifications need to be made. **Without the blue-wire fix, the ethernet PHY connected to the RGMII2 interface does not function properly with the on-board ethernet PHY**. **As a result of the blue-wire fix, the TCAN1043 (U29) cannot be used simultaneously with the on-board ethernet PHY.** For additional information, refer to Section 5.1.A.

Note

The AM263Px Control Card requires a 5 V, 3 A power supply to function. While a USB type-C cable is included, A 5 V, 3 A power supply is not included in the kit and must be ordered separately The *Belkin USB-C Wall Charger* is known to work with the Control Card and supplied type-C cable. For more information on power requirements, refer to Section 2.2. If there is an insufficient power input, then the red LED (LD1) glows. For more information on power status LEDs, refer to Section 2.2.2.

Note

TMDSCNCD263P includes a PMIC U7, which can exceed 55℃ case temperature during normal operation. This user guide's statement and the PCB warning sticker from the table below have been added to alert users to these higher temperature components.

	Caution	Hot surface. Contact can cause burns. Do not touch!

Note

External power supply or power accessory requirements:

- Nominal output voltage: 5-VDC
- Max output current: 3000 mA
- Efficiency Level V

Note

TI recommends using an external power supply or accessory which complies with applicable regional safety standards such as (by example) UL, CSA, VDE, CCC, PSE.

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1.2 Kit Contents

The Sitara AM263Px Control card development kit contains the following items:

- AM263Px Sitara series control card development board
- Type-A to Micro-B USB cable (1 meter length)
- USB Type-C cable (1 meter length)

Note

The maximum length of the IO cables shall not exceed 3 meters.

Not included:

- HSEC 180-pin Baseboard Docking Station
- Standoffs
- USB Type-C 5-V/3-A AC/DC supply and cable

1.3 Device Information

The AM263Px Sitara Arm® Microcontrollers are built to meet the complex real-time processing needs of next generation industrial and automotive embedded products. The AM263Px MCU family consists of multiple pin-to-pin compatible devices with up to four 400 MHz Arm® Cortex™-R5F cores. As an option, the Arm R5F subsystem can be programmed to run in lockstep or dual-core mode for a multiple functional safety configurations. The industrial communications subsystem (PRU-ICSS) enables integrated industrial Ethernet communication protocols such as PROFINET®, TSN, Ethernet/IP™, EtherCAT™ (among many others), standard Ethernet connectivity, and even custom I/O interfaces. The family is designed for the future of motor control and digital power applications with advanced analog sensing and digital actuation modules.

The multiple R5F cores are arranged in cluster subsystems with 256KB of shared tightly coupled memory (TCM) along with 3MB of shared SRAM, greatly reducing the need for external memory. Extensive ECC is included for on-chip memories, peripherals, and interconnects for enhanced reliability. Granular firewalls managed by the Hardware Security Manager (HSM) enable developers to implement stringent security-minded system design requirements. Cryptographic acceleration and secure boot are also available on AM263Px devices.

For additional information, refer to the AM263Px data sheet (SPRSP81).

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1.3.1 HSEC 180-pin Control Card Docking Station

The *TMDSHSECDOCK 180-pin docking station* is available for purchase through Texas Instruments. The docking station is a baseboard that enables rapid prototyping. There is a power switch on the docking station that determines whether power to the control card is supplied by the 5 V connector or USB connector.

Note

The docking station power switch must to be toggled to the EXT-ON side to meet the power requirements of the AM263Px Control Card. EXT-ON indicates that the power is being sourced from the Barrell connector of the Control Card Dock. The mini-USB (USB-ON) connector does not meet the power requirements of the AM263Px Control Card.

The AM263Px Control Card has a power mux (TPS2121RUXT) that supplies power from the type-C connection as long as the voltage supplied by the type-C connection is equal to or greater than the voltage supplied by the HSEC docking station. Therefore, if both a type-C connection is present and the control card is connected to a powered HSEC docking station, then the power mux routes the type-C supplied voltage to VMAIN of the control card. If there is no type-C connection and voltage is being supplied through the HSEC docking station, then the power mux routes that voltage to VMAIN of the control card.

For more information on the docking station, refer to the *Informational Guide*.

1.3.2 Security

The AM263Px Control Card features a High Security, Field Securable (HS-FS) device. An HS-FS device has the ability to use a one time programming to convert the device from HS-FS to High Security, Security Enforced (HS-SE).

The AM263Px device leaves the TI factory in an HS-FS state where customer keys are not programmed and has the following attributes:

- Does not enforce the secure boot process
- M4 JTAG port is closed
- R5 JTAG port is open
- Security Subsystem firewalls are closed
- SoC Firewalls are open
- ROM Boot expects a TI signed binary (encryption is optional)
- TIFS-MCU binary is signed by the TI private key

The One Time Programmable (OTP) keywriter converts the secure device from HS-FS to HS-SE. The OTP keywriter programs customer keys into the device eFuses to enforce secure boot and establish a root of trust. The secure boot requires an image to be encrypted, which is optional, and signed using customer keys, which is verified by the SoC. A secure device in the HS-SE state has the following attributes:

- M4, R5 JTAG ports are both closed
- Security subsystems and SoC firewalls are both closed
- TIFS-MCU and SBL need to be signed with active customer key

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2 Hardware

2.1 Component Identification

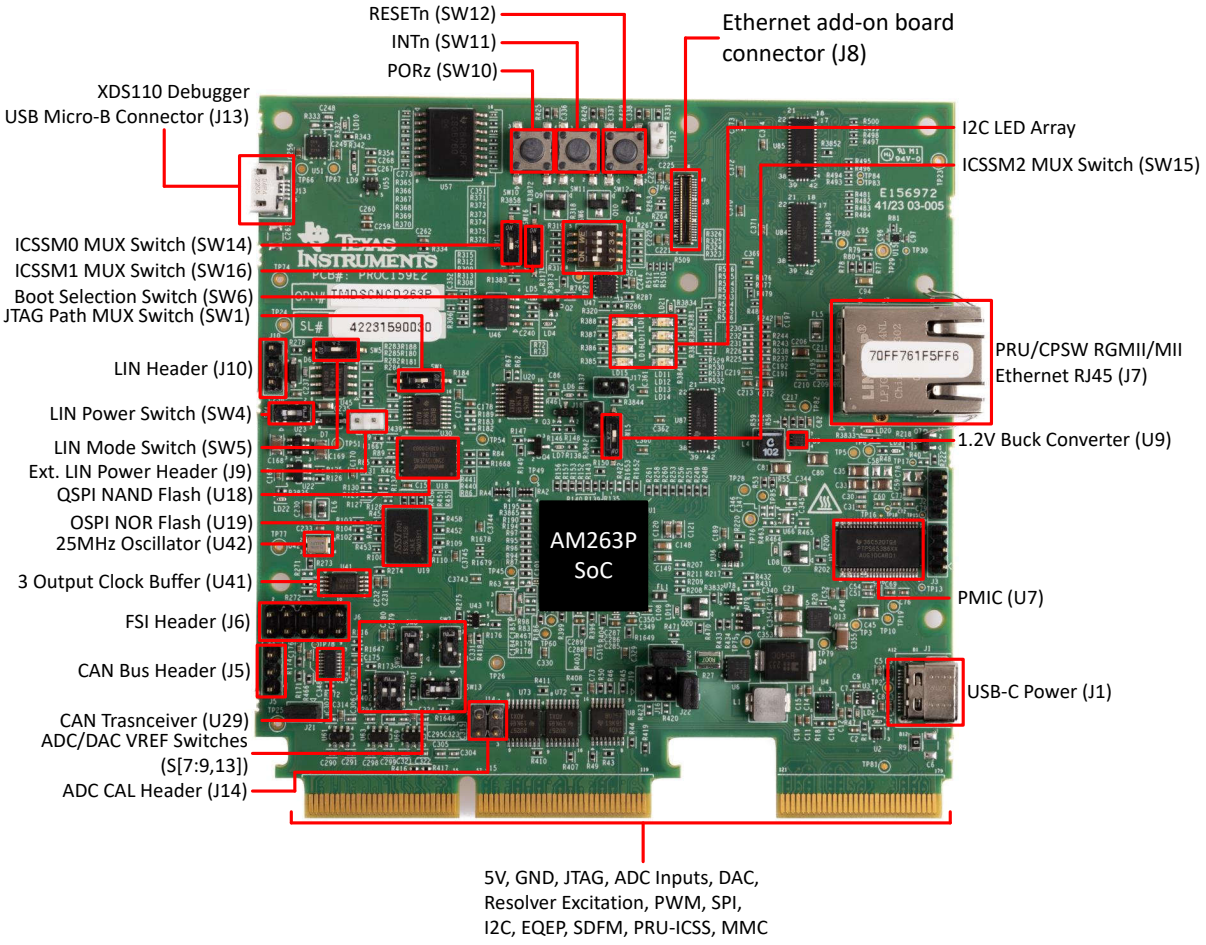

Figure 2-1. Component Identification (Front View)

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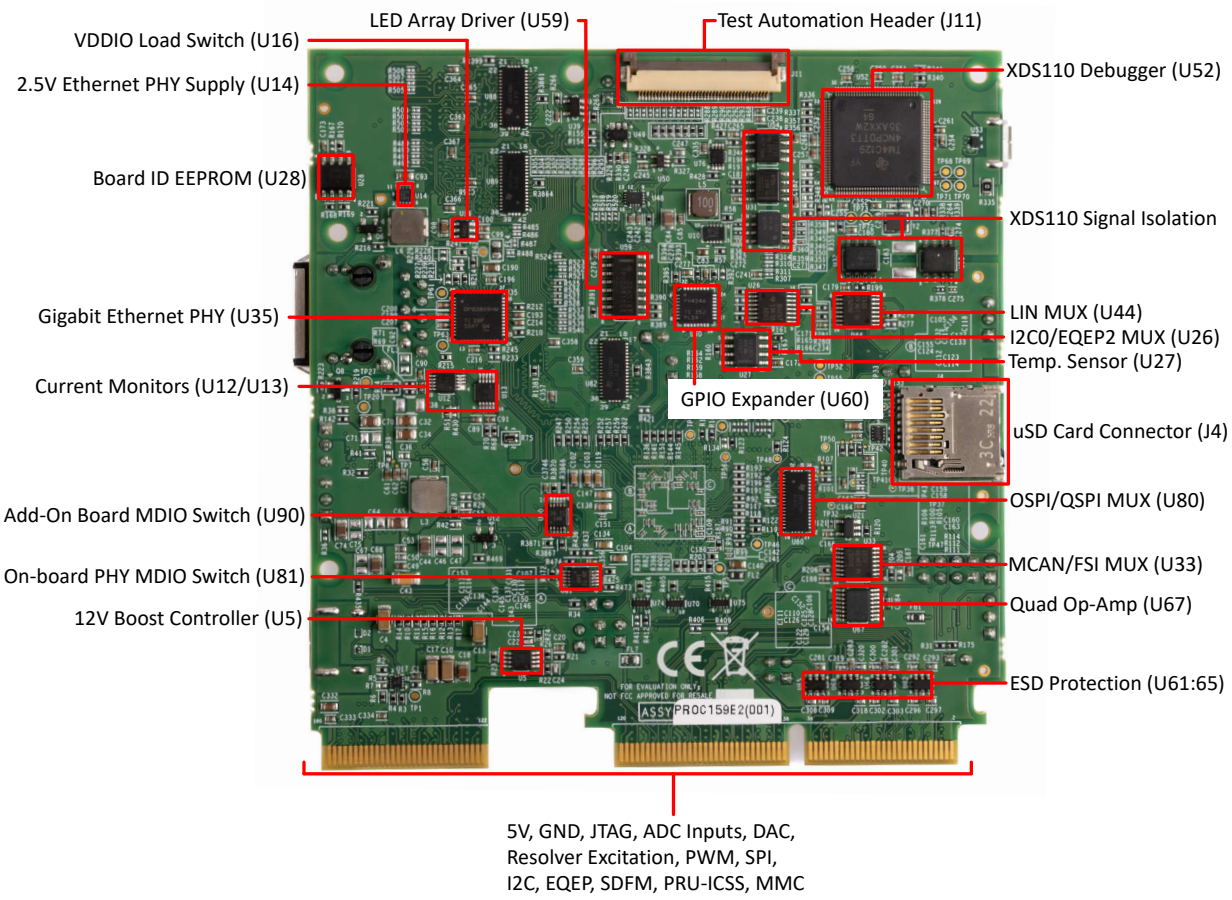

Figure 2-2. Component Identification (Back View)

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2.2 Power Requirements

The AM263Px Control Card is powered from a 5 V, 3 A USB type-C input or from a 5 V, 3 A HSEC connection supplied by the docking station. The following sections describe the power distribution network topology that supply the AM263Px Control Card, supporting components and the reference voltages.

Power supply designs that are compatible with the AM263Px Control Card:

- When using the USB type-C input:
  - 5 V, 3 A power adapter with USB-C receptacle
  - 5 V, 3 A power adapter with captive USB-C cable
  - PC USB type-C port that has Power Delivery classification
    - Thunderbolt
    - Battery behind USB logo

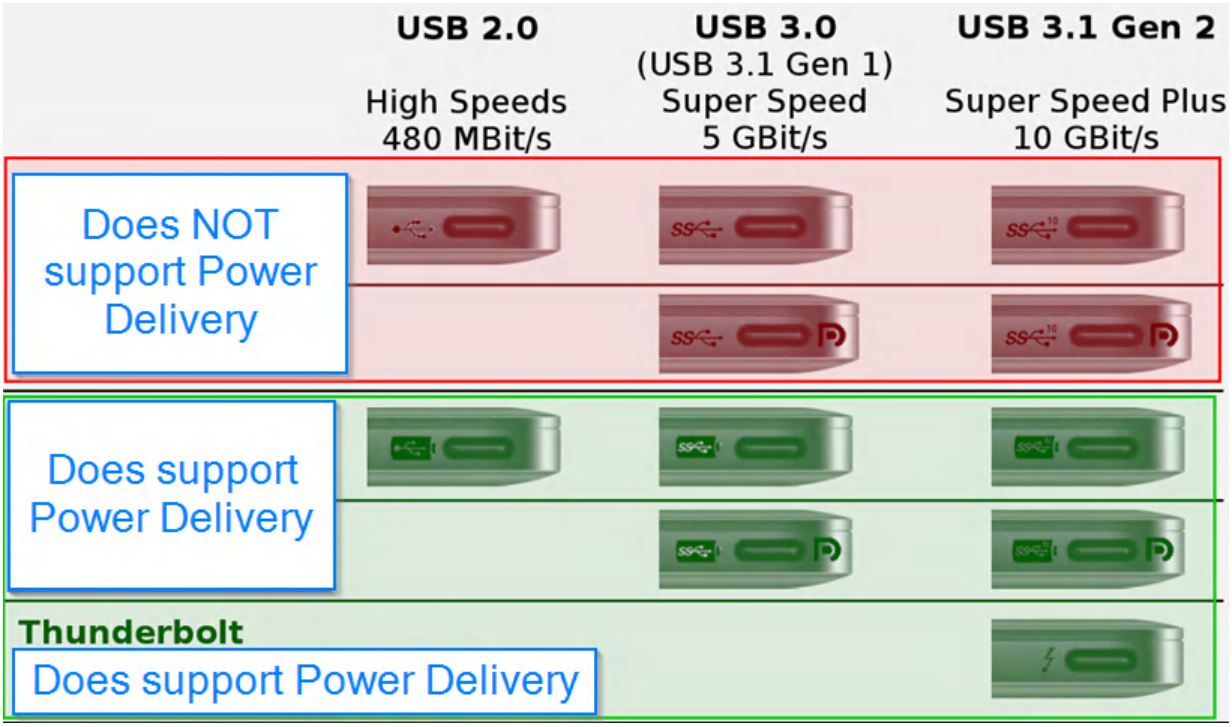

Figure 2-3. USB Type-C Power Delivery Classification

- When using the HSEC DC barrel jack power input:
  - A power adapter that is at least 15 W

Power supply designs that are **NOT** compatible with the AM263Px Control Card:

- When using USB type-C input:
  - Any USB adapter cables such as:
    - Type-A to type-C
    - micro-B to type-C
    - DC barrel jack to type-C
  - 5 V, 1.5 A power adapter with USB-C captive cable or receptacle
  - PC USB type-C port not capable of 3 A

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2.2.1 Power Input Using USB Type-C Connector

The AM263Px Control Card can be powered through a USB type-C connection. The USB Type-C source is capable of providing 3 A at 5 V and advertises the current sourcing capability through the CC1 and CC2 signals. On this EVM, the CC1 and CC2 from the USB type-C connector are interfaced to the port controller IC (TUSB320LAIRWBR). This device uses the CC pins to determine port attach/detach, cable orientation, role detection, and port control for Type-C current mode. The CC logic detects the Type-C current mode as default, medium, or high depending on the role detected.

The Port pin is pulled down to ground with a resistor to configure the IC in upward facing port (UFP) mode. VBUS detection is implemented to determine a successful attach in UFP mode. The OUT1 and OUT2 pins are connected to a NOR gate. Active low on both the OUT1 and OUT2 pins advertises high current (3A) in the attached state which enables the load switch (TPS22965DSGT) to provide the VBUS_MAIN supply which powers other regulators that create the power rails for the device.

In UFP mode, the port controller IC constantly presents pull-down resistors on both CC pins. The port controller IC also monitors the CC pins for the voltage level corresponding to the Type-C mode current advertisement by the connected DFP. The port controller IC de-bounces the CC pins and waits for VBUS detection before successfully attaching. As a UFP, the port controller device detects and communicates the advertised current level of the DFP to the system through the OUT1 and OUT2 GPIOs.

The power requirement of the AM263Px Control Card is 5 V at 3 A. If the source is not capable of providing the required power, then the output at the NOR gate becomes low that disables the VBUS_MAIN power switch. Therefore, if the power requirement is not met, all power supplies except VSYS_TA_3V3 remains in the off state. The board gets powered on completely only when the source can provide 5 V at 3 A.

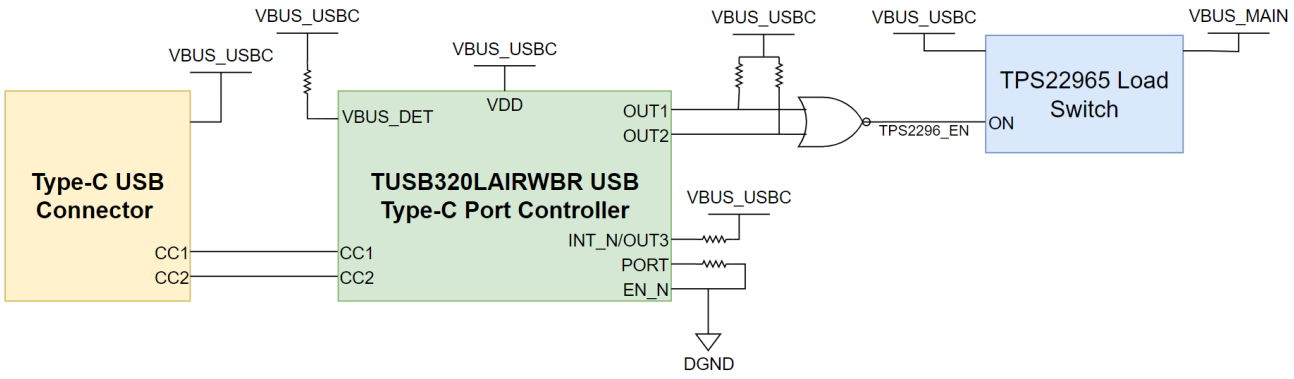

Figure 2-4. Type-C CC Configuration

Table 2-1. Current Sourcing Capability and State of USB Type-C Cable

OUT1	OUT2	Advertisement
H	H	Default current in unattached state
H	L	Default current in attached state
L	H	Medium current (1.5A) in attached state
L	L	High current (3.0A) in attached state

The AM263Px Control Card includes a power supply based on a Power Management Integrated Chip (PMIC) for each of the power rails. During the initial stage of the power supply, 5 V supplied by the type-C USB connector is used to generate all of the necessary voltages required by the PMIC and subsequently the rest of the board via the PMIC LDO outputs. For more information about the PMIC, refer to Section 2.2.5.

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2.2.2 Power Status LEDs

Multiple power-indication LEDs are provided on-board to indicate to users the output status of major supplies. The LEDs indicate power across various domains as shown in the table below.

Table 2-2. Power Status LEDs(1)

Name	Default Status	Operation	Function
LD1	OFF	Type-C CC Logic	Power Error Indication. Type-C connection not supplying 5 V @ 3 A
LD2	ON	VMAIN_12V0	Power indicator for VMAIN 12 V supply
LD3	ON	VSYS_3V3_LDO1	Power indicator for PMIC LDO 3.3 V supply
LD4	ON	VSYS_1V2_PG	Power Good indicator for 1.2 V supply rail
LD5	ON	VSYS_TA_3V3	Power indicator test automation header 3.3 V supply
LD6	OFF	USER_LED0	User Programmable Red LED
LD7	OFF	USER_LED1	User Programmable Green LED
LD8	OFF	PMIC_SAFE_OUT2	Safety Error indicator output from PMIC
LD9	OFF	XDS110_PROG_STAZ1	LED glows after XDS configuration
LD10	OFF	XDS110_PROG_STAZ2	
LD19	OFF	SAFETY_ERROR	Safety error output status pin from AM263Px
LD20	ON	VCC_1V8_LDO4	Power indicator PMIC LDO 1.8 Vsupply
LD21	ON	VDD_5V0_LDO3	Power indicator for PMIC LDO 5.0 V supply
LD22	ON	VSYS_3V3_LDO2	Power indicator for PMIC LDO 3.3 V supply

(1) LD[19:22] are not included in the E1 version of the Control Card.

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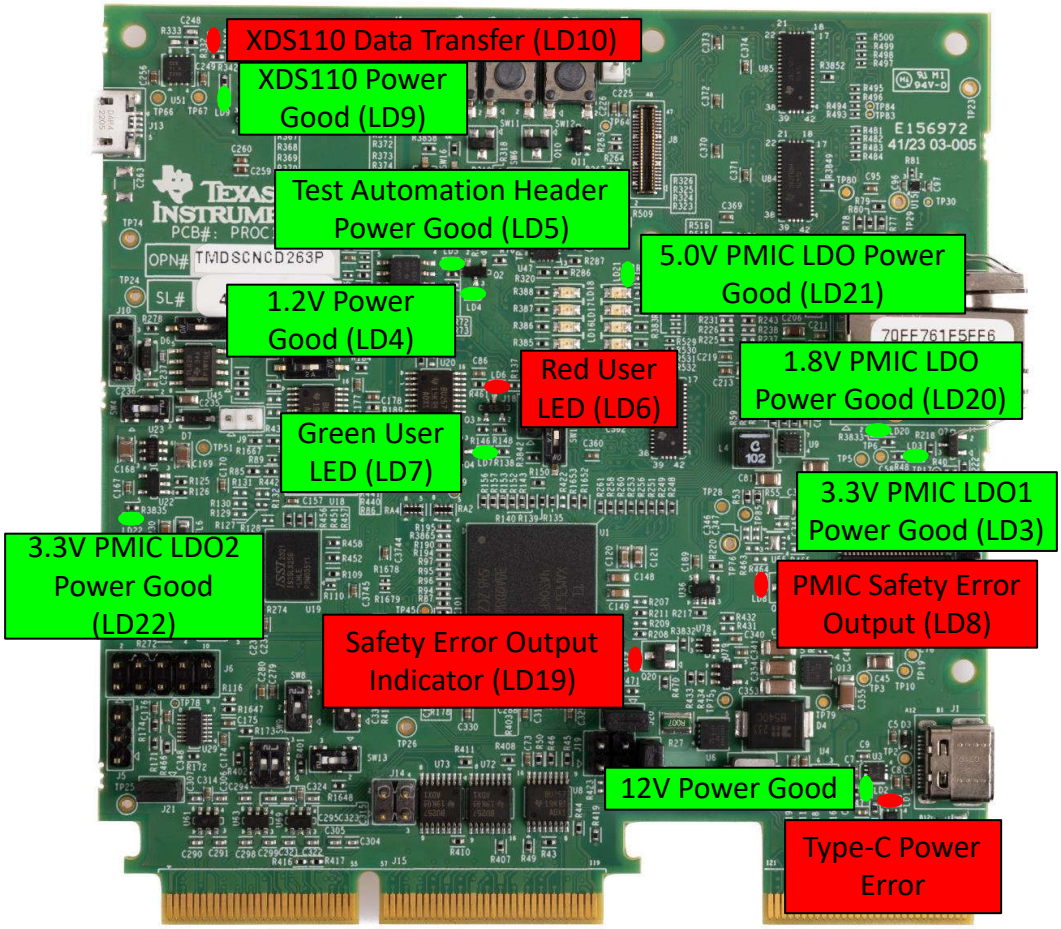

Figure 2-5. Power Status LEDs

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2.2.3 Power Tree

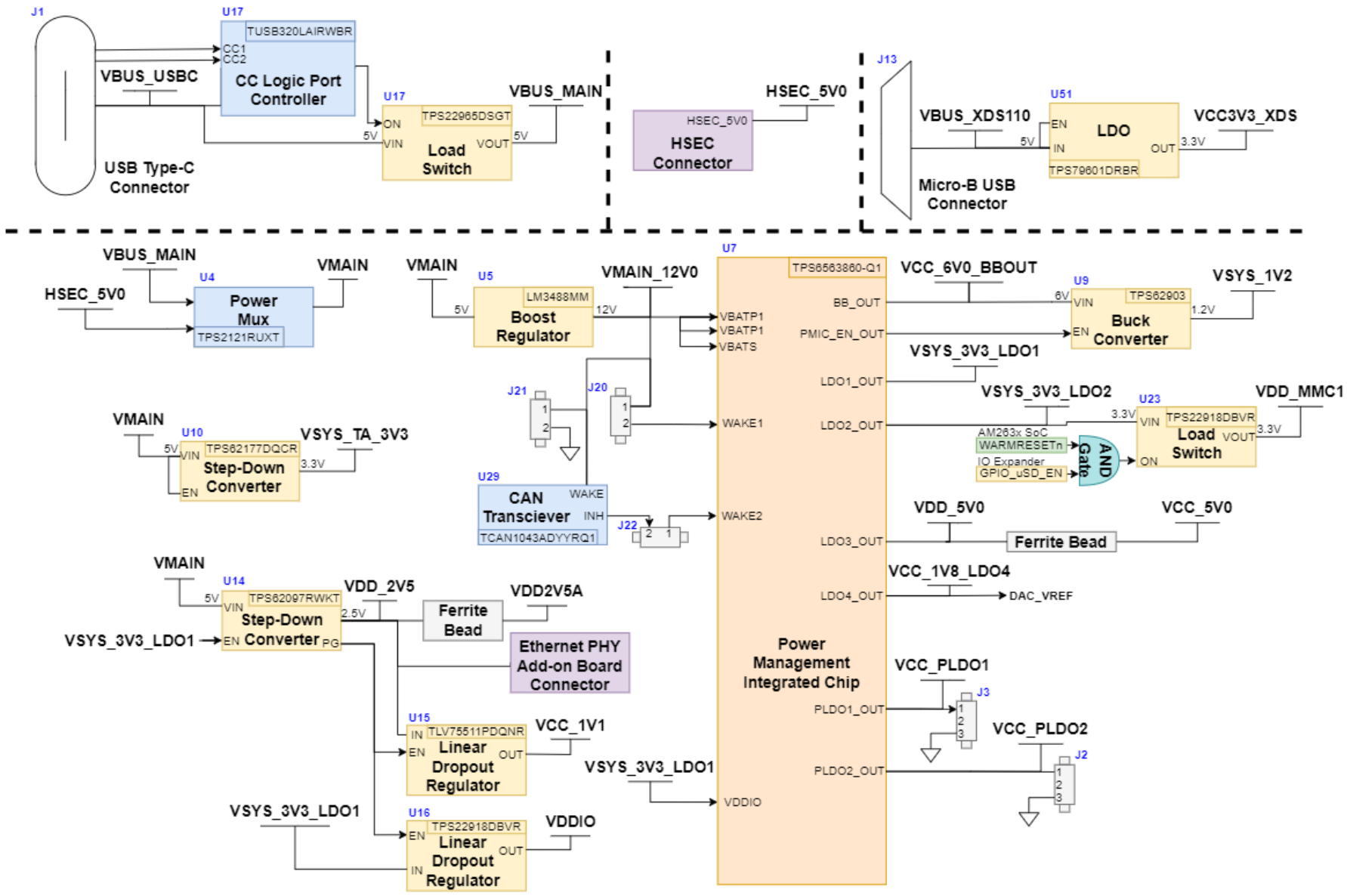

Figure 2-6. Power Tree

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2.2.4 Power Sequence

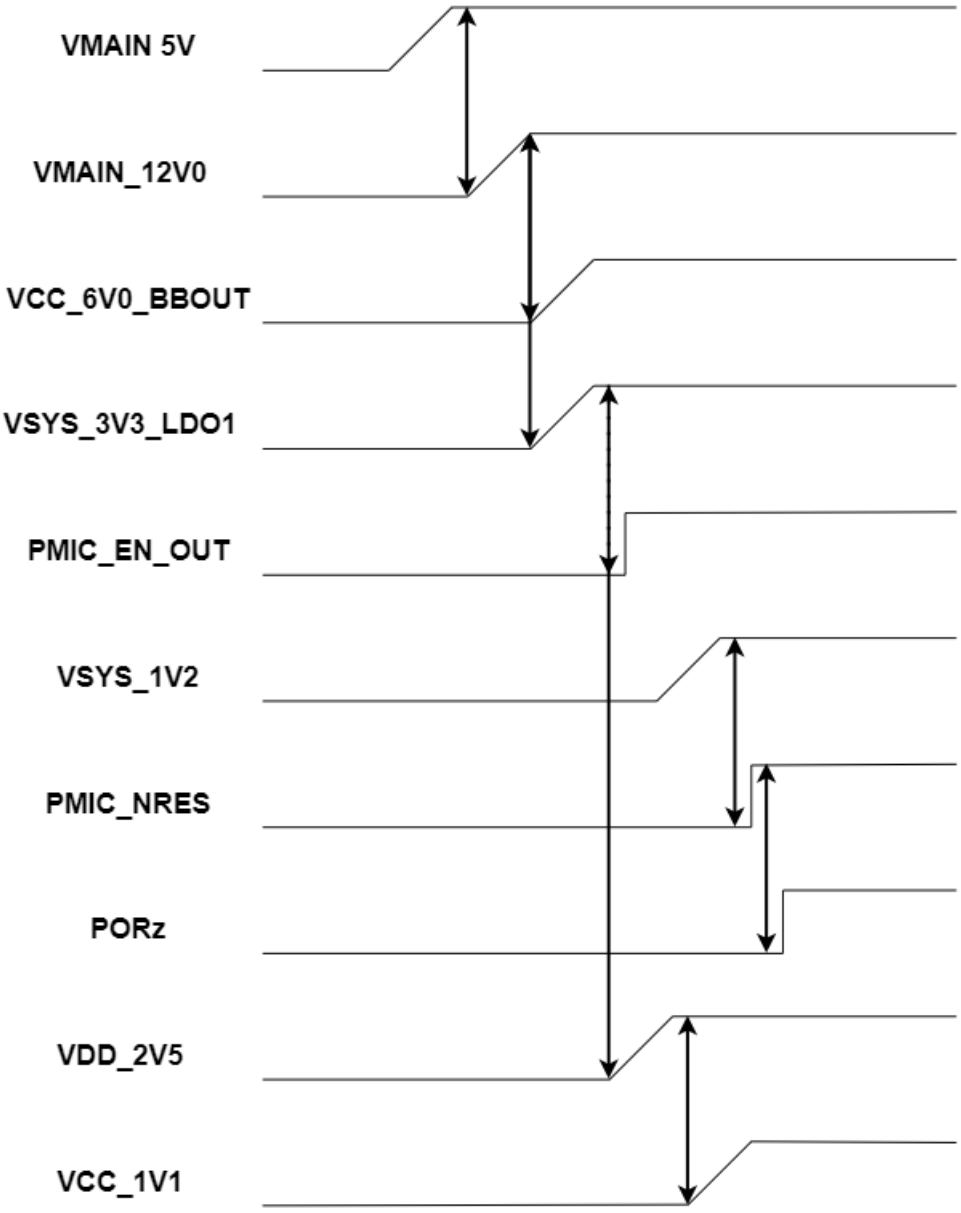

Figure 2-7. Power Sequence Diagram

Note

LDO[2:4]_OUT and PLDO[1:2]_OUT and the associated power supplies are intentionally not included in this diagram since these LDO outputs are not powered on by default and require a SPI write to enable these supply rails.

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2.2.5 PMIC

The AM263Px Control Card makes use of a multirail power supply for microcontrollers in safety-relevant applications (TPS6563860-Q1). The PMIC integrates multiple supply rails to power the MCU, CAN, and other on-board peripherals.

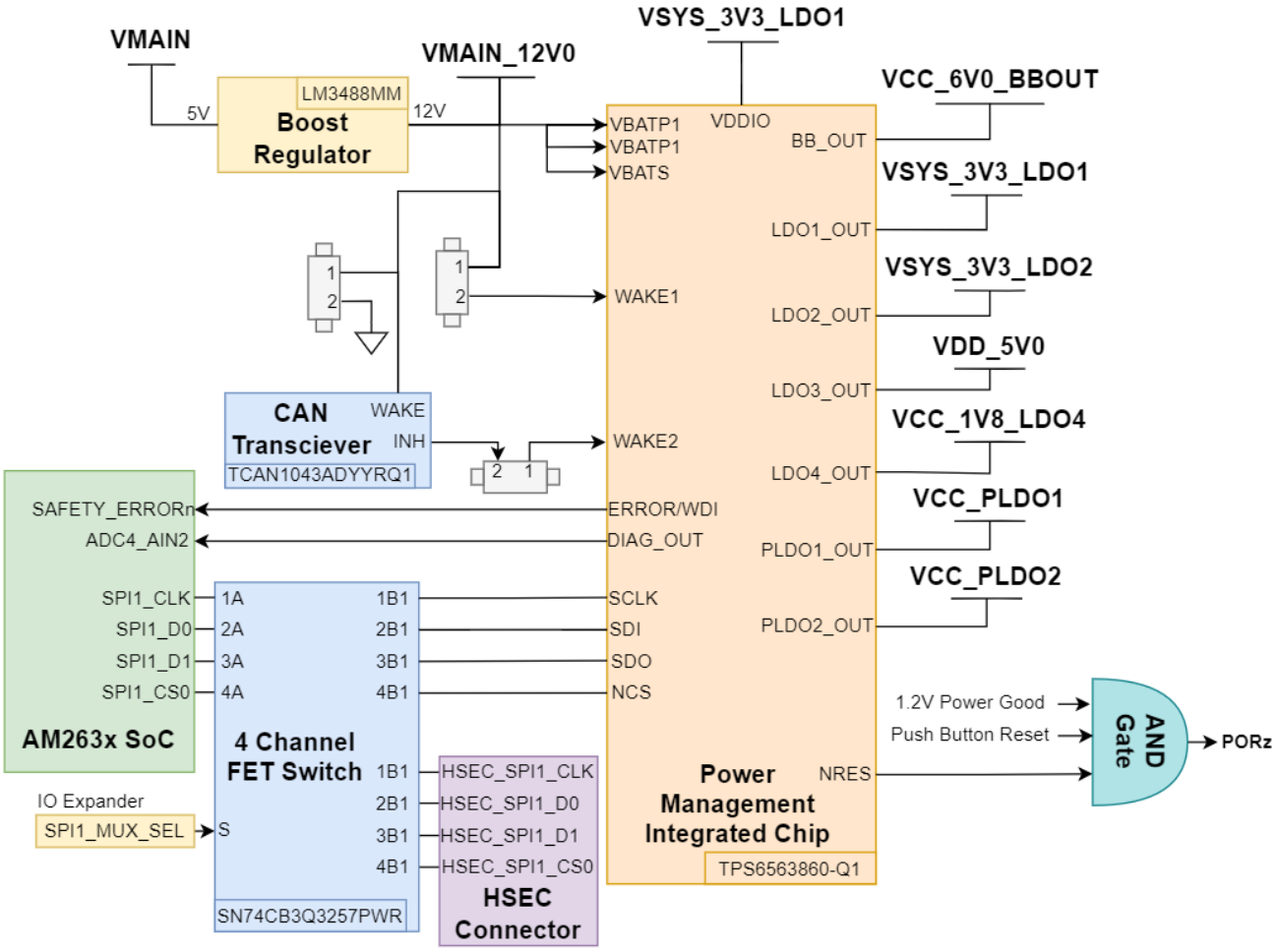

Figure 2-8. PMIC

Note

BB_OUT and LDO1_OUT are powered on by default. LDO[2:4]_OUT and PLDO[1:2]_OUT are not powered on by default and require a SPI write to enable these supply rails.

The PMIC supports wake-up from WAKE1 (VMAIN_12V0) or wake-up from a CAN transceiver (INH).

An independent voltage monitoring unit inside the PMIC monitors undervoltage and overvoltage on all internal supply rails and regulator outputs of the battery supply. All supplies are protected with current limiting and overtemperature warning and shutdown.

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2.3 Functional Block Diagram

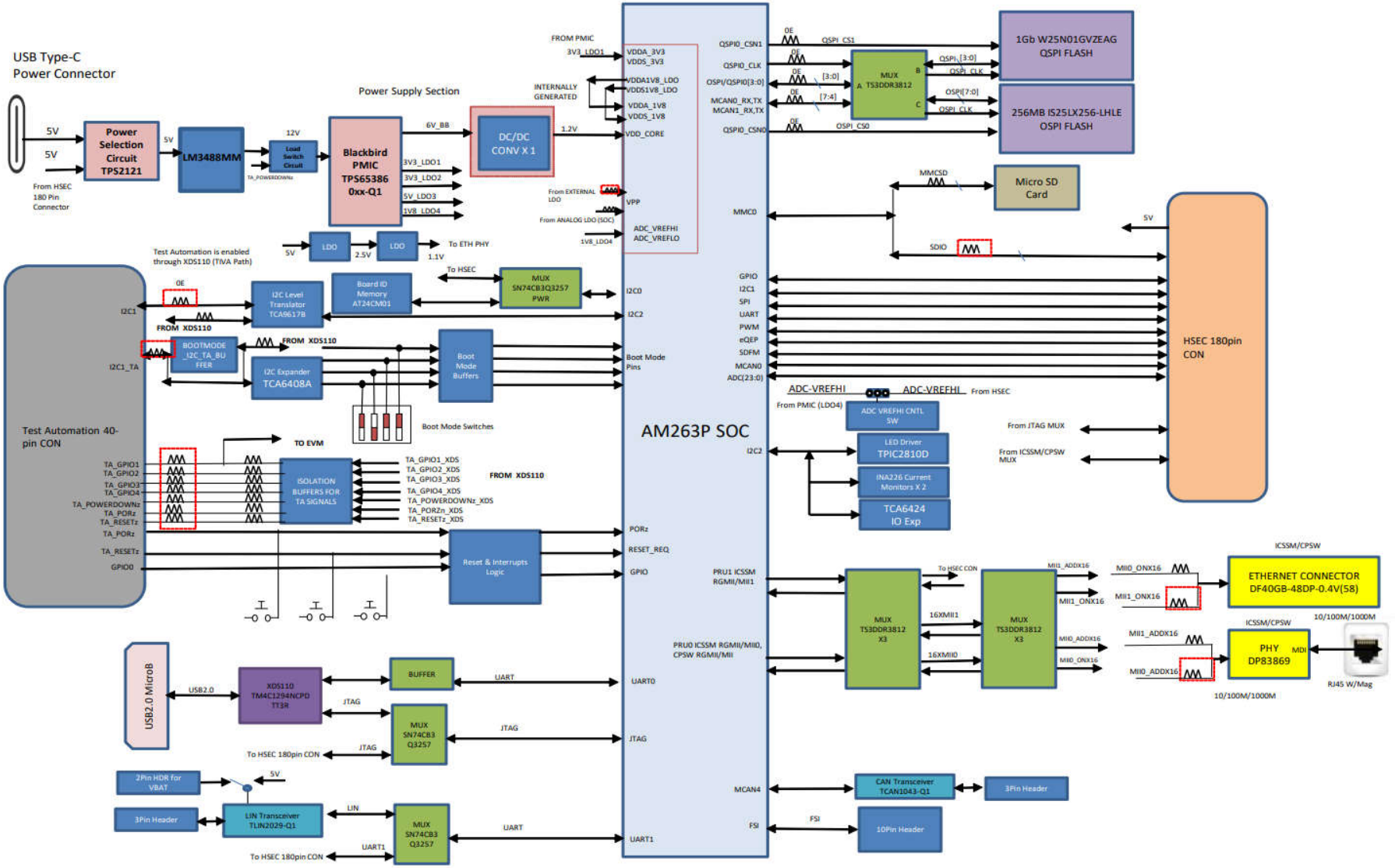

Figure 2-9. AM263Px Control Card E2 Block Diagram

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2.4 Reset

Figure 2-10 shows the reset architecture of the AM263Px Control Card.

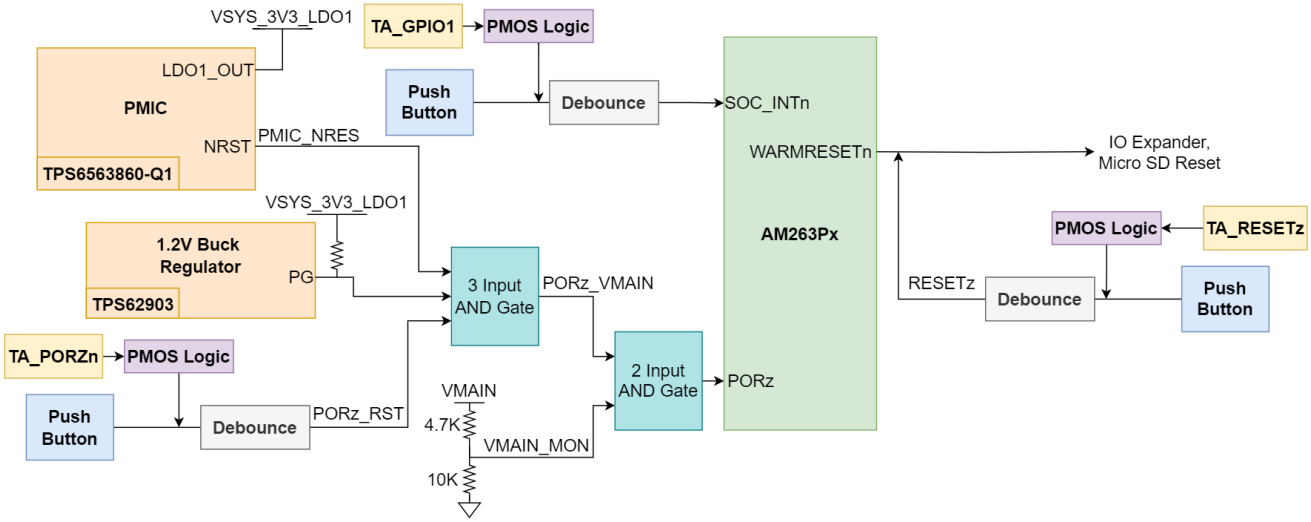

Figure 2-10. Reset Architecture

The AM263Px SoC has the following resets:

- PORz is the Power-On-Reset for the MAIN Domain.
- WARMRESETn is the Warm Reset to MAIN Domain.

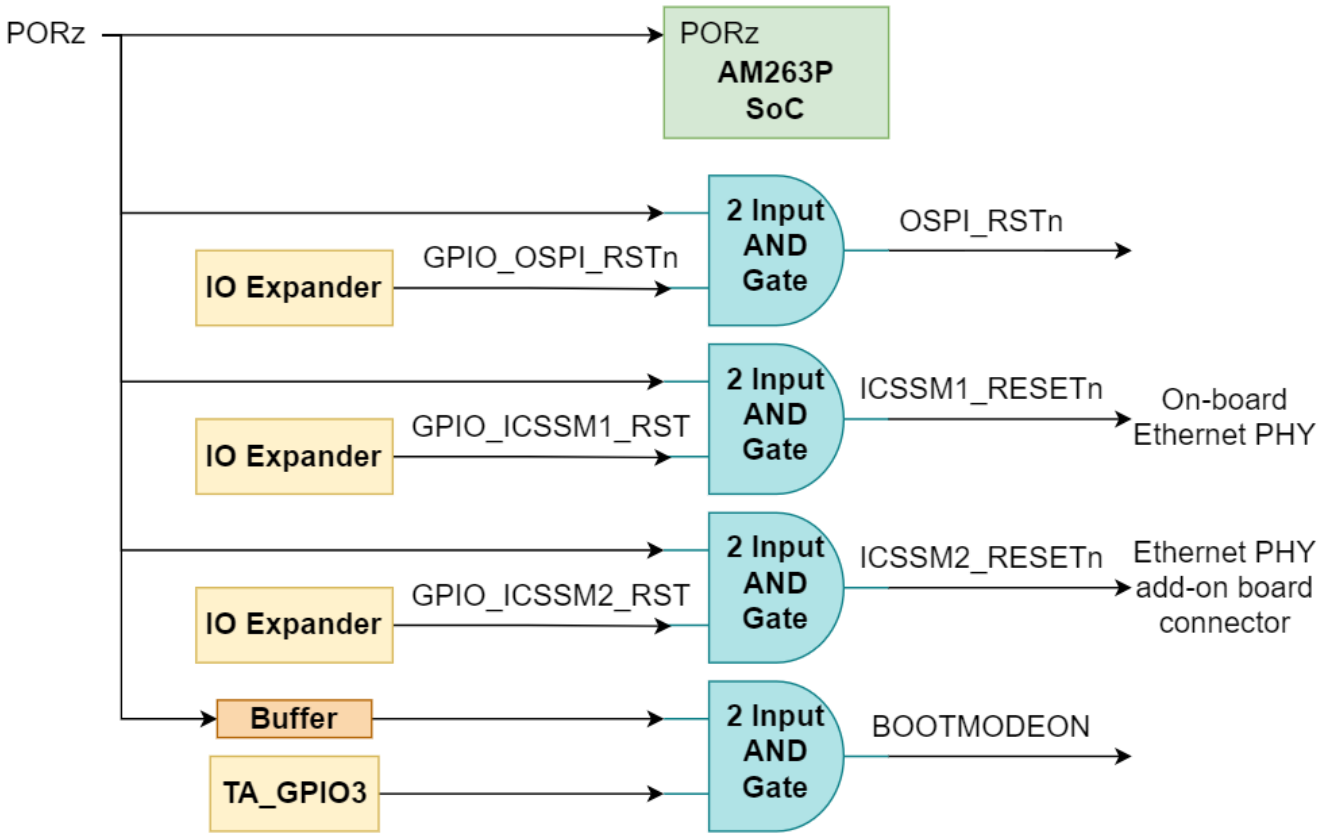

Figure 2-11. PORz Reset Signal Tree

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The PORz signal is driven by a 3-input AND gate that generates a power on reset for the MAIN domain when:

- The PMIC drives the NRES, MCU Reset output signal low.
- The 1.2 V buck regulator outputs a low signal for the power good signal.
- The user push button (SW10) is pressed.
- The Test Automation Header outputs a logic LOW signal (TA_PORZn) to a P-Channel MOSFET gate which causes V_GS of the PMOS to be less than zero and so the PORz signal connects to the PMOS drain which is tied directly to ground.

The PORz signal is tied to:

- AM263Px SoC PORz input
- OSPI Flash Reset
- On-board Gigabit Ethernet PHY reset
- Ethernet add-on board connector
- BOOTMODE buffer output enable
- High-Speed Edge Connector (HSEC)

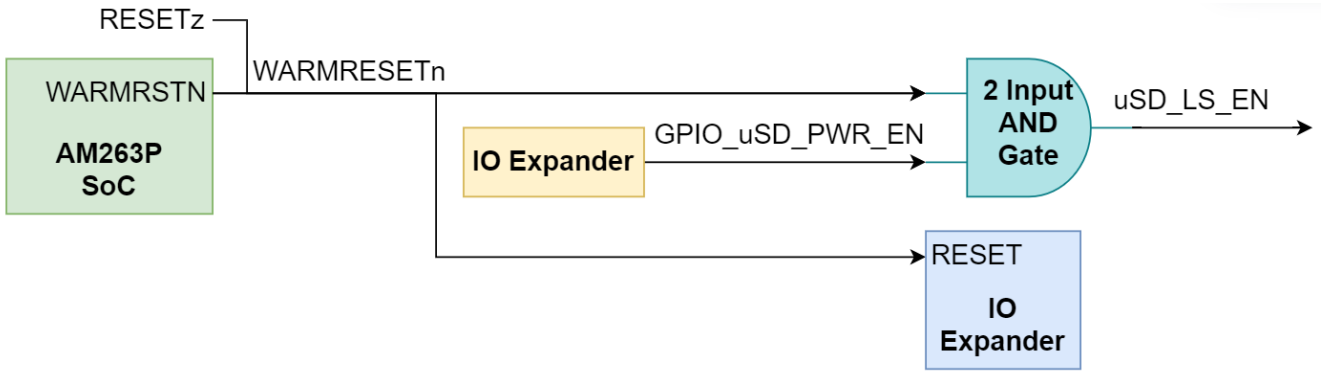

Figure 2-12. WARMRESETn Reset Signal Tree

The WARMRESETn signal creates a warm reset to the MAIN domain when:

- The user push button (SW12) is pressed.
- The Test Automation Header outputs a logic LOW signal (TA_RESETz) to a P-Channel MOSFET gate which causes V_GS of the PMOS to be less than zero and so the RESETz signal connects to the PMOS drain which is tied directly to ground.

The WARMRESETn signal is tied to:

- AM263Px SoC WARMRESETN output
- RESETz signal created from push button + PMOS logic
- IO Expander reset
- Micro SD reset
- HSEC

The AM263Px Control Card also has an external interrupt to the SoC, INTn, that occurs when:

- The user push button (SW11) is pressed.
- The Test Automation Header outputs a logic LOW signal (TA_GPIO1) to a P-Channel MOSFET gate which causes V_GS of the PMOS to be less than zero and so the INTn signal connects to the PMOS drain which is tied directly to ground.

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2.5 Clock

The AM263Px SoC requires a 25MHz clock input for XTAL_XI. All reference clocks required for the SoC and the three Ethernet PHY's are generated from a single four output clock buffer (LMK1C1103PWR), which is sourced from a single 25MHz LVCMOS Oscillator by default. A clock buffer is used for level translation from 3.3V to 1.8V.

The Control Card also requires a 16MHz clock source for the TM4C129 microcontroller for UART-USB JTAG support.

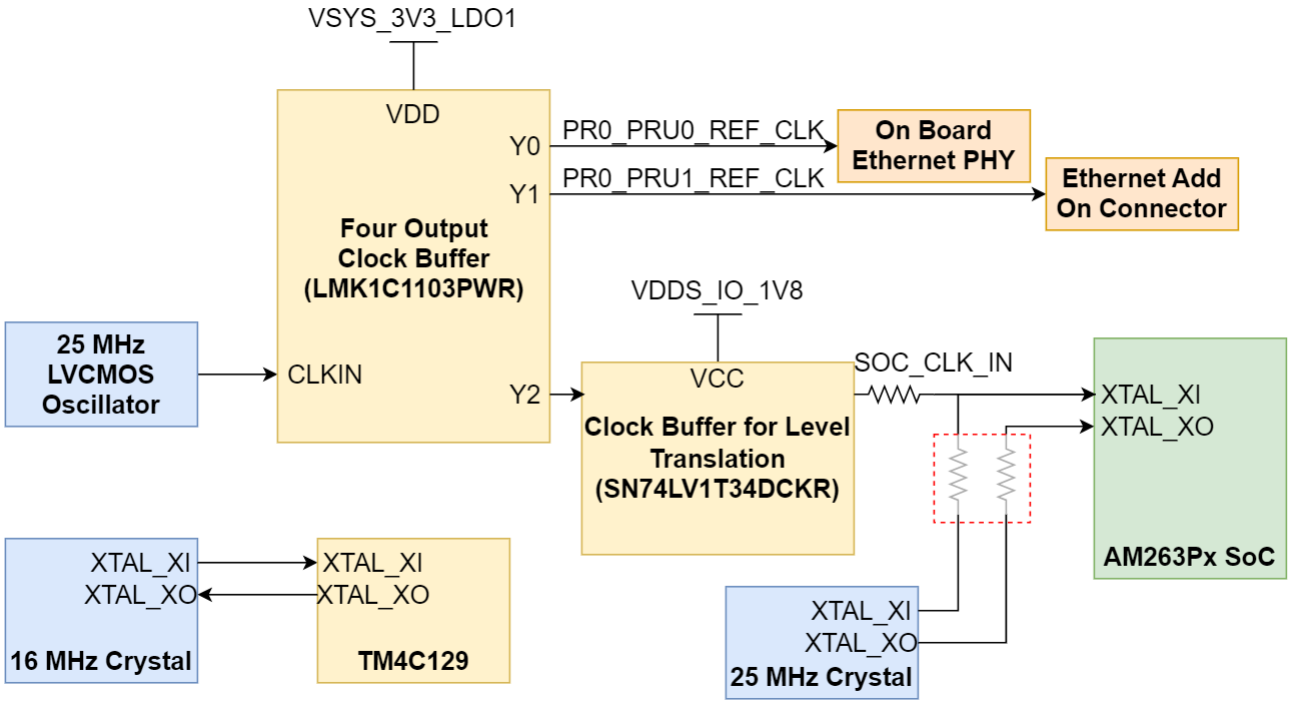

Figure 2-13. Oscillator Clock Tree

Alternatively, the SoC clock input can be sourced from a single 25-MHz crystal. To use the crystal there must be resistors mounted and unmounted. When the Crystal is used as a clock source then the AM263Px CLKOUT0 signal is used to source the four output clock buffer for the Ethernet PHY reference clock signals.

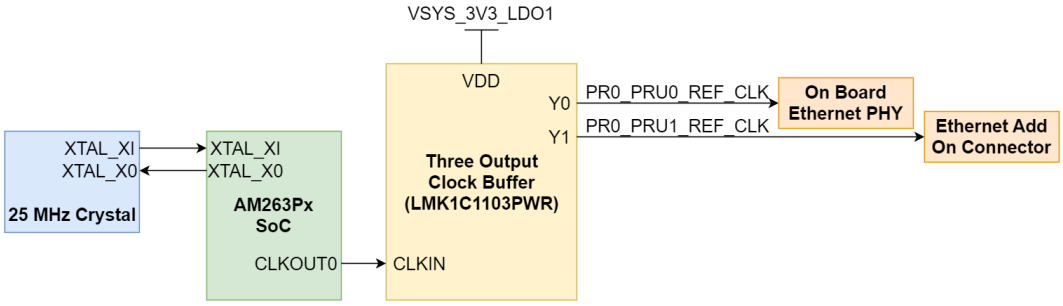

Figure 2-14. Crystal Clock Tree

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The following table describes the proper resistors to be mounted and DNI'd for each clock source configuration.

Table 2-3. Clock Source

Clock Source	Mounted	DNI
25-MHz LVCMOS Oscillator (default)	R273, R176	R178, R179, R271
25-MHz Crystal	R178, R179, R271	R273, R176

2.6 Boot Mode Selection

The bootmode for the AM263Px is selected by a DIP switch (SW6) or the test automation header. The test automation header uses an I2C IO expansion buffer to drive the bootmode when PORz is toggled. The supported boot modes are as shown in Table 2-4.

Table 2-4. Supported Boot Modes

Boot Mode/Peripheral	Boot Media/Host	Notes
QSPI(4S), 50 MHz	Flash Memory	ROM configures OSPI controller in QSPI 4S mode and downloads image from external flash, supports UART fallback boot mode if any failures.
UART	External Host	ROM configures UART0 with baud rate of 115200bps and downloads image from external PC terminal using x-modem protocol.
QSPI(1S), 50 MHz	Flash Memory	ROM configures OSPI controller in QSPI 1S mode and downloads image from external flash, supports UART fallback boot mode if any failures.
OSPI(8S), 50 MHz	Flash Memory	ROM configures OSPI controller in 8S mode and downloads image from external flash, supports UART fallback boot mode if any failures.
xSPI (1S->8D) , 25 MHz, SFDP	QSPI Flash / External Host	ROM configures OSPI controller in xSPI 8D mode ,Reads SFDP table for read command and downloads image from external flash, Flashes with SFDP are of JEDEC standard Rev D only supported.
DevBoot	N/A	No SBL. Used for development purposes only.

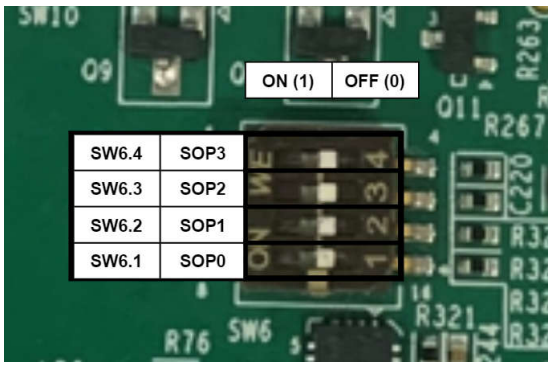

Figure 2-15. SW6 Switch Positions

Table 2-5. Boot-Mode Selection Table

Boot Mode	SPI0_D0_pad (SOP3)	SPI0_CLK_pad (SOP2)	OSPI_D1 (SOP1)	OSPI_D0 (SOP0)
QSPI(4S), 50 MHz	0	0	0	0
UART	0	0	0	1
QSPI(1S), 50 MHz	0	0	1	0
OSPI(8S), 50 MHz	0	0	1	1
xSPI (1S->8D) , 25 MHz, SFDP	1	1	0	0
DevBoot	1	0	1	1
Unsupported Boot Mode	All other combinations not defined above.			

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2.7 JTAG Path Selection

The AM263Px Control Card allows for JTAG connections to the SoC through the on-board XDS110 or an external emulator via the HSEC docking station. A switch (SW1) is used to drive the select line of a mux (U30) to determine the JTAG path for the SoC. The following image shows proper switch position for SW1 for the two JTAG paths.

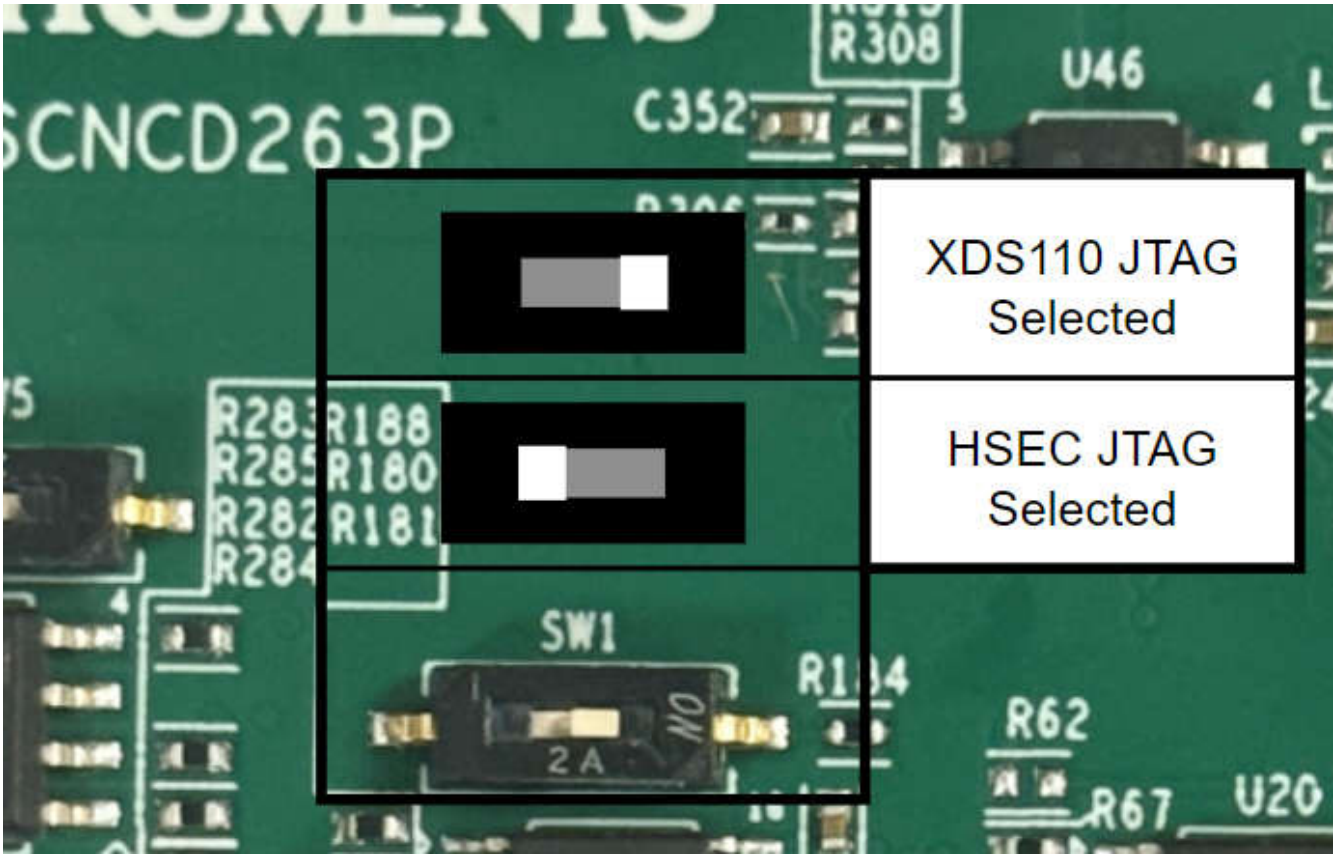

Figure 2-16. JTAG Path Switch Position

2.8 Header Information

This version of the AM263Px has 11 different headers. For the locations of each header, refer to Section 2.1. The signal details for each header pin is detailed below.

- PMIC Headers
  - For more information about the PMIC, refer to Table 2-6.

Table 2-6. PMIC

Designator	Pin 1	Pin 2	Pin 3
J2	VCC_PLDO2	NC	DGND
J3	VCC_PLDO1	NC	DGND
J20	VMAIN_12V0	PMIC_WKUP1	N/A
J21	TCAN_WAKE	DGND	N/A

- Test Automation Bootmode Control Header
  - For more information about the Test Automation Header, refer to Table 2-7.

Table 2-7. Test Automation Header

Designator	Pin 1	Pin 2
J12	TA_GPIO3	DGND

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- MCAN Header
  - For more information about the MCAN interface, refer to Table 2-8.

Table 2-8. MCAN Header

Designator	Pin 1	Pin 2	Pin 3
J5	MCAN4_CAN_H	DGND	MCAN4_CAN_L
J21	TCAN_WAKE	DGND	N/A
J22	PMIC_WKUP2	MCAN INH	N/A

- FSI Header
  - For more information about the FSI Interface, refer to Table 2-9.

Table 2-9. FSI Header

Designator	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10
J6	FSIRX2_CLK	FSITX2_CLK	DGND	DGND	FSIRX2_DATA0	FSITX2_DATA0	FSIRX2_DATA1	FSITX2_DATA1	DGND	VSYS_3V3A

- PRU-ICSS IEP Headers
  - For more information about the PRU-ICSS, refer to Table 2-10.

Table 2-10. PRU-ICSS IEP Headers

Designator	Pin 1	Pin 2
J19	PR0_IEP0_EDIO_DATA_IN_OUT_31	DGND
J18	PR0_IEP0_EDC_SYNC_OUT1	DGND
J17	PR0_IEP0_EDIO_DATA_IN_OUT_30	DGND
J16	PR0_IEP0_EDC_SYNC_OUT0	DGND

- LIN Headers
  - For more information about the LIN interface, refer to Table 2-11.

Table 2-11. LIN Headers

Designator	Pin 1	Pin 2	Pin 3
J10	VLIN	LIN	DGND
J9	VBAT_LIN	DGND	N/A

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2.9 GPIO Mapping

Table 2-12. E2 GPIO Mapping Table

Sl No.	GPIO Description	GPIO	Pin Name	Functionality	Net Name	Active Status
1	Interrupt To SoC	GPIO21	LIN2_RXD	Interrupt	SOC_INTn	LOW
2	Interrupt To Ethernet PHY connector	GPIO67	EPWM12_A	Interrupt	ICSSM2_PWDN/INTn	LOW
3	User Defined LED	GPIO66	EPWM11_B	GPIO	USER_LED1	PREFERABLE
4	Interrupt on-board ethernet PHY	GPIO68	EPWM12_B	Interrupt	ICSSM1_INT	LOW
5	User Defined LED	GPIO22	LIN2_TXD	GPIO	USER_LED0	PREFERABLE
8	Reset input to on-board ethernet PHY	GPIO35	RGMII1_TXC	Reset	GPIO_ICSSM1_RST	LOW
9	Reset input to ethernet connector	GPIO36	RGMII1_TX_CTL	Reset	GPIO_ICSSM2_RST	LOW
10	Interrupt to SoC from PMIC	GPIO29	RGMII1_RXC	Interrupt	PMIC_INTn	LOW
11	Select for OSPI/QSPI Mux	GPIO37	RGMII1_TD0	MUX SEL	OSPI/QSPI_MUX_SEL	PREFERABLE
IO Expander 01						
12	Reset input to OSPI		P00	Reset	GPIO_OSPI_RSTn	LOW
13	Enable control to clock buffer		P01	Enable	CLK_BUF_EN	HIGH
14	Select line for ICSS MII1 HSEC Mux		P02	Mux Selection	ICSSM1_MUX_SEL	SW16
15	Select line for ICSS on-board PHY/		P03	Mux Selection	ICSSM2_MUX_SEL	SW15
16	Select line for OSPI and HSEC UART		P04	Mux Selection	FSI_MUX_SEL	PREFERABLE
17	Select line for ADC MUX		P05	Mux Selection	ADC3_MUX_SEL	PREFERABLE
18	Select line for ADC MUX		P06	Mux Selection	ADC4_MUX_SEL	PREFERABLE
19	Enable control to SD load switch		P07	Load SW Enable	GPIO_uSD_PWR_EN	High
20	Select line for ADC MUX		P10	Mux Selection	ADC5_MUX_SEL	PREFERABLE
21	Select line for I2C0 MUX		P11	Mux Selection	I2C0_MUX_SEL	PREFERABLE
22	Select line for SPI1 MUX		P12	Mux Selection	SPI1_MUX_SEL	PREFERABLE
23	Select line for UART2 MUX		P13	Mux Selection	UART2_MUX_SEL	PREFERABLE
24	Enable control to 1.7V LDO		P14	LDO Enable	VPP_LDO_EN	PREFERABLE
25	Select line for LIN/UART MUX		P15	Mux Selection	LIN_MUX_SEL	PREFERABLE
26	Select line for ADC MUX		P16	Mux Selection	ADC1_MUX_SEL	PREFERABLE
27	Select line for ADC MUX		P17	Mux Selection	ADC2_MUX_SEL	PREFERABLE
28	HSEC GPIO		P20	GPIO	HSEC_GPIO	PREFERABLE
29	Standby signal for MCAN Transceiver		P21	MCAN Standby	MCAN1_STB	High
30	MDIO Signal selection for on-board PHY		P22	Mux Selection	MDIO/MDC_MUX_SEL1	High
31	MDIO signal selection for Ethernet add on board		P23	Mux Selection	MDIO/MDC_MUX_SEL2	High
32	Select line for ICSS MII0 HSEC Mux		P24	Mux Selection	ICSSM0_MUX_SEL	SW14

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2.10 Push Buttons

The control card supports multiple user push buttons that provide reset inputs and user interrupts to the processor.

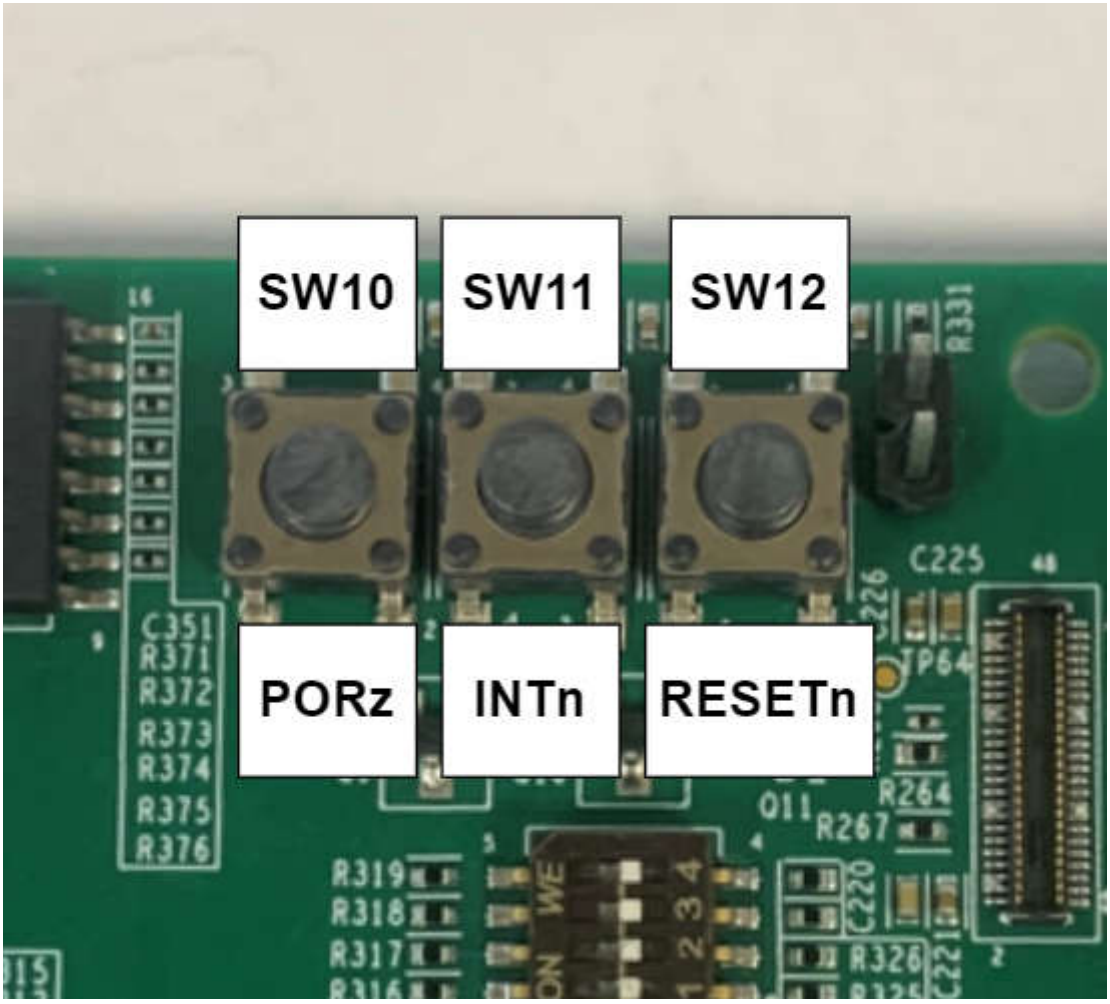

Figure 2-17. Push Buttons

Table 2-13 lists the push buttons that are placed on the top side of the AM263Px control card board.

Table 2-13. Control Card Push Buttons

Push Button	Signal	Function
SW11	INTn	User Interrupt signal
SW10	PORz	SoC PORz reset input
SW12	RESETn	SoC warm reset input

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2.11 Interfaces

2.11.1 Memory Interface

2.11.1.1 OSPI/QSPI

The AM263Px Control Card has a 128Mbit QSPI NAND flash memory device (W25N01GVZEJ), which is connected to the QSPI0 interface of the AM263Px SoC. The QSPI supports single data rates with memory speeds up to 104 MHz. The QSPI flash is powered by the 3.3-V IO supply (VSYS_3V3_LDO1).

Note

There is typically a reset pin for Flash memory. The Reset pin is not present in the WSON package that is used in the Control Card.

The QSPI0_D0/D1 signals are also used for BOOTMODE control logic. There are 10-kΩ resistors used to isolate the BOOTMODE control logic after the value is latched.

The AM263Px Control Card also has a 32Mbit OSPI NOR flash memory device (IS25LX256-LHLE), which is connected to the OSPI0 interface of the AM263Px SoC.

There is a high speed data switch that controls the routing of the memory data signals between the two flash memories. GPIO37 from the AM263Px SoC is used to drive the select line of the high-speed data switch. There is a pull-up resistor on the select line and therefore the OSPI memory device is selected by default.

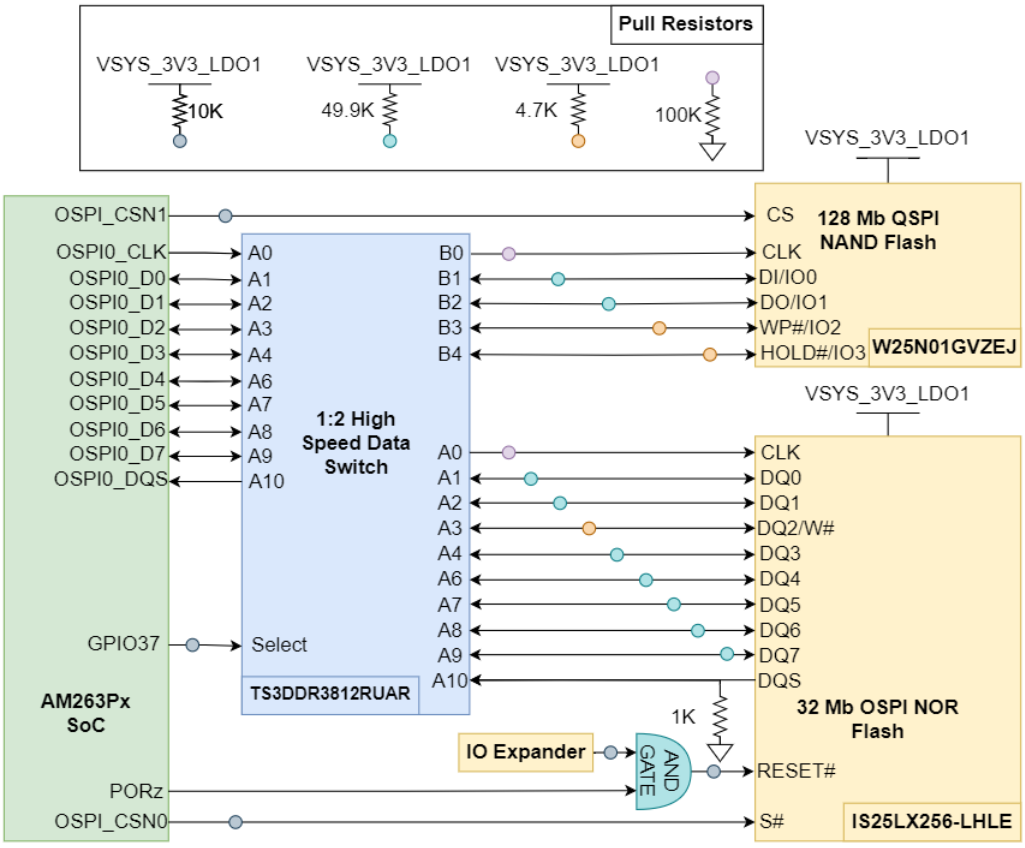

Figure 2-18. OSPI/QSPI Interface

Table 2-14. Memory Mux Table

Select	Condition	Mux Function
HIGH	OSPI NOR flash selected	A→B port
LOW	QSPI NAND flash selected	A→C port

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2.11.1.2 Board ID EEPROM

The AM263Px Control Card has a I2C based 1Mbit EEPROM (CAT23M01WI-GT3) to store board configuration details. The Board ID EEPROM is connected to the I2C0 interface of the AM263Px via a 1:2 Mux (SN74CB3Q3257PWR). The default I2C address of the EEPROM is set to 0x50 by pulling down the address pins A1 and A2 to ground. The Write Protect pin for the EEPROM is by default pulled down to ground and therefore Write Protect is disabled. There is also the option to enable write protect by removing the 10 KΩ pull down resistor (R273) and mounting a pull up resistor (R268) to the 3.3 V IO voltage supply.

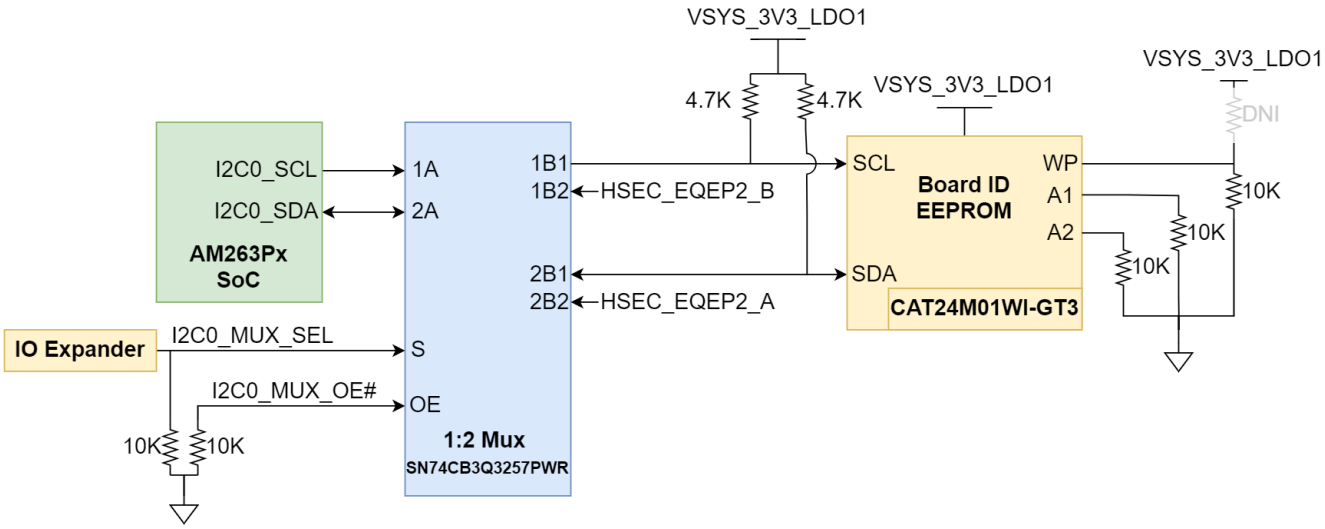

Figure 2-19. Board ID EEPROM

The GPIO Expander is used to control the select signal (I2C0_MUX_SEL) of the 1:2 Mux.

Table 2-15. EEPROM Mux Table

Select	Condition	Mux Function
HIGH	HSEC EQEP Selected	A→B2 port
LOW	I2C0 Selected	A→B1 port

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2.11.2 Ethernet Interface

The AM263Px SoC is equipped with two separate Ethernet interfaces. The first interface is a Gigabit Ethernet Switch (CPSW) subsystem that has two ports with selectable MII, RMII, and RGMII interfaces.

Note

The ZCZ_S package that is used on the Control Card is equipped with a Resolver interface in place of one of the CPSW Ethernet ports. As a result, the only CPSW port that is accessible on the Control Card is RGMII2/RMII2/MII2.

The second Ethernet interface is the Programmable Real-Time Unit Industrial Communication Subsystem (PRU-ICSS) which includes two cores (PRU0 and PRU1) that can each be configured as a Real-Time Ethernet Port.

Each of the Ethernet interfaces has an associated Management Data Input/Output (MDIO) module for PHY management. The CPSW and PRU-ICSS MDIO signals are to be routed to the PHY based on which port is routed to the PHY. The Control Card includes two analog switches that determine which MDIO module is routed to the on-board PHY or Ethernet add-on board connector.

The Ethernet port from the Gigabit Ethernet Switch (port 2) and Real-Time Ethernet Port that can be configured for PRU0 (PR0_PRU0_MII0) are routed to the same balls on the SoC such that the pinmux configuration determines which peripheral is being used at one time.

The Control Card includes an on-board gigabit Ethernet PHY transceiver (DP83869HMRGZT). For additional details on the on-board PHY, refer to Section 2.11.2.2. There is also an external connector to attach different Ethernet add-on boards for an additional automotive or industrial Ethernet PHY. For additional details about the boards that can be attached to the Ethernet add-on board connector, refer to the respective board user guide.

The Control Card also includes multiple, 1:2 MUX/DEMUX high-speed switches to route all Ethernet ports between the HSEC, on-board Ethernet PHY, and Ethernet add-on board connector. For a complete description of all Ethernet routing for the control card, refer to Section 2.11.2.1.

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2.11.2.1 Control Card Ethernet Routing

The AM263Px SoC includes multiple Ethernet Ports and MDIO modules that can be routed to different locations based upon MUX/analog switch settings as well as which 0 Ω resistors are populated on the board. There are three single-pole single-throw (SPST) switches as well as IO control signals from the IO expander that determine the state of the MUX/analog switch routing.

Figure 2-20 Shows a high-level overview of the routing scheme for all ethernet ports and MDIO signals.

Table 2-16 details the various available configurations for ethernet and MDIO routing on the Control Card. The Default setting is configuration 1 which is also highlighted in green.

Note

Various configurations require soldering and removal of 0 Ω resistors.

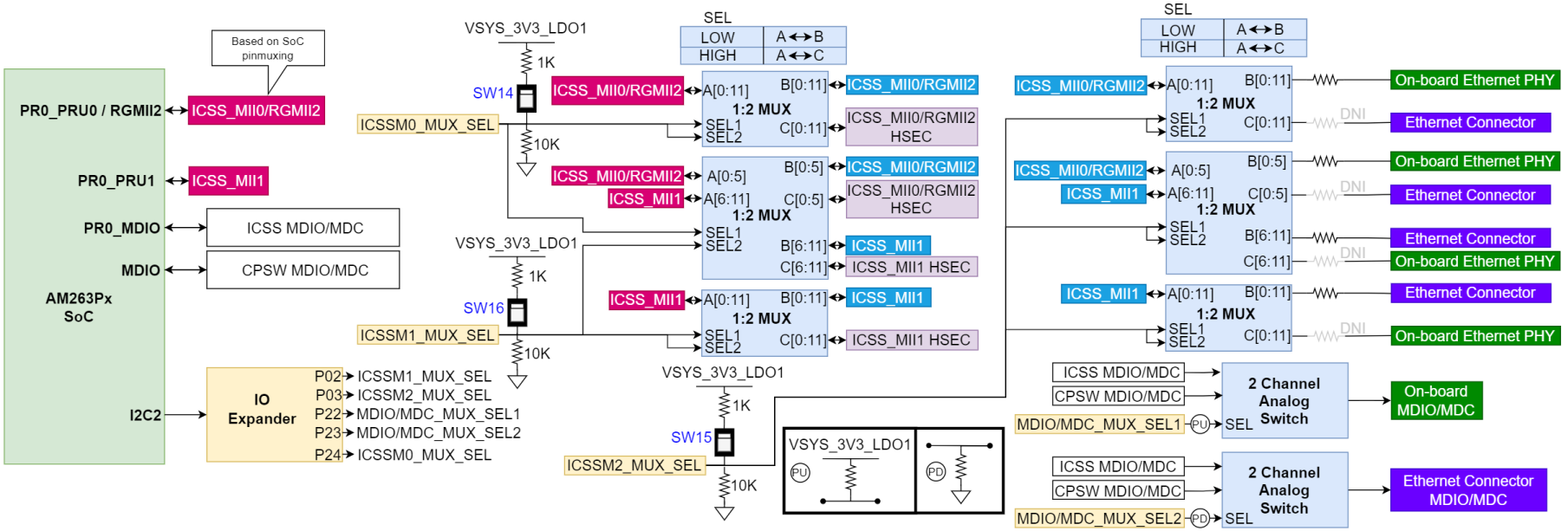

Figure 2-20. Ethernet Routing Overview

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Represents the default state out-of-box	Represents areas that require soldering/desoldering components

Table 2-16. Ethernet Routing

SoC Source	Destination	Config. #	ICSSM0_ MUX_SEL (SW14)	ICSSM1_ MUX_SEL (SW16)	ICSSM2_ MUX_SEL (SW15)	MDIO/MDC_ MUX_SEL1	MDIO/MDC_ MUX_SEL2	R476:R484 R493:R500	R509:R516 R525:R532	R485:R492 R501:R508	R517:R524 R533:R540
			Controlled by IO expander **OR** SW[14:16]			Controlled by IO expander		Requires soldering and removing components			
CPSW RGMII2	On-board PHY	1 Default	Low	Low	Low	High	Low	POP	POP	DNI	DNI
PRU1 MII1	Ethernet Add-on Connector										
N/A	HSEC										
PRU MII0	Not Connected										
PRU0 MII0	On-board PHY	2	Low	Low	Low	Low	Low	POP	POP	DNI	DNI
PRU1 MII1	Ethernet Add-on Connector										
N/A	HSEC										
CPSW RGMII2	Not Connected										
PRU1 MII1	On-board PHY	3	Low	Low	High	Low	Low	DNI	DNI	POP	POP
PRU0 MII0	Ethernet Add-on Connector										
N/A	HSEC										
CPSW RGMII2	Not Connected										
PRU1 MII1	On-board PHY	4	Low	Low	High	Low	High	DNI	DNI	POP	POP
CPSW RGMII2	Ethernet Add-on Connector										
N/A	HSEC										
PRU0 MII0	Not Connected										
PRU0 MII0	On-board PHY	5	Low	High	Low	Low	X	POP	X	DNI	X
N/A	Ethernet Add-on Connector										
PRU1 MII1	HSEC										
CPSW RGMII2	Not Connected										
CPSW RGMII2	On-board PHY	6	Low	High	Low	High	X	POP	X	DNI	X
N/A	Ethernet Add-on Connector										
PRU1 MII1	HSEC										
PRU0 MII0	Not Connected										
N/A	On-board PHY	7	Low	High	High	X	Low	DNI	X	POP	X
PRU0 MII0	Ethernet Add-on Connector										
PRU1 MII1	HSEC										
CPSW RGMII2	Not Connected										
N/A	On-board PHY	8	Low	High	High	X	High	DNI	X	POP	X
CPSW RGMII2	Ethernet Add-on Connector										
PRU1 MII1	HSEC										
PRU0 MII0	Not Connected										

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Table 2-16. Ethernet Routing (continued)

SoC Source	Destination	Config. #	ICSSM0_ MUX_SEL (SW14)	ICSSM1_ MUX_SEL (SW16)	ICSSM2_ MUX_SEL (SW15)	MDIO/MDC_ MUX_SEL1	MDIO/MDC_ MUX_SEL2	R476:R484 R493:R500	R509:R516 R525:R532	R485:R492 R501:R508	R517:R524 R533:R540
N/A	On-board PHY	9	High	Low	Low	X	Low	X	POP	X	DNI
PRU1 MII1	Ethernet Add-on Connector										
PR_MII0 or RGMII2	HSEC										
N/A	Not Connected										
PRU1 MII1	On-board PHY	10	High	Low	High	Low	X	X	DNI	X	POP
N/A	Ethernet Add-on Connector										
PR_MII0 or RGMII2	HSEC										
N/A	Not Connected										
N/A	On-board PHY	11	High	High	X	X	X	X	X	X	X
N/A	Ethernet Add-on Connector										
PR_MII0 or RGMII2 PR_MII1	HSEC										
	Not Connected										

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2.11.2.2 On Board Ethernet PHY

The AM263Px Control Card uses one port of RGMII signals and the PRU0 core of the PRU-ICSS to be connected to a 48pin ethernet PHY (DP83TG730SWRHARQ1). The PHY is configured to advertise 1-Gb operation. The ethernet data signals of the PHY are terminated to an RJ45 Connector. LEDs are used to indicate link status and activity.

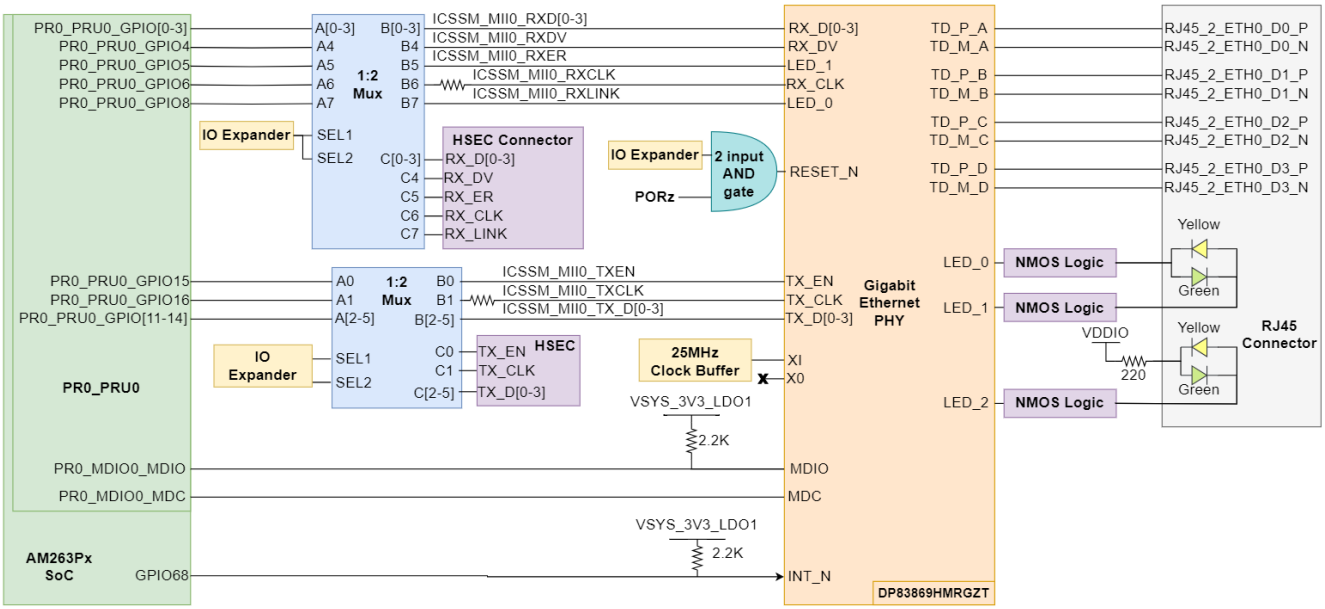

Figure 2-21. E1 Control Card On Board Ethernet PHY

The Ethernet PHY requires three separate power sources. There are two dedicated LDO for the 1.1 V and 2.5 V supplies for the Ethernet PHY. The VDDIO supply for the ethernet PHY is supplied through a load switch (U16) that is enabled once the 2.5 V power good signal is driven high.

The RGMII2 port of the CPSW signals are internally muxed on the same balls as the PRU-ICSS ethernet signals. To use RGMII2, the balls must be set to the appropriate mux mode for RGMII2.

There are series termination resistors on the transmit and receive clock signals located near the AM263Px SoC.

The MDIO and Interrupt signals from the SoC to the PHY require 2.2KΩ pull up resistors to the I/O supply voltage for proper operation. The interrupt signal is driven by a GPIO signal that is mapped from the AM263Px SoC.

The reset signal for the Ethernet PHY is driven by a 2-input AND gate. The AND gate's inputs are a GPIO signal that is generated by the IO Expander and PORz.

The Ethernet PHY uses many functional pins as strap option to place the device into specific modes of operation.

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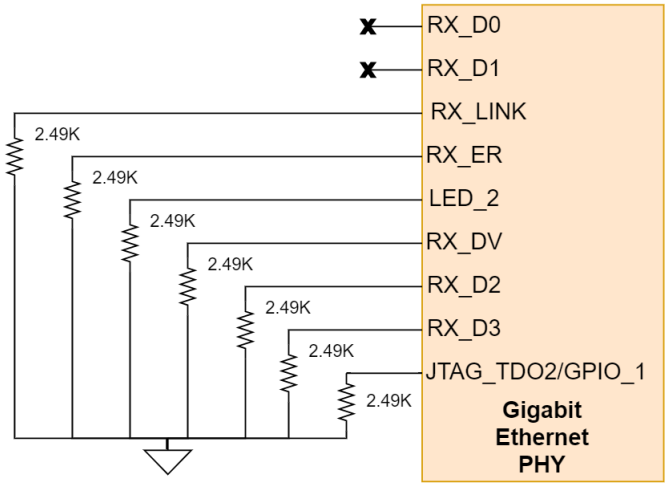

Figure 2-22. Industrial Ethernet PHY Strapping Resistors

Table 2-17. Industrial Gigabit Ethernet PHY Strapping Resistors

Functional Pin	Default Mode	Mode in CC	Function
RX_D0	0	0	PHY address: 0000
RX_D1	0	0	
JTAG_TDO/GPIO_1	0	0	RGMII to Copper
RX_D3	0	0	
RX_D2	0	0	
LED_0	0	0	Auto-negotiation, 1000/100/10 advertised, auto MDI-X
RX_ER	0	0	
LED_2	0	0	
RX_DV	0	0	Port Mirroring Disabled

2.11.2.3 LED Indication in RJ45 Connector

The AM263Px Control Card has one RJ45 network ports for the ICSSM port on PRU0 of the AM263Px SoC. Each RJ45 connector contains two bi-color LEDs that are used to indicate link and activity.

- RJ45 Connector LED indication for the ICSSM PRU0 port:

Table 2-18. ICSSM PRU1 RJ45 Connector LED indication

LED	Color	Indication
Right LED	Green	Ethernet PHY power established
	Yellow	10BT speed link is up
Left LED	Green	Link OK
	Yellow	1000BT speed link is up

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2.11.3 I2C

The AM263Px Control Card uses three AM263Px SoC inter-integrated circuit (I2C) ports to operate as a controller for various targets. All I2C data and clock lines pulling up to the 3.3V IO voltage supply to enable communication are important.

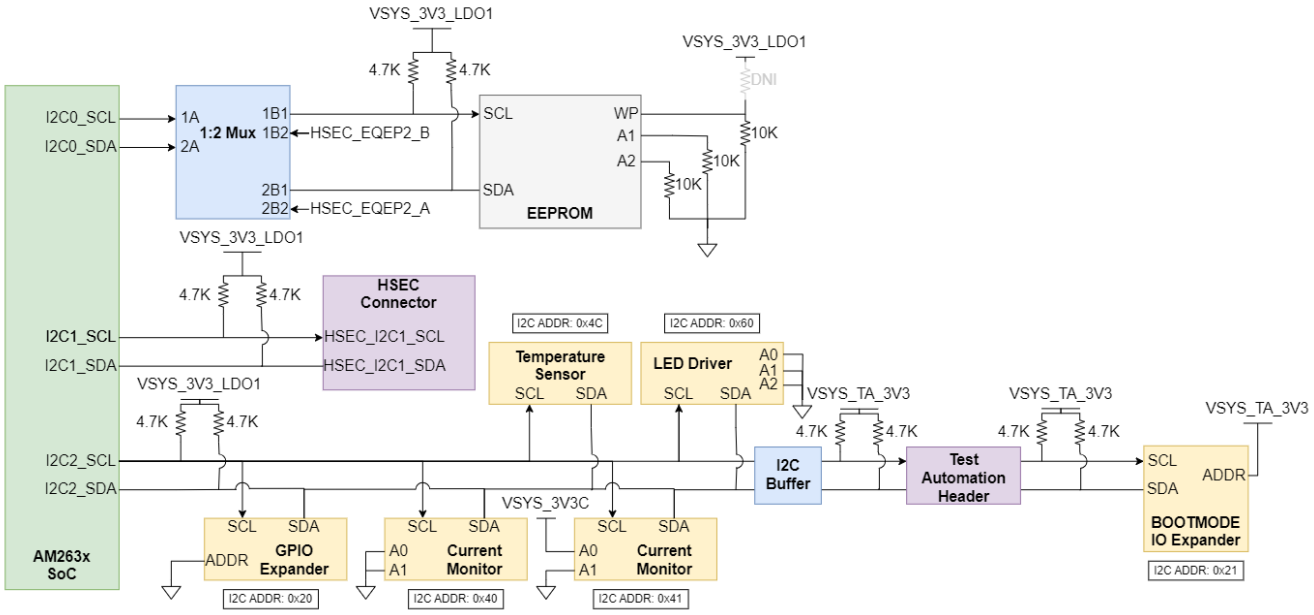

Figure 2-23. I2C Instances Tree

Table 2-19. I2C Addressing

Target	I2C Instance	I2C Address Bit Description	Device Configuration	CC Config.	I2C Address
Board ID EEPROM	I2C0	The first 4 bits of the device address are set to 1010, the next two are set by the A2 and A1 pins, the seventh bit, a16, is the most significant internal address bit	0b10110[A2][A1][a16] A1/A2 are connected to ground	0b1010000	0x50
GPIO Expander	I2C2	The first 6 bits of the target address are set to 010000, the next bit is determined by the addr pin of the IO expander	0b010000[ADDR] ADDR pin connected to ground	0b0100000	0x20
BOOTMODE IO Expander	I2C2/ I2C1_TA	The first 6 bits of the target address are set to 010000, the next bit is determined by the addr pin of the IO expander	0b010000[ADDR] ADDR pin connected to 3.3V IO supply	0b0100001	0x21
Current Monitor	I2C2	The first three bits of the target address are 100, the following four bits are determined by what is hooked up to A1 and A0	Refer to Address pin table from *Device Data Sheet*.	0b1000000	0x40
Current Monitor	I2C2	The first three bits of the target address are 100, the following four bits are determined by what is hooked up to A1 and A0	Refer to Address pin table from *Device Data Sheet*.	0b1000001	0x41
Temperature Sensor	I2C2	Fixed value of 1001100 for part number TMP411Ax	N/A	0b1001100	0x4C
LED Driver	I2C2	The first four bits of the target address are 1100, the following three are determined by A2, A1, and A0	0b1100[A2][A1][A0] A2/A1/A0 all connected to ground	0b1100000	0x60

Note

Underlined address bits are fixed based on the device addressing and cannot be configured.

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2.11.4 Industrial Application LEDs

The AM263Px Control Card has an LED driver (TPIC2810D) that is used for Industrial Communication LEDs. The driver is connected to eight green LEDs and has an I2C address of 0x60.

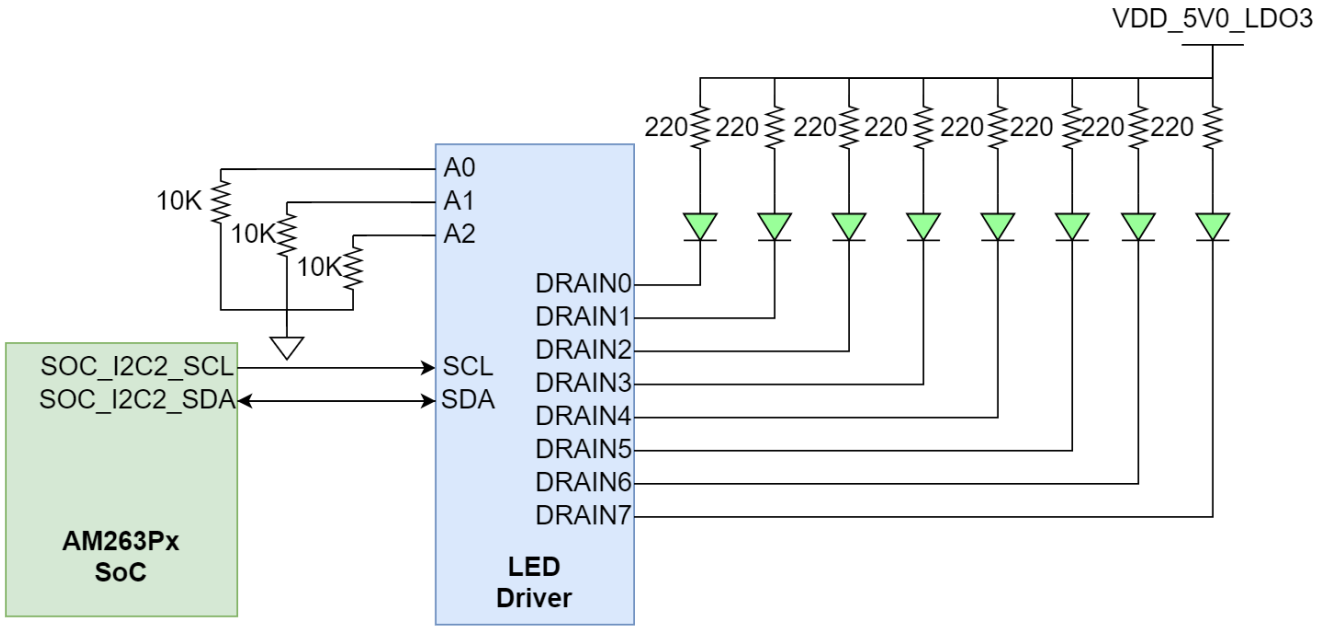

Figure 2-24. Industrial Application LED Driver

2.11.5 SPI

The AM263Px Control Card maps two SPI instances (SPI0,SPI1) from the AM263Px SoC to the HSEC 180 pin connector. Series termination resistors are placed near the SoC for each SPI clock signal.

There is 4-channel FET Switch that routes SPI1 between the PMIC and the HSEC Connector. This FET Switch has the select line driven by SPI1_MUX_SEL of the IO Expander. Additionally, there is an external pull-down resistor on the Select line such that the PMIC routing for the SPI signals is the default state.

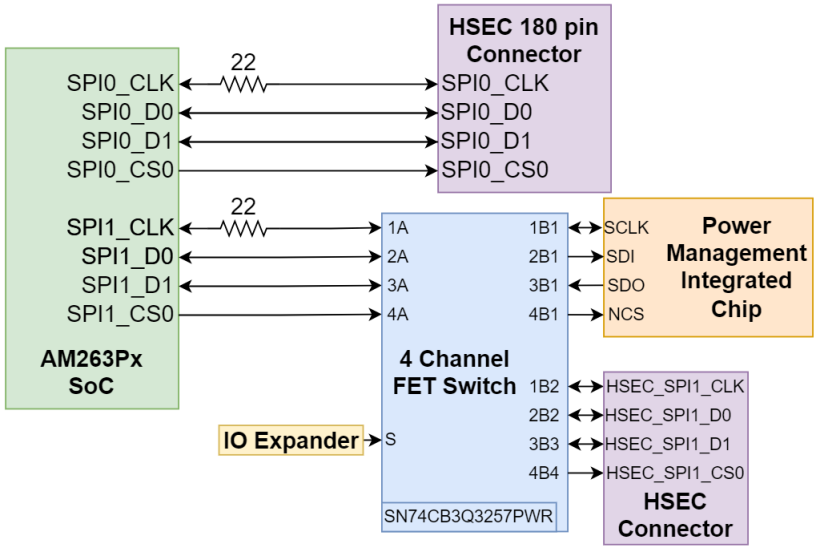

Figure 2-25. SPI

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2.11.6 UART

The AM263Px Control Card uses the XDS110 as a USB2.0 to UART bridge for terminal access. UART0 transmit and receive signals of the AM263Px SoC are mapped to the XDS110 with a dual channel isolation buffer (ISO7221CDR) for translating from the 3.3V IO voltage supply (VSYS_3V3C) to the 3.3V XDS supply. The XDS110 is connected to a micro-B USB connector for the USB 2.0 signals. ESD protection is provided to the USB 2.0 signals by a transient voltage suppression device (TPD4E004DRYR). The VBUS 5V power of the micro-B USB connector is mapped to a low dropout regulator (TPS79601DRBR) to generate the 3.3V XDS supply. A separate 3.3V supply for the XDS110 allows for the emulator to maintain a connection when power to the Control Card is removed.

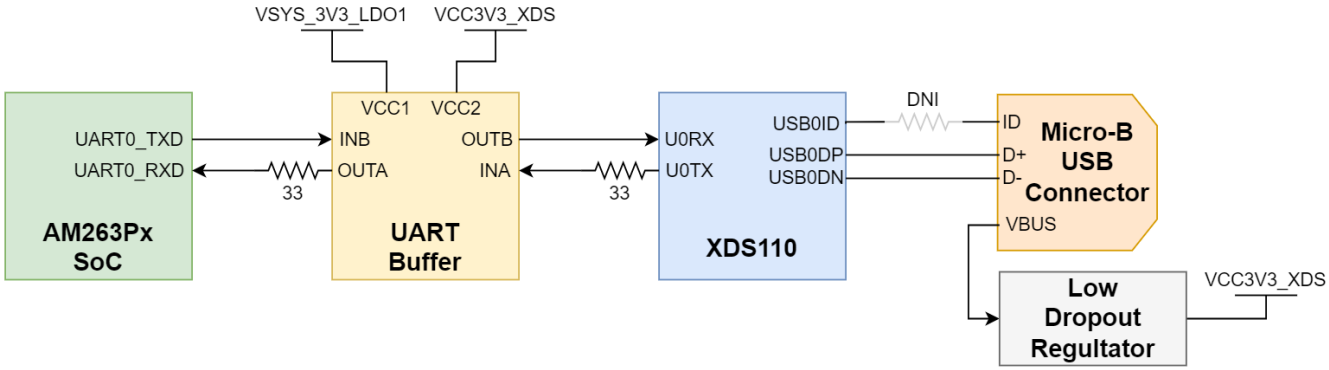

Figure 2-26. UART-USB Bridge for Emulation

The Control Card supports an additional UART1 and UART2 instance that has the transmit and receive signals mapped from the AM263Px SoC to the HSEC connector. To make use of UART1, the select line of a 1:2 mux must be high. The select line is driven by a GPIO signal (LIN_MUX_SEL) that is sourced from the IO expander. To make use of UART2, the select line of a 1:2 mux must be high. The select line is driven by a GPIO signal (UART2_MUX_SEL) that is sourced from the IO expander.

Table 2-20. UART Mux Select Logic

Instance	Select	Condition	Function
UART1	LOW	LIN Selected	A→B1
	HIGH	HSEC UART1 Selected	A→B2
UART2	LOW	SOC_INTn/USER_LED0 Selected	A→B1
	HIGH	HSEC UART2 Selected	A→B2

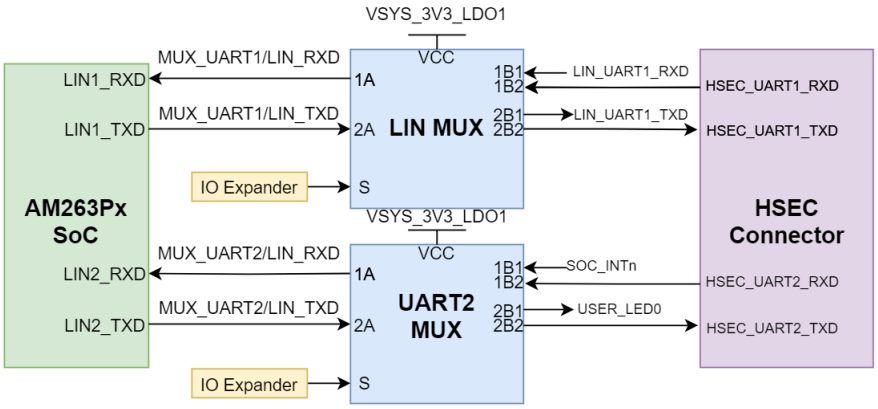

Figure 2-27. UART 1:2 MUX to HSEC

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2.11.7 MCAN

The Control Card is equipped with a single MCAN transceiver (TCAN1024H-Q1) that is connected to the MCAN4 interface of the AM263Px SoC. The MCAN5 interface of the AM263Px SoC is mapped directly to the HSEC connector.

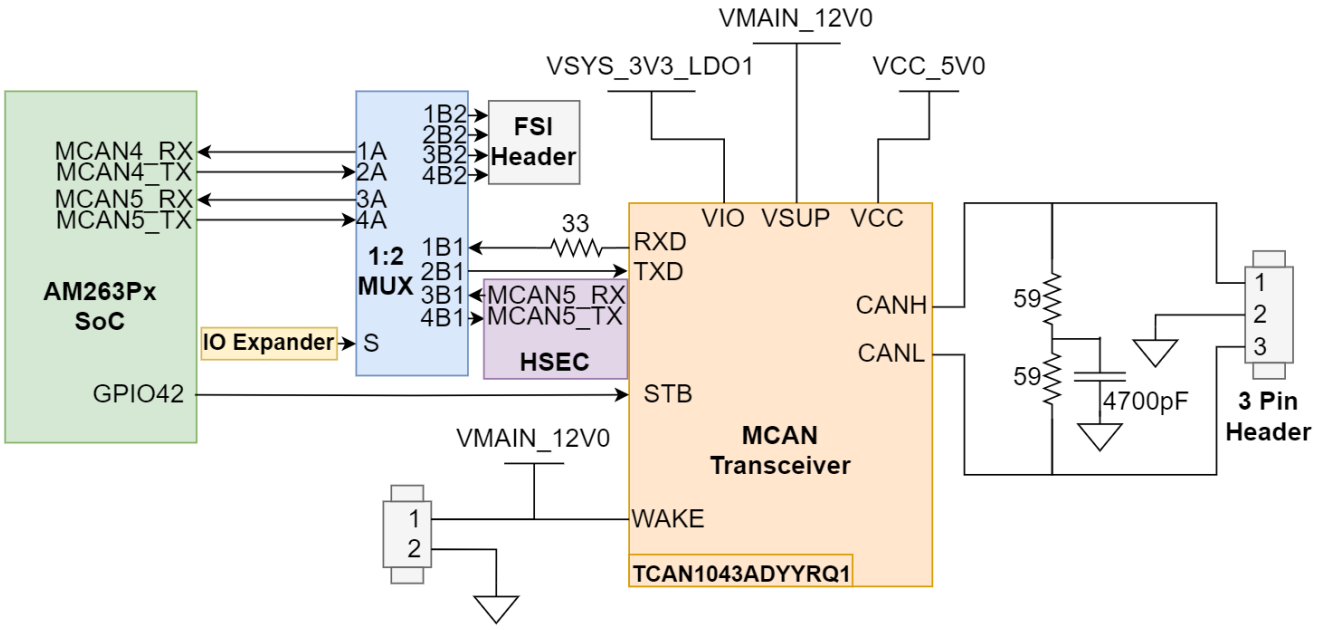

Figure 2-28. MCAN Transceiver

The MCAN transceiver has three power inputs, VIO is the transceiver I/O level shifting supply voltage and VCC is the transceiver 5 V supply voltage, and VSUP is the 12 V supply voltage. The SoC CAN data transmit data input is mapped to TXD of the transceiver and the CAN receive data output of the transceiver is mapped to the MCAN RX signal of the SoC with a series termination resistor close to the transceiver.

The standby control signal is a GPIO signal sourced from the IO expander. The STB control input is active high and a pull-down resistor is used to have the transceiver operate in normal mode as opposed to the standby mode that is default due to a weak internal pull up.

The system has a 120 Ω split termination on the CANH and CANL signals to improve EMI performance. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions.

The low and high level CAN bus input output lines are terminated to a three pin header.

The MCAN signals go through a 1:2 signal routing mux. There is a pull-down resistor on the select line of the mux and therefore the MCAN signal routing is the default.

Table 2-21. MCAN and FSI Mux

Select	Condition	Function
Low (default)	MCAN signals selected	A → B1
High	FSI signals selected	A → B2

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2.11.8 FSI

The AM263Px Control Card supports a fast serial interface by terminating the SoC signals to a 10 pin header. The interface has two lines of data and a clock line for both the receive and transmit signals. The header is connected to the 3.3 V IO voltage supply (VSYS_3V3_LDO1).

The FSI signals go through a 1:2 signal routing mux. There is a pull-up resistor on the select line of the mux and therefore the FSI signal routing is the default. To use MCAN4 and MCAN5, the FSI_MUX_SEL GPIO of the IO expander must be configured as a logic low output.

Table 2-22. MCAN and FSI Mux

Select	Condition	Function
Low	MCAN signals selected	A → B1
High (default)	FSI signals selected	A → B2

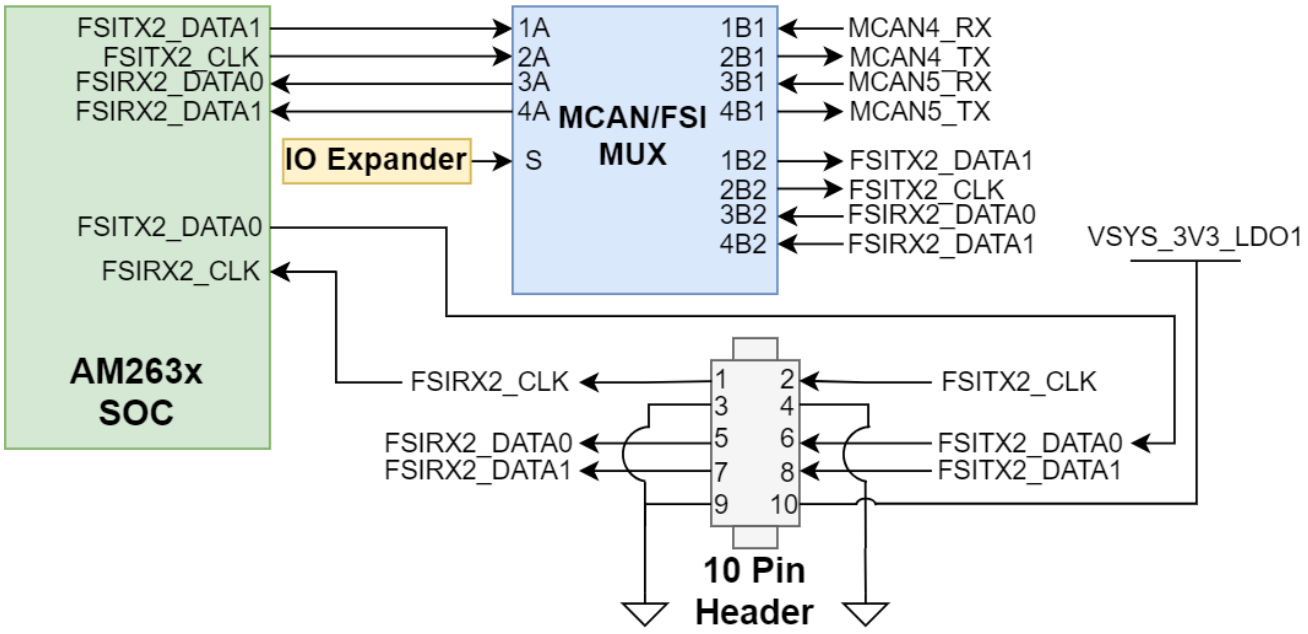

Figure 2-29. FSI Header

2.11.9 JTAG

The AM263Px Control Card includes an XDS110 class on-board emulator. The control card also has the option to map the JTAG signals from the AM263Px SoC to the HSEC connector.

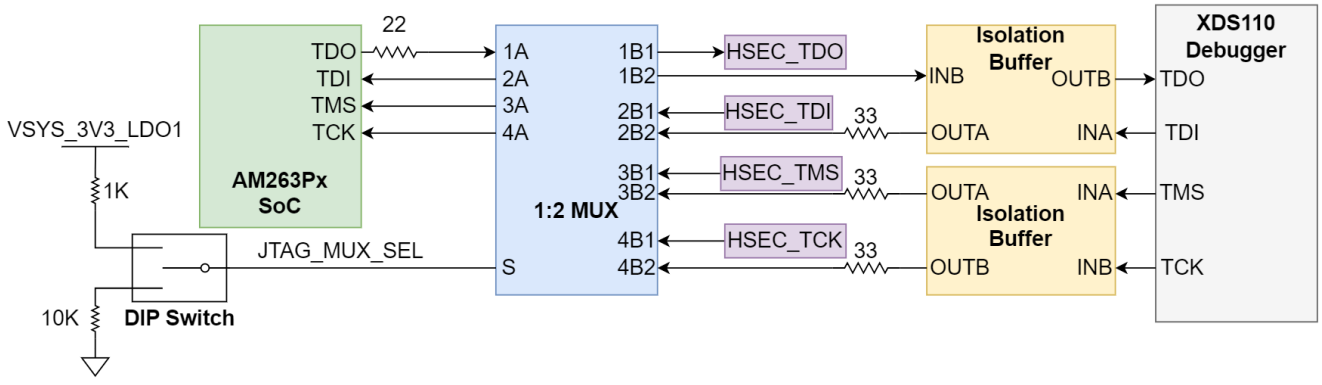

Figure 2-30. JTAG

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A DIP switch (SW1) is used to drive the select line of a 1:2 mux (SN74CB3Q3257PWR) that determines the pathing of the AM263Px SoC JTAG signals.

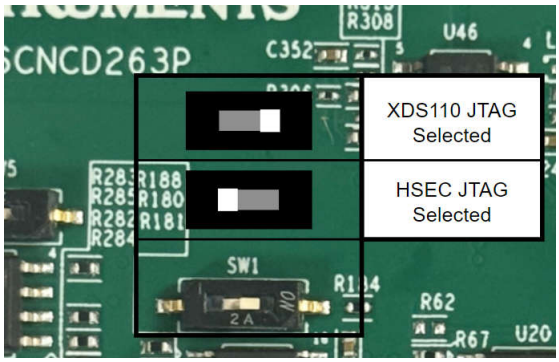

Figure 2-31. JTAG Path Switch

The Control Card includes all circuitry needed for XDS110 emulation. The emulator uses a USB 2.0 micro-B connector to interface the USB 2.0 signals that are created from the UART-USB bridge. The VBUS power from the connector is used to power the emulation circuit so that the connection to the emulator is not lost when power to the Control Card is removed.

The XDS110 controls two power status LED's. For more information refer to Section 2.2.2.

2.11.10 Test Automation Header

The AM263Px Control Card supports a 40 pin test automation header that allows an external controller to manipulate basic operations such as power down, PORz, warm reset, and bootmode control.

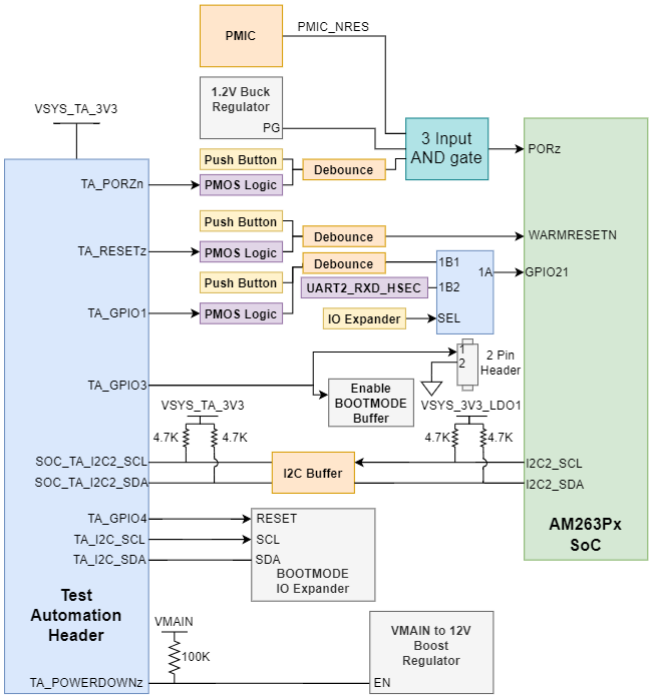

Figure 2-32. Test Automation Header

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The Test Automation Circuit is powered by a dedicated 3.3 V power supply (VSYS_TA_3V3) that is generated by a 5 V to 3.3 V buck regulator (TPS62177DQCR).

The AM263Px SoC I2C2 instance is connected to both the Test Automation Header and the bootmode IO expander (TCA6408ARGTR).

Table 2-23 details the Test Automation GPIO mapping:

Table 2-23. Test Automation Header GPIO Mapping

Signal Name	Description	Direction
TA_POWERDOWN	when logic low, disables the 3.3 V buck regulator (TPS62913RPUR) that is used in the first stage of DC/DC conversion	Output
TA_PORZn	when logic low, connects the PORz signal to ground due to the PMOS V_GS being less than zero creating a power on reset to the MAIN domain	Output
TA_RESETz	when logic low, connects the WARMRESETn signal to ground due to the PMOS V_GS being less than zero creating a warm reset to the MAIN domain	Output
TA_GPIO1	when logic low, connects the INTn signal to ground due to the PMOS V_GS being less than zero creating an interrupt to the SoC	Output
TA_GPIO3	when logic low, disables the bootmode buffer output enable	Output
TA_GPIO4	Reset signal for Bootmode IO Expander (TCA6408ARGTR)	Output

2.11.11 LIN

The AM263Px Control Card supports Local Interconnect Network communication through the use of a LIN transceiver (TLIN2029-Q1) that outputs the LIN Bus to the second pin of a 3 pin header.

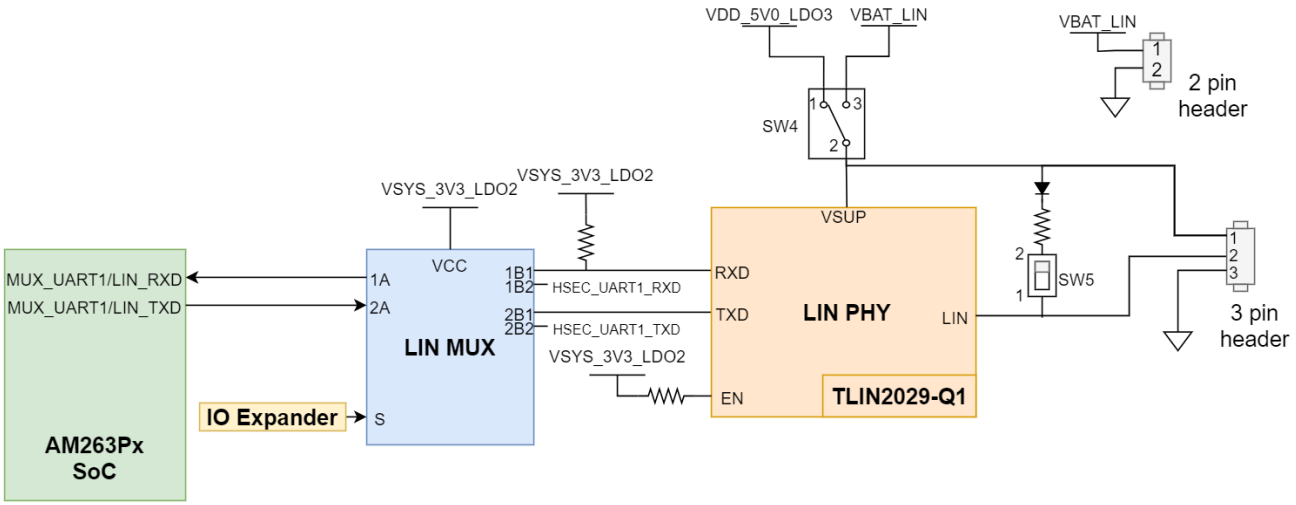

Figure 2-33. LIN PHY

The LIN transmit and receive signals are internally muxed on the AM263Px with the UART1 transmit and receive signals. Because of the internal muxing, there is an external 1:2 mux (SN74CB3Q3257PWR) which has a select line that is driven by the GPIO Expander.

Table 2-24. LIN MUX Select Logic

Select Logic	Condition	Function
LOW	LIN Selected	A→B1
HIGH	HSEC UART Selected	A→B2

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The AM263Px SoC does not have an integrated pull up for the LIN RX signal, therefore, an external pull up resistor is needed to the processor I/O supply voltage is required.

The AM263Px Control Card includes a double pole single throw switch (SW4) to control the voltage supply for the LIN Transceiver.

Table 2-25. LIN Switch Logic

LIN Voltage Switch Position	Voltage Supply Selected
Pin 1-2	VMAIN, 5 V supply output from either the USB-C connection or HSEC power connection.
Pin 2-3	VBAT_LIN, external voltage supply from pin 1 of 2 pin header

There is also a single pole throw switch (SW5) that drives the LIN Node application.

Table 2-26. LIN Node Application Switch

LIN Node Application Switch Position	LIN Node Application
Pin 1	Device node application
Pin 2	Controller node application

The Control Card pulls up the enable pin of the LIN transceiver for the transceiver to be in normal operational mode when the I/O Voltage supply is brought up.

2.11.12 MMC

The AM263Px Control Card provides a micro SD card interface that is mapped to the MMC0 instance of the AM263Px SoC.

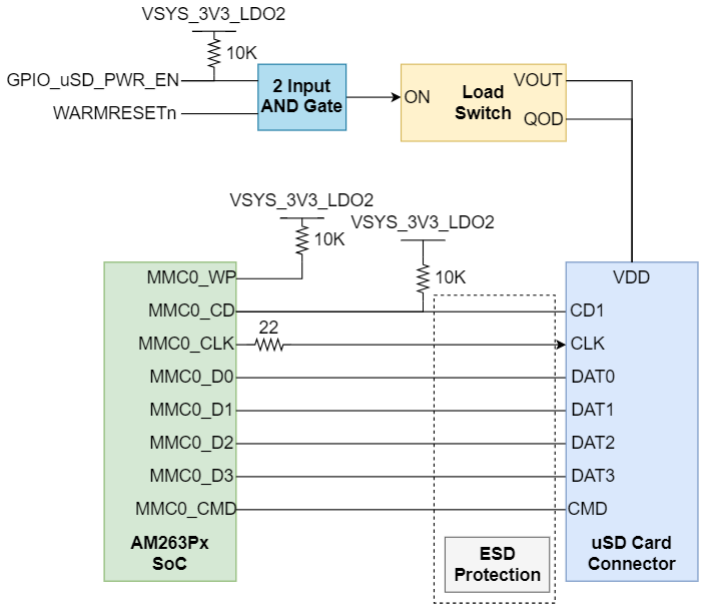

Figure 2-34. Micro-SD Connector Interface

A load switch (TPS22918DBVR) is used to power the micro SD card connector. The load switch is driven by the output of a 2-input AND gate between WARMRESETn and GPIO_uSD_PWR_EN to power cycle the card upon reset. The load switch uses quick output discharge (QOD) to verify that the supply voltage reaches <10% of nominal value during reset.

Inline ESD protection is provided for the MMC signals in the form of a six channel transient voltage suppressor device (TPD6E001RSER).

The Write Protect (WP) and Card Detect (CD) signals of the SD card connector are pulled up to the 3.3 V IO voltage supply. A series termination resistor is provided for the MMC clock signal.

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2.11.13 ADC and DAC

The AM263Px Control Card supports 24 ADC signal channels that are mapped for the AM263Px SoC and terminated to the HSEC connector. All ADC signals are ESD protected (TPD4E001DBVR).

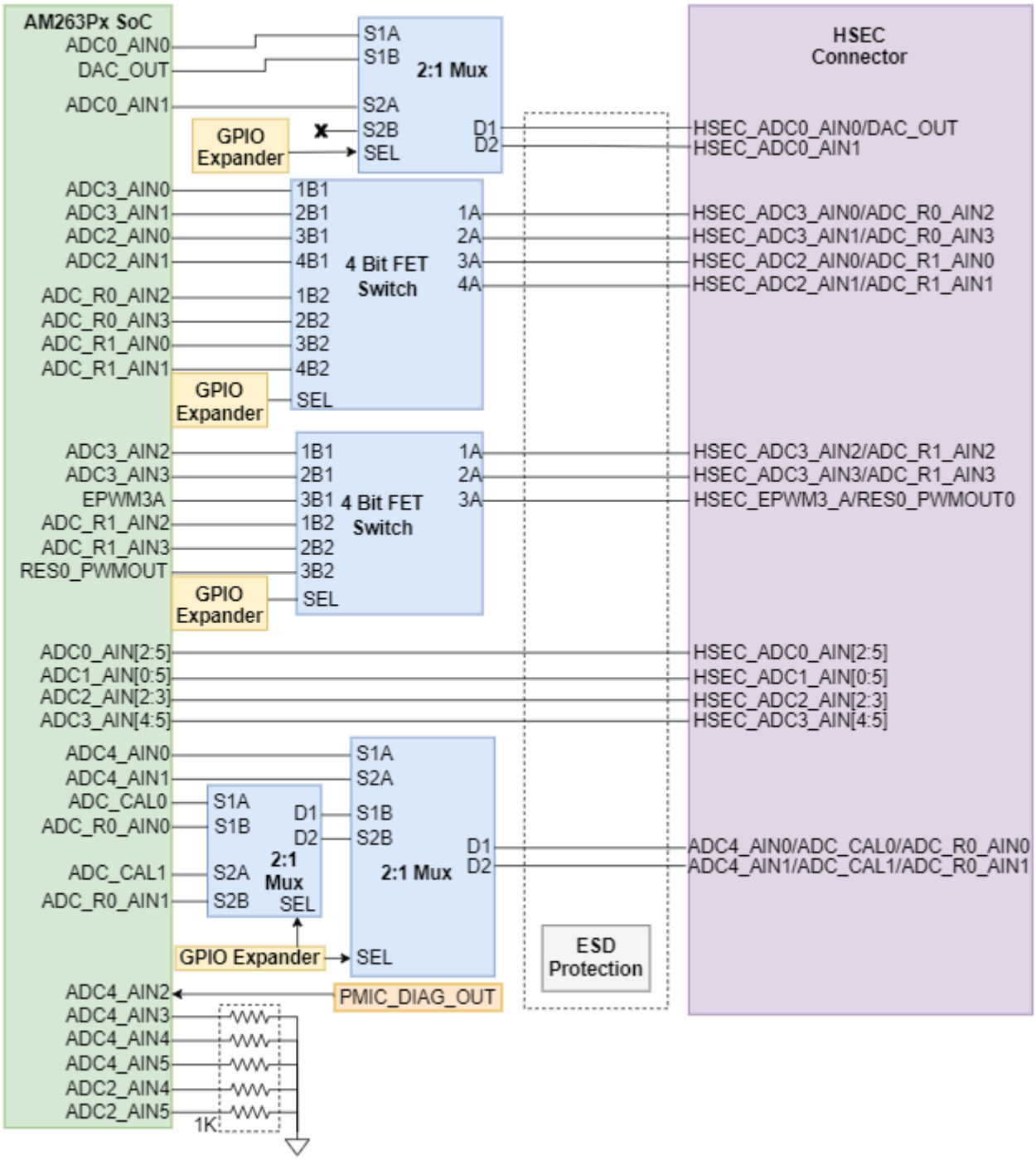

Figure 2-35. E1 ADC HSEC Connections

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There are two muxes (TMUX1136DQAR) that determine the pathing of ADC signals to and from the HSEC Connector.

Table 2-27. E1 ADC MUX Select Logic

MUX Select Signal	Condition	Function	Description
ADC1_MUX_SEL	SEL Signal HIGH	S1A → D1	HSEC_ADC0_AIN0 selected
		S2A → D2	HSEC_ADC0_AIN1 selected
	SEL Signal LOW	S1B → D1	HSEC_DAC_OUT selected
		S2B → D2	HSEC_DAC_OUT selected
ADC2_MUX_SEL	SEL Signal HIGH	S1A → D1	HSEC_ADC4_AIN0 selected
		S2A → D2	HSEC_ADC4_AIN1 selected
	SEL Signal LOW	S1B → D1	ADC_CAL0 selected
		S2B → D2	ADC_CAL1 selected

There are three switches that are used to configure the reference voltages for the ADC and DAC.

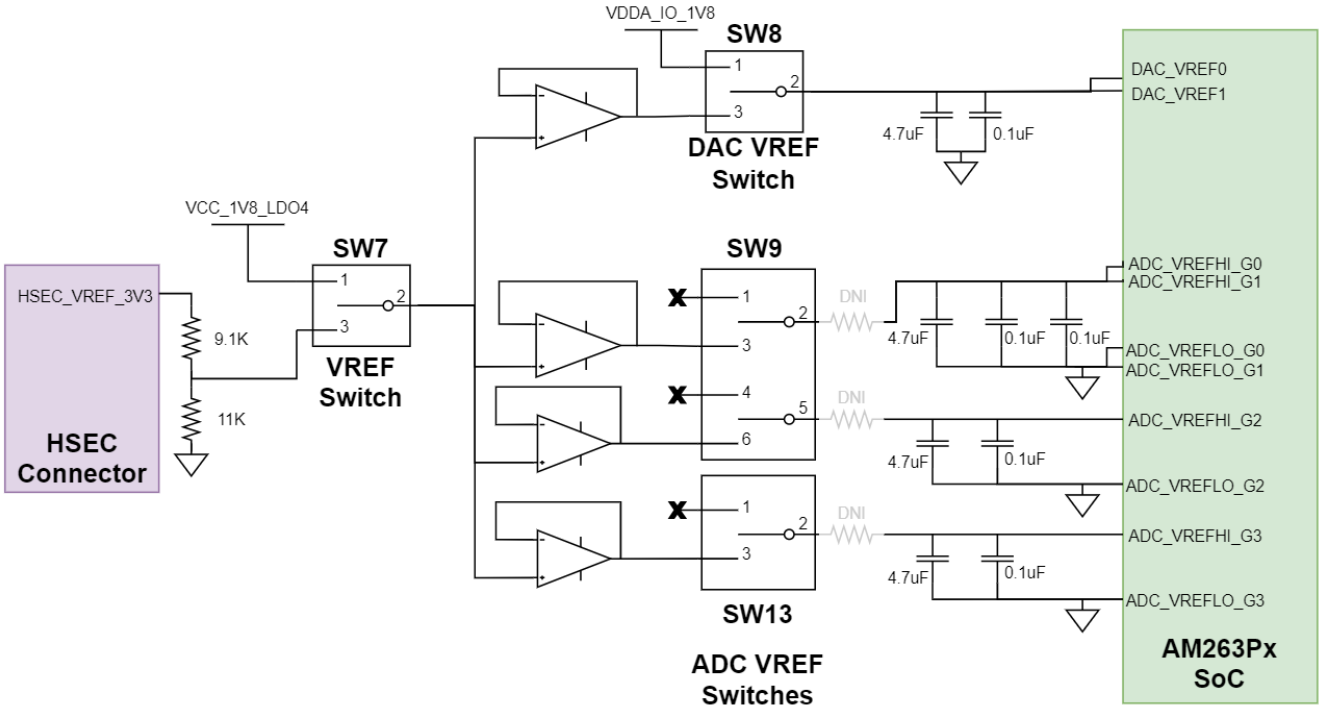

Figure 2-36. ADC Switch Routing

- The VREF Switch (SW7) is a single pole double throw switch that controls which 1.8 V reference is used for ADC and DAC.

Table 2-28. VREF Switch

VREF Switch Position	Reference Selection
Pin 1-2	On board 1.8 V Reference (REF3318AIDBZT)
Pin 2-3	HSEC VREF

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- The DAC VREF Switch (SW8) is a single pole double throw switch that controls the input for the DAC VREF inputs of the AM263Px SoC.

Table 2-29. DAC VREF Switch

DAC VREF Switch Position	Reference Selection
Pin 1-2	AM263Px on-die LDO
Pin 2-3	Output of VREF Switch

- The ADC VREF Switch (SW9) contains two single pole double throw switches that control the input for the ADC VREF inputs of the AM263Px SoC.

Table 2-30. ADC VREF Switch

ADC VREF Switch Position	Reference Selection
Pin 1-2	OPEN - Allow for reference to be AM263Px on-die LDO reference
Pin 2-3	Output of VREF Switch
Pin 4-5	OPEN - Allow for reference to be AM263Px on-die LDO reference
Pin 5-6	Output of VREF Switch

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2.12 HSEC Pinout and Pinmux Mapping

Table 2-31 shows the pinout of the 180 High-Speed Edge Connector and all available pinmux options for each pin. Table 2-32 shows all AM263Px balls and the available pinmux mode options for each ball.

Table 2-31. HSEC Pinout

Pin #	Ball	Package Signal Name	Muxed Signal Options		Muxed Signal Options	Signal Package Name	Ball	Pin #
1		NC	NC		NC	NC		2
3	D5	HSEC_TMS	TMS		NC	NC		4
5	B3	HSEC_TCK	TCK		TDO	HSEC_TDO	C4	6
7		GND	GND		TDI	HSEC_TDI	C5	8
9	V15/ T5	HSEC_ADC0_AIN0/ DAC_OUT	HSEC_ADC0_AIN0/DAC_OUT		GND	GND		10
11	U15/ T5	HSEC_ADC0_AIN1/ DAC_OUT	HSEC_ADC0_AIN1/DAC_OUT		ADC1_AIN0	ADC1_AIN0	T11	12
13		GND	GND		ADC1_AIN1	ADC1_AIN1	U11	14
15	T14	ADC0_AIN2	ADC0_AIN2		GND	GND		16
17	U14	ADC0_AIN3	ADC0_AIN3		ADC1_AIN2	ADC1_AIN2	T12	18
19		GND	GND		ADC1_AIN3	ADC1_AIN3	V12	20
21	U13	ADC0_AIN4	ADC0_AIN4		GND	GND		22
23	R14	ADC0_AIN5	ADC0_AIN5		ADC1_AIN4	ADC1_AIN4	U12	24
25	U6/ U16	ADC4_AIN0/ADC_CAL0	ADC4_AIN0/ADC_CAL0		ADC1_AIN5	ADC1_AIN5	R12	26
27	V5/T 15	ADC4_AIN1/ADC_CAL1	ADC4_AIN1/ADC_CAL1		ADC3_AIN0/ADC_R0_AIN2	ADC3_AIN0/ ADC_R0_AIN2	U7/ U18	28
29		GND	GND		ADC3_AIN1/ADC_R0_AIN3	ADC3_AIN1/ ADC_R0_AIN3	U8/ T17	30
31	R10/ R16	ADC2_AIN0/ ADC_R1_AIN0	ADC2_AIN0/ADC_R1_AIN0		GND	GND		32
33	T10/ R18	ADC2_AIN1/ ADC_R1_AIN1	ADC2_AIN1/ADC_R1_AIN1		ADC3_AIN2/ADC_R1_AIN2	ADC3_AIN2/ ADC_R1_AIN2	T7/ P18	34
35		GND	GND		ADC3_AIN3/ADC_R1_AIN3	ADC3_AIN3/ ADC_R1_AIN3	R7/ P17	36
37	U10	ADC2_AIN2	ADC2_AIN2		GND	GND		38
39	T9	ADC2_AIN3	ADC2_AIN3		ADC3_AIN4	ADC3_AIN4	V8	40
41		NC	NC		ADC3_AIN5	ADC3_AIN5	U9	42
43		GND	GND		NC	NC		44
45		HSEC_VREF_3V3	HSEC_VREF_3V3		GND	GND		46
47		GND	GND		HSEC_5V0	HSEC_5V0		48
49	B2	EPWM0_A	EPWM0_A, GPIO43		EPWM2_A, GPIO47, EPWM2_A	EPWM2_A	C2	50
51	B1	EPWM0_B	EPWM0_B, GPIO44		EPWM2_B, GPIO48, EPWM2_B	EPWM2_B	C1	52
53	D3	EPWM1_A	EPWM1_A, GPIO45		EPWM3_A, GPIO49, EPWM3_A	EPWM3_A	E2	54
55	D2	EPWM1_B	EPWM1_B, GPIO46, EPWM4_B		EPWM3_B, GPIO50, EPWM6_A	EPWM3_B	E3	56
57	D1	EPWM4_A	EPWM4_A, GPIO51		EPWM6_A, SPI5_D0, FSIRX1_CLK, GPIO55, EPWM3_B	EPWM6_A	E1	58
59	E4	EPWM4_B	EPWM4_B, FSITX1_CLK, GPIO52, EPWM1_B		EPWM6_B, SPI5_D1, FSIRX1_D0, GPIO56, EPWM6_B	EPWM6_B	F3	60
61	F2	EPWM5_A	EPWM5_A, SPI5_CS0, FSITX1_D0, GPIO53		EPWM7_A, SPI6_CS0, FSIRX1_D1, GPIO57, EPWM7_A	EPWM7_A	F4	62

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Table 2-31. HSEC Pinout (continued)

Pin #	Ball	Package Signal Name	Muxed Signal Options		Muxed Signal Options	Signal Package Name	Ball	Pin #
63	G2	EPWM5_B	EPWM5_B, SPI5_CLK, FSITX1_D1, GPIO54, EPWM8_B		EPWM7_B, SPI6_CLK, GPIO58, EPWM5_B	EPWM7_B	F1	64
65		GND	GND		NC	NC		66
67	C10	SPI0_D0	SPI0_D0, FSITX0_D0, GPIO13, CHANNEL2		PR0_PRU1_GPIO19, UART3_RXD, PR0_IEP0_EDC_SYNC_OUT0, TRC_CLK, XBAROUT13, GPIO119, EQEP1_A	EQEP1_A	D15	68
69	B11	SPI0_D1	SPI0_D1, FSITX0_D1, GPIO14, CHANNEL3		PR0_PRU1_GPIO18, UART3_TXD, PR0_IEP0_EDIO_DATA_IN_OUT31, TRC_CTL, XBAROUT14, GPIO120, EQEP1_B	EQEP1_B	C15	70
71	A11	SPI0_CLK	SPI0_CLK, UART3_TXD, LIN3_TXD, FSITX0_CLK, GPIO12, CHANNEL1		CLKOUT1, GPIO122, SDFM0_CLK0, EQEP1_STROBE	EQEP1_STROBE	B16	72
73	C11	SPI0_CS0	SPI0_CS0, UART3_RXD, LIN3_RXD, GPIO11, CHANNEL0		EXT_REFCLK0, XBAROUT15, GPIO121, EQEP1_INDEX	EQEP1_INDEX	P2	74
75	B10	SPI1_D0	SPI1_D0, UART5_TXD, XBAROUT3, FSIRX0_D0, GPIO17, CHANNEL6		LIN1_RXD, UART1_RXD, SPI2_CS0, OSPI_ECC_FAIL, XBAROUT5, GPIO19, OSPI_RESET_OUT1	UART1_RXD	A9	76
77	D9	SPI1_D1	SPI1_D1, UART5_RXD, XBAROUT4, FSIRX0_D1, GPIO18, CHANNEL7		LIN1_TXD, UART1_TXD, SPI2_CLK, OSPI_RESET_OUT0, XBAROUT6, GPIO20	UART1_TXD	B9	78
79	A10	SPI1_CLK	SPI1_CLK, UART4_RXD, LIN4_RXD, XBAROUT2, FSIRX0_CLK, GPIO16, CHANNEL5		EPWM10_A, UART1_CTSn, SPI7_D0, MCAN5_RX, FSIRX2_D0, GPIO63, EPWM7_B	MCAN5_RX	G4	80
81	C9	SPI1_CS0	SPI1_CS0, UART4_TXD, LIN4_TXD, XBAROUT1, GPIO15, CHANNEL4		EPWM10_B, UART2_RTSn, SPI7_D1, MCAN5_TX, OSPI_RESET_OUT0, FSIRX2_D1, GPIO64, EPWM10_B	MCAN5_TX	J3	82
83		GND	GND		HSEC_5V0	HSEC_5V0		84
85	C8	I2C1_SDA	I2C1_SDA, SPI3_CLK, XBAROUT8, GPIO24		EPWM11_A, UART2_CTSn, OSPI_ECC_FAIL, MCAN6_RX, OSPI_RESET_OUT1, OSPI_CSn0, GPIO65	EPWM11_A	H1	86
87	D7	I2C1_SCL	I2C1_SCL, SPI3_CS0, XBAROUT7, GPIO23		NC	NC		88
89	L17	EPWM21_A	PR0_MDIO0_MDIO, EPWM21_A, GPIO85, EPWM21_A		PR0_MDIO0_MDC, EPWM21_B, GPIO86, EPWM21_B	EPWM21_B	L18	90
91	D14	SDFM0_D0	PR0_ECAP0_APWM_OUT, GPIO123, SDFM0_D0		I2C0_SDA, GPIO134, EQEP2_A, SDFM1_CLK2	EQEP2_A	B13	92
93	A13	EQEP2_B	I2C0_SCL, GPIO135, EQEP2_B, SDFM1_CLK3		MCAN2_RX, UART2_RTSn, GPIO137, EQEP2_INDEX, SDFM1_D3	EQEP2_INDEX	A12	94
95	B12	EQEP2_STROBE	MCAN2_TX, UART1_RTSn, GPIO136, EQEP2_STROBE, SDFM1_D2		NC	NC		96
97		GND	GND		MDIO0_MDIO, GPIO41	HSEC_GPIO	N16	98
99	D13	SDFM0_D1	PR0_PRU1_GPIO17, UART5_CTSn, PR0_IEP0_EDIO_DATA_IN_OUT30, GPIO125, SDFM0_D1		UART4_CTSn, SPI4_CS0, GPIO131, EQEP0_B, SDFM1_D0	EQEP0_B	A14	100
101	A16	SDFM0_CLK1	PR0_PRU1_GPIO7, CPTS0_TS_SYNC, UART5_RTSn, PR0_IEP0_EDC_SYNC_OUT1, I2C3_SDA, GPIO124, SDFM0_CLK1		UART4_RTSn, SPI4_CLK, GPIO130, EQEP0_A, SDFM1_CLK0	EQEP0_A	B14	102
103	C13	SDFM0_D2	UART5_RXD, GPIO127, SDFM0_D2, CHANNEL0		UART4_TXD, LIN4_TXD, SPI4_D0, GPIO132, EQEP0_STROBE, SDFM1_CLK1, CHANNEL2	EQEP0_STROBE	C12	104
105	B15	SDFM0_CLK2	UART5_TXD, I2C3_SCL, GPIO126, SDFM0_CLK2, CHANNEL8		UART4_RXD, LIN4_RXD, SPI4_D1, GPIO133, EQEP0_INDEX, SDFM1_D1, CHANNEL3	EQEP0_INDEX	D11	106
107	C14	SDFM0_D3	MCAN3_RX, GPIO129, SDFM0_D3, CHANNEL1		PR0_PRU0_GPIO5, RMII2_RX_ER, MII2_RX_ER, EPWM22_A, GPIO87, EPWM22_A	MII0_RXER	G17	108
109	A15	SDFM0_CLK3	MCAN3_TX, UART5_RXD, GPIO128, SDFM0_CLK3, CHANNEL9		PR0_PRU0_GPIO9, PR0_UART0_CTSn, MII2_COL, EPWM22_B, GPIO88	MII0_COL	F17	110
111		GND	GND		HSEC_5V0	HSEC_5V0		112
113		PMIC_SAFE_OUT1	PMIC_SAFE_OUT1		PMIC_WKUP1	PMIC_WKUP1		114
115		NC	NC		NC	NC		116
117		VCC_5V0	VCC_5V0		HSEC_5V0	HSEC_5V0		118
119		VSYS_3V3_LDO1	VSYS_3V3_LDO1		PORz	PORz		120
121	G18	ICSS_MII0_CRS	PR0_PRU0_GPIO10, RMII2_CRS_DV, PR0_UART0_RTSn, MII2_CRS, EPWM23_A, GPIO89, EPWM22_B		PR0_PRU0_GPIO8, EPWM23_B, GPIO90, EPWM29_A	ICSS_MII0_RXLINK	G15	122
123	K15	ICSS_MII0_RXCLK	PR0_PRU0_GPIO6, RMII2_REF_CLK, RGMII2_RXC, MII2_RXCLK, EPWM24_A, GPIO91, EPWM24_A		PR0_PRU0_GPIO4, RGMII2_RX_CTL, MII2_RXDV, EPWM24_B, GPIO92, EPWM24_B	ICSS_MII0_RXDV	K16	124

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Table 2-31. HSEC Pinout (continued)

Pin #	Ball	Package Signal Name	Muxed Signal Options		Muxed Signal Options	Signal Package Name	Ball	Pin #
125	K17	ICSS_MII0_RXD0	PR0_PRU0_GPIO0, RMII2_RXD0, RGMII2_RD0, MII2_RXD0, EPWM25_A, GPIO93, EPWM25_A		PR0_PRU0_GPIO1, RMII2_RXD1, RGMII2_RD1, MII2_RXD1, EPWM25_B, GPIO94, EPWM25_B	ICSS_MII0_RXD1	K18	126
127	J18	ICSS_MII0_RXD2	PR0_PRU0_GPIO2, RGMII2_RD2, MII2_RXD2, EPWM26_A, GPIO95, EPWM26_A		PR0_PRU0_GPIO3, RGMII2_RD3, MII2_RXD3, EPWM26_B, GPIO96, EPWM26_B	ICSS_MII0_RXD3	J17	128
129	H18	ICSS_MII0_TXCLK	PR0_PRU0_GPIO16, RGMII2_TXC, MII2_TXCLK, EPWM27_A, GPIO97, EPWM27_A		PR0_PRU0_GPIO15, RMII2_TX_EN, RGMII2_TX_CTL, MII2_TX_EN, EPWM27_B, GPIO98	ICSS_MII0_TXEN	L16	130
131	M16	ICSS_MII0_TXD0	PR0_PRU0_GPIO11, RMII2_TXD0, RGMII2_TD0, MII2_TXD0, EPWM28_A, GPIO99, EPWM28_A		PR0_PRU0_GPIO12, RMII2_TXD1, RGMII2_TD1, MII2_TXD1, EPWM28_B, GPIO100, EPWM28_B	ICSS_MII0_TXD1	M15	132
133	H17	ICSS_MII0_TXD2	PR0_PRU0_GPIO13, RGMII2_TD2, MII2_TXD2, EPWM29_A, GPIO101, EPWM27_B		PR0_PRU0_GPIO14, RGMII2_TD3, MII2_TXD3, EPWM29_B, GPIO102, EPWM29_B	ICSS_MII0_TXD3	H16	134
135		GND	GND		NC	NC		136
137	F15	ICSS_MII1_RXER	PR0_PRU1_GPIO5, SPI5_CS0, TRC_DATA0, EPWM30_A, GPIO103, CHANNEL6, EPWM30_A		PR0_PRU1_GPIO9, SPI5_CLK, PR0_UART0_RXD, TRC_DATA1, EPWM30_B, GPIO104, CHANNEL7	ICSS_MII1_COL	C18	138
139	D17	ICSS_MII1_CRS	PR0_PRU1_GPIO10, SPI5_D0, PR0_UART0_TXD, TRC_DATA2, EPWM31_A, GPIO105, RES0_PWMOUT0, EPWM31_A		PR0_PRU1_GPIO8, SPI5_D1, TRC_DATA3, EPWM31_B, GPIO106, RES0_PWMOUT1, EPWM31_B	ICSS_MII1_RXLINK	D18	140
141	E16	ICSS_MII1_RXCLK	PR0_PRU1_GPIO6, MCAN0_RX, FSITX2_CLK, TRC_DATA4, GPIO107		PR0_PRU1_GPIO4, MCAN0_TX, FSITX2_D0, TRC_DATA5, GPIO108	ICSS_MII1_RXDV	F16	142
143	F18	ICSS_MII1_RXD0	PR0_PRU1_GPIO0, MCAN1_RX, FSITX2_D1, TRC_DATA6, GPIO109, EPWM23_A		PR0_PRU1_GPIO1, MCAN1_TX, FSIRX2_CLK, TRC_DATA7, GPIO110	ICSS_MII1_RXD1	G16	144
145	E17	ICSS_MII1_RXD2	PR0_PRU1_GPIO2, MCAN4_RX, FSIRX2_D0, TRC_DATA8, GPIO111		PR0_PRU1_GPIO3, MCAN4_TX, FSIRX2_D1, TRC_DATA9, GPIO112, EPWM23_B	ICSS_MII1_RXD3	E18	146
147	C16	ICSS_MII1_TXCLK	PR0_PRU1_GPIO16, MCAN5_RX, FSITX3_CLK, TRC_DATA10, GPIO113		PR0_PRU1_GPIO15, MCAN5_TX, FSITX3_D0, TRC_DATA11, GPIO114	ICSS_MII1_TXEN	A17	148
149	B18	ICSS_MII1_TXD0	PR0_PRU1_GPIO11, MCAN6_RX, SPI6_CS0, FSITX3_D1, TRC_DATA12, EPWM16_A, GPIO115		PR0_PRU1_GPIO12, MCAN6_TX, SPI6_CLK, FSIRX3_CLK, TRC_DATA13, EPWM16_B, GPIO116	ICSS_MII1_TXD1	B17	150
151	D16	ICSS_MII1_TXD2	PR0_PRU1_GPIO13, MCAN7_RX, SPI6_D0, FSIRX3_D0, TRC_DATA14, XBAROUT11, GPIO117, RES0_PWMOUT0		PR0_PRU1_GPIO14, MCAN7_TX, SPI6_D1, FSIRX3_D1, TRC_DATA15, XBAROUT12, GPIO118, RES0_PWMOUT1	ICSS_MII1_TXD3	C17	152
153	K4	HSEC_EPWM13_A	EPWM13_A, UART1_RIn, SPI7_CLK, OSPI_D3, GPIO69		EPWM13_B, UART1_DTRn, SPI7_D0, OSPI_ECC_FAIL, GPIO70, EPWM13_B	EPWM13_B	K3	154
155		NC	NC		NC	NC		156
157		GND	GND		HSEC_5V0	HSEC_5V0		158
159		NC	NC		NC	NC		160
161	B8	UART2_RXD	LIN2_RXD, UART2_RXD, SPI2_D0, GPIO21		LIN2_TXD, UART2_TXD, SPI2_D1, GPIO22	UART2_TXD	A8	162
163	B6	HSEC_MMC0_CLK	MMC_CLK, UART0_RXD, LIN0_RXD, MCAN0_RX, EPWM17_A, GPIO77, SDFM1_CLK0, EPWM17_A		MMC_CMD, UART0_TXD, LIN0_TXD, MCAN0_TX, EPWM17_B, GPIO78, SDFM1_D0, EPWM17_B	HSEC_MMC0_CMD	A4	164
165	B5	HSEC_MMC0_D0	MMC_DAT0, UART2_RXD, I2C1_SCL, MCAN1_RX, EPWM18_A, GPIO79, SDFM1_CLK1, EPWM18_A		MMC_DAT1, MCAN1_TX, EPWM18_B, GPIO80, SDFM1_D1, EPWM18_B	HSEC_MMC0_D1	B4	166
167	A3	HSEC_MMC0_D2	MMC_DAT2, UART2_TXD, I2C1_SDA, MCAN4_RX, EPWM19_A, GPIO81, SDFM1_CLK2, EPWM19_A		MMC_DAT3, UART3_RTSn, MCAN4_TX, EPWM19_B, GPIO82, SDFM1_D2, EPWM19_B	HSEC_MMC0_D3	A2	168
169	C6	HSEC_MMC0_WP	MMC_SDWP, UART0_RTSn, I2C2_SCL, MCAN5_RX, EPWM20_A, GPIO83, SDFM1_CLK3, EPWM20_A		MMC_SDCD, UART0_CTSn, I2C2_SDA, MCAN5_TX, EPWM20_B, GPIO84, SDFM1_D3, EPWM20_B	HSEC_MMC0_SDCD	A5	170
171		PMIC_COMP2_IN+	PMIC_COMP2_IN+		NC	PMIC_WKUP2		172
173		PMIC_COMP2_IN-	PMIC_COMP2_IN-		NC	NC		174
175		PMIC_COMP1_IN+	PMIC_COMP1_IN+		NC	NC		176
177		PMIC_COMP1_IN-	PMIC_COMP1_IN-		PMIC_SAFE_OUT2	PMIC_SAFE_OUT2		178
179		GND	GND		HSEC_5V0	HSEC_5V0		180

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Table 2-32. Pinmux Mapping Table

BALL	Pinlist	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9	Mode10
P1	OSPI0_CSn0	OSPI0_CSn0						OSPI_D0	GPIO0			
R3	OSPI0_CSn1	OSPI0_CSn1		MCAN5_TX		SPI4_CS1	XBAROUT0	UART2_RTSn	GPIO1	FSIRX2_D1		EPWM10_B
N2	OSPI0_CLK	OSPI0_CLK		MCAN7_RX		SPI7_CS0		UART3_CTSn	GPIO2			EPWM12_A
N1	OSPI0_D0	OSPI0_D0		MCAN7_TX		SPI7_CLK		UART1_DCDn	GPIO3			EPWM12_B
N4	OSPI0_D1	OSPI0_D1				SPI7_D0		UART1_RIn	GPIO4			EPWM13_A
M4	OSPI0_D2	OSPI0_D2						OSPI_D6	GPIO5			
P3	OSPI0_D3	OSPI0_D3						OSPI_D4	GPIO6			
M1	MCAN0_RX	MCAN0_RX	SPI4_CS0	OSPI_D4				OSPI_DQS	GPIO7			
L1	MCAN0_TX	MCAN0_TX	SPI4_CLK	OSPI_D5				OSPI_D2	GPIO8			
L2	MCAN1_RX	MCAN1_RX	SPI4_D0	OSPI_D6				OSPI_CLK	GPIO9			
K1	MCAN1_TX	MCAN1_TX	SPI4_D1	OSPI_D7		SPI7_D1		UART1_DTRn	GPIO10			EPWM13_B
C11	SPI0_CS0	SPI0_CS0	UART3_RXD	LIN3_RXD					GPIO11		CHANNEL0	
A11	SPI0_CLK	SPI0_CLK	UART3_TXD	LIN3_TXD				FSITX0_CLK	GPIO12		CHANNEL1	
C10	SPI0_D0	SPI0_D0						FSITX0_D0	GPIO13		CHANNEL2	
B11	SPI0_D1	SPI0_D1						FSITX0_D1	GPIO14		CHANNEL3	
C9	SPI1_CS0	SPI1_CS0	UART4_TXD	LIN4_TXD			XBAROUT1		GPIO15		CHANNEL4	
A10	SPI1_CLK	SPI1_CLK	UART4_RXD	LIN4_RXD			XBAROUT2	FSIRX0_CLK	GPIO16		CHANNEL5	
B10	SPI1_D0	SPI1_D0	UART5_TXD				XBAROUT3	FSIRX0_D0	GPIO17		CHANNEL6	
D9	SPI1_D1	SPI1_D1	UART5_RXD				XBAROUT4	FSIRX0_D1	GPIO18		CHANNEL7	
A9	LIN1_RXD	LIN1_RXD	UART1_RXD	SPI2_CS0	OSPI_ECC_FAIL		XBAROUT5		GPIO19	OSPI_RESET_OUT1		
B9	LIN1_TXD	LIN1_TXD	UART1_TXD	SPI2_CLK	OSPI_RESET_OUT0		XBAROUT6		GPIO20			
B8	LIN2_RXD	LIN2_RXD	UART2_RXD	SPI2_D0					GPIO21			
A8	LIN2_TXD	LIN2_TXD	UART2_TXD	SPI2_D1					GPIO22			
D7	I2C1_SCL	I2C1_SCL		SPI3_CS0			XBAROUT7		GPIO23			
C8	I2C1_SDA	I2C1_SDA		SPI3_CLK			XBAROUT8		GPIO24			
C7	UART0_RTSn	UART0_RTSn	I2C2_SCL	SPI3_D0	MCAN3_TX		XBAROUT9		GPIO25			
B7	UART0_CTSn	UART0_CTSn	I2C2_SDA	SPI3_D1	MCAN3_RX	SPI0_CS1	XBAROUT10		GPIO26			
A7	UART0_RXD	UART0_RXD	LIN0_RXD						GPIO27			
A6	UART0_TXD	UART0_TXD	LIN0_TXD						GPIO28			
R17	RGMII1_RXC	RGMII1_RXC	RMII1_REF_CLK	MII1_RXCLK				FSITX0_CLK	GPIO29	EQEP2_A		EPWM14_A
M18	RGMII1_TX_CTL	RGMII1_TX_CTL	RMII1_TX_EN	MII1_TX_EN				FSITX1_D0	GPIO36	EQEP0_STROBE		EPWM15_B
P16	RGMII1_TD0	RGMII1_TD0	RMII1_TXD0	MII1_TXD0				FSITX1_D1	GPIO37	EQEP1_A	EPWM15_A	EPWM15_B
M17	MDIO0_MDC	MDIO0_MDC							GPIO42			
B2	EPWM0_A	EPWM0_A							GPIO43			EPWM0_A
B1	EPWM0_B	EPWM0_B							GPIO44			EPWM0_B
D3	EPWM1_A	EPWM1_A							GPIO45			EPWM1_A
D2	EPWM1_B	EPWM1_B							GPIO46			EPWM4_B
C2	EPWM2_A	EPWM2_A							GPIO47			EPWM2_A
C1	EPWM2_B	EPWM2_B							GPIO48			EPWM2_B
E2	EPWM3_A	EPWM3_A							GPIO49			EPWM3_A

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Table 2-32. Pinmux Mapping Table (continued)

BALL	Pinlist	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9	Mode10
E3	EPWM3_B	EPWM3_B							GPIO50			EPWM6_A
D1	EPWM4_A	EPWM4_A							GPIO51			EPWM4_A
E4	EPWM4_B	EPWM4_B						FSITX1_CLK	GPIO52			EPWM1_B
F2	EPWM5_A	EPWM5_A			SPI5_CS0			FSITX1_D0	GPIO53			EPWM5_A
G2	EPWM5_B	EPWM5_B			SPI5_CLK			FSITX1_D1	GPIO54			EPWM8_B
E1	EPWM6_A	EPWM6_A			SPI5_D0			FSIRX1_CLK	GPIO55			EPWM3_B
F3	EPWM6_B	EPWM6_B			SPI5_D1			FSIRX1_D0	GPIO56			EPWM6_B
F4	EPWM7_A	EPWM7_A			SPI6_CS0			FSIRX1_D1	GPIO57			EPWM7_A
F1	EPWM7_B	EPWM7_B			SPI6_CLK				GPIO58			EPWM5_B
G3	EPWM8_A	EPWM8_A	UART4_TXD	I2C3_SDA	SPI6_D0			FSITX2_CLK	GPIO59			EPWM8_A
H2	EPWM8_B	EPWM8_B	UART4_RXD	I2C3_SCL	SPI6_D1			FSITX2_D0	GPIO60			EPWM9_B
G1	EPWM9_A	EPWM9_A			SPI7_CS0	MCAN4_RX		FSITX2_D1	GPIO61			EPWM9_A
J2	EPWM9_B	EPWM9_B	UART1_RTSn		SPI7_CLK	MCAN4_TX		FSIRX2_CLK	GPIO62			EPWM11_B
G4	EPWM10_A	EPWM10_A	UART1_CTSn		SPI7_D0	MCAN5_RX		FSIRX2_D0	GPIO63			EPWM7_B
J3	EPWM10_B	EPWM10_B	UART2_RTSn		SPI7_D1	MCAN5_TX	OSPI_RESET_OUT0	FSIRX2_D1	GPIO64			EPWM10_B
H1	EPWM11_A	EPWM11_A	UART2_CTSn	OSPI_ECC_FAIL		MCAN6_RX	OSPI_RESET_OUT1	OSPI_CSn0	GPIO65			EPWM11_A
J1	EPWM11_B	EPWM11_B	UART3_RTSn	OSPI_RESET_OUT0		MCAN6_TX		OSPI_D1	GPIO66			EPWM12_B
K2	EPWM12_A	EPWM12_A	UART3_CTSn	SPI4_CS1		MCAN7_RX		OSPI_D5	GPIO67			EPWM12_A
J4	EPWM12_B	EPWM12_B	UART1_DCDn	SPI7_CS0		MCAN7_TX		OSPI_D7	GPIO68			EPWM10_A
K4	EPWM13_A	EPWM13_A	UART1_RIn	SPI7_CLK				OSPI_D3	GPIO69			EPWM13_A
K3	EPWM13_B	EPWM13_B	UART1_DTRn	SPI7_D0				OSPI_ECC_FAIL	GPIO70			EPWM13_B
L3	UART1_RXD	UART1_RXD	LIN1_RXD	OSPI_LBCLKO			EPWM16_A		GPIO75			EPWM16_A
M3	UART1_TXD	UART1_TXD	LIN1_TXD	OSPI_DQS			EPWM16_B		GPIO76			EPWM16_B
B6	MMC_CLK	MMC_CLK	UART0_RXD	LIN0_RXD	MCAN0_RX		EPWM17_A		GPIO77	SDFM1_CLK0		EPWM17_A
A4	MMC_CMD	MMC_CMD	UART0_TXD	LIN0_TXD	MCAN0_TX		EPWM17_B		GPIO78	SDFM1_D0		EPWM17_B
B5	MMC_DAT0	MMC_DAT0	UART2_RXD	I2C1_SCL	MCAN1_RX		EPWM18_A		GPIO79	SDFM1_CLK1		EPWM18_A
B4	MMC_DAT1	MMC_DAT1			MCAN1_TX		EPWM18_B		GPIO80	SDFM1_D1		EPWM18_B
A3	MMC_DAT2	MMC_DAT2	UART2_TXD	I2C1_SDA	MCAN4_RX		EPWM19_A		GPIO81	SDFM1_CLK2		EPWM19_A
A2	MMC_DAT3	MMC_DAT3	UART3_RTSn		MCAN4_TX		EPWM19_B		GPIO82	SDFM1_D2		EPWM19_B
C6	MMC_SDWP	MMC_SDWP	UART0_RTSn	I2C2_SCL	MCAN5_RX		EPWM20_A		GPIO83	SDFM1_CLK3		EPWM20_A
A5	MMC_SDCD	MMC_SDCD	UART0_CTSn	I2C2_SDA	MCAN5_TX		EPWM20_B		GPIO84	SDFM1_D3		EPWM20_B
L17	PR0_MDIO0_MDIO	PR0_MDIO0_MDIO					EPWM21_A		GPIO85			EPWM21_A
L18	PR0_MDIO0_MDC	PR0_MDIO0_MDC					EPWM21_B		GPIO86			EPWM21_B
G17	PR0_PRU0_GPIO5	PR0_PRU0_GPIO5		RMII2_RX_ER		MII2_RX_ER	EPWM22_A		GPIO87			EPWM22_A
F17	PR0_PRU0_GPIO9	PR0_PRU0_GPIO9			PR0_UART0_CTSn	MII2_COL	EPWM22_B		GPIO88			
G18	PR0_PRU0_GPIO10	PR0_PRU0_GPIO10		RMII2_CRS_DV	PR0_UART0_RTSn	MII2_CRS	EPWM23_A		GPIO89			EPWM22_B
G15	PR0_PRU0_GPIO8	PR0_PRU0_GPIO8					EPWM23_B		GPIO90			EPWM29_A
K15	PR0_PRU0_GPIO6	PR0_PRU0_GPIO6		RMII2_REF_CLK	RGMII2_RXC	MII2_RXCLK	EPWM24_A		GPIO91			EPWM24_A

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Table 2-32. Pinmux Mapping Table (continued)

BALL	Pinlist	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9	Mode10
K16	PR0_PRU0_GPIO4	PR0_PRU0_GPIO4			RGMII2_RX_CTL	MII2_RXDV	EPWM24_B		GPIO92			EPWM24_B
K17	PR0_PRU0_GPIO0	PR0_PRU0_GPIO0		RMII2_RXD0	RGMII2_RD0	MII2_RXD0	EPWM25_A		GPIO93			EPWM25_A
K18	PR0_PRU0_GPIO1	PR0_PRU0_GPIO1		RMII2_RXD1	RGMII2_RD1	MII2_RXD1	EPWM25_B		GPIO94			EPWM25_B
J18	PR0_PRU0_GPIO2	PR0_PRU0_GPIO2			RGMII2_RD2	MII2_RXD2	EPWM26_A		GPIO95			EPWM26_A
J17	PR0_PRU0_GPIO3	PR0_PRU0_GPIO3			RGMII2_RD3	MII2_RXD3	EPWM26_B		GPIO96			EPWM26_B
H18	PR0_PRU0_GPIO16	PR0_PRU0_GPIO16			RGMII2_TXC	MII2_TXCLK	EPWM27_A		GPIO97			EPWM27_A
L16	PR0_PRU0_GPIO15	PR0_PRU0_GPIO15		RMII2_TX_EN	RGMII2_TX_CTL	MII2_TX_EN	EPWM27_B		GPIO98			
M16	PR0_PRU0_GPIO11	PR0_PRU0_GPIO11		RMII2_TXD0	RGMII2_TD0	MII2_TXD0	EPWM28_A		GPIO99			EPWM28_A
M15	PR0_PRU0_GPIO12	PR0_PRU0_GPIO12		RMII2_TXD1	RGMII2_TD1	MII2_TXD1	EPWM28_B		GPIO100			EPWM28_B
H17	PR0_PRU0_GPIO13	PR0_PRU0_GPIO13			RGMII2_TD2	MII2_TXD2	EPWM29_A		GPIO101			EPWM27_B
H16	PR0_PRU0_GPIO14	PR0_PRU0_GPIO14			RGMII2_TD3	MII2_TXD3	EPWM29_B		GPIO102			EPWM29_B
F15	PR0_PRU1_GPIO5	PR0_PRU1_GPIO5		SPI5_CS0		TRC_DATA0	EPWM30_A		GPIO103		CHANNEL6	EPWM30_A
C18	PR0_PRU1_GPIO9	PR0_PRU1_GPIO9		SPI5_CLK	PR0_UART0_RXD	TRC_DATA1	EPWM30_B		GPIO104		CHANNEL7	
D17	PR0_PRU1_GPIO10	PR0_PRU1_GPIO10		SPI5_D0	PR0_UART0_TXD	TRC_DATA2	EPWM31_A		GPIO105	RES0_PWMOUT0		EPWM31_A
D18	PR0_PRU1_GPIO8	PR0_PRU1_GPIO8		SPI5_D1		TRC_DATA3	EPWM31_B		GPIO106	RES0_PWMOUT1		EPWM31_B
E16	PR0_PRU1_GPIO6	PR0_PRU1_GPIO6	MCAN0_RX		FSITX2_CLK	TRC_DATA4			GPIO107			
F16	PR0_PRU1_GPIO4	PR0_PRU1_GPIO4	MCAN0_TX		FSITX2_D0	TRC_DATA5			GPIO108			
F18	PR0_PRU1_GPIO0	PR0_PRU1_GPIO0	MCAN1_RX		FSITX2_D1	TRC_DATA6			GPIO109			EPWM23_A
G16	PR0_PRU1_GPIO1	PR0_PRU1_GPIO1	MCAN1_TX		FSIRX2_CLK	TRC_DATA7			GPIO110			
E17	PR0_PRU1_GPIO2	PR0_PRU1_GPIO2	MCAN4_RX		FSIRX2_D0	TRC_DATA8			GPIO111			
E18	PR0_PRU1_GPIO3	PR0_PRU1_GPIO3	MCAN4_TX		FSIRX2_D1	TRC_DATA9			GPIO112			EPWM23_B
C16	PR0_PRU1_GPIO16	PR0_PRU1_GPIO16	MCAN5_RX		FSITX3_CLK	TRC_DATA10			GPIO113			
A17	PR0_PRU1_GPIO15	PR0_PRU1_GPIO15	MCAN5_TX		FSITX3_D0	TRC_DATA11			GPIO114			
B18	PR0_PRU1_GPIO11	PR0_PRU1_GPIO11	MCAN6_RX	SPI6_CS0	FSITX3_D1	TRC_DATA12	EPWM16_A		GPIO115			
B17	PR0_PRU1_GPIO12	PR0_PRU1_GPIO12	MCAN6_TX	SPI6_CLK	FSIRX3_CLK	TRC_DATA13	EPWM16_B		GPIO116			
D16	PR0_PRU1_GPIO13	PR0_PRU1_GPIO13	MCAN7_RX	SPI6_D0	FSIRX3_D0	TRC_DATA14	XBAROUT11		GPIO117	RES0_PWMOUT0		
C17	PR0_PRU1_GPIO14	PR0_PRU1_GPIO14	MCAN7_TX	SPI6_D1	FSIRX3_D1	TRC_DATA15	XBAROUT12		GPIO118	RES0_PWMOUT1		
D15	PR0_PRU1_GPIO19	PR0_PRU1_GPIO19		UART3_RXD	PR0_IEP0_EDC_SYNC_OUT0	TRC_CLK	XBAROUT13		GPIO119		EQEP1_A	
C15	PR0_PRU1_GPIO18	PR0_PRU1_GPIO18		UART3_TXD	PR0_IEP0_EDIO_DATA_IN_OUT31	TRC_CTL	XBAROUT14		GPIO120		EQEP1_B	
P2	EXT_REFCLK0	EXT_REFCLK0					XBAROUT15		GPIO121		EQEP1_INDEX	

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Table 2-32. Pinmux Mapping Table (continued)

BALL	Pinlist	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9	Mode10
B16	SDFM0_CLK0	CLKOUT1							GPIO122	SDFM0_CLK0	EQEP1_STROBE	
D14	SDFM0_D0	PR0_ECAP0_APWM_OUT							GPIO123	SDFM0_D0		
A16	SDFM0_CLK1	PR0_PRU1_GPIO7	CPTS0_TS_SYNC	UART5_RTSn	PR0_IEP0_EDC_SYNC_OUT1		I2C3_SDA		GPIO124	SDFM0_CLK1		
D13	SDFM0_D1	PR0_PRU1_GPIO17		UART5_CTSn	PR0_IEP0_EDIO_DATA_IN_OUT30				GPIO125	SDFM0_D1		
B15	SDFM0_CLK2	UART5_TXD					I2C3_SCL		GPIO126	SDFM0_CLK2	CHANNEL8	
C13	SDFM0_D2	UART5_RXD							GPIO127	SDFM0_D2	CHANNEL0	
A15	SDFM0_CLK3	MCAN3_TX	UART5_RXD						GPIO128	SDFM0_CLK3	CHANNEL9	
C14	SDFM0_D3	MCAN3_RX							GPIO129	SDFM0_D3	CHANNEL1	
B14	EQEP0_A	UART4_RTSn			SPI4_CLK				GPIO130	EQEP0_A	SDFM1_CLK0	
A14	EQEP0_B	UART4_CTSn			SPI4_CS0				GPIO131	EQEP0_B	SDFM1_D0	
C12	EQEP0_STROBE	UART4_TXD	LIN4_TXD		SPI4_D0				GPIO132	EQEP0_STROBE	SDFM1_CLK1	CHANNEL2
D11	EQEP0_INDEX	UART4_RXD	LIN4_RXD		SPI4_D1				GPIO133	EQEP0_INDEX	SDFM1_D1	CHANNEL3
B13	I2C0_SDA	I2C0_SDA							GPIO134	EQEP2_A	SDFM1_CLK2	
A13	I2C0_SCL	I2C0_SCL							GPIO135	EQEP2_B	SDFM1_CLK3	
B12	MCAN2_TX	MCAN2_TX	UART1_RTSn						GPIO136	EQEP2_STROBE	SDFM1_D2	
A12	MCAN2_RX	MCAN2_RX	UART2_RTSn						GPIO137	EQEP2_INDEX	SDFM1_D3	
M2	CLKOUT0	CLKOUT0							GPIO138			
C3	WARMRSTn	WARMRSTn										
D4	SAFETY_ERRORn	SAFETY_ERRORn										
C5	TDI	TDI										
C4	TDO	TDO										
D5	TMS	TMS										
B3	TCK	TCK										
LB	OSPI_CLKLB	OSPI_CLKLB										
R2	PORz	PORz										
T1	XTAL_XI	XTAL_XI										
R1	XTAL_XO	XTAL_XO										
V15	ADC0_AIN0	ADC0_AIN0										
U15	ADC0_AIN1	ADC0_AIN1										
T14	ADC0_AIN2	ADC0_AIN2										
U14	ADC0_AIN3	ADC0_AIN3										
U13	ADC0_AIN4	ADC0_AIN4										
R14	ADC0_AIN5	ADC0_AIN5										
T11	ADC1_AIN0	ADC1_AIN0										
U11	ADC1_AIN1	ADC1_AIN1										
T12	ADC1_AIN2	ADC1_AIN2										
V12	ADC1_AIN3	ADC1_AIN3										
U12	ADC1_AIN4	ADC1_AIN4										

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Table 2-32. Pinmux Mapping Table (continued)

BALL	Pinlist	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9	Mode10
R12	ADC1_AIN5	ADC1_AIN5										
R10	ADC2_AIN0	ADC2_AIN0										
T10	ADC2_AIN1	ADC2_AIN1										
U10	ADC2_AIN2	ADC2_AIN2										
T9	ADC2_AIN3	ADC2_AIN3										
V9	ADC2_AIN4	ADC2_AIN4										
T8	ADC2_AIN5	ADC2_AIN5										
U7	ADC3_AIN0	ADC3_AIN0										
U8	ADC3_AIN1	ADC3_AIN1										
T7	ADC3_AIN2	ADC3_AIN2										
R7	ADC3_AIN3	ADC3_AIN3										
V8	ADC3_AIN4	ADC3_AIN4										
U9	ADC3_AIN5	ADC3_AIN5										
U6	ADC4_AIN0	ADC4_AIN0										
V5	ADC4_AIN1	ADC4_AIN1										
V4	ADC4_AIN2	ADC4_AIN2										
U5	ADC4_AIN3	ADC4_AIN3										
V3	ADC4_AIN4	ADC4_AIN4										
U4	ADC4_AIN5	ADC4_AIN5										
V14	ADC_VREFHI_G0	ADC_VREFHI_G0										
V13	ADC_VREFLO_G0	ADC_VREFLO_G0										
V10	ADC_VREFHI_G1	ADC_VREFHI_G1										
V11	ADC_VREFLO_G1	ADC_VREFLO_G1										
V6	ADC_VREFHI_G2	ADC_VREFHI_G2										
V7	ADC_VREFLO_G2	ADC_VREFLO_G2										
U16	ADC_CAL0	ADC_CAL0										
T15	ADC_CAL1	ADC_CAL1										
T13	DAC_VREF0	DAC_VREF0										
T6	DAC_VREF1	DAC_VREF1										
T5	DAC_OUT	DAC_OUT										
U1	RSVD_U1	RSVD_U1										
U2	VSYS_MON	VSYS_MON										
U3	RSVD_U3	RSVD_U3										
V2	RSVD_V2	RSVD_V2										
U17	ADC_CAL2	ADC_CAL2										
T18	ADC_R0_AIN0	ADC_R0_AIN0										
T16	ADC_R0_AIN1	ADC_R0_AIN1										
U18	ADC_R0_AIN2	ADC_R0_AIN2										
T17	ADC_R0_AIN3	ADC_R0_AIN3										
V16	ADC_VREFLO_G3	ADC_VREFLO_G3										
V17	ADC_VREFHI_G3	ADC_VREFHI_G3										

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Table 2-32. Pinmux Mapping Table (continued)

BALL	Pinlist	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7	Mode8	Mode9	Mode10
R16	ADC_R1_AIN0	ADC_R1_AIN0										
R18	ADC_R1_AIN1	ADC_R1_AIN1										
P18	ADC_R1_AIN2	ADC_R1_AIN2										
P17	ADC_R1_AIN3	ADC_R1_AIN3										
N17	ADC_CAL3	ADC_CAL3										

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3 Hardware Design Files

To download the zip file containing the latest design files for the EVM, click the following link.

4 Additional Information

4.1 If You Need Assistance

If you have any feedback or questions, support for the Sitara MCUs and the AM263Px Control Card development kit is provided by the TI Product Information Center (PIC) and the TI E2E™ Forum. Contact information for the PIC can be found on the TI website. Additional device-specific information can be found in Section 6.1.

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5 Related Documentation

5.1 Supplemental Content

5.1.A E1 Board Modifications

1. OSPI Modification - Implemented to all E1 boards out-of-box.

   The initial design of the AM263Px Control Card E1 included a 2.5 inch stub hanging off of the OSPI DQ0 and DQ1 signal lines. These stubs lead to unreliable use of the OSPI peripheral. Below is a list of the modifications that were carried out on all E1 versions of the Control Card.

   - Cut the OSPI DQ0 and DQ1 traces on the outside of the vias next to the termination resistors and the mux.
   - Solder a blue wire from R91 to U80 pin 4.
   - Solder a blue wire from R90 to U80 pin 3.
   - Solder one side of the 10 kΩ resistor to each of the blue wires added above.
   - Remove R122 and R119.
   - Add blue wire from R91 bluewire 10 kΩ resistor to R122 pad closest to U48.
   - Add blue wire from R90 bluewire 10 kΩ resistor to R119 pad closest to U48.
2. CPSW Ethernet Modification - Must be implemented by the user.

Note

This modification was not done to the E1 boards.

Note

This does not apply to E2 versions of the board and beyond.

Note

The board has the PRU0 MII0 signals routed by default to enable CPSW RGMII2. The following modifications need to be followed

Note

The MCAN transceiver and on-board Ethernet cannot be used simultaneously on the E1 version of the AM263Px Control Card.

The E1 AM263Px Control Card had a blue-wire fix to enable the CPSW RGMII2 Gigabit ethernet port with the associated MDIO. The changes are listed below:

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- **Routing MDIO0_MDIO to the on-board Ethernet PHY:**
  - Remove R208 and solder wire from exposed pad that is not connected to L17 of the SoC to HSEC pin 96.
- **Routing MDIO0_MDC to the on-board Ethernet PHY:**
  - Remove R466 and solder wire from R466 pad tied to MCAN1_STB signal.
  - Remove R211 and solder the other end of the MCAN1_STB wire to the R211 exposed pad that is not connected to L18 of the SoC.
- **TCAN1043 Enable driven low**
  - Since MCAN1_STB is now routed for MDIO0_MDC, the MCAN transceiver needs to be disabled to avoid any leakage current along the MCAN1_STB trace.

5.1.B E2 Design Changes

The AM263Px Control Card had various design changes for the E2 revision of the board. The changes are listed below:

1. **Added MDIO/MDC Analog switches to control where MDIO signals are routed.**
2. **Added various LED indicators**
   - SoC SAFETY_ERRORn LED (LD19) to indicate when PORz is pressed
   - Added additional power status LEDs for PMIC LDO outputs (LD20, LD21, LD22)
3. **Added jumper (J22) for CAN INH signal routing to PMIC**
4. **Select line default state for FSI/MCAN Mux (U33) changed from High to Low**
5. **Added additional muxing for Ethernet port and MDIO signal routing**
6. **Signals rearranged on ADC MUXs**

6 References

6.1 Reference Documents

In addition to this document, the following references are available for download at www.ti.com.

- *AM263P4 Sitara™ Microcontrollers*
- *AM263Px Sitara™ Microcontrollers Data Sheet*
- *AM263Px Sitara™ Microcontrollers Technical Reference Manual*
- *AM263Px Sitara™ Microcontrollers TRM Register Addendum*
- *Texas Instruments Code Composer Studio*
- *Updating XDS110 Firmware*

6.2 Other TI Components Used in This Design

This Control Card uses various other TI components for the functions. A consolidated list of these components with links to the TI product pages is shown below.

- *TPS212x Power MUX*
- *LM3488 Boost DC-DC Converter*
- *TUSB320LAI USB Type-C Configuration Channel Logic and Port Control*
- *TPS62177 Step-Down Converter*
- *TPS62903 Buck Converter*
- *INA228 Current Monitor with I2C Interface*
- *TPS62097 Step-Down Converter*
- *TLV755P Low Dropout Regulator*
- *TPS22918 Load Switch*
- *TMP411 Temperature Sensor*
- *TCAN1043A-Q1 CAN FD Transceiver*
- *XDS110 JTAG Debug Probe*
- *DP83869HM 10/100/1000 Ethernet Physical Layer Transceiver*
- *LMK1C110x LVCMOS Clock Buffer*
- *TLIN2029-Q1 LIN Transceiver*

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7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2023) to Revision A (January 2024)	Page
• Added updated Component identification diagrams for E2	5
• Added a note about E2 Changes to Control Card Power Tree	11
• Added the *Clock* section to describe the clocking options and the clock tree routing	17
• Changed Boot mode switch reference designator	18
• Changed reference designator in *Ethernet Routing* table	26
• Updated reference designator of switch	37
• Updated reference designators for ADC/DAC switches	39
• Updated HSEC Pinout for E2 Pinout	42

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FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

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(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

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Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

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https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

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2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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