

EVM User's Guide: AM2754, AM2754-Q1, AM2752, AM2752-Q1

AM275x Evaluation Module User's Guide



Description

The AM275x evaluation module (EVM) is a standalone test, development and evaluation platform that lets developers evaluate AM275x functionality and develop prototypes for a variety of applications. The AM275x EVM is equipped with an AM275x microcontroller along with additional components to allow the user to make use of the various device interfaces including the Ethernet™, dual CAN-FD and others to easily create prototypes. Onboard current measurement capabilities are available to monitor power consumption for power-conscious applications. The supplied USB cable paired with embedded emulation logic allows for emulation and debugging using standard development tools such as Code Composer Studio™ (CCSTUDIO).

Features

- Powered through two 5V, 3A USB Type-C® input
- Multirail power supply designed for safety-relevant Applications
- Multi-channel stereo ADC and DAC input/output lines.
- Two Audio expansion connectors
- Two Ethernet add-on board connector for an automotive or industrial Ethernet PHY
- On-board XDS110 debug probe
- Four push buttons:
 - PORz
 - RESETz
 - User Interrupt
 - IO Retention Wake
- Two LEDs for user testing
- CAN connectivity with on-board CAN transceiver
- MMC interface to micro SD card connector
- On-board memory
 - 512 Mb OSPI NOR flash
 - 1 Kb I2C EEPROM
 - 512 Mb HYBERBUS HYPERRAM
 - 256Gb eMMC™ Flash



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1 Evaluation Module Overview

1.1 Introduction

The AM275x EVM was developed to enable easy and rapid prototyping of the AM275 EVM and all of the peripherals. There are several on-board transceiver and PHYs to enable the many interfaces of the AM275x SoC (System on a Chip). This user's guide details the design of the EVM and how to properly use each interface. The user's guide also details many important aspects of the board including but not limited to pin header descriptions, test points, and mux/switch signal routing.

1.2 Preface Read This First

1.2.1 Important Usage Notes

Note

This is the first revision of the User Guide and more content will be added in a short time to fully complete the user guide content. For any questions or points of clarity, refer to [E2E®](#)

Note

If only the red power status LED (LD14) is on during power-up then the connected power supply is not able to successfully negotiate power delivery with the PD controller on the EVM. This means that the power-up sequence will not be initiated and that connecting to the SoC will not be possible. A PD-capable power adapter is required for this EVM.

Note

The E1 revision of the EVM has a known issue surrounding BOOTMODE8 logic during power-up and reset. BOOTMODE8 has two buffers that can both drive during bootup and created unexpected states on BOOTMODE8. With BOOTMODE8 in an unexpected state, any bootmode that depends on BOOTMODE8 configuration will be affected. Please refer to the [Boot Mode Selection](#) chapter for more details on bootmode configuration.

Ensure that J22 is not connected during power-up and reset to have proper BOOTMODE8 values.

All other bootmode signals and configurations are unaffected.

Note

External power supply or power accessory requirements:

- Nominal output voltage: 5-VDC
 - Max output current: 3000mA
 - Efficiency Level V
-

Note

TI recommends using an external power supply or accessory which complies with applicable regional safety standards such as (by example) UL, CSA, VDE, CCC, PSE.

1.3 Kit Contents

The AM275x Evaluation module kit contains the following items:

- AM275x Evaluation module board
- Type-A to Micro-B USB cable (1 meter length)
- USB Type-C 5V/3A AC/DC cable

Note

The maximum length of the IO cables shall not exceed 3 meters.

Not included:

- Standoffs
- USB Power delivery enabled power supply

1.4 Device Information

The AM275x family of highly-integrated, high-performance microcontrollers is based on the Arm® Cortex™ R5F and C7x floating point DSP cores. The microcontrollers enable original equipment manufacturers (OEM) and original design manufacturers (ODM) to quickly bring to market devices with robust software support and rich user interfaces. The device offers the maximum flexibility of a fully integrated, mixed processor design

The AM275x features extensive audio interfacing with 5x McASP peripherals. Peripherals supporting system level connectivity is included, such as 2-port Gigabit Ethernet, USB, OSPI/QSPI, CAN-FD, UARTs, SPI and GPIOs. The AM275x supports the latest cybersecurity requirements with the built-in Hardware Security Module (HSM). The dual-core R5Fs are arranged in one or two cluster subsystems with 128KB TCM per cluster (64KB per core) and up to two C7x DSP cores with 2.25MB of L2 SRAM per C7x DSP, greatly reducing the need for external memory.

1.4.1 Security

The AM275x EVM features a High Security, Field Securable (HS-FS) device. An HS-FS device has the ability to use a one time programming to convert the device from HS-FS to High Security, Security Enforced (HS-SE).

The AM275x device leaves the TI factory in an HS-FS state where customer keys are not programmed and has the following attributes:

- Does not enforce the secure boot process
- R5 and C7 JTAG ports are open
- Security Subsystem firewalls are closed
- SoC Firewalls are open
- ROM Boot expects a TI signed binary (encryption is optional)
- TIFS-MCU binary is signed by the TI private key

The One Time Programmable (OTP) keywriter converts the secure device from HS-FS to HS-SE. The OTP keywriter programs customer keys into the device eFuses to enforce secure boot and establish a root of trust. The secure boot requires an image to be encrypted, which is optional, and signed using customer keys, which is verified by the SoC. A secure device in the HS-SE state has the following attributes:

- C7, R5 JTAG ports are both closed
- Security subsystems and SoC firewalls are both closed
- TIFS-MCU and SBL need to be signed with active customer key

1.5 Audio Expansion Connectors

The AM275x EVM features two symmetric shielded 80-pin Audio Expansion Connectors (AEC1 & AEC2) for external Audio device interfacing. AEC1 and AEC2 are placed at fixed distances and specific locations on the left and right side of the AM275x EVM.

The AEC Pinout includes:

- Interspersed Ground Pins to limit EMI
- Audio
 - 2x McASP instances
 - 8 Serializers for both instances
 - transmit and receive bit clock/frame sync for both instances
 - Reference clock input/output to/from the daughter card
 - 2x eCAP inputs
- General Connectivity
 - SPI, I2C, MCAN, UART
- Power
 - 5V, I/O VDD
- 3x PWM Channels
- Up to 47 GPIOs
- 10x Reserved pins for futureproofing

For more information on Audio expansion connectors refer to the [AEC Mapping](#) chapter.

2 Hardware

2.1 Component Identification

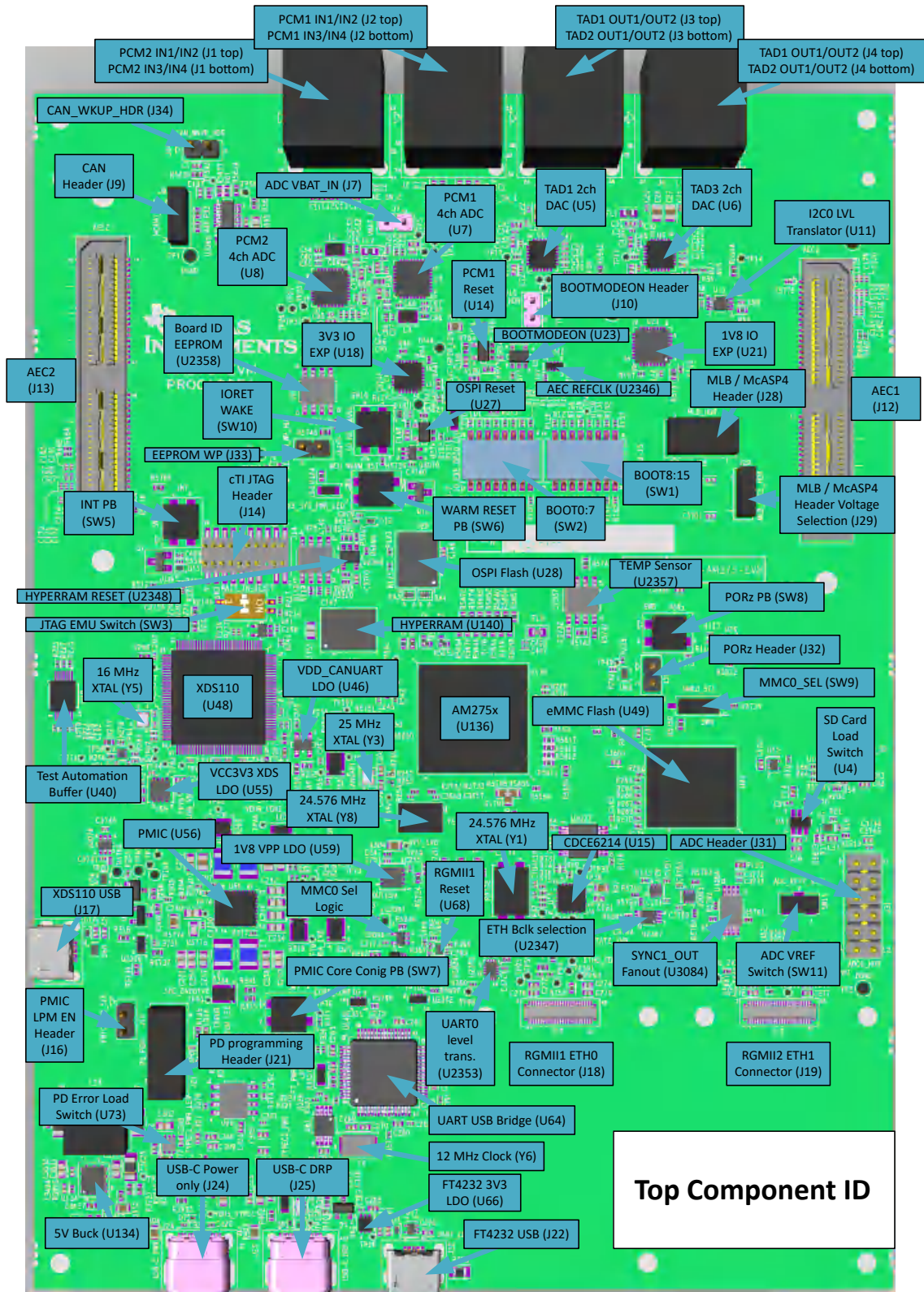


Figure 2-1. Top Component Identification

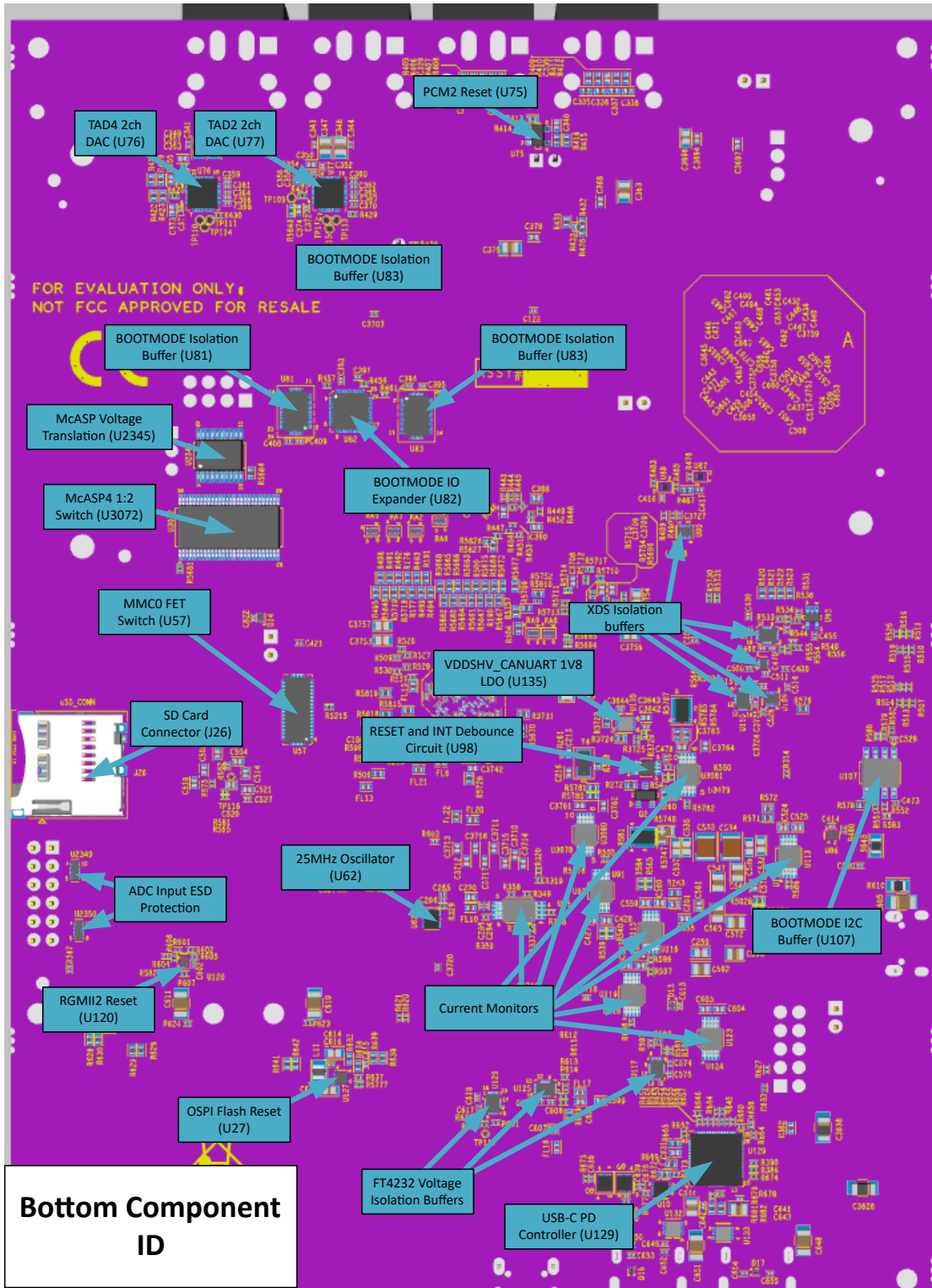


Figure 2-2. Bottom Component ID

2.2 Power Requirements

The AM275x EVM is powered from either of two USB Type-C inputs. The following sections describe the power distribution network topology that supply the AM275x EVM, supporting components and the reference voltages.

Power supply designs that are compatible with the AM275x EVM:

- Power delivery enabled power adapter with USB-C® receptacle
- Power delivery enabled power adapter with captive USB-C cable
- PC USB Type-C port that has power delivery classification
 - Thunderbolt
 - Battery behind USB logo












	USB 2.0 High Speeds 480 MBit/s	USB 3.0 (USB 3.1 Gen 1) Super Speed 5 GBit/s	USB 3.1 Gen 2 Super Speed Plus 10 GBit/s
Does NOT support Power Delivery			
			
Does support Power Delivery			
			
Thunderbolt			
Does support Power Delivery			

Figure 2-3. USB Type_C Power Delivery Classification

Power supply designs that are NOT compatible with the AM275x EVM:

- Any USB adapter cables such as:
 - Type-A to Type-C
 - micro-B to Type-C
 - DC barrel jack to Type-
- 5V, 1.5A power adapter with USB-C captive cable or receptacle
- PC USB Type-C port not capable of 3A

2.2.1 Power Input Using USB Type-C Connector

The AM275x is powered through either of the two USB Type-C connections. The USB Type-C source is capable of providing power delivery of more than 15W (3A at 5V). On this EVM, the channel configuration pins, CC1 and CC2, from either of the two the USB Type-C connector are interfaced to the Type C DUAL Power Delivery (PD) Controller (TPS65988DHRSHR). The PD controller monitors the USBC_CONNx_CC1 and USBC_CONNx_CC2 pins of either of both USB-C connectors to detect port attach/detach, attached device type (source, sink, or dual role power), cable orientation, and cable capacity. When a power source device is connected, the PD controller detects the device and identifies its role (source, sink, or dual role power). The PD controller then uses the PD protocol over the USBC_CONNx_CC1 and USBC_CONNx_CC2 pins to negotiate power requirements with the power source.

The minimum power requirement of the AM275x EVM is 15W (5V at 3A). When the power negotiation is unsuccessful and the source is not capable of providing the required power, then the output at the OR gate remains low which means the VMAIN Load switch (TPS22810DRV1T) is disabled. Therefore, if the power requirement is not met, all power supplies remains in the off state. The board gets powered on completely only when the source can provide a minimum of 15W (5V at 3A).

The AM275x EVM includes a power supply based on a Burton (TPS6522430) Power Management Integrated Chip (PMIC) for each of the power rails. During the initial stage of the power supply, A minimum 5V supplied by the Type-C USB connector is used to generate all of the necessary voltages required by the PMIC and subsequently the rest of the board via the PMIC LDO outputs. For more information about the PMIC, refer to [Section 2.2.5](#).

2.2.2 Power Status LEDs

Multiple power-indication LEDs are provided on-board to indicate to users the output status of major supplies. The LEDs indicate power across various domains as shown in the table below.

Table 2-1. Power Status LEDs

Name	Default Status	Operation	Function
LD1	OFF	SoC_GPIO1_49	User Test LED
LD2	ON	VDDR_CORE	Power indicator for VDDR CORE
LD3	ON	XDS Data	Red LED glows during XDS110 data transaction
LD4	ON	PMIC_RSTOUT	Power Good indicator for PMIC
LD5	OFF	XDS Power	XDS Power Green LED
LD6	ON	VCC_3V3_SYS	Power indicator LED for VCC_3V3_SYS
LD7	OFF	VCC_3V3_FT4232	FT4232 Power LED
LD9	OFF	VBUS_TYPEC2	Indicator LED for Type_C USB connector 2
LD10	OFF	IO_EXP_TEST_LED	User Test LED for 3V3 IO expander
LD13	OFF	VBUS_TYPEC2	Indicator LED for Type_C USB connector 2
LD14	OFF	VMAIN_EN	Power Delivery Error Indicator, Type-C connection not supplying minimum 15W (5V at 3A)

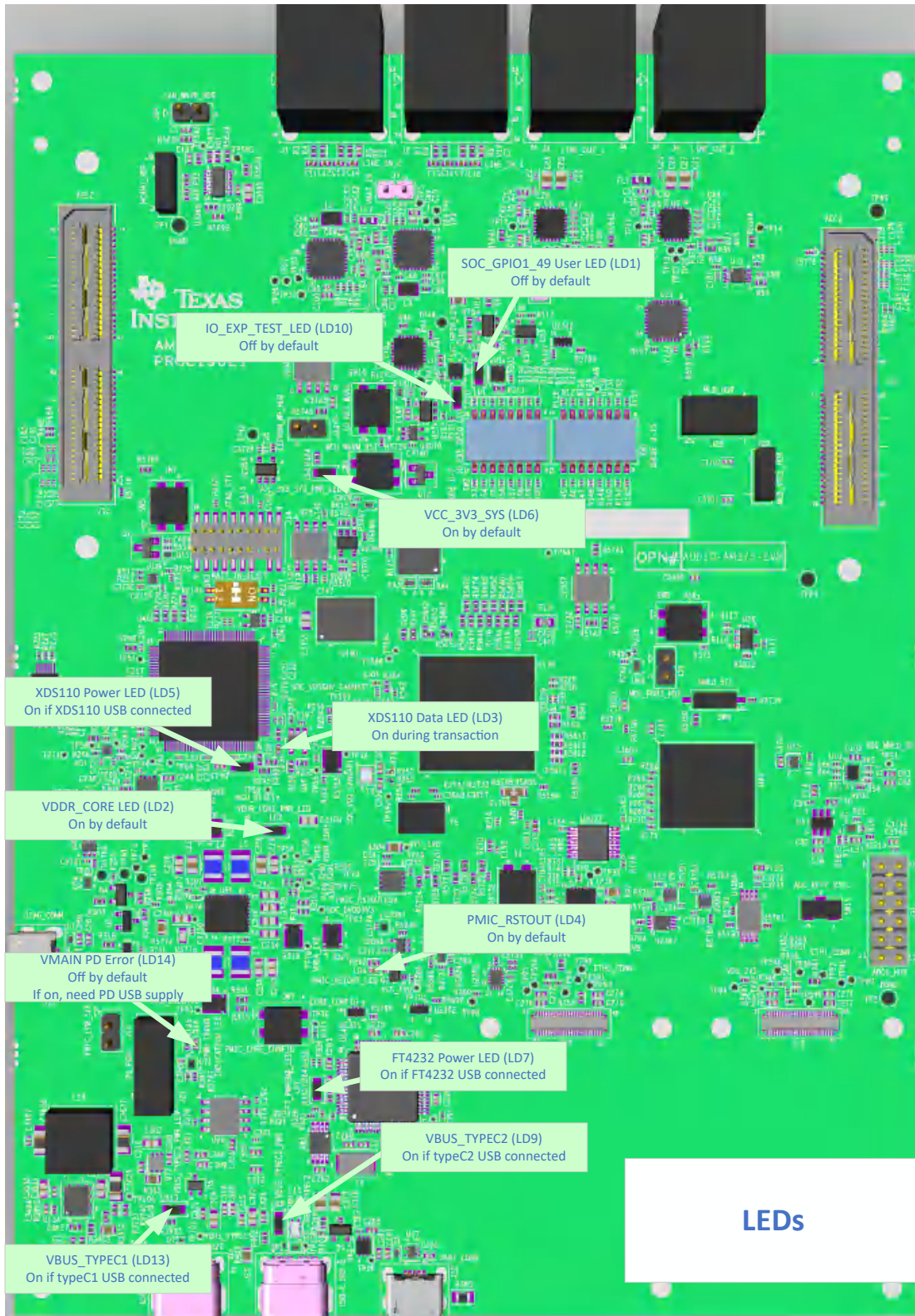
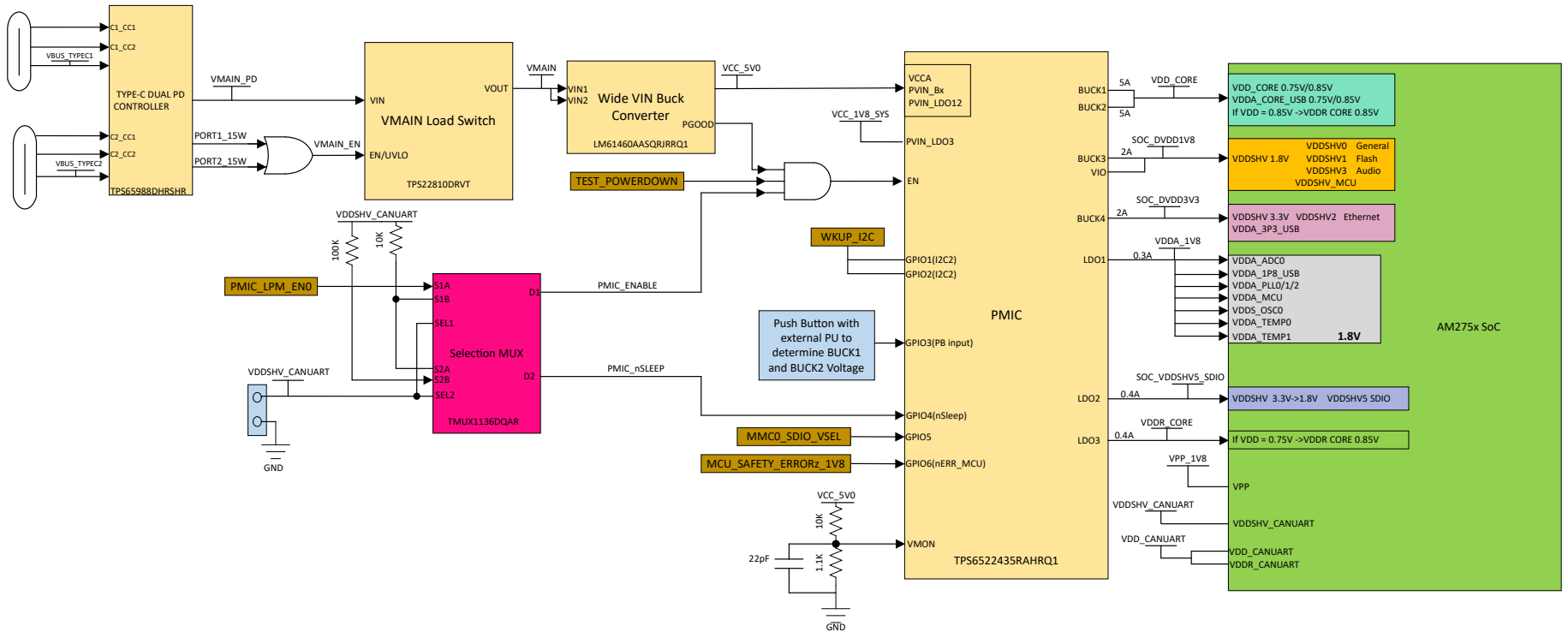
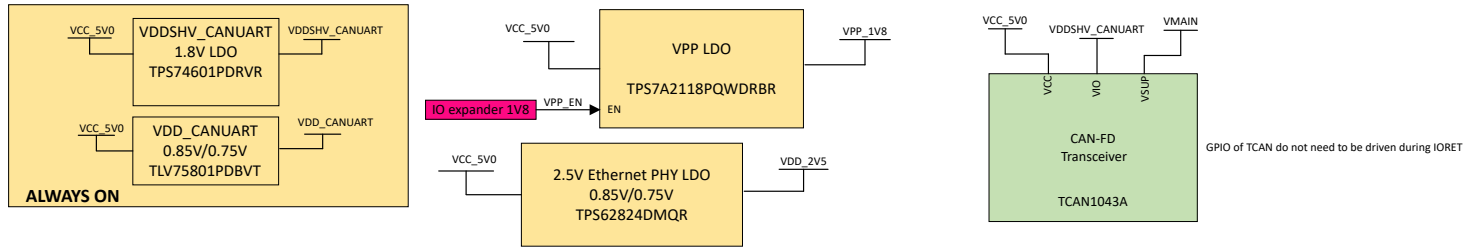


Figure 2-4. Power Status LEDs

2.2.3 Power Tree



2.2.4 Power Sequence

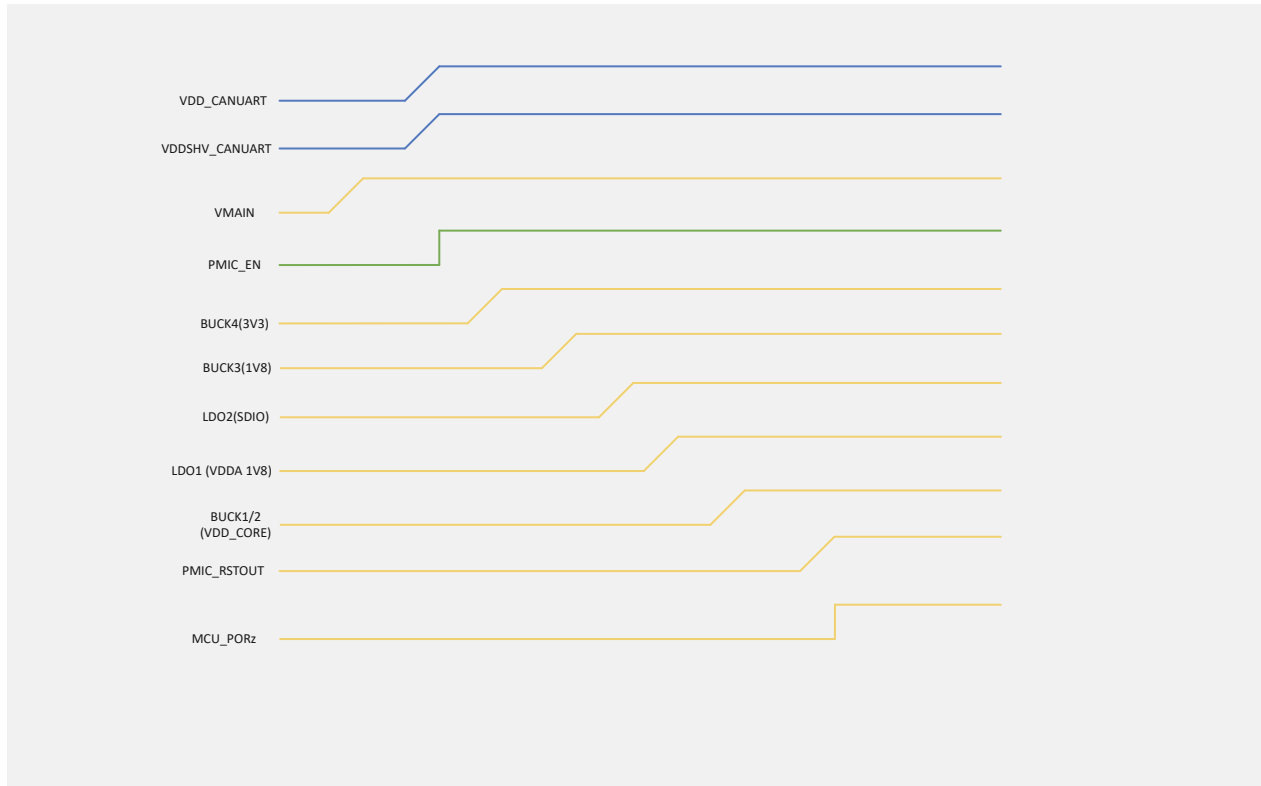


Figure 2-6. Power Sequence Diagram

Note

LDO3 is intentionally not included in this diagram because this configuration is for a 0.85V VDD Core which is shared with VDDR Core. LDO3 is OFF by default unless BUCK1/2 are configured for 0.75V.

2.2.5 PMIC

The AM275x EVM makes use of a Burton multirail power management IC (PMIC) (TPS6522435RAHRQ1). The PMIC integrates multiple supply rails to power the MCU, and other on-board peripherals.

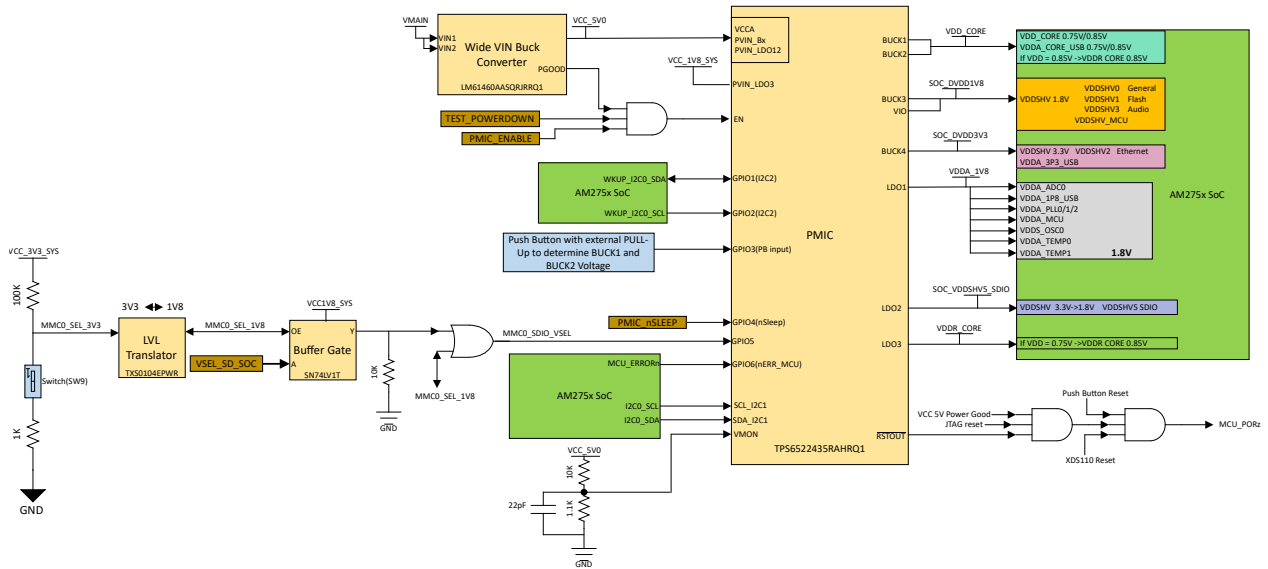


Figure 2-7. PMIC

The PMIC supports wake-up from Am275x SoC wake-up I2C lines.

An independent voltage monitoring unit inside the PMIC monitors undervoltage and overvoltage on all internal supply rails and regulator outputs of the power delivery supply. All supplies are protected with current limiting and overtemperature warning and shutdown.

The PMIC features multiple GPIO pins which serve as boot pins and various interfaces post-boot.

The Table below shows the functions, boot configuration and default states of the GPIOs:

Table 2-2. PMIC GPIOs

GPIOx	Function	Boot Configuration
GPIO1	I2C SDA Wake-up	N/A
GPIO2	I2C SCL Wake-up	N/A
GPIO3	Push Button for Buck1/2 voltage	Populated External pull-up to 1.8V: VDD_CORE = 0.85V (DEFAULT)
		Non-populated External pull-up to 1.8V: VDD_CORE= 0.75V
GPIO4	PMIC Sleep signal (nSLEEP)	N/A
GPIO5	SD card or eMMC I/O voltage select	Digital high: 1.8V LDO2 output
		Digital Low: 3.3V LDO2 output
GPIO6	Watchdog timeout Enable/Disable	Populated External pull-up to 1.8V: Watchdog Timer disabled
		Non-populated External pull-up to 1.8V: Watchdog timeout enabled

2.3 Reset

Figure 2-8 shows the reset architecture of the AM275x EVM.

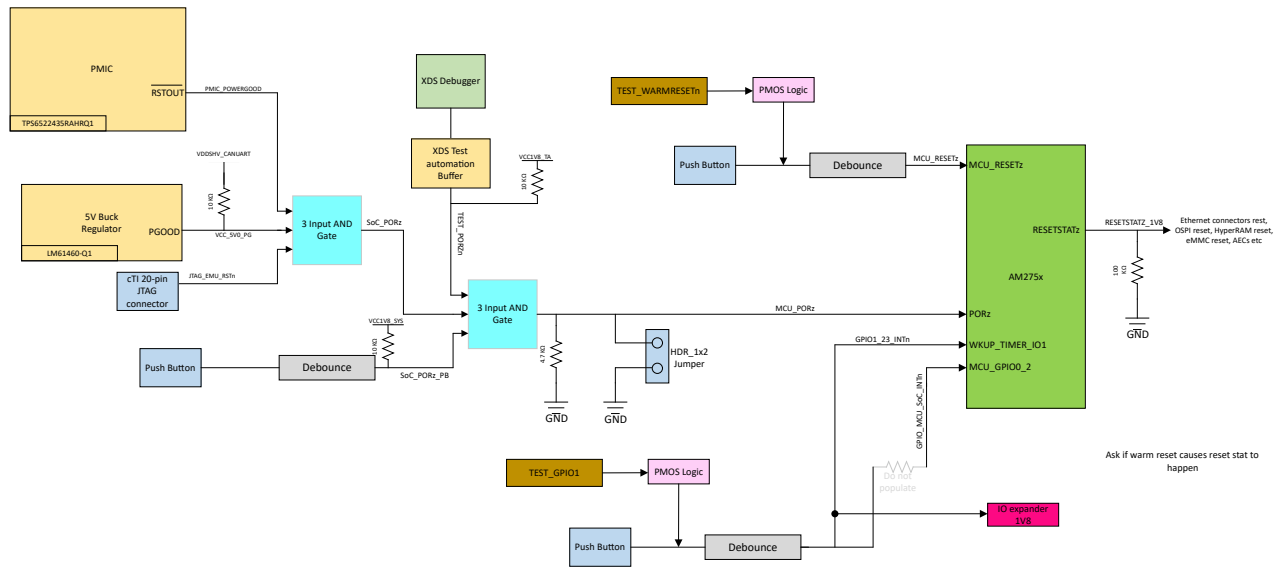


Figure 2-8. Reset Architecture Diagram

The AM275x SoC has the following resets:

- MCU_PORz is the Power-On-Reset for the AM275 SoC.
- MCU_RESEZt is the Warm Reset to AM275 SoC.
- RESEZSTATz_1V8 is the reset for the Main Domain.

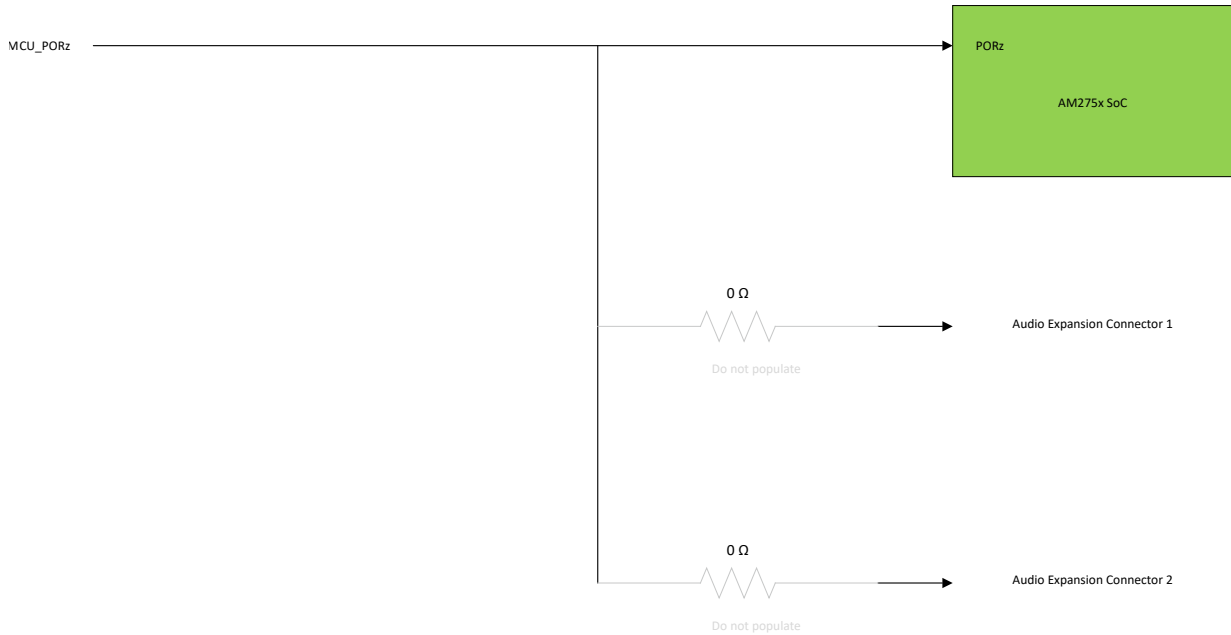


Figure 2-9. MCU_PORz Reset Signal Tree

The MCU_PORz signal is driven by a 3-input AND gates that generates a power on reset to the SoC when:

- The PMIC drives the PMIC PowerGood output signal low.
- The 5V buck regulator outputs a low signal for the power good signal.
- An external JTAG debugger drives the JTAG emulation reset signal low.
- The XDS Test Automation Header outputs a logic LOW signal (TEST_MCU_PORzn).
- The user push button (SW8) is pressed.

The MCU_PORz signal is tied to:

- AM275x SoC PORz input

MCU_PORz is also driven LOW by populating Jumper J32.

The MCU_RESETz signal creates a warm reset to the SoC when:

- The user push button (SW6) is pressed.
- The Test Automation Header outputs a logic LOW signal (TEST_WARMRESETn) to a P-Channel MOSFET gate which causes V_{GS} of the PMOS to be less than zero and so the MCU_RESETz signal connects to the PMOS drain which is tied directly to ground.

The MCU_RESETz signal is tied to:

- AM275x SoC MCU_RESETz input
- Audio Expansion Connectors (1&2)

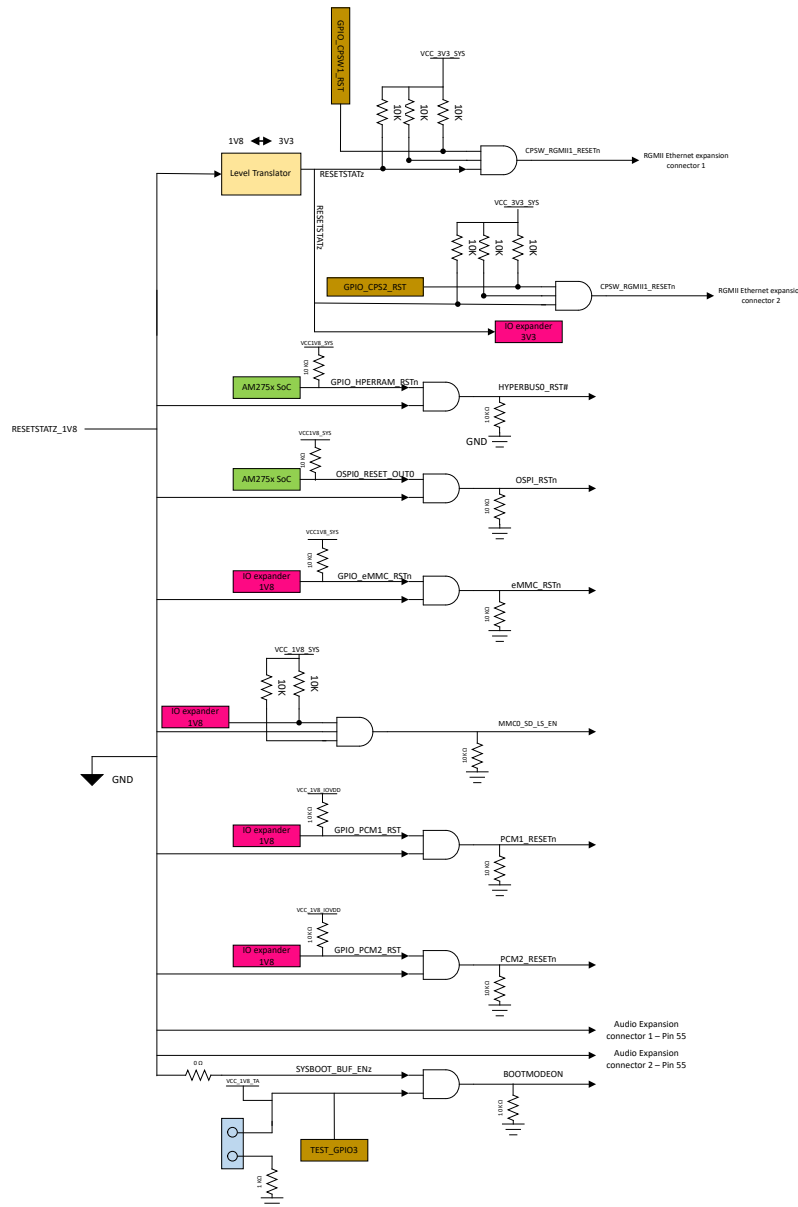


Figure 2-10. RESETSTATz Reset Signal Tree

The RESETSTATz_1V8 signal is the reset status signal for when a power-on reset or warm reset is triggered

The RESETSTATz_1V8 signal is tied to:

1. Ethernet Expansion Connector reset (1&2)
2. IO expander(U18) reset
3. HYPERRAM reset
4. OSPI reset
5. eMMC reset
6. MMC0 SD enable
7. PCM reset(1&2)
8. Audio Expansion Connector(1&2)
9. BOOTMODE buffer output enable

The AM275x EVM also has an external interrupt to the SoC, GPIO1_23_INTn, that occurs when:

- The user push button (SW5) is pressed.
- The Test Automation Header outputs a logic LOW signal (TEST_GPIO1) to a P-Channel MOSFET gate which causes V_{GS} of the PMOS to be less than zero and so the GPIO1_23_INTn signal connects to the PMOS drain which is tied directly to ground.

2.4 Clock

The AM275x SoC requires a 25 MHz clock input for MCU_OSC0. All reference clocks required for the SoC and the two Ethernet expansion connectors are generated from a single three output clock buffer (LMK1C1103PWR), which is sourced from a single 25MHz LVCMOS Oscillator (LMK6CE25000) by default.

The EVM also requires a 16 MHz clock source for the TM4C129 microcontroller for UART-USB JTAG support, and another 16MHz clock source for the USB-to-UART bridge FTDI chip.

A 32.768KHz low frequency crystal is also available for Real Time Clock (RTC) applications.

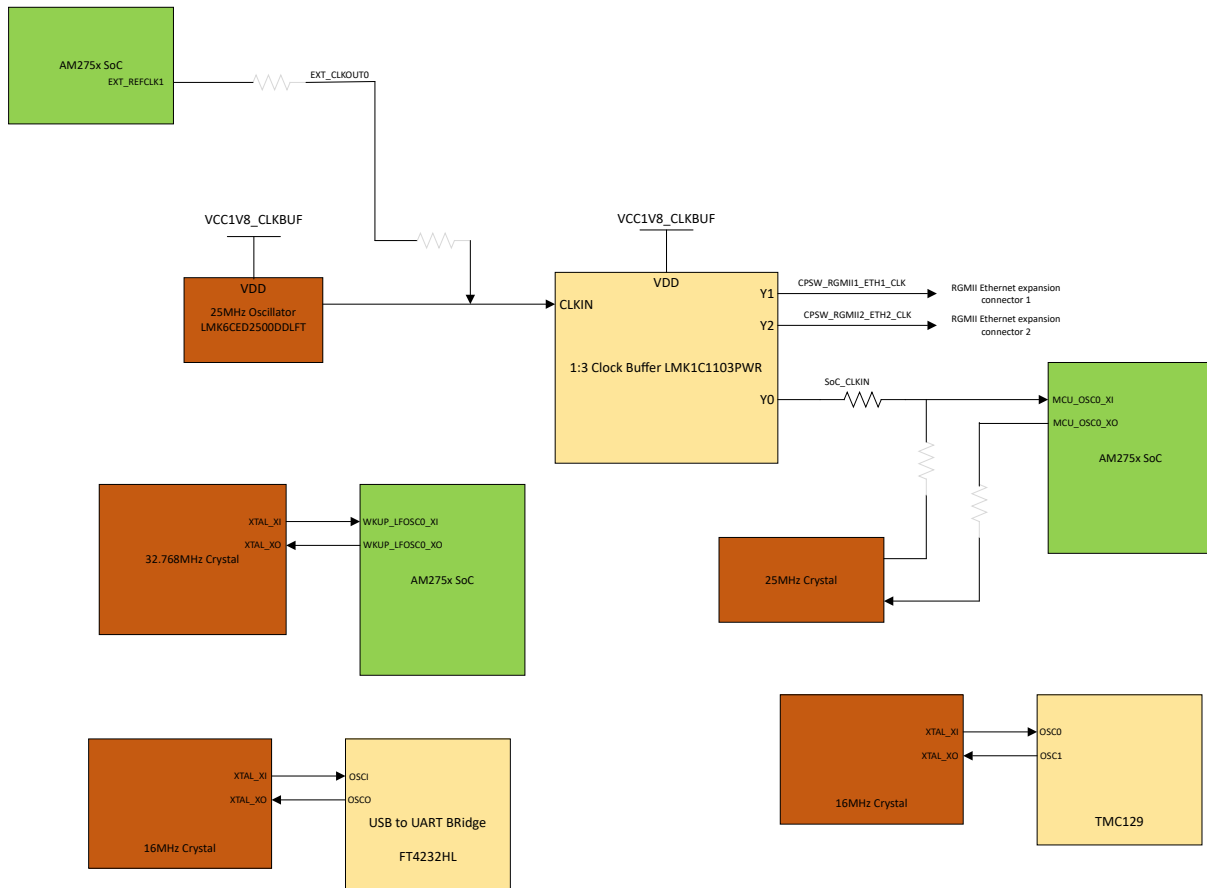


Figure 2-11. Oscillator Clock Tree

The SoC clock input can also be sourced from a single 25 MHz crystal. To use the crystal there must be resistors mounted and unmounted. When the crystal is used as a clock source then the AM275x CLKOUT0 (P1) signal is used to source the three output clock buffer for the Ethernet expansion connector reference clock signals.

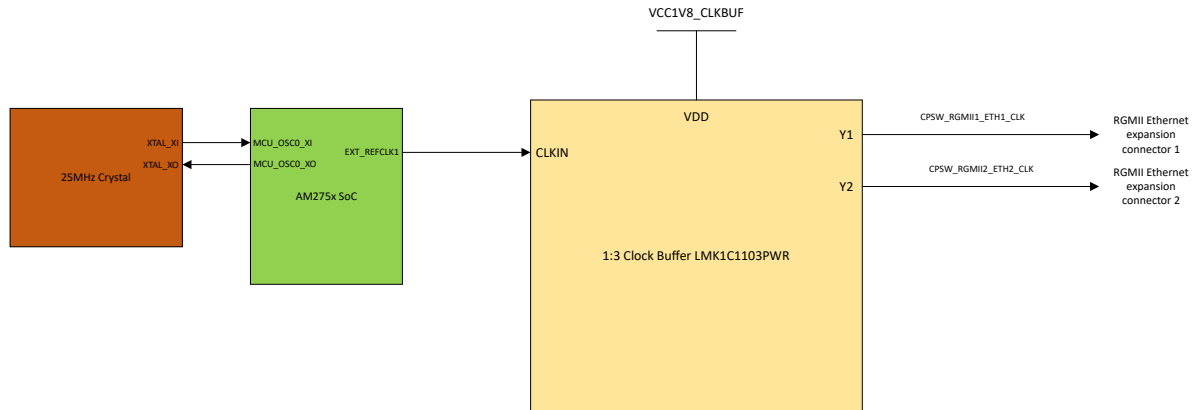


Figure 2-12. Crystal Clock Tree

The following table describes the proper resistors and capacitors to be mounted and DNI'd for each clock source configuration.

Table 2-3. Clock Source

Clock Source	Mounted	DNI
25 MHz LVCMOS Oscillator (default)	R336, R249, R349	R337, R170, R252, R253,C205,C209
25 MHz Crystal	R337, R170, R252, R253,C205,C209	R336, R249, R349

The AM275x EVM has three bi-directional Audio external reference clock signals used to provide audio reference clocks from external audio devices to the AM275x Multi Channel Audio Serial Ports (McASP), or from the internal audio clock sources such as McASP high-clocks or the Audio PLL to external audio devices:

- AUDIO_EXT_REFCLK2
- AUDIO_EXT_REFCLK1
- AUDIO_EXT_REFCLK0

AUDIO_EXT_REFCLK2 reference clock signal source is selected through a Multiplexer (TS5A3357QDCURQ1) from three inputs:

- CPSW_RGMII1_BCLK_1V8 signal, an Ethernet Audio Video Bridging (eAVB) bit clock signal from RGMII Ethernet connector 1 for Audio over ethernet applications.
- CPSW_RGMII2_BCLK_1V8 signal, an eAVB bit clock signal from RGMII Ethernet connector 2 for Audio over ethernet applications.
- CDCE_CLK_OUT1 signal, a clock output generated from a clock generator(CDCE6214RGET) that has a 24.576MHz crystal as a clock source.

The AVB bit clock signals from both RGMII Ethernet connectors (CPSW_RGMII1_BCLK) are both level translated by Level Translator (SN74AVC2T244DQMR), from 3.3V to 1.8V before being applied to the Multiplexer inputs.

AUDIO_EXT_REFCLK2_S0 and AUDIO_EXT_REFCLK2_S1 serve as Multiplexer input selection bits for selecting AUDIO_EXT_REFCLK2 clock input.

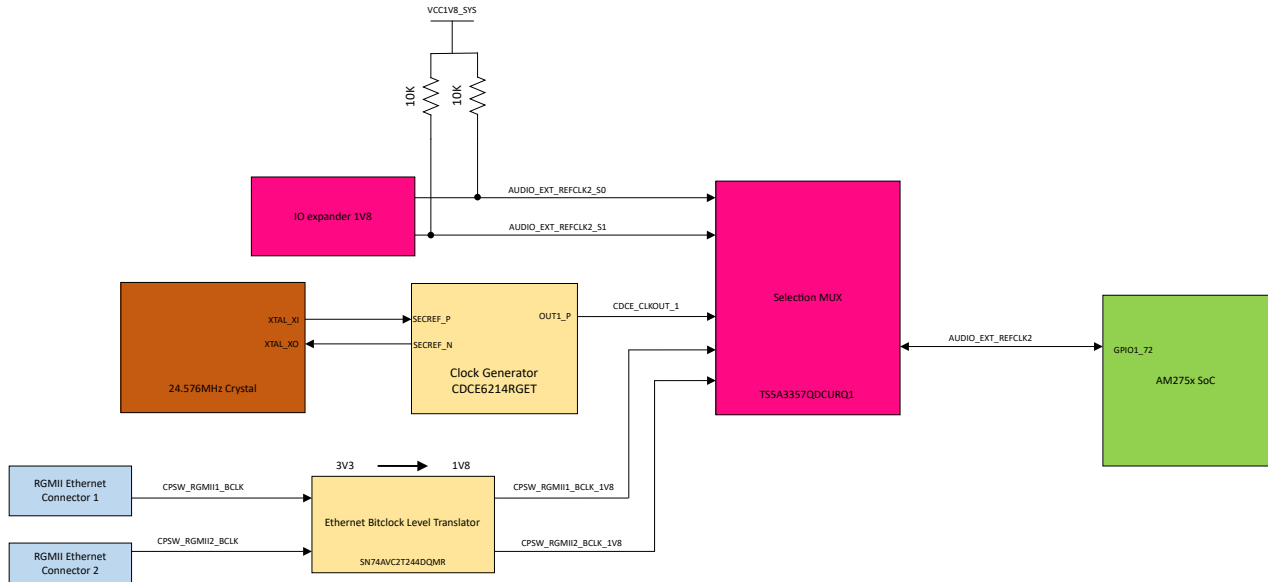


Figure 2-13. Audio_EXT_REFCLK2 Clock Tree

The following Truth Table shows the selection options for AUDIO_EXT_REFCLK2 reference clock source:

Table 2-4. AUDIO_EXT_REFCLK2 Selection Truth Table

AUDIO_EXT_REFCLK2_S0	AUDIO_EXT_REFCLK2_S1	AUDIO_EXT_REFCLK2
0	0	————
1	0	CPSW_RGMII2_BCLK_1V8
0	1	CPSW_RGMII1_BCLK_1V8
1	1	CDCE_CLK_OUT1(DEFAULT SELECTION)

AUDIO_EXT_REFCLK1 and AUDIO_EXT_REFCLK0 reference clock signals are selected through the same bi-directional Multiplexer (TMUX1136DQAR) from two options each:

AUDIO_EXT_REFCLK0 is selected from:

- AEC1_REFCLKOUT, a reference audio clock signal from Audio Expansion Connector 1. If AEC1_REFCLKOUT is selected (Default), it gets output to AUDIO_EXT_REFCLK0 signal.
- AEC1_REFCLKIN, a reference audio clock to Audio Expansion Connector 1. If AEC1_REFCLKIN is selected, it gets the reference audio clock signal AUDIO_EXT_REFCLK0, from the AM275x SoC.

AUDIO_EXT_REFCLK1 is selected from:

- AEC2_REFCLKOUT, a reference audio clock signal from Audio Expansion Connector 2. If AEC2_REFCLKOUT is selected, it gets output to AUDIO_EXT_REFCLK1 signal.
- AEC2_REFCLKIN, a reference audio clock to Audio Expansion Connector 2. If AEC2_REFCLKIN is selected, it gets the reference audio clock signal AUDIO_EXT_REFCLK1, from the AM275x SoC.

AEC1_REFCLK_SEL and AEC2_REFCLK_SEL serve as Multiplexer input selection bits to AUDIO_EXT_REFCLK0 and AUDIO_EXT_REFCLK1 respectively.

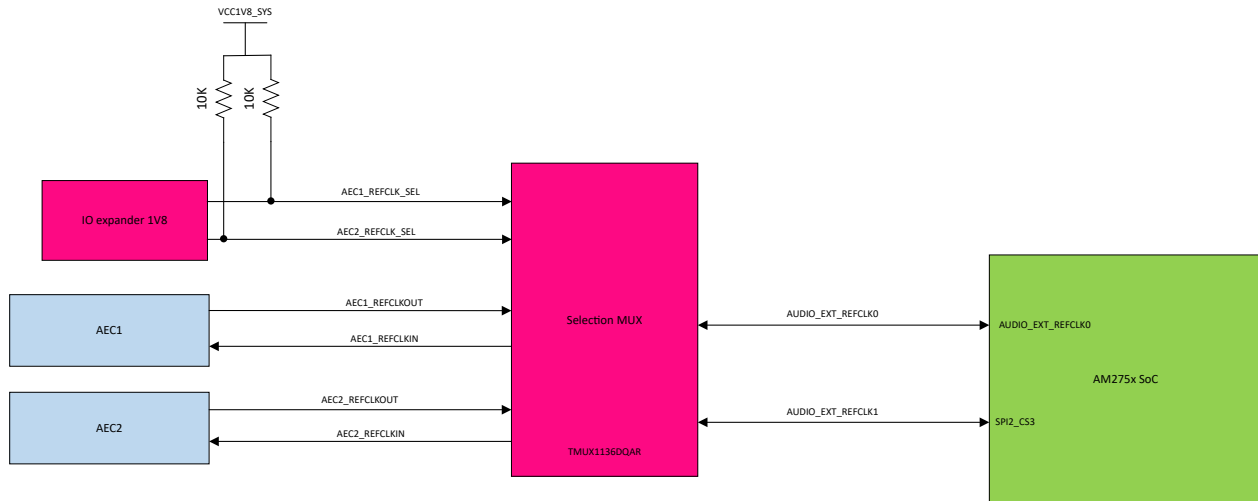


Figure 2-14. AUDIO_EXT_REFCLK0 and AUDIO_EXT_REFCLK1 Clock Tree

The following Truth Table shows the selection options for AUDIO_EXT_REFCLK0 and AUDIO_EXT_REFCLK1 reference clock signals:

Table 2-5. AUDIO_EXT_REFCLK0 and AUDIO_EXT_REFCLK1 Selection Truth Table

AEC _x _REFCLK_SEL	AUDIO_EXT_REFCLK0	AUDIO_EXT_REFCLK1
0	AEC1_REFCLKOUT	AEC2_REFCLKOUT
1(DEFAULT SELECTION)	AEC1_REFCLKIN	AEC2_REFCLKIN

A 24.576MHz crystal is also used to provide an Audio clock input OSC1 to the AM275x SoC for applications requiring specific audio frequencies.

2.5 Boot Mode Selection

The bootmode for the AM275x is selected by two DIP switches SW2(0:7) and SW1(8:15), or the test automation header. The test automation header uses an I2C IO expansion buffer to drive the bootmode when PORz is toggled.

Table 2-6. PLL Reference Clock Selection BOOTMODE[2:0]

SW2.3	SW2.2	SW2.1	PLL REF CLK (MHz)
OFF	OFF	OFF	RVSD
OFF	OFF	ON	RSVD
OFF	ON	OFF	24 MHz
OFF	ON	ON	25 MHz
ON	OFF	OFF	26 MHz
ON	OFF	ON	RSVD
ON	ON	OFF	RSVD
ON	ON	ON	RSVD

Table 2-7. Primary Boot Mode Selection[6:3]

SW2.7	SW2.6	SW2.5	SW2.4	Primary Boot Mode Selected
OFF	OFF	OFF	OFF	Serial NAND
OFF	OFF	OFF	ON	OSPI

Table 2-7. Primary Boot Mode Selection[6:3] (continued)

SW2.7	SW2.6	SW2.5	SW2.4	Primary Boot Mode Selected
OFF	OFF	ON	OFF	QSPI
OFF	OFF	ON	ON	SPI
OFF	ON	OFF	OFF	RGMII1
OFF	ON	OFF	ON	RMII1
OFF	ON	ON	OFF	I2C0
OFF	ON	ON	ON	UART0
ON	OFF	OFF	OFF	MMC/SD Card
ON	OFF	OFF	ON	eMMC
ON	OFF	ON	OFF	USB
ON	OFF	ON	ON	RSVD
ON	ON	OFF	OFF	RSVD
ON	ON	OFF	ON	Fast-xSPI
ON	ON	ON	OFF	xSPI
ON	ON	ON	ON	No-boot/Dev boot

Table 2-8. Primary Boot Mode Configuration[9:7]

SW1.2	SW1.1		SW2.8		Primary Boot Mode
RVSD	Read Mode2	0: RSVD (Read mode is taken from Read Mode 1) 1: SPI/ 1-1-1 Mode (Read mode is taken from Read Mode 2 and Read Mode 1 is ignored)	Read Mode1	0 : OSPI/ 1-1-8 Mode (valid only when Read Mode 2 is 0) 1 : QSPI/ 1-1-4 Mode (valid only when Read Mode 2 is 0)	Serial NAND
RVSD	RSVD		Csel	0: Chip Select 0 1: Chip Select 1	OSPI
RVSD	RSVD		Csel	0: Chip Select 0 1: Chip Select 1	QSPI
RVSD	Mode	0: SPI Mode 0 1: SPI Mode 3	Csel	0: Chip Select 0 1: Chip Select 1	SPI
0	0		Link stat	0: Phy scan used for speed/duplex setup 1: RGMII status register used for speed/duplex setup	RGMII1
CLKOUT	0: 50 MHz clock not generated on CLKOUT0 1: 50 MHz clock generated on CLKOUT0	CLK SRC	0: External clock source 1: Internal clock source		RMII1
Bus reset	0: Hung bus reset attempt after 1ms 1: No hung Bus reset attempted	RSVD		Addr	0: 0x50 1: 0x51
RSVD	RSVD		RSVD		UART0

Table 2-8. Primary Boot Mode Configuration[9:7] (continued)

SW1.2		SW1.1		SW2.8		Primary Boot Mode
0		RSVD		Fs/Raw	0: FileSystem Mode 1: Raw Mode	MMC/SD Card
RSVD		RSVD		RSVD		eMMC
Core Volt	0: 0.85V Core Voltage	Mode	0: DFU(Device)	Lane Swap	0: No swapping of DP/DM	USB
	1: 0.75V Core Voltage		1: TBD		1: DP/DM is swapped	
RSVD		RSVD		RSVD		RSVD
RSVD		RSVD		RSVD		RSVD
RSVD		RSVD		RSVD		Fast-xSPI
SFDP	0: SFDP disabled	Read Cmd	0: 0x0B Read Command	Mode	0: 1S-1S-1S mode @ 50MHz	xSPI
	1: SFDP enabled		1: 0xEE Read Command		1: 8D-8D-8D mode @ 25 MHz	
RSVD		ARM/ Thumb	0: ARM mode	No/Dev	0: Development Boot	No-boot/Dev boot
			1: Thumb mode		1: No Boot	

Table 2-9. Backup Bootmode Selection BOOTMODE[12:10]

SW1.5	SW1.4	SW1.3	Backup Boot Mode Selected
OFF	OFF	OFF	None
OFF	OFF	ON	USB
OFF	ON	OFF	RSVD
OFF	ON	ON	UART
ON	OFF	OFF	Ethernet
ON	OFF	ON	MMC
ON	ON	OFF	SPI
ON	ON	ON	I2C

Table 2-10. Backup Bootmode Configuration BOOTMODE[13]

SW1.6		Backup Boot Mode	Defaulted Values for Backup Boot Mode
RSVD		None	
Mode	0: DFU(Device)	USB	Core Volt bit = 0 Lane Swap bit = 0
	1: TBD		
RSVD		RSVD	
RSVD		UART	
IF	0: RGMII with internal Delay	Ethernet	Link Stat bit = 0 (If RGMII)
	1: RGMII with external clock source		ClkOut bit= 0 & Clksrc bit = 1 (If RMII)
0		MMC	Mode bit = 0
RSVD		SPI	Csel bit = 0 Mode = 0
RSVD		I2C	Addr = 0 Bus Rest = 0

2.6 Header Information

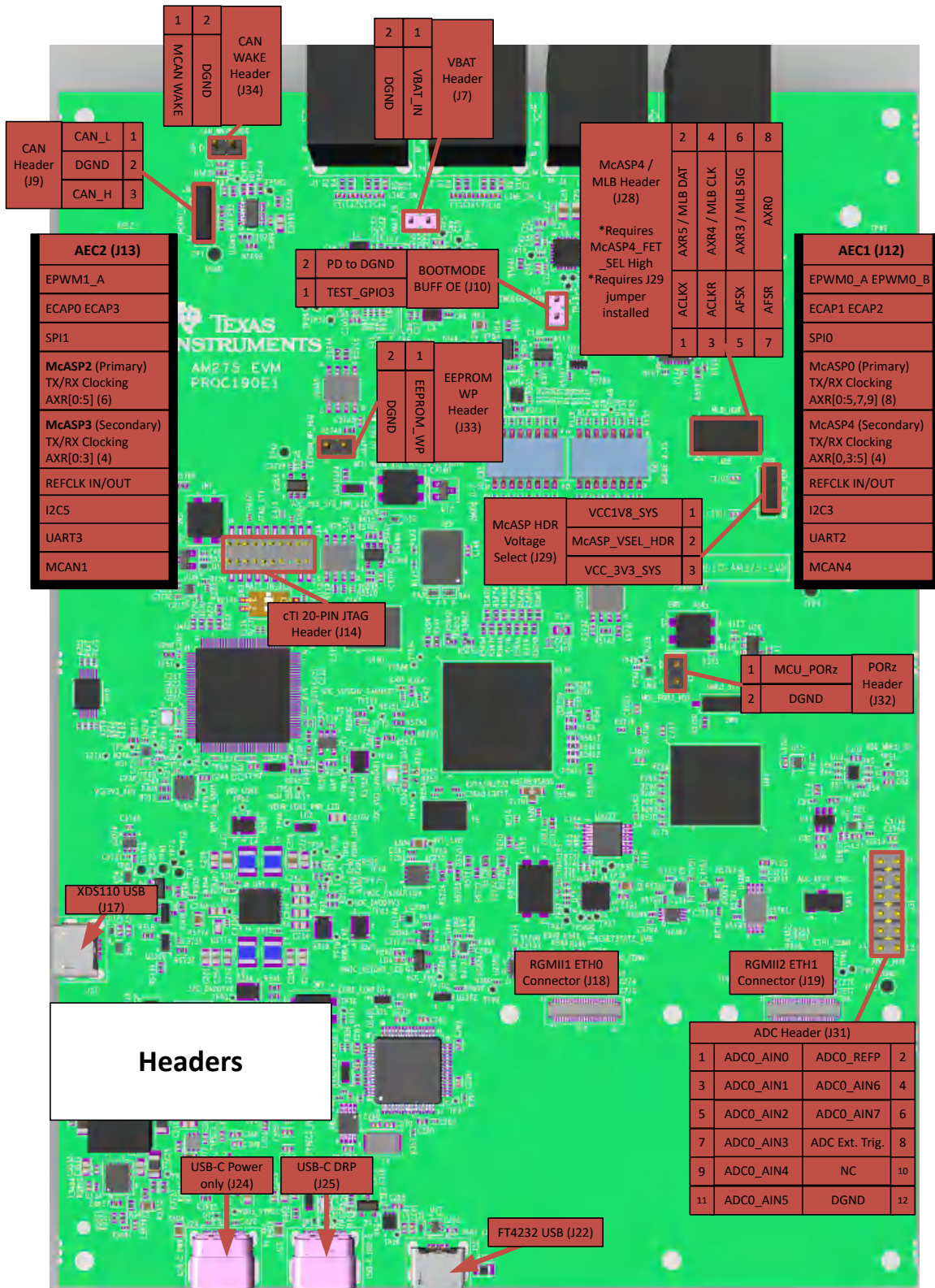


Figure 2-15. Headers

2.7 Push Buttons

The EVM supports multiple user push buttons that provide reset inputs to the processor.

[EVM Push Buttons](#) lists the push buttons for AM275x EVM.

Table 2-11. Push Buttons

Push Button	Signal	Function
SW8	PORz	SoC PORz Reset Input
SW6	RESETz	SoC Warm Reset input
SW5	INTn	User Interrupt Signal
SW10	IO RET WAKE PB	I/O retention wake input

2.8 Switches

SW9 dictates routing logic of MMC0 IO to eMMC or SDcard.

Table 2-12. SW9 Position Table

Switch position	MMC0 Routing
ON	uSD Interface
OFF	eMMC Interface

SW11 dictates which reference 1.8V the AM275x ADC0 uses: VDDA_1V8 PMIC analog output, or an external 1.8V reference from Header J31(Pin 2)

Table 2-13. SW11 Position Table

Switch position	ADC Reference Source
SW11 Position 1-2	VDDA_1V8
SW11 Position 3-2	ADC0_REFP_HDR (External Reference from J31)

2.9 Interfaces

2.9.1 Ethernet Interface

The AM275 EVM offers two 1Gb Ethernet Ports for external Communication. The AM275x SoC offers two CPSW3G Ethernet Reduced Gigabit Media Independent Interface(RGMII) Channels, RGMII1 and RGMII2, that are routed to two separate Ethernet Expansion Connectors .

The Ethernet Expansion Connectors can be interfaced with an Industrial Ethernet Daughter Card or an Automotive Ethernet Daughter Card, which provides flexibility.

Ethernet Expansion Connectors (CPSW RGMII1 and CPSW RGMII2) Ports share a common MDIO Bus to communicate with an external PHY Transceiver.

2.9.1.1 Ethernet Add-on Connectors

The AM275x EVM features two Common Platform Switch (CPSW) RGMII Ethernet Expansion Connectors.

The Tables below lists the pinouts for the ethernet expansion connectors:

Note

I/O direction refers to the direction from the Ethernet Expansion connector perspective.

Table 2-14. CPSW RGMII Ethernet Expansion Connector 1 Pinout

Pin Number	Net Name/Signal	I/O Direction	Pin Number	Net Name/Signal	I/O Direction
1	DGND	POWER	2	EXT_VMON2_1	POWER
3	CPSW_RGMII1_TXC	INPUT	4	VDD_2V5	POWER

Table 2-14. CPSW RGMII Ethernet Expansion Connector 1 Pinout (continued)

Pin Number	Net Name/Signal	I/O Direction	Pin Number	Net Name/Signal	I/O Direction
5	DGND	POWER	6	VDD_2V5	POWER
7	CPSW_RGMII1_TD0	INPUT	8	DGND	POWER
9	CPSW_RGMII1_TD1	INPUT	10	CPSW_RGMII_INTn	OUTPUT
11	CPSW_RGMII1_TD2	INPUT	12	CPSW_RGMII1_RESETn	INPUT
13	CPSW_RGMII1_TD3	INPUT	14	CPSW_RGMII1_COL	OUTPUT
15	DGND	POWER	16	DGND	POWER
17	DGND	POWER	18	DGND	POWER
19	CPSW_RGMII1_RXC	OUTPUT	20	CPSW_RGMII1_MDC	INPUT
21	DGND	POWER	22	CPSW_RGMII1_MDIO	BIDIRECTIONAL
23	CPSW_RGMII1_RD0	OUTPUT	24	DGND	POWER
25	CPSW_RGMII1_RD1	OUTPUT	26	RGMII1_INH_3V3	OUTPUT
27	CPSW_RGMII1_RD2	OUTPUT	28	CPSW_RGMII1_ETH1_CLK	INPUT
29	CPSW_RGMII1_RD3	OUTPUT	30	CPSW_RGMII1_CRS	OUTPUT
31	DGND	POWER	32	DGND	POWER
33	DGND	POWER	34	DGND	POWER
35	CPSW_RGMII1_TX_EN	INPUT	36	CPSW_RGMII1_BRD_CONN_DET	OUTPUT
37	I2C_ADDR0_A2	INPUT	38	SYNC1_OUT_ETH1	INPUT
39	RGMII1_RX_ER	OUTPUT	40	SoC_I2C0_SCL	INPUT
41	DGND	POWER	42	SoC_I2C0_SDA	BIDIRECTIONAL
43	RGMII1_RX_LINK	OUTPUT	44	VCC_3V3_SYS	POWER
45	CPSW_RGMII1_RX_DV	OUTPUT	46	VCC_3V3_SYS	POWER
47	I2C_ADDR0_A0	INPUT	48	CPSW_RGMII1_BCLK	OUTPUT

Table 2-15. CPSW RGMII Ethernet Expansion Connector 2 Pinout

Pin Number	Net Name/Signal	I/O Direction	Pin Number	Net Name/Signal	I/O Direction
1	DGND	POWER	2	EXT_VMON2_2	POWER
3	CPSW_RGMII1_TXC	INPUT	4	VDD_2V5	POWER
5	DGND	POWER	6	VDD_2V5	POWER
7	CPSW_RGMII2_TD0	INPUT	8	DGND	POWER
9	CPSW_RGMII2_TD1	INPUT	10	CPSW_RGMII_INTn_R	OUTPUT
11	CPSW_RGMII2_TD2	INPUT	12	CPSW_RGMII2_RSTn	INPUT
13	CPSW_RGMII2_TD3	INPUT	14	CPSW_RGMII2_COL	OUTPUT
15	DGND	POWER	16	DGND	POWER
17	DGND	POWER	18	DGND	POWER
19	CPSW_RGMII2_RXC	OUTPUT	20	CPSW_RGMII2_MDC	INPUT
21	DGND	POWER	22	CPSW_RGMII2_MDIO	BIDIRECTIONAL
23	CPSW_RGMII2_RD0	OUTPUT	24	DGND	POWER

Table 2-15. CPSW RGMII Ethernet Expansion Connector 2 Pinout (continued)

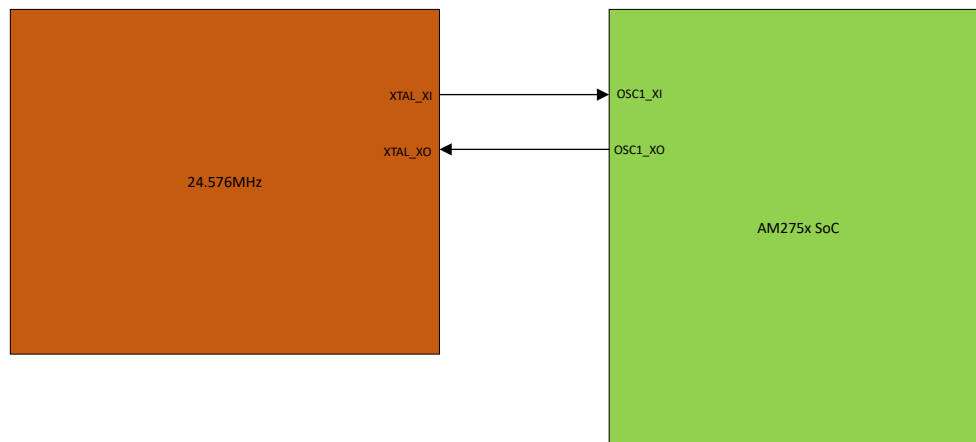
Pin Number	Net Name/Signal	I/O Direction	Pin Number	Net Name/Signal	I/O Direction
25	CPSW_RGMII2_RD1	OUTPUT	26	RGMII2_INH_3V3	OUTPUT
27	CPSW_RGMII2_RD2	OUTPUT	28	CPSW_RGMII2_ETH2_CLK	INPUT
29	CPSW_RGMII2_RD3	OUTPUT	30	CPSW_RGMII2_CRS	OUTPUT
31	DGND	POWER	32	DGND	POWER
33	DGND	POWER	34	DGND	POWER
35	CPSW_RGMII2_TX_EN	INPUT	36	CPSW_RGMII2_BRD_CONN_DET	OUTPUT
37	I2C_ADDR0_A2	INPUT	38	SYNC1_OUT_ETH2	INPUT
39	RGMII2_RX_ER	OUTPUT	40	SoC_I2C0_SCL	INPUT
41	DGND	POWER	42	SoC_I2C0_SDA	BIDIRECTIONAL
43	RGMII2_RX_LINK	OUTPUT	44	VCC_3V3_SYS	POWER
45	CPSW_RGMII2_RX_DV	OUTPUT	46	VCC_3V3_SYS	POWER
47	I2C_ADDR0_A0	INPUT	48	CPSW_RGMII2_BCLK	OUTPUT

2.9.2 Audio Interfaces

2.9.2.1 Audio Clocking

The AM275x EVM features two options for an audio clock reference on each MCASP Transmit(X) and Receive(R).

- An internally generated audio reference clock using the 24.576MHz crystal input on OSC1

**Figure 2-16. Internal Audio Reference Clock**

- An externally generated audio reference clock from three options:
 - External Audio reference clock generated from clock generator(CDCE6214) to AUDIO_EXT_REFCLK2
 - External Audio reference clock generated from Audio expansion connectors AEC1 and AEC2 via AUDIO_EXT_REFCLK0 and AUDIO_EXT_REFCLK1 respectively

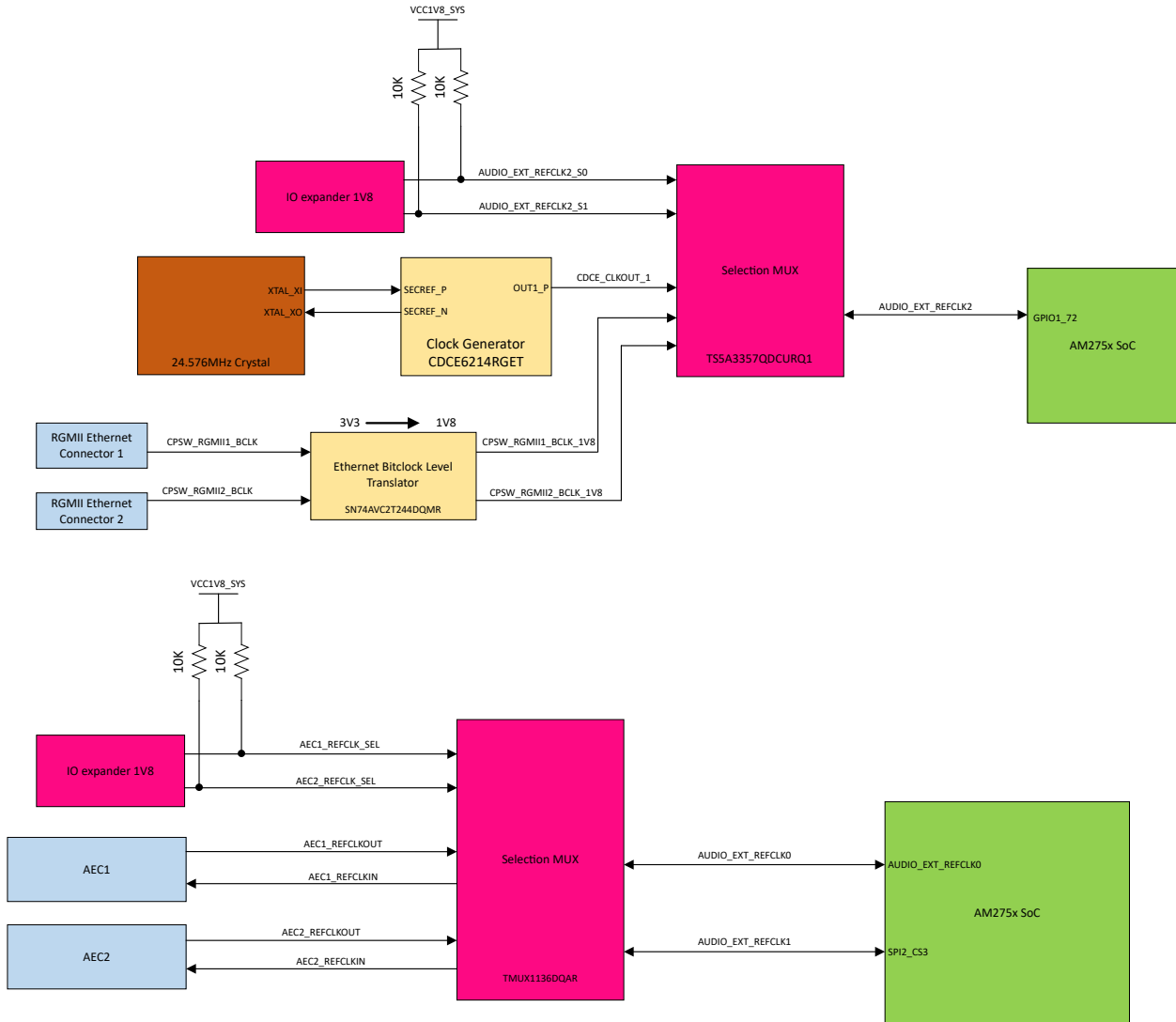


Figure 2-17. External Audio Reference Clocks

2.9.2.2 McASP

The AM275x features five Multichannel Audio Serial Ports (McASP), McASP[0:4]. Each McASP features independent clock zones for transmit and receive.

McASP1 is used for AM275x EVM on-board ADC/DAC Input and Outputs.

The ADC/DAC Input and Outputs featured on the AM275x EVM consist of:

- Four output 3.5mm TRS Audio Jack connectors for Eight Stereo Channel DAC Line AC-coupled outputs. . Each individual TRS Audio Jack Connector is connected to a two-channel Stereo Audio DAC(TAD5212) device (Four DACs in total) .
- Four input 3.5mm TRS Audio Jack connectors for Eight Stereo Channel Microphone/Line AC-coupled inputs.. Each Pair of the TRS Audio Jack Connectors are connected to a four-channel Audio ADC(PCM6240) device (Two ADCs in total).

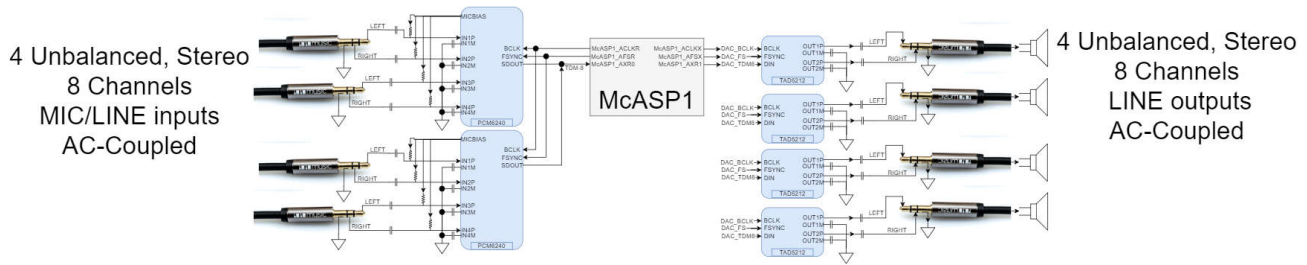


Figure 2-18. MCASP1

McASP0 is used as the primary McASP interface for Audio Expansion Connector 1 (AEC1). McASP0 has Eight Audio Transmit/Receive channels (McASP0_AXR[0:7]).

McASP4 is used as the secondary McASP interface for Audio Expansion Connector 1 (AEC1). McASP4 has Four Transmit/Receive channels (McASP4_AXR0, McASP4_AXR[3:5]).

McASP2 is used as the primary McASP interface for Audio Expansion Connector 2 (AEC2). McASP2 has Six Audio Transmit/Receive channels (McASP2_AXR[0:5]).

McASP3 is used as the primary McASP interface for Audio Expansion Connector 2 (AEC2). McASP3 has Four Audio Transmit/Receive channels (McASP3_AXR[0:3]).

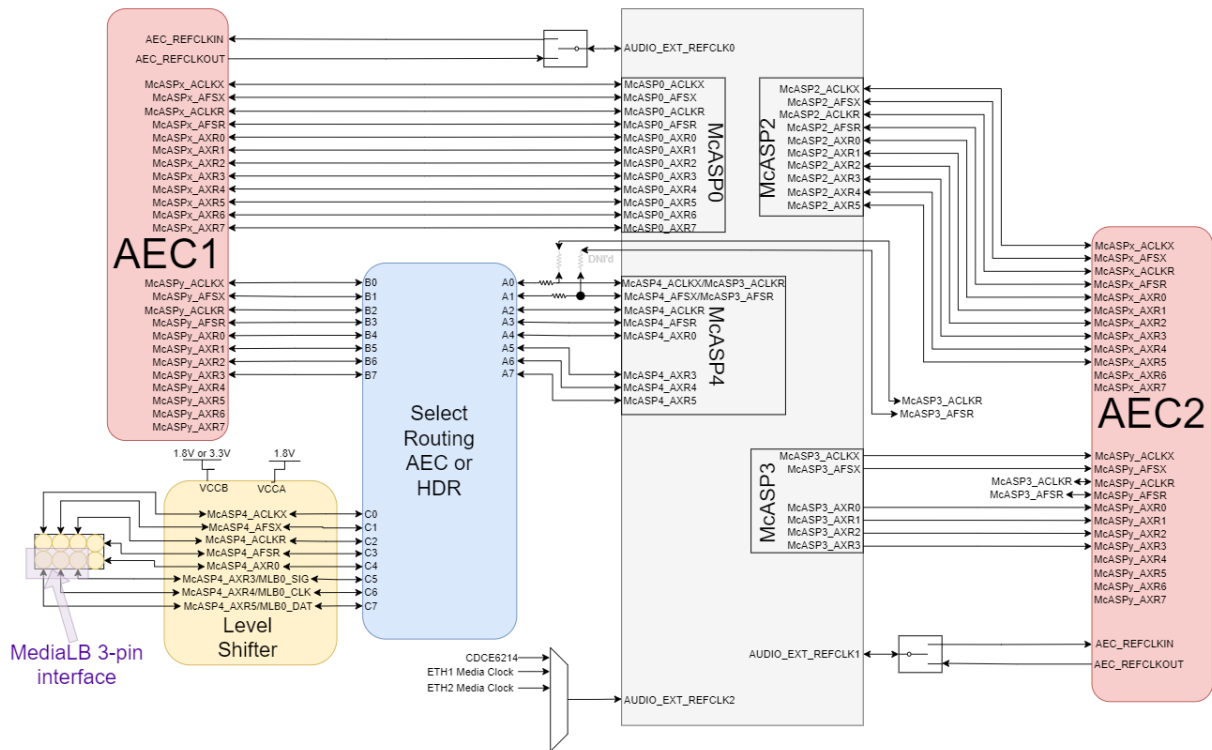


Figure 2-19. McASP0, McASP2, McASP3, McASP4

Note

For additional Information on McASP features and configuration, go to

2.9.2.3 MLB

The AM275x EVM features a Media Local Bus (MLB) Header option. A 1:2 Switch MUX (SN74CBTLV) selects the AM275x SoC Audio signals between the MLB header or AEC1. The McASP_FET_SEL signal is the selection bit for this MUX. The MLB header option goes through a Level Shifter (TXB0108PWR) which has the voltage level defined by header J29.

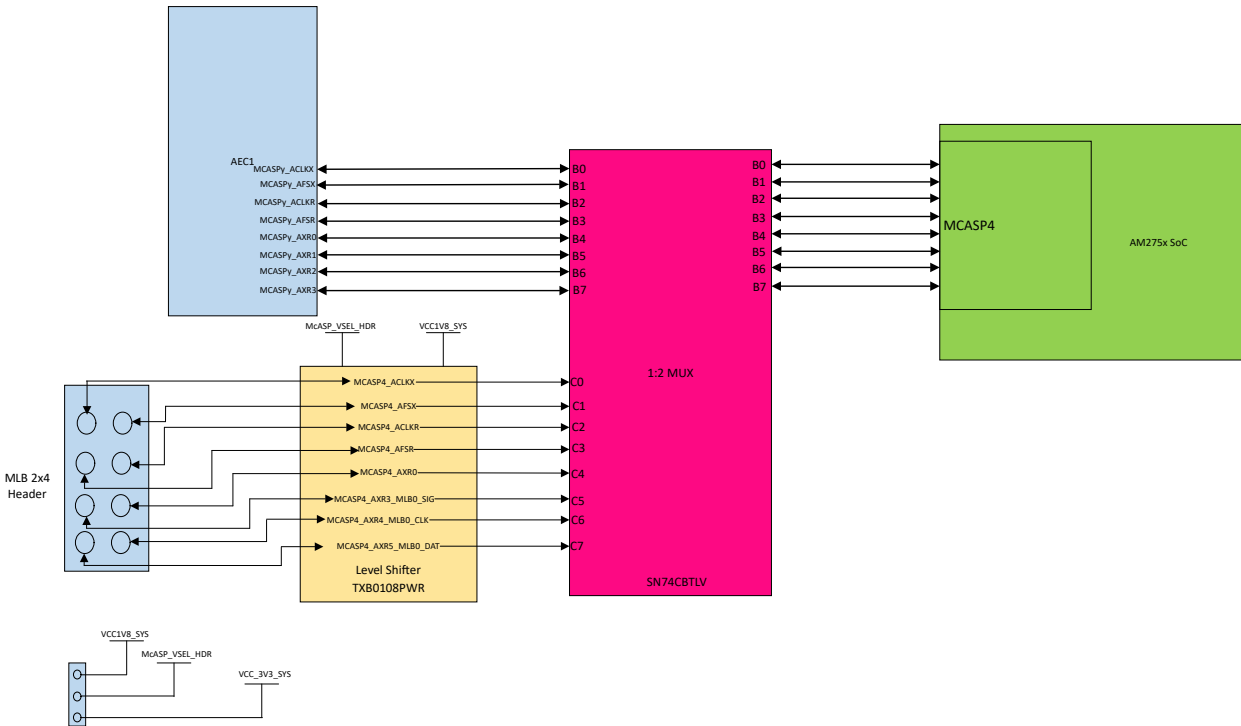


Figure 2-20. MLB Header

2.10 AEC Mapping

2.10.1 Audio Expansion Connector 1

The following interfaces and IOs are included on Audio Expansion Connector 1 (AEC1):

- 1 x SPI : SPI0 with two chip selects (SPI0_CS0 and SPI0_CS1)
- 1 x I2C : I2C3
- 1 x UART : UART2
- 2 x PWM: EPWM0_A and EPWM0_B
- 1 x Reference Clock Input: AEC1_REFCLKIN
- 1 x Reference Clock Output: AEC1_REFCLKOUT
- 1 x MCAN: MCAN4
- 2 x eCAP: ECAP1 and ECAP2
- 2 x McASP : McASP0 and McASP4
- 2 x GPIO: AEC1_GPIO_0 and AEC1_GPIO_1
- 5V and 1.8V supply voltages (Current limited to 150mA and 250mA)

The Table below lists all the AM275 EVM signals routed to AEC1:

Table 2-16. AEC1 Pinout

Pin Number	NET NAME	Pin Number	NET NAME
1	MCU_PORz	2	VCC_5V0
3	EPWM0_A	4	VCC_5V0

Table 2-16. AEC1 Pinout (continued)

Pin Number	NET NAME	Pin Number	NET NAME
5	EPWM0_B	6	VCC_5V0
7	DGND	8	DGND
9	ECAP1_IN_APWM_OUT	10	VCC1V8_SYS
11	ECAP2_IN_APWM_OUT	12	VCC1V8_SYS
13	NC	14	NC
15	DGND	16	DGND
17	SPI0_CLK	18	I2C3_SCL_1V8
19	SPI0_D0	20	I2C3_SDA_1V8
21	SPI0_D1	22	DGND
23	SPI0_CS0	24	SPI0_CS1
25	DGND	26	DGND
27	MCASP0_AXR0	28	MCASP0_AXR2
29	MCASP0_AXR1	30	MCASP0_AXR3
31	DGND	32	MCASP0_AXR4
33	AEC1_REFCLKIN	34	MCASP0_AXR5
35	DGND	36	DGND
37	MCASP0_ACLKX	38	MCASP0_AXR7
39	MCASP0_AFSX	40	MCASP0_AXR9
41	MCASP0_AFSR	42	AEC1_GPIO0_0
43	MCASP0_ACLKR	44	AEC1_GPIO0_1
45	DGND	46	DGND
47	AEC1_REFCLKOUT	48	NC
49	DGND	50	DGND
51	MCAN4_TX	52	NC
53	MCAN4_RX_R	54	NC
55	RESETSTATZ_1V8	56	NC
57	DGND	58	DGND
59	NC	60	UART2_TXD
61	NC	62	UART2_RXD
63	NC	64	NC
65	DGND	66	DGND
67	MCASP4_AXR0	68	NC
69	MCASP4_AXR3	70	NC
71	MCASP4_AXR4	72	NC
73	MCASP4_AXR5	74	NC
75	DGND	76	DGND
77	MCASP4_ACLKX	78	MCASP4_ACLKR
79	MCASP4_AFSX	80	MCASP4_AFSR

2.10.2 Audio Expansion Connector 2

The following interfaces and IOs are included on Audio Expansion Connector 2 (AEC2):

- 1 x SPI : SPI1 with two chip selects (SPI1_CS0 and SPI1_CS1)
- 1 x I2C : I2C5
- 1 x UART : UART3
- 1 x PWM: EPWM1_A
- 1 x Reference Clock Input: AEC2_REFCLKIN
- 1 x Reference Clock Output: AEC2_REFCLKOUT
- 1 x MCAN: MCAN1
- 2 x eCAP: ECAP0 and ECAP3
- 2 x McASP : McASP2 and McASP3
- 2 x GPIO: AEC2_GPIO_0 and AEC2_GPIO_1
- 5V and 1.8V supply voltages (Current limited to 150mA and 250mA)

The Table below lists all the AM275 EVM signals routed to AEC1:

Table 2-17. AEC2 Pinout

Pin Number	NET NAME	Pin Number	NET NAME
1	MCU_PORz	2	VCC_5V0
3	EPWM1_A	4	VCC_5V0
5	NC	6	VCC_5V0
7	DGND	8	DGND
9	ECAP3_IN_APWM_OUT	10	VCC1V8_SYS
11	ECAP0_IN_APWM_OUT	12	VCC1V8_SYS
13	NC	14	NC
15	DGND	16	DGND
17	SPI1_CLK	18	I2C5_SCL_1V8
19	SPI1_D0	20	I2C5_SDA_1V8
21	SPI1_D1	22	DGND
23	SPI1_CS0	24	SPI1_CS1
25	DGND	26	DGND
27	MCASP2_AXR0	28	MCASP2_AXR2
29	MCASP2_AXR1	30	MCASP2_AXR3
31	DGND	32	MCASP2_AXR4
33	AEC2_REFCLKIN	34	MCASP2_AXR5
35	DGND	36	DGND
37	MCASP2_ACLKX	38	NC
39	MCASP2_AFSX	40	NC
41	MCASP2_AFSR	42	AEC2_GPIO0_0
43	MCASP2_ACLKR	44	AEC2_GPIO0_1
45	DGND	46	DGND
47	AEC2_REFCLKOUT	48	NC
49	DGND	50	DGND
51	MCAN1_TX	52	NC
53	MCAN1_RX_R	54	NC
55	RESETSTATZ_1V8	56	NC

Table 2-17. AEC2 Pinout (continued)

Pin Number	NET NAME	Pin Number	NET NAME
57	DGND	58	DGND
59	NC	60	UART3_TXD
61	NC	62	UART3_RXD
63	NC	64	NC
65	DGND	66	DGND
67	MCASP3_AXR0	68	NC
69	MCASP3_AXR1	70	NC
71	MCASP3_AXR2	72	NC
73	MCASP3_AXR3	74	NC
75	DGND	76	DGND
77	MCASP3_ACLKX	78	MCASP3_ACLKR
79	MCASP3_AFSX	80	MCASP3_AFSR

2.11 Test Points

The AM275 EVM features multiple testpoints for Power, Ground, and critical signals.

The Table below outlines tespoints for each power output on the AM275x EVM:

Table 2-18. Test Points

Power Supply	Test Point	Voltage
VBUS_TYPEC1	TP107	5V/9V/15V
VBUS_TYPEC2	TP108	5V/9V/15V
VMAIN	TP104	5V/9V/15V
FT4232_USB_VBUS	TP96	5V
SOC_DVDD1V8	TP86	1.8V
SOC_DVDD3V3	TP83	3.3V
VCC_5V0	TP103	5V
VDDA_1V8	TP79	1.8V
VDD_CORE	TP53	0.85V/0.75V
VDDR_CORE	TP60	0.85V
VDD_2V5	TP92	2.5V
VPP_1V8	TP69	1.8V
VCC3V3_XDS	TP68	3.3V
VDD_MMC0_SD	TP21	3.3V
XDS_USB_VBUS	TP78	5V
VINT_LDO	TP74	1.8V
VCC_3V3_SYS	J29.3	3.3V
VCC1V8_SYS	J29.1	1.8V
VDDSHV_CANUART	TP80	1.8V
VDD_CANUART	TP52	0.85V
PMIC_LPM_EN0	TP75	1.8V

Table 2-18. Test Points (continued)

Power Supply	Test Point	Voltage
PMIC_EN	TP81	1.8V
MCU_ERRORn	TP54	1.8V
MCU_RESEZ	TP50	1.8V
RESETSTATz	TP592	1.8V
RESETSTATz_1V8	TP100	1.8V
WKUP_CLKOUT0	TP586	1.8V
MCU_PORz	TP49	1.8V
OSBCLK0	TP587	1.8V
DGND	J34.2, J9.2, TP1, J7.2, TP40, TP44, TP42, TP41, TP85, J32.2, TP106, J2.2, J21.2, J21.10, J31.12, TP2	0V

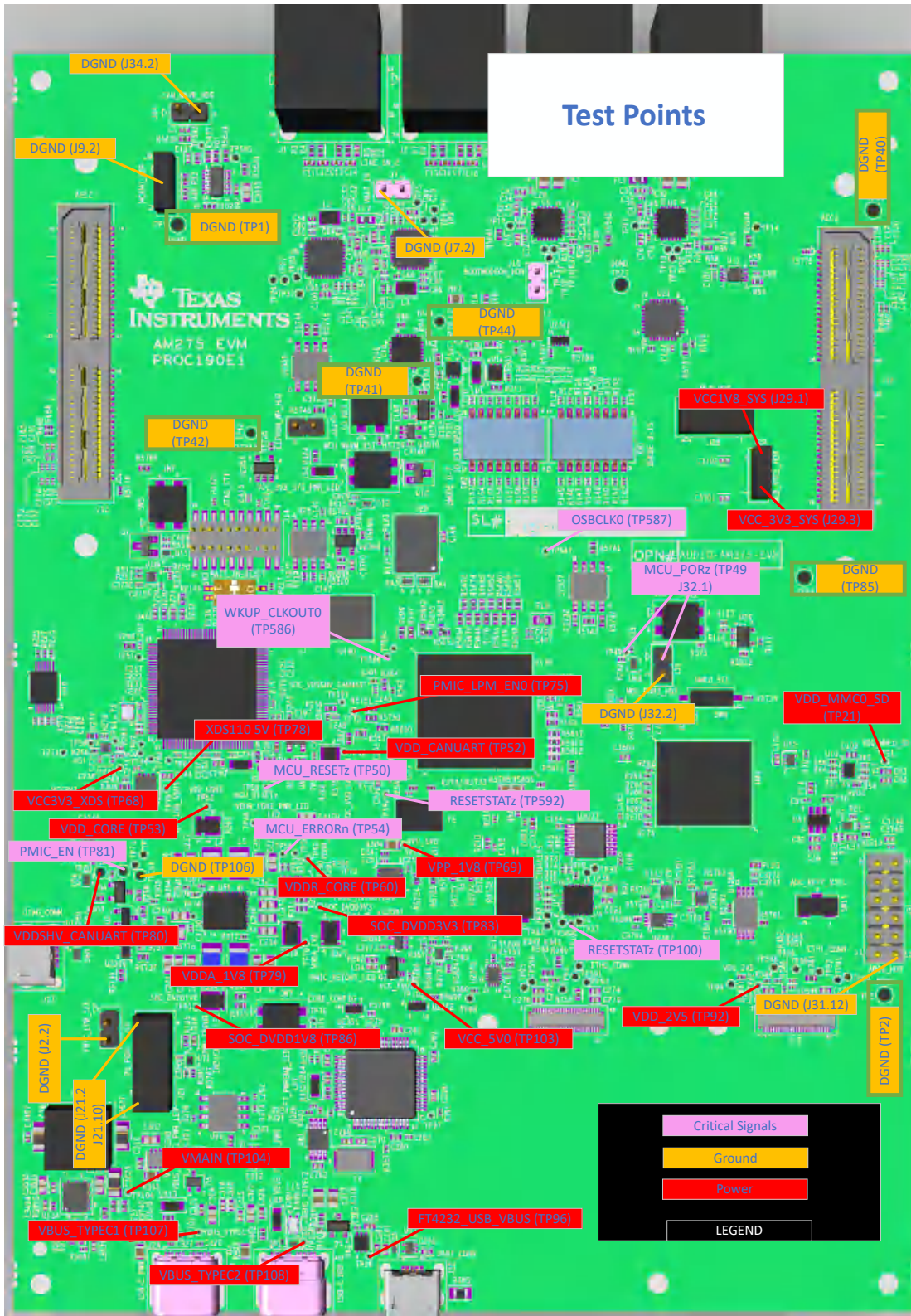


Figure 2-21. Test Points

3 Hardware Design Files

To download the zip file containing the latest design files for the EVM, click the following [link](#)

4 Additional Information

4.1 If You need Assistance

If you have any feedback or questions, support for the AM275x EVM is provided by the TI Product Information Center (PIC) and the [TI E2E™ Forum](#). Contact information for the PIC can be found on the [TI website](#). Additional device-specific information can be found in [Section 5.1](#).

4.2 Trademarks

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5 References

5.1 Reference Documents

In addition to this document, the following references are available for download at www.ti.com.

- [AM275x Signal Processing Microcontrollers](#)
- [AM275x Signal Processing Microcontrollers Data Sheet](#)
- [AM275x Signal Processing Microcontrollers Technical Reference Manual](#)
- [Texas Instruments Code Composer Studio](#)
- [Updating XDS110 Firmware](#)

5.2 Other TI Components Used This Design

This EVM uses various other TI components for the functions. A consolidated list of these components with links to the TI product pages is shown below.

- [TPS65224-Q1 PMIC](#)
- [TPS746 Low Dropout Regulator](#)
- [TLV7589P Low Dropout Regulator](#)
- [TPS7A21-Q1 Low Dropout Regulator](#)
- [TPS22810 Load Switch](#)
- [TPS65988 Power Delivery Controller](#)
- [LM61460-Q1 Step-Down Converter](#)
- [TMUX154E 2:1 Analog Switch](#)
- [LMK6C LVCMOS Oscillator](#)
- [LMK1C1103 Clock Buffer](#)
- [TMC1294NCPDT XDS110 Controller](#)
- [TMP411 Temperature Sensor](#)
- [TAD5212 stereo audio DAC](#)
- [PCM6240 Audio ADC](#)
- [CDCE6214 Clock Generator](#)
- [TS5A3357-Q1 3:1 Analog Switch Multiplexer](#)
- [TPS22919 Load Switch](#)
- [TPS22918 Load Switch](#)
- [TPS62824 Load Switch](#)
- [TS3DDR3812 1:2 Switch Multiplexer](#)
- [TMUX1136 2:1 Analog Switch](#)
- [TXB0108 Voltage-Level Translator](#)
- [INA228 Current Monitor with I2C Interface](#)
- [TCAN1043A-Q1 CAN Transceiver](#)
- [TCA6424A I/O Expander](#)
- [SN74AVC8T245 Boot Buffer](#)

6 Revision History

DATE	REVISION	NOTES
December 2024	*	Initial release.

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