WHITE PAPER

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Customizable system interfaces add value to embedded processors

Matching an application's requirements with an embedded processor's set of standard interfaces seldom results in a perfect match. Customizable interfaces help fill the gaps.

Introduction

Standard interfaces integrated into an embedded processor helps ease a system designer's work by providing interoperability with other products and reducing design cost and cycle time. But they can also make the choice of an embedded processor a bit problematic.

Realizing the importance of standard interfaces, embedded processor vendors such as Texas Instruments (TI), offer products with various combinations of embedded memory and peripheral interfaces. The goal is to match, as best as possible, the requirements of typical embedded applications.

Unfortunately, not all applications fit neatly into the definition of "typical". In this situation, the system designer may need to select a processor that integrates one or more interfaces that the application does not require, or, may have to add an external circuit to provide needed functionality adding extra cost in the solution. At times, both are required.

To address this problem, TI developed two circuits, the programmable real-time unit (PRU) and the universal Parallel Port (uPP), that are flexible enough to take the place of a peripheral interface or other function(s). For example, the PRU offers system designers the flexibility to configure an interface to networks including controller area network (CAN), PROFIBUS and various communications applications.

Since the PRU contains two packet data structure processor cores, it can be utilizied to provide real-time processing resources while the uPP is a good fit for system processors requiring interfaces with high-speed DACs, ADCs, digital signal processors (DSPs) and FPGAs capable of data transfers of the order of 250 MB/s.

In addition to providing an overview of the PRU and uPP architectures and benefits, this white paper will also describe TI's implementations of various standard interfaces including the USB, SATA, DDR and EMAC and their variants.

PRU: Real-time processing

The PRU is a small, 32-bit processing engine with a four-bus architecture allowing instructions to be fetched and executed concurrently with data transfers. Additionally, external status information can be reflected in an internal processor status register.

Available on the Sitara™ ARM® microprocessors (MPUs) platform, TI designed a large amount of flexibility into the PRU to enable a wide range of functions. For example, PRU has full visibility of the host system's resources, including all system memory, input/output (I/Os) and interrupts.

To minimize its on-chip footprint, TI maintained the PRU's internal resources relatively modest with four KBytes of instruction memory and 512 Bytes of data memory. Additionally, the PRU provides its own GPIOs with latencies measured in nanoseconds.

The PRU can be programmed with simple assembly code to implement custom logic. The instruction set is divided into four categories:

1. to move data in or out of the processor's internal registers
2. to perform arithmetic operations

3. to perform logical operations
4. to control program flow

In addition to being an I/O replacement, the PRU can be programmed to execute a variety of control, monitoring or other functions not available on-chip. This flexibility is helpful in applications encompassing control requirements that do not match those available on any of the standard processor configurations.

Frequently used industrial interfaces that PRU can implement include:

- **Process Field Bus (PROFIBUS)**: A standard for field bus communication in automation technology. It has two implementations. PROFIBUS Decentralized Peripherals (DP): For sensors and actuators and utilizes a centralized controller. PROFIBUS Process Automation (PA) monitors measuring equipment with a process-control system.
- **CAN-Lite bus**: Typically, CAN networks consist of sensors, actuators and other control devices. These devices are not connected directly to the bus, but through a host processor and a CAN controller.
- **IEEE 1588 or precision protocol (PTP)**: A high-precision time-stamping capability for time synchronization protocol used in network measurement and control systems.
- **IO-LINK**: Up to eight UARTs can be configured with the PRU to support the new process automation standard that links sensors and actuators to control devices.

Figure 1 illustrates how the PRU running interacts in a PROFIBUS DP master and slave application. It can also be configured as industrial Ethernet (PROFINET) slaves and for sampling and signal conditioning.

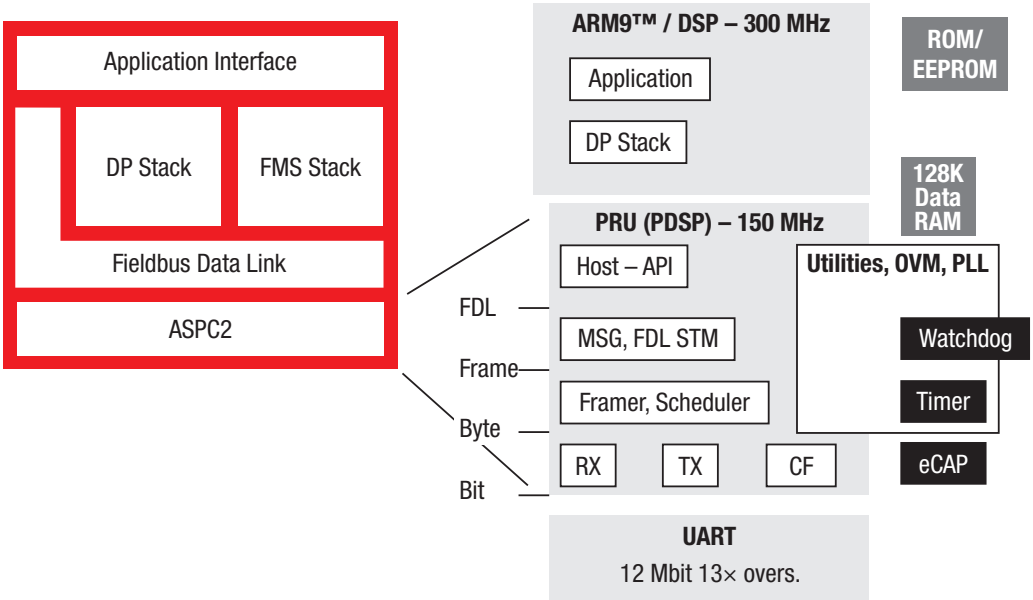

Figure 1. PRU implemented in a PROFIBUS application

Without the PRU, the PROFIBUS interface shown in Figure 1 would typically be implemented in a 32-pin ASIC in a DIP package. Eliminating the ASIC from the design saves about U.S. $5 to system cost and the PRU solution also saves board space and design time. Both master and slave PROFIBUS functionality can be implemented using the PRU.

uPP: A configurable parallel data bus

The basic architecture of the uPP includes separate, parallel data buses that can be configured to handle more than one word length. Data widths of eight to 16 bits per channel are possible. The uPP also has an internal DMA block so data transfers do not draw down the CPU's MIPS budget. Single or double data rates and multiple data packing formats are also part of the uPP's features.

The uPP is available on a variety of TI DSPs such as processors with the TMS320C674x cores, an OMAP-L138 device with a C674x core and the AM1x Sitara ARM9™ MPUs. Unlike serial peripherals such as SPI and UARTs, uPP offers designers the advantages of a parallel data bus with a data width of eight to 16 bits per channel.

When running at its maximum clock speed of 75 MHz, uPP transfers data much faster than the serial port peripherals. For example, a single 16-bit uPP channel operating at 75 MHz is as much as 24 times faster than a SPI peripheral operating at 50 MHz.

A simplified uPP block diagram is shown in Figure 2.

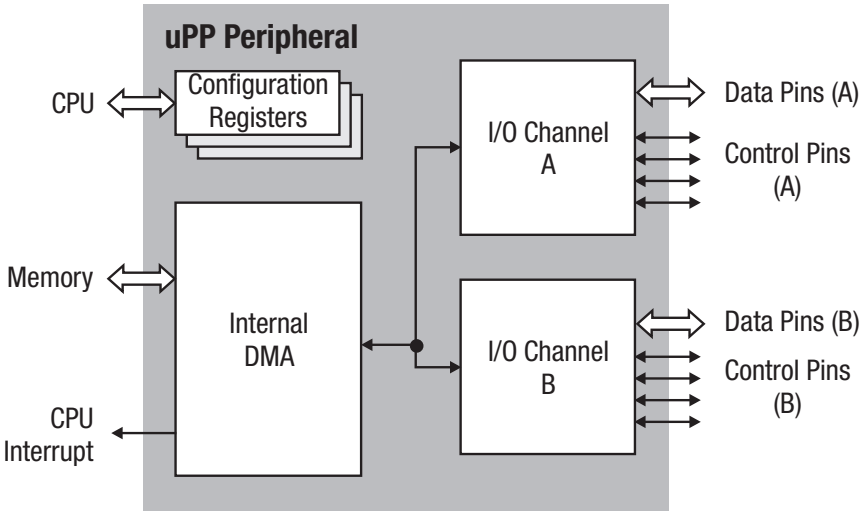

Figure 2. uPP simplified block diagram.

Features of the uPP include:

- Two independent channels with separate data buses
  - Channels can operate in same or opposing directions simultaneously
- I/O speeds up to 75 MHz with 8–16-bit data width per channel
- Internal DMA – leaves chip-level EDMA free

- Simple protocol with few control pins (configurable: 2–4 per channel)
- Single and double data rates (use one or both edges of clock signal)
  - Double data rate imposes a maximum clock speed of 37.5 MHz
- Multiple data packing formats for 9–15-bit data widths
- Data interleave mode (single channel only)

uPP bears some resemblance to another TI peripheral dedicated to configurable data handling, the host port interface (HPI). While the two hold various similarities, they differ significantly. Like HPI, uPP offers a high-speed parallel data bus. Unlike HPI, however, uPP does not grant direct memory access to an external device; and, it requires I/O transfers to be queued by device software. Perhaps the biggest difference is that uPP is considerably faster than HPI and possess much simpler protocol.

uPP can be configured to have one or two channels, 8- or 16-bit words, and either one-way or two-way data transfer simultaneously. Table 1 shows both theoretical and experimental data speeds for several operating modes.

A comparison to HPI is included on the bottom row of the table. The uPP peripheral has a maximum clock speed of 75 MHz but can support a clock of only 50 MHz in the two-channel, one-way, 16-bit configuration.

Table 1.

uPP Mode	Theoretical (MB/s)	Realistic (MB/s)
1 ch, 8-bit	75	60
1 ch, 16-bit	150	120
2 ch, 1 way, 8-bit	150	120
2 ch, 1 way, 16-bit	200	160
2 ch, 2 way, 8-bit	150	120
2 ch, 2 way, 16-bit	300	240
HPI (16 bit)	–	50

In addition to the two custom peripherals described above, TI offers a range of standard peripherals. Although the interface itself conforms to a standard, in many instances, the on-chip implementation is specific to TI and offers greater efficiency or performance.

EMAC

The EMAC module provided by TI provides a complete on-chip subsystem that implements an efficient interface between the core processor and the external Ethernet network. It supports 10Base-T (10 Mb/s) and 100Base-TX (100 Mb/s) in either half- or full-duplex mode, and 1000Base-T (1000 Mb/s) in full-duplex mode, with hardware flow control and quality-of-service (QoS) support.

The functionality specified for the physical layer (PHY) by the IEEE 802.3 Ethernet standard is implemented in a management data input/output (MDIO) module. The MAC layer of the protocol is implemented by the EMAC.

The EMAC module has a communications port programming interface (CPPI) buffer manager that manages 8K Bytes of CPPI RAM. Four 32-bit words are used as buffer descriptors that point to buffers in the processor memory.

The control registers of the EMAC and MDIO modules are memory mapped into device memory space. The MDIO module implements an 802.3 serial management interface to control up to 32 Ethernet PHYs over a shared two-wire bus.

Application software utilizes the MDIO module to configure the auto-negotiation parameters of each PHY attached to the EMAC, retrieve the negotiation results and configure required parameters in the EMAC module for correct operation. The module is designed to allow almost transparent operation of the MDIO interface, with very little maintenance from the core processor. A single MDIO is shared by both EMACs.

Both the EMAC and MDIO modules access the system core through MAC control module, which also optimizes data flow. In completely integrated solutions such as embedded processors from TI, the custom interface is considered integral to the EMAC/MDIO peripheral.

A complete EMAC subsystem is illustrated in Figure 3.

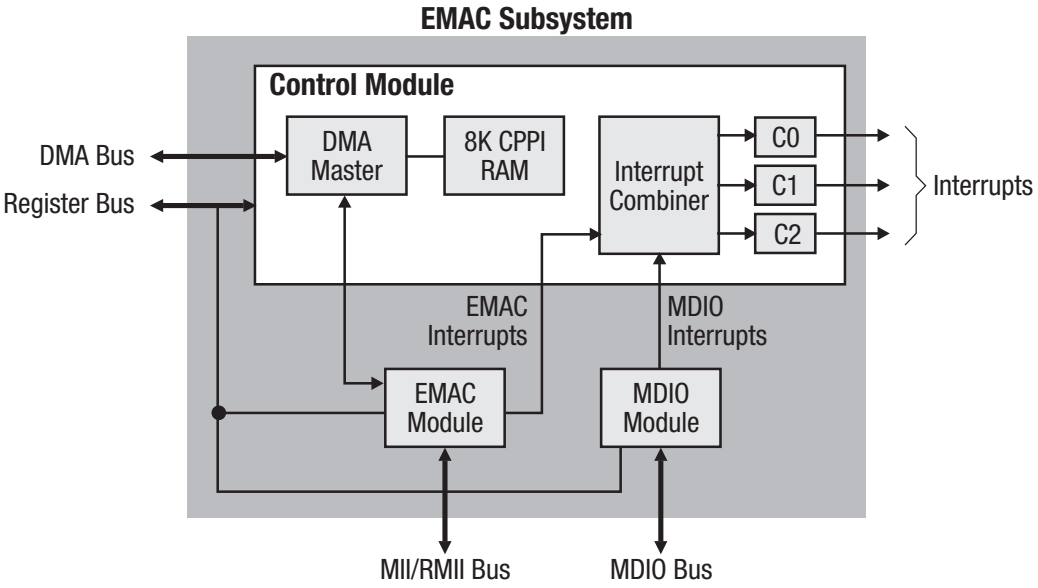

Figure 3. EMAC subsystem.

Given that Ethernet is so widely used, embedded processors typically integrate one or more EMAC interfaces on chip. There is some variation in the way different vendors implement the complete EMAC subsystem described above. The quality and extent of software support and libraries for implementing Ethernet interfaces is another decision point in choosing an embedded processor vendor.

USB

The universal serial bus (USB) interface describes three device classes of primary interest to design engineers. The USB human interface device (HID) class interfaces to keyboards, mice and oscilloscopes. USB communication device class (CDC) was created for modems and faxes but supports simple networking with

its interface for transmitting Ethernet packets. Similarly, USB mass storage device (MSD) targets hard disk drives and other storage media.

USB 2.0 is by far the most common USB variant. It has three speed options:

- High-speed (480 Mbps)
- Low-speed (1.5Mbps), and
- Full-speed (12 Mbps)

The specification also defines three basic devices, host controllers, hubs and peripherals.

USB 2.0 utilizes a tiered-star topology with a hub at the center of each star. Each wire segment is a point-to-point connection between the host and a hub or function, or a hub connected to another hub or function.

The addressing scheme used for devices in a USB 2.0 system allows for up to 127 devices to be connected to a single host. Any combination of hubs or peripherals is allowed.

TI adds value to its USB implementations by having available royalty-free software libraries to target specific USB functionality. Instead of writing their own code to implement the interface, system designers simply make a function call.

An example of a comprehensive sub-set of USB functions is offered for TI Sitara™ processors. It includes code to implement the following functionality:

- Peripheral devices:
  - HID keyboard
  - HID mouse
  - CDC Serial
  - Mass storage
  - Audio
  - Device firmware upgrade
  - Oscilloscope

- Host examples:
  - Mass storage
  - HID keyboard
  - HID mouse

In 2007, the USB 3.0 Promoter Group was formed to create a faster USB variant that will be backward compatible with previous USB standards but deliver ten times the data of USB 2.0. USB 3.0 uses a new signaling scheme. Backward compatibility is maintained by keeping the USB 2.0 two-wire interface.

DDR2/Mobile DDR

Created to provide high-performance memory transfers, DDR2 transfers data on the rising and falling edges of the bus clock signal and operates at a high bus speed that its predecessor, DDR, to achieve a total off our data transfers per internal clock cycle. A simplified DDR2 controller interface and its relationship to the DDR2 memory chip and core logic are shown in Figure 4.

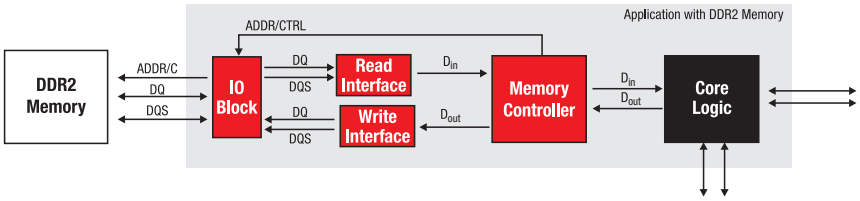

Figure 4. Simplified DDR2 controller implementation

The memory control block issues accesses from memory to the application-specific core logic or vice versa. The read physical block handles external signal timing that captures data during read cycles; and the write physical block manages the issuance of clock and data with the appropriate external signal timing.

A byte-wide, bidirectional data strobe (DQS) is transmitted externally along with data (DQ) for capture. DQS is transmitted edge-aligned by the controller during reads to memory and center aligned during writes to memory. On-chip delay-lock loops (DLLs) are used to clock out DQS and corresponding DQs. This assures that they can track each other during changes in voltage and temperature.

DDR2 SRAMs have differential clock inputs to reduce the effects of duty cycle variations on clock inputs. DDR2 SRAMs also support data mask signals to mask data bits during write cycles.

Mobile DDR (MDDR), also referred to as low-power double-data-rate memory (LPDDR), operates at 1.8 volts as opposed to the more traditional 2.5 volts and is commonly used in portable electronics. As with all DDR memory, the double data rate is achieved by transferring data on both clock edges of the device.

SATA

The serial ATA (SATA) bus connects host bus adapters to mass storage devices such as hard disk drives and optical drives. SATA's serial data format uses two differential pairs and can support interfaces to data storage devices at both 1.5 Gbits/s and 3.0 Gbits/s line speeds.

SATA attains its high performance in part by implementing an advanced system memory structure to accommodate high-speed serial data. The advanced host controller interface (AHCI) memory structure contains a generic area for control and status and a command list data table. Each entry in the command list table contains information for programming a SATA device as well as a pointer to a descriptor table for transferring data between system memory and the device.

Most SATA controllers support hot swapping and the use of a port multiplier to increase the number of devices that can be attached to the single HBA port. The SATA standard includes a long list of features but few SATA controllers support all of them. Features supported by TI include:

- Support for the AHCI controller spec 1.1
- Integrated SERDES PHY

- Integrated Rx and Tx data buffers
- Support for SATA power management features
- Internal DMA engine per port
- Hardware-assisted native command queuing (NCQ) for up to 32 entries
- 32-bit addressing
- Support for a port multiplier
- Activity LED support
- Mechanical presence detect

Conclusion

Although standard interfaces play a critical role in designing systems that are interoperable, low cost and require less time to design, their utility is still limited for a design team that needs to differentiate its product. Designers should research chip vendors for a wide variety of standard interfaces in multiple combinations. High-quality software libraries that help implement the interfaces efficiently are other differentiating factors for chip vendors. Offering an additional level of flexibility is also helpful and can be accomplished by configurable interfaces such as TI's PRU and uPP. By providing numerous options in tools kits, system designers can be creative while simultaneously keeping component costs low.

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