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ADDENDUM
TMS320C54x, TMS320LC54x, TMS320VC54x DATA SHEET (SPRS039B/C)

This addendum provides current updated information regarding different speed performance versions and available derivative devices in the ’54x family.

This addendum provides changed dc characteristics and parameter data that apply to the 66 and 80 MIPS version of the TMS320LC548 devices only.

Data in the unshaded cells is new and applies only to the TMS320LC548-66 and TMS320LC548-80 devices as indicated. The data in the shaded areas has not changed from that supplied in the current TMS320C54x, TMS320LC54x, TMS320VC54x data sheet (literature number SPRS039B/C). Please note the page numbers referenced apply to the SPRS039B/C data sheet.

electrical characteristics over recommended operating case temperature range (unless otherwise noted) (see page 61)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage‡		V_{DD} = 3.3 ± 0.3 V, I_{OH} = MAX	2.4			V
V_{OL}	Low-level output voltage‡		I_{OL} = MAX			0.4	V
I_{IZ}	Input current in high impedance	A[22:0] (’548/’549 only)	V_{DD} = MAX, V_O = V_{SS} to V_{DD}	–150		250	µA
		All other ’54x devices	V_{DD} = MAX, V_O = V_{SS} to V_{DD}	–10		10	
I_I	Input current (V_I = V_{SS} to V_{DD})	$\overline{TRST}$	With internal pulldown	–10		800	µA
		HPIENA	With internal pulldown, $\overline{RS}$ = 0	–10		400	
		TMS, TCK, TDI, HPI‖	With internal pullups	–400		10	
		D[15:0], HD[7:0]	Bus holders enabled, V_{DD} = MAX, V_I = V_{SS} to V_{DD}	–150		250	
		All other input-only pins		–10		10	
I_{DDC}	Supply current, core CPU		DV_{DD} = 3.0 V, f_X = 40 MHz,§ T_C = 25°C		28¶		mA
I_{DDC}	Supply current, core CPU (’549 only)		CV_{DD} = 2.5 V, f_X = 40 MHz,§ T_C = 25°C		20¶		mA
I_{DDP}	Supply current, pins		V_{DD} = 3.0 V, f_X = 40 MHz,§ T_C = 25°C		10.8#		mA
I_{DD}	Supply current, standby	IDLE2	PLL × 1 mode, 40 MHz input		2		mA
		IDLE3	Divide-by-two mode, CLKIN stopped		5		µA
C_i	Input capacitance				10		pF
C_o	Output capacitance				10		pF

† All values are typical unless otherwise specified.
‡ All input and output voltage levels except $\overline{RS}$, $\overline{INT0}$–$\overline{INT3}$, $\overline{NMI}$, CNT, X2/CLKIN, CLKMD0–CLKMD3 are LVTTL-compatible.
§ Clock mode: PLL × 1 with external source
¶ This value was obtained with 50% usage of MAC and 50% usage of NOP instructions. Actual operating current varies with program being executed.
# This value was obtained with single-cycle external writes, CLKOFF = 0 and load = 15 pF. For more details on how this calculation is performed, refer to the *Calculation of TMS320C54x Power Dissipation* application report (literature number SPRA164).
‖ HPI input signals except for HPIENA.

timing requirements over recommended operating conditions (see page 65)

		'LC548-80		UNIT
		MIN	MAX	
$t_{c(CI)}$	Cycle time, X2/CLKIN	6.25	†	ns
$t_{f(CI)}$	Fall time, X2/CLKIN		1	ns
$t_{r(CI)}$	Rise time, X2/CLKIN		1	ns
$t_{w(CIL)}$	Pulse duration, X2/CLKIN low	3	†	ns
$t_{w(CIH)}$	Pulse duration, X2/CLKIN high	2	†	ns

† This device utilizes a fully static design and therefore can operate with $t_{c(CI)}$ approaching ∞. The device is characterized at frequencies approaching 0 Hz.

switching characteristics over recommended operating conditions for a memory read ($\overline{MSTRB}$ = 0) [H = 0.5 $t_{c(CO)}$]†‡ (see page 68)

PARAMETER		'LC548-80		UNIT
		MIN	MAX	
$t_{d(CLKL-A)}$	Delay time, address valid from CLKOUT low§	0	6	ns
$t_{d(CLKH-A)}$	Delay time, address valid from CLKOUT high (transition)¶	0	5	ns
$t_{d(CLKL-MSL)}$	Delay time, $\overline{MSTRB}$ low from CLKOUT low	0	6	ns
$t_{d(CLKL-MSH)}$	Delay time, $\overline{MSTRB}$ high from CLKOUT low	0	5	ns
$t_{h(CLKL-A)R}$	Hold time, address valid after CLKOUT low§	0	6	ns
$t_{h(CLKH-A)R}$	Hold time, address valid after CLKOUT high¶	0	5	ns

† Address, $\overline{PS}$, and $\overline{DS}$ timings are all included in timings referenced as address.
‡ See Table 15, Table 16, and Table 17 for address bus timing variation with load capacitance.
§ In the case of a memory read preceded by a memory read
¶ In the case of a memory read preceded by a memory write

switching characteristics over recommended operating conditions for a memory write ($\overline{MSTRB}$ = 0) [H = 0.5 $t_{c(CO)}$]†‡ (see page 71)

PARAMETER		'LC548-80		UNIT
		MIN	MAX	
$t_{d(CLKH-A)}$	Delay time, address valid from CLKOUT high§	– 2	5	ns
$t_{d(CLKL-A)}$	Delay time, address valid from CLKOUT low¶	0	6	ns
$t_{d(CLKL-MSL)}$	Delay time, $\overline{MSTRB}$ low from CLKOUT low	0	6	ns
$t_{d(CLKL-D)W}$	Delay time, data valid from CLKOUT low	0	7	ns
$t_{d(CLKL-MSH)}$	Delay time, $\overline{MSTRB}$ high from CLKOUT low	0	5	ns
$t_{d(CLKH-RWL)}$	Delay time, R/$\overline{W}$ low from CLKOUT high	– 1	4	ns
$t_{d(CLKH-RWH)}$	Delay time, R/$\overline{W}$ high from CLKOUT high	– 1	4	ns
$t_{d(RWL-MSTRBL)}$	Delay time, $\overline{MSTRB}$ low after R/$\overline{W}$ low	H – 2	H + 2	ns
$t_{h(A)W}$	Hold time, address valid after CLKOUT high§	– 1	5	ns

† Address, $\overline{PS}$, and $\overline{DS}$ timings are all included in timings referenced as address.
‡ See Table 15, Table 16, and Table 17 for address bus timing variation with load capacitance.
§ In the case of a memory write preceded by a memory write.
¶ In the case of a memory write preceded by an I/O cycle.

switching characteristics over recommended operating conditions for a parallel I/O port read ($\overline{IOSTRB}$ = 0) [H = 0.5 $t_{c(CO)}$]†‡ (see page 73)

PARAMETER		’LC548-80		UNIT
		MIN	MAX	
$t_{d(CLKL-A)}$	Delay time, address valid from CLKOUT low	0	6	ns
$t_{d(CLKH-ISTRBL)}$	Delay time, $\overline{IOSTRB}$ low from CLKOUT high	– 1	4	ns
$t_{d(CLKH-ISTRBH)}$	Delay time, $\overline{IOSTRB}$ high from CLKOUT high	– 1	4	ns
$t_{h(A)IOR}$	Hold time, address after CLKOUT low	0	6	ns

† Address and $\overline{IS}$ timings are included in timings referenced as address.
‡ See Table 15, Table 16, and Table 17 for address bus timing variation with load capacitance.

timing requirements over recommended operating conditions for a parallel I/O port read ($\overline{IOSTRB}$ = 0) [H = 0.5 $t_{c(CO)}$]†‡ (see page 74)

		’LC548–66		’LC548-80		UNIT
		MIN	MAX	MIN	MAX	
$t_{a(A)IO}$	Access time, read data access from address valid		3H–10		3H–5	ns
$t_{a(ISTRBL)IO}$	Access time, read data access from $\overline{IOSTRB}$ low		2H–10		2H–5	ns
$t_{su(D)IOR}$	Setup time, read data before CLKOUT high	5		4		ns
$t_{h(D)IOR}$	Hold time, read data after CLKOUT high	2		2		ns
$t_{h(ISTRBH-D)R}$	Hold time, read data after $\overline{IOSTRB}$ high	0		0		ns

† Address and $\overline{IS}$ timings are included in timings referenced as address.
‡ See Table 15, Table 16, and Table 17 for address bus timing variation with load capacitance.

switching characteristics over recommended operating conditions for a parallel I/O port write ($\overline{IOSTRB}$ = 0) [H = 0.5 $t_{c(CO)}$]† (see page 75)

PARAMETER		’LC548-80		UNIT
		MIN	MAX	
$t_{d(CLKL-A)}$	Delay time, address valid from CLKOUT low‡	0	6	ns
$t_{d(CLKH-ISTRBL)}$	Delay time, $\overline{IOSTRB}$ low from CLKOUT high	– 1	4	ns
$t_{d(CLKH-D)IOW}$	Delay time, write data valid from CLKOUT high	H–5	H + 6	ns
$t_{d(CLKH-ISTRBH)}$	Delay time, $\overline{IOSTRB}$ high from CLKOUT high	– 1	4	ns
$t_{d(CLKL-RWL)}$	Delay time, R/$\overline{W}$ low from CLKOUT low	0	4	ns
$t_{d(CLKL-RWH)}$	Delay time, R/$\overline{W}$ high from CLKOUT low	0	5	ns
$t_{h(A)IOW}$	Hold time, address valid from CLKOUT low‡	0	6	ns
$t_{h(D)IOW}$	Hold time, write data after $\overline{IOSTRB}$ high	H–4	H+4	ns
$t_{su(D)IOSTRBH}$	Setup time, write data before $\overline{IOSTRB}$ high	H–4	H+1	ns
$t_{su(A)IOSTRBL}$	Setup time, address valid before $\overline{IOSTRB}$ low	H–5	H+5	ns

† See Table 15, Table 16, and Table 17 for address bus timing variation with load capacitance.
‡ Address and $\overline{IS}$ timings are included in timings referenced as address.

timing requirements over recommended operating conditions for externally generated wait states [H = 0.5 $t_{c(CO)}$]† (see page 79)

		’LC548-80		UNIT
		MIN	MAX	
$t_{su(RDY)}$	Setup time, READY before CLKOUT low	6		ns
$t_{h(RDY)}$	Hold time, READY after CLKOUT low	0		ns
$t_{v(RDY)MSTRB}$	Valid time, READY after $\overline{MSTRB}$ low‡		4H – 10	ns
$t_{h(RDY)MSTRB}$	Hold time, READY after $\overline{MSTRB}$ low‡	4H		ns
$t_{v(RDY)IOSTRB}$	Valid time, READY after $\overline{IOSTRB}$ low‡		5H – 10	ns
$t_{h(RDY)IOSTRB}$	Hold time, READY after $\overline{IOSTRB}$ low‡	5H		ns
$t_{v(MSCL)}$	Valid time, $\overline{MSC}$ low after CLKOUT low	0	4	ns
$t_{v(MSCH)}$	Valid time, $\overline{MSC}$ high after CLKOUT low	0	4	ns

† The hardware wait states can be used only in conjunction with the software wait states to extend the bus cycles. To generate wait states by READY, at least two software wait states must be programmed. READY is not sampled until the completion of the internal software wait states.
‡ These timings are included for reference only. The critical timings for READY are those referenced to CLKOUT.

switching characteristics over recommended operating conditions for memory control signals and $\overline{HOLDA}$ [H = 0.5 $t_{c(CO)}$] (see page 84)

PARAMETER		’LC548-66		’LC548-80		UNIT
		MIN	MAX	MIN	MAX	
$t_{dis(CLKL-A)}$	Disable time, CLKOUT low to address, $\overline{PS}$, $\overline{DS}$, $\overline{IS}$ high impedance		5		5	ns
$t_{dis(CLKL-RW)}$	Disable time, CLKOUT low to R/$\overline{W}$ high impedance		5		5	ns
$t_{dis(CLKL-S)}$	Disable time, CLKOUT low to $\overline{MSTRB}$, $\overline{IOSTRB}$ high impedance		5		5	ns
$t_{en(CLKL-A)}$	Enable time, CLKOUT low to address, $\overline{PS}$, $\overline{DS}$, $\overline{IS}$		2H + 5		2H+5	ns
$t_{en(CLKL-RW)}$	Enable time, CLKOUT low to R/$\overline{W}$ enabled		2H + 5		2H+5	ns
$t_{en(CLKL-S)}$	Enable time, CLKOUT low to $\overline{MSTRB}$, $\overline{IOSTRB}$ enabled		2H + 5	2	2H+5	ns
$t_{v(HOLDA)}$	Valid time, $\overline{HOLDA}$ low after CLKOUT low	0†	5	0	5	ns
	Valid time, $\overline{HOLDA}$ high after CLKOUT low	– 2	3	0	4	ns
$t_{w(HOLDA)}$	Pulse duration, $\overline{HOLDA}$ low duration	2H – 3		2H – 3		ns

timing requirements over recommended operating conditions for reset, interrupt, $\overline{BIO}$, and MP/$\overline{MC}$ [H = 0.5 $t_{c(CO)}$] (see page 87)

		’LC548-66		’LC548-80		UNIT
		MIN	MAX	MIN	MAX	
$t_{h(RS)}$	Hold time, $\overline{RS}$ after CLKOUT low	0		0		ns
$t_{h(BIO)}$	Hold time, $\overline{BIO}$ after CLKOUT low	0		0		ns
$t_{h(INT)}$	Hold time, $\overline{INTn}$, $\overline{NMI}$, after CLKOUT low†	0		0		ns
$t_{h(MPMC)}$	Hold time, MP/$\overline{MC}$ after CLKOUT low	0		0		ns
$t_{w(RSL)}$	Pulse duration, $\overline{RS}$ low‡¶	4H+10		4H+7		ns
$t_{w(BIO)S}$	Pulse duration, $\overline{BIO}$ low, synchronous	2H+10		2H+7		ns
$t_{w(BIO)A}$	Pulse duration, $\overline{BIO}$ low, asynchronous	4H		4H		ns
$t_{w(INTH)S}$	Pulse duration, $\overline{INTn}$, $\overline{NMI}$ high (synchronous)	2H+10		2H+7		ns
$t_{w(INTH)A}$	Pulse duration, $\overline{INTn}$, $\overline{NMI}$ high (asynchronous)	4H		4H		ns
$t_{w(INTL)S}$	Pulse duration, $\overline{INTn}$, $\overline{NMI}$ low (synchronous)	2H+10		2H+7		ns
$t_{w(INTL)A}$	Pulse duration, $\overline{INTn}$, $\overline{NMI}$ low (asynchronous)	4H		4H		ns
$t_{w(INTL)WKP}$	Pulse duration, $\overline{INTn}$, $\overline{NMI}$ low for IDLE2/IDLE3 wakeup	10		10		ns
$t_{su(RS)}$	Setup time, $\overline{RS}$ before X2/CLKIN low§	5		5		ns
$t_{su(BIO)}$	Setup time, $\overline{BIO}$ before CLKOUT low	10	13	10	13	ns
$t_{su(INT)}$	Setup time, $\overline{INTn}$, $\overline{NMI}$, $\overline{RS}$ before CLKOUT low	10	14	10	14	ns
$t_{su(MPMC)}$	Setup time, MP/$\overline{MC}$ before CLKOUT low	10		10		ns

† The external interrupts ($\overline{INT0}$–$\overline{INT3}$, $\overline{NMI}$) are synchronized to the core CPU by way of a two flip-flop synchronizer which samples these inputs with consecutive falling edges of CLKOUT. The input to the interrupt pins is required to represent a 1–0–0 sequence at the timing that is corresponding to three CLKOUTs sampling sequence.

‡ If the PLL mode is selected, then at power-on sequence, or at wakeup from IDLE3, $\overline{RS}$ must be held low for at least 50 μs to assure synchronization and lock-in of the PLL.

§ Divide-by-two mode

¶ Note that $\overline{RS}$ may cause a change in clock frequency, therefore changing the value of H (see the PLL section).

switching characteristics over recommended operating conditions for $\overline{IAQ}$ and $\overline{IACK}$ [H = 0.5 $t_{c(CO)}$] (see page 89)

PARAMETER		’LC548-66		’LC548-80		UNIT
		MIN	MAX	MIN	MAX	
$t_{d(CLKL-IAQL)}$	Delay time, $\overline{IAQ}$ low from CLKOUT low	0	5	0	5	ns
$t_{d(CLKL-IAQH)}$	Delay time, $\overline{IAQ}$ high from CLKOUT low	– 2	3	0	5	ns
$t_{d(A)IAQ}$	Delay time, address valid before $\overline{IAQ}$ low		4		4	ns
$t_{d(CLKL-IACKL)}$	Delay time, $\overline{IACK}$ low from CLKOUT low	– 2	3	– 1	4	ns
$t_{d(CLKL-IACKH)}$	Delay time , $\overline{IACK}$ high from CLKOUT low	– 2	3	– 1	4	ns
$t_{d(A)IACK}$	Delay time, address valid before $\overline{IACK}$ low		3		3	ns
$t_{h(A)IAQ}$	Hold time, address valid after $\overline{IAQ}$ high	0		– 4		ns
$t_{h(A)IACK}$	Hold time, address valid after $\overline{IACK}$ high	0		– 3		ns
$t_{w(IAQL)}$	Pulse duration, $\overline{IAQ}$ low	2H – 3		2H – 3		ns
$t_{w(IACKL)}$	Pulse duration, $\overline{IACK}$ low	2H – 3		2H – 3		ns

switching characteristics over recommended operating conditions for external flag (XF) and TOUT [H = 0.5 $t_{c(CO)}$] (see page 90)

PARAMETER		’LC548-66		’LC548-80		UNIT
		MIN	MAX	MIN	MAX	
$t_{d(XF)}$	Delay time, XF high after CLKOUT low	0	5	0	5	ns
	Delay time, XF low after CLKOUT low	0	5	0	5	
$t_{d(TOUTH)}$	Delay time, TOUT high after CLKOUT low	– 2	3	0	4	ns
$t_{d(TOUTL)}$	Delay time, TOUT low after CLKOUT low	–2	3	0	4	ns
$t_{w(TOUT)}$	Pulse duration, TOUT	2H – 3		2H – 3		ns

timing requirements over recommended operating conditions for serial port receive [H = 0.5 $t_{c(CO)}$] (see page 91)

		’LC548-66		’LC548-80		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(SCK)}$	Cycle time, serial port clock	6H	†	6H	†	ns
$t_{f(SCK)}$	Fall time, serial port clock		6		6	ns
$t_{r(SCK)}$	Rise time, serial port clock		6		6	ns
$t_{w(SCK)}$	Pulse duration, serial port clock low/high	3H		3H		ns
$t_{su(FSR)}$	Setup time, FSR before CLKR falling edge	6		4		ns
$t_{su(DR)}$	Setup time, DR before CLKR falling edge	6		4		ns
$t_{h(FSR)}$	Hold time, FSR after CLKR falling edge	6		6		ns
$t_{h(DR)}$	Hold time, DR after CLKR falling edge	6		6		ns

† The serial port design is fully static and, therefore, can operate with $t_{c(SCK)}$ approaching ∞. It is characterized approaching an input frequency of 0 Hz but tested at a much higher frequency to minimize test time.

switching characteristics over recommended operating conditions for serial port transmit with external clocks and frames [H = 0.5$t_{c(CO)}$] (see page 92)

PARAMETER		’LC548-66		’LC548-80		UNIT
		MIN	MAX	MIN	MAX	
$t_{d(DX)}$	Delay time, DX valid after CLKX rising		25		25	ns
$t_{h(DX)}$	Hold time, DX valid after CLKX rising	– 5		– 5		ns
$t_{dis(DX)}$	Disable time, DX after CLKX rising		40		40	ns

timing requirements over recommended operating conditions for serial port transmit with external clocks and frames [H = 0.5$t_{c(CO)}$] (see page 92)

		’LC548-66		’LC548-80		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(SCK)}$	Cycle time, serial port clock	6H	‡	6H	‡	ns
$t_{h(FSX)}$	Hold time, FSX after CLKX falling edge (see Note 1)	6		6		ns
$t_{h(FSX)H}$	Hold time, FSX after CLKX rising edge (see Note 1)		2H–5§		2H–3§	ns
$t_{f(SCK)}$	Fall time, serial port clock		6		6	ns
$t_{r(SCK)}$	Rise time, serial port clock		6		6	ns
$t_{w(SCK)}$	Pulse duration, serial port clock low/high	3H		3H		ns
$t_{d(FSX)}$	Delay time, FSX after CLKX rising edge		2H–5		2H–3	ns

‡ The serial port design is fully static and, therefore, can operate with $t_{c(SCK)}$ approaching ∞. It is characterized approaching an input frequency of 0 Hz but tested at a much higher frequency to minimize test time.

§ If the FSX pulse does not meet this specification, the first bit of serial data is driven on DX until the falling edge of FSX. After the falling edge of FSX, data is shifted out on DX pin. The transmit buffer-empty interrupt is generated when the $t_{h(FSX)}$ and $t_{h(FSX)H}$ specification is met.

NOTE 1: Internal clock with external FSX and vice versa are also allowable. However, FSX timings to CLKX always are defined depending on the source of FSX, and CLKX timings always are dependent upon the source of CLKX. Specifically, the relationship of FSX to CLKX is independent of the source of CLKX.

switching characteristics over recommended operating conditions for serial port transmit with internal clocks and frames [H = 0.5$t_{c(CO)}$] (see page 93)

PARAMETER		’LC548-66			’LC548-80			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$t_{c(SCK)}$	Cycle time, serial port clock		8H			8H		ns
$t_{d(FSX)}$	Delay time, CLKX rising to FSX			15			7	ns
$t_{d(DX)}$	Delay time, CLKX rising to DX			15			7	ns
$t_{dis(DX)}$	Disable time, CLKX rising to DX			20			20	ns
$t_{h(DX)}$	Hold time, DX valid after CLKX rising edge	–5			–2			ns
$t_{f(SCK)}$	Fall time, serial port clock		4				3	ns
$t_{r(SCK)}$	Rise time, serial port clock		4				3	ns
$t_{w(SCK)}$	Pulse duration, serial port clock low/high	4H–8			4H–4			ns

switching characteristics over recommended operating conditions [H = 0.5tc(CO)] (see page 97)

PARAMETER		’LC548-66		’LC548-80		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(SCK)}$	Cycle time, serial port clock, internal clock	20	62H	20	62H	ns
$t_{d(BFSX)}$	Delay time, BFSX after BCLKX rising edge (see Notes 3 and 4)		10		10	ns
$t_{d(BDX)}$	Delay time, BDX valid after BCLKX rising edge		8		8	ns
$t_{dis(BDX)}$	Disable time, BDX after BCLKX rising edge	0	5	0	5	ns
$t_{dis(BDX)pcm}$	Disable time, PCM mode, BDX after BCLKX rising edge		5		5	ns
$t_{en(BDX)pcm}$	Enable time, PCM mode, BDX after BCLKX rising edge	7		7		ns
$t_{h(BDX)}$	Hold time, BDX valid after BCLKX rising edge	0		0		ns
$t_{f(SCK)}$	Fall time, serial port clock		4		4	ns
$t_{r(SCK)}$	Rise time, serial port clock		4		4	ns
$t_{w(SCK)}$	Pulse duration, serial port clock low/high	6		6		ns

NOTES: 3. Internal clock with external BFSX and vice versa are also allowable. However, BFSX timings to BCLKX always are defined depending on the source of BFSX, and BCLKX timings always are dependent upon the source of BCLKX.
4. Timings for BCLKX and BFSX are given with polarity bits (BCLKP and BFSP) set to 0.

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