TCI6634K2K

Communications Infrastructure KeyStone SOC

Silicon Revisions 1.0, 1.1

Silicon Errata

Literature Number: SPRZ400
June 2013

Release History

Release	Date	Description/Comments
SPRZ400	June 2013	Initial Release

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Introduction

This document describes the silicon updates to the functional specifications for the TCI6634K2K fixed-/floating-point digital signal processor. See the device-specific data manual for more information.

Device and Development Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all devices and support tools. Each family member has one of two prefixes: X or [blank]. These prefixes represent evolutionary stages of product development from engineering prototypes through fully qualified production devices/tools.

Device development evolutionary flow:

- **X:** Experimental device that is not necessarily representative of the final device's electrical specifications
- **[Blank]:** Fully qualified production device

Support tool development evolutionary flow:

- **X:** Development-support product that has not yet completed Texas Instruments internal qualification testing.
- **[Blank]:** Fully qualified development-support product

Experimental (X) and fully qualified [Blank] devices and development-support tools are shipped with the following disclaimer:

Developmental product is intended for internal evaluation purposes.

Fully qualified and production devices and development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that experimental devices (X) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

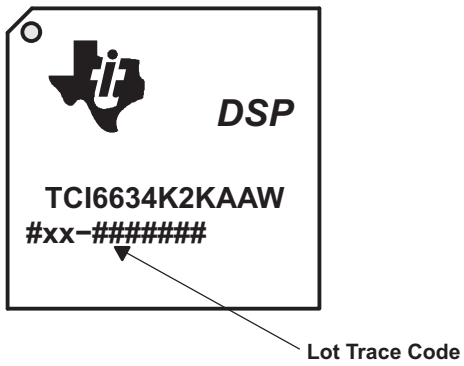
TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, AAW), the temperature range (for example, blank is the default case temperature range), and the device speed range, in Megahertz (for example, blank is 1000 MHz [1 GHz]).

For device part numbers and further ordering information for TCI6634in the AAW package type, see the TI website www.ti.com or contact your TI sales representative.

Package Symbolization and Revision Identification

The device revision can be determined by the lot trace code marked on the top of the package. The location of the lot trace code for the CMS package is shown in Figure 1. Figure 1 also shows an example of TCI6634 package symbolization.

Figure 1 Lot Trace Code Example for TCI6634K2K (CMS Package)



Silicon revision correlates to the lot trace code marked on the package. This code is of the format #xx-#######. Note that there may be an additional leading character (not shown in this example) and xx may actually be two or three characters. If xx is ***10***, then the silicon is revision 1.0. Table 1 lists the silicon revisions associated with each lot trace code for the TCI6634 devices.

Table 1 Lot Trace Codes

Lot Trace Code (xx)	Silicon Revision	Comments
10	1.0	Initial silicon revision
11	1.1	Silicon revision 1.1

The TCI6634 device contains multiple read-only register fields that report revision values. The JTAG ID (JTAGID) and C66x CorePac Revision ID registers allow the customer to read the current device and CPU level revision of the TCI6634.

The JTAG ID register (JTAGID) is a read-only register that identifies to the customer the JTAG/Device ID.

The C66x CorePac Revision ID register is a read-only register that identifies to the customer the revision of the C66x CorePac. The value in the VERSION field of the C66x CorePac Revision ID Register changes based on the version of the C66x CorePac implemented on the device. More details on the C66x CorePac Revision ID register can be found in the part-specific data manual.

Table 2 shows the contents of the C66x CorePac REVID Register and the JTAGID register for each silicon revision of the TCI6634 device.

Table 2 Silicon Revision Variables

Silicon Revision	C66x CorePac REVID Register (address location: 0x0181_2000)	TCI6634 JTAGID Register (address location: 0x0262_0018)
1.0	0x0009_ 0000	0x0b98_102f
1.1	0x0009_0002	0x1b98_102f
End of Table 2		

More details on the JTAG ID and CorePac Revision ID Registers can be found in the device-specific data manual.

Silicon Updates

Table 3 lists the silicon updates applicable to each silicon revision. For details on each advisory, click on the link below.

Table 3 Silicon Revision 1.0 Updates

Silicon Update Advisory	See[1]	Applies To Silicon Revision	
		1.0	1.1
Boot ROM Missed EMIF PHY Configuration Registers	KeyStoneII.BTS_errata_advisory.1	X	
SRIO Boot Mode Packet DMA Cleanup Missing	KeyStoneII.BTS_errata_advisory.4	X	
Sync-Ethernet Push Event IO Control Tie-Off Incorrect	KeyStoneII.BTS_errata_advisory.5	X	
DDR3A Lanes 5 and DDR3B Lane 8 Have PHY to PUB DFI Hold Time Failures	KeyStoneII.BTS_errata_advisory.10	X	
SPI Boot Size Limitation, C66x Master Boot	KeyStoneII.BTS_errata_usagenote.1	X	
Debug System (DebugSS) Trace Buffer (TBR) EDMA via System Port is not Functional	KeyStoneII.BTS_errata_usagenote.3	X	X
Boot I^2C Frequency Incorrect	KeyStoneII.BTS_errata_usagenote.5	X	X
Access to DDR3 Without Configuring PHY Properly Can Cause Hang	KeyStoneII.BTS_errata_usagenote.6	X	X
End of Table 3			

1. Not all KeyStone II errata apply to all KeyStone II parts. Therefore, numbering gaps in the errata list are normal.

Boot ROM Missed EMIF PHY Configuration Registers

Revision(s) Affected 1.0

Details Boot ROM missed initializing some EMIF PHY Configuration registers.

On PG1.0 Boot ROM, the built- in DDR3 PHY configuration for the DWCPUB PHY does not include values needed for PHY Config. The following values are needed to support configuring the PHY registers:

DDR3A_PLLCR offset 0x00000018

DDR3A_DSGCR offset 0x00000040

DDR3A_ZQ0CR1 offset 0x00000184

DDR3A_ZQ1CR1 offset 0x00000194

DDR3A_ZQ2CR1 offset 0x000001A4

DDR3A_ZQ3CR1 offset 0x000001B4

Workaround If the non-default values are required in these registers, a two stage boot must be used.

KeyStoneII.BTS_errata_advisory.4

SRIO Boot Mode Packet DMA Cleanup Missing

Revision(s) Affected 1.0

Details The issue is within the Boot ROM. In SRIO Boot Mode, the Packet DMA is not torn down when the SRIO boot is complete.

On PG1.0 devices, in SRIO boot mode, the boot ROM did not perform the Packet DMA cleanup (the Packet DMA is not torn down) when the boot is complete. All queues are emptied and the QM is torn down, but the Packet DMA is left up.

Workaround Before reconfiguration, the existing configuration should be torn down.

KeyStoneII.BTS_errata_advisory.5

Sync-Ethernet Push Event IO Control Tie-Off Incorrect

Revision(s) Affected 1.0

Details The tie-off for IO control for the two Sync-Ethernet Push Events is connected incorrectly in the design.

On PG1.0 devices, the tie-off for IO control for the two Sync-Ethernet Push Event (TSPUSHEVT0 (PPS Push Event from GPS for IEEE1588) and TSPUSHEVT1 (Push Event from BCN for IEEE1588)) IOs is connected incorrectly in the design. Consequence of this is that the TSPUSHEVT0 and TSPUSHEVT1 pads are being forced to outputs when not in reset, and thus **cannot** be selected as inputs. These pads are functionally used as inputs.

Workaround None.

KeyStoneII.BTS_errata_advisory.10

DDR3A Lanes 5 and DDR3B Lane 8 Have PHY to PUB DFI Hold Time Failures

Revision(s) Affected

1.0

Details

DDR3A Bit Errors in Data Byte Lane 5

It has been observed that operating DDR3A in 64-bit mode results in occasional read errors. The problem is observed across all frequencies of operation.

The read errors occur across byte lane 5 of the DDR3A interface due to hold time violations on the DFI interface between the PHY Utility Block and SDRAM PHY on this specific byte lane. Since the hold violations are only on byte lane 5, this issue impacts only 64-bit DDR3A operation and not 32-bit or 16-bit DDR3A operations.

Table 4 DDR3A

72 bit with ECC	Nonfunctional
64 bit without ECC	Nonfunctional
36 bit with ECC	Functional
32 bit without ECC	Functional
16 bit without ECC	Functional

Workaround

The only stable work around available at this time is to operate the DDR3A interface in 32-bit or 16-bit mode. These configurations would ensure the faulty byte lane is never activated.

Details

DDR3B Bit Errors in ECC Byte Lane

It has been observed that error correction is currently nonfunctional on the DDR3B interface. Turning on ECC during DDR3B operation results in occasional read errors as a result of miscalculated ECC values.

Table 5 DDR3B

72 bit with ECC	Nonfunctional
64 bit without ECC	Functional
36 bit with ECC	Nonfunctional
32 bit without ECC	Functional
16 bit without ECC	Functional

Workaround

The only stable work around available at this time is to operate DDR3B interface in non ECC mode. This configuration would ensure the faulty byte lane is never activated.

KeyStoneII.BTS_errata_usagenote.1

SPI Boot Size Limitation, C66x Master Boot

Revision(s) Affected 1.0

Details The issue is within the Boot ROM. In C66x Master, SPI Boot Mode, the SPI Boot Size is limited by the Boot ROM to a single block.

In SPI Boot Mode, the SPI Boot Size is limited by the Boot ROM to a single block. The max block read size is 8K bytes for C66x master boot.

Workaround A workaround is available that contains the fix in that first block read. The workaround can simply be prepended to customer boot images when placed on the flash. To obtain the workaround contact the TI E2E Forum or your local TI representative.

KeyStoneII.BTS_errata_usagenote.3

Debug System (DebugSS) Trace Buffer EDMA via System Port Not Functional

Revision(s) Affected 1.0, 1.1

Details Debug System (DebugSS) Trace Buffer (TBR) EDMA via System Port is not functional.

The TBR in the DebugSS is used to capture the output of CP-Tracers and System Trace Module (STM). The trace data can be accessed by debugger or application from either the configuration port or the system port. The system port is ideal for another master such as EDMA to read the trace data to a larger memory region. This allows more trace data to be captured into on-chip memory beyond the limited size of trace buffer.

The DebugSS TBR clock is integrated incorrectly in the design. Consequence of this is preventing the usage of EDMA to drain the contents of TBR.

Workaround None for the EDMA use case from the system port. The TBR can still be accessed via the configuration port.

Boot I^2C Frequency Incorrect

Revision(s) Affected 1.0, 1.1

Details The issue is within the Boot ROM. Initial boot I^2C frequency incorrect on $\overline{\text{RESET}}$ reset.

For I^2C boot, the code to determine the device frequency assumes that the PLL is in bypass. This is true for power on reset, but for $\overline{\text{RESET}}$, with the PLL reset isolated this is incorrect. The code should check to see if the PLL is enabled and if it is, it should return the e-fuse device frequency.

On a normal $\overline{\text{POR}}$ or $\overline{\text{RESETFULL}}$, boot with I^2C as the boot master, the boot code will correctly assume the system is running at 312 MHz (max possible) and scale the I^2C clock to run at 20 KHz. So the actual frequency will scale based on the actual reference clock. After boot execute a $\overline{\text{RESET}}$, the initial frequency will be much higher, running faster by a multiple equal to the actual effective PLL multiplier value.

For example if the actual reference clock is 50 MHz and the device frequency is e-fused for 1400 MHz, the initial I^2C will read using a data clock of 20 * 50 / 312 = 3.2 KHz. After a $\overline{\text{RESET}}$ reset, with the PLL reset isolated, the initial read will be at 20 * 1400 / 312 = 89 KHz. This will work with almost all I^2C devices that are compliant to the 100 KHz bus standard specified in the original I^2C specification. This represents the worst case for these devices.

Workaround None.

KeyStoneII.BTS_errata_usagenote.6

Access to DDR3 Without Configuring PHY Properly Can Cause Hang

Revision(s) Affected 1.0, 1.1

Details If the DDR3 is not configured properly before the C66x CorePac issuing an access to DRR3, the device could lock up.

If the DDR3 PHY Utility Block (PUB), DDR3 PHY and the EMIF Controller are not configured or improperly configured, any access to the DRR3 memory space is issued by the C66x CorePac, including opening a memory window view from the Code Composer Studio (CCS) that is pointed to the DDR3 memory space, the device could lock up.

Workaround It is recommended that before issuing an access to the DDR3, the device must properly initialize the DDR3 PUB, DDR3 PHY, and EMIF controller.

Refer to the KeyStone II DDR3 Programming Sequence documented in the KeyStone II DDR3 User Guide (SPRUGV8) or the KeyStone II DDR3 Initialization Sequence document (SPRABL2).

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