TEXAS INSTRUMENTS

SR40 0.095-µm High-Speed Copper Standard Cell/Gate Array ASIC

March 4, 2002

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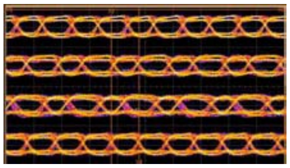
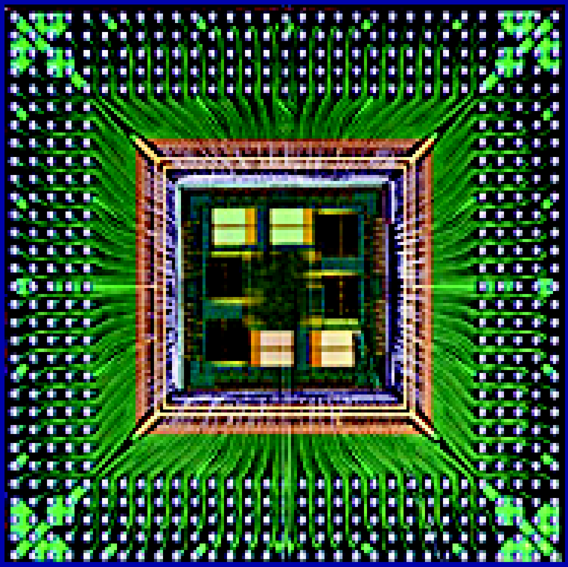
SR40 95-Nanometer High-Speed Standard Cell/ Gate Array ASIC

Product Specifications

- **95-nm Ldrawn transistor**
- **6 or 7 layers of second-generation dual-damascene copper** with low-K dielectric optimized for high performance
- 0.35 µm minimum metal pitch with hierarchical pitch optimized for performance and power distribution
- **Transistor performance of 37.4 GHz** (ring oscillator fanout of 3)
- Gate delays of 25ps (2-input NAND gate)
- Power dissipation of 9 nW/MHz/gate
- Power supply: 1.2v
- I/O power supply: 1.2v, 2.5v and 3.3v
- Synthesis-optimized libraries with macros in 5-11 drive strengths up to 32X
- Extremely high density SRAM compilers up to 450K bits/mm2 based on industry's smallest SRAM bit cell of 1.95 μm^2
- SRAM compilers up to 2Mb each and performance up to 950 MHz
- Spare gate array cells for fast metal-level changes
- Broad range of wirebond packages to 900 pins
- High-performance flipchip packaging to 2500 pins
- Scalable SERDES I/O technology providing in excess of 40Gbps synchronous and 2.5Gbps serial bandwidth per I/O or 640Gbps full duplex per device





The explosion in network bandwidth driven by the convergence of voice and data communications requires a specialized ASIC product. Optimized for the high-speed communications market, SR40 provides unparalleled performance and time-to-market. SR40 gives network equipment chip designers the tools they need to enable next-generation Dense Wavelength Division Multiplexing (DWDM) systems, backbone routers and multi-gigabit Ethernet switches.

Features and Benefits

SR40, the newest offering from TI ASIC, has the performance, integration, and low-peak power benefits to make next-generation internetwork applications a reality. SR40 brings to market TI’s industry-leading high-performance processor silicon process for maximum core speed. When combined with TI’s barrier-breaking SERDES I/O technology and integration expertise, ASIC designers can create the scalable aggregate bandwidth required for today’s exploding network demand.

The SR40 product is positioned to take advantage of TI’s world leadership in key areas of system-level integration and systems-on-a-chip design:

- World’s leading supplier of embedded ARM™ and MIPS™ cores, including the ARM 7 and ARM 9 families of RISC processors, and MIPS Jade™ and Opal™ processors
- World’s leading Digital Signal Processor (DSP) supplier
- World’s leading supplier of analog and data transmission solutions, including the IEEE 1394 link core, the Universal Serial Bus (USB) function controller, and the Universal Asynchronous Receiver/Transmitter (UART)
- Easy integration of DSP, ARM and MIPS cores with standard cell, gate-array logic and flexible choice of dense memories
- High complexity, high-gate-count design methodology with integrated hardware/software coverification
- Advanced 95-nm L_{drawn} process technology
- Superior design support and manufacturing— "no excuses" ramp to production

Advanced Technology

TI’s advanced process technology provides top-tier performance at reduced risk by using the second-generation of copper metal system used in TI’s high-performance processors. This provides a 46-percent reduction in interconnect delay and a 56-percent reduction in gate delay when compare to previous ASIC products. Combined with a 1.2v core power supply and low-peak power dissipation, SR40 provides the speed and power management capabilities critical for power-budgeted broadband equipment.

High-Speed I/O Interface Solutions

The SERDES high-speed I/O interface solutions are differential transceiver cores that support more than 128 channels at full duplex data rates from 0.5 Gigabits per second to in excess of 3.2 Gbps. Combined with the superior core logic performance of SR40, the SERDES solution enables the bandwidth required by today’s datacom/telecom data, video and voice transmission applications. Ideal for gigabit Ethernet applications, features include:

- Under 150 mW power per port at 3.2 Gbps
- Data serialization and deserialization

- Synchronous, uni- and bi-directional interfaces
- Differential receiver sensitivity of 100mV
- Flip-chip interface
- Low 10^{-18} bit error rate
- On-chip termination
- Loss of signal indication
- At-speed built-in self-test (BIST)
- Clock generation
- Clock recovery for the physical layer interface
- Selectable 8-bit and 10-bit interface
- No external loop components— monolithic PLL design
- Programmable output rise/fall times
- ESD protection greater than 2 kV

For applications such as synchronous digital hierarchy (SDH) and asynchronous transfer mode (ATM), SR40 includes macros for phase alignment and digital clock recovery with selectable I/O interface options. These provide for implementation of up to OC768 channels through a variety of speeds and are an excellent choice for cost-effective optical interfaces.

Open Design System

The Pyramid design system and high-performance, high-gate-count design methodology is focused on meeting the designer's predictability and time-to-market needs. This design approach lets the designer take full advantage of the high-performance characteristics that deep-submicron technology offers. Pyramid is an open EDA system that integrates the best technology from both TI and EDA industry design tools from multiple vendors in an environment that facilitates predictably meeting timing goals.

Features include:

- **Multi-vendor EDA strategy** based on industry standards. This system, combined with enhancements in the design flow, simplifies and speeds the design process to help you achieve timing closure. See Table 3 on page 11 for a list of supported CAD tools.
- **Clock tree synthesis (CTS)** design flow that provides automatic synthesis of clock trees in physical design to meet designers' skew and insertion delay goals. The TI CTS flow supports more than 200 clock domains and clock gating for low power, and consistently achieves less than 50 ps clock skew.
- **Complete STA signoff methodology** enables comprehensive verification and minimizes gate-level simulation efforts at design hand-off. The Synopsys PrimeTime™-based signoff flow is supported with delay fault test generation capability.
- **VHDL and Verilog™ signoff flows** for reduced cycle time and improved accuracy
- **Synopsys™ Power Compiler™ support** for power management

Packaging for Performance and Bandwidth

- **Package options** include thin quad flat pack (TQFP), MicroStar$^{\text{TM}}$ BGA, Plastic BGA, Generic BGA (Cavity Down), PowerPad and peripheral and array flip-chip. For more details, see Table 3 on page 11.

High-Speed Library

The SR40 family macro library has been optimized for high-performance design. As a result, the SR40 family library features:

- High-speed I/Os
- A rich set of Boolean functions
- A wide variety of gates with inverting inputs
- 5 to 11 multiple-drive-strength gates up to 32X
- Ultra-high-performance flip-flop and core macros

Analog functions include feedthroughs and high-frequency PLLs. The special function macros include electrically-readable die ID fuse-array macros.

Library Characterization

Every timing path through each SR40 family core and I/O macro is characterized at multiple voltage, temperature, process, input slew, and output load points. No global derating with respect to voltage, temperature, or process is used with the SR40 family. The characterized data coupled with nonlinear delay modeling allows SPICE-level accuracy in delay calculation.

Gate Array Macros

Using TI's unique TImeCell capability, designers have the flexibility to implement ECO changes at the point when the new functionality is known— after physical design. Using cells implemented as a gate-array architecture, the new functionality can be implemented quickly through metal-level changes with little or no impact on die size.

I/O Macros

SR40 provides a wide selection of interfaces such as 3.3-V low-voltage CMOS (LVCMOS), LVTTL, PCI, and differential signaling. LVCMOS and LVTTL buffers are available in two noise performance options: high performance and low noise. To minimize system noise and power pins, select the lowest noise output that the application allows. Low-noise I/Os typically require only half the number of power pins that high-performance I/Os require.

The designer can create a bidirectional macro for I/Os by selecting an input and an output and combining the functions in the netlist. You can add pullup and pulldown macros to I/Os in the same manner. I/O macros include:

- LVCMOS, LVTTL, TTL
- LVDS, PCI, SSTL_2, HSTL, DPECL
- Low noise, high performance and failsafe options
- 2/2mA - 12/24 mA output drivers

Table 1: I/O Specifications

Type	Maximum Frequency	Signal Swing	Signal Type
3.3 V LVCMOS	250 MHz	3.3 V	single
TTL	250 MHz	3.3 V	single
PCI	66 MHz	3 V	single
LVDS	800 MHz	0.25 - 0.45 V	100 mV
DPECL	800 MHz	0.6 - 1.3 V	300 mV
HSTL	400 MHz	1.5 V	single/differential
SSTL_2	200 MHz	2.5 V	single
TLV	250 MHz	0.8 V	300 mV

The maximum frequency rating is load, package, voltage, and slew dependent.

Memories

SR40 supports synchronous single-port, two-port, and dual-port memory compilers and ROM, CAM and asynchronous two-port compilers. These dense memories let you specify the exact word and bit counts for each memory to meet the application’s need. All memories can have synchronous operation, zero dc power and zero hold times. By providing a wide range of compiler options with access performance up to 950 MHz, maximum throughput in core logic is assured. The WebACE™ Toolkit allows you to easily create all model views using the most current data available for supported libraries. WebACE creates data sheets, logic and layout models for simulation, testing, and layout based on the required number of words, number of bits per word, and the column multiplex factor.

Table 2: Memories Summary

Name	Description	Max Bits	Min Bits	Max Words	Max Bits/ Word
BW/BX	1-port CROM, fast, via2 program	1Mbit	1	64K	64
BRE	1-port CRAM, multistrobe, page mode, low power	128K	512	4K	64
MW/BL	1-port CRAM, area optimized, bit write (BL)	128K	1	16K	64
MZE/MVE	1-port CRAM, density optimized, bit write (MV)	1Mbit	64K	32K	32
MG/BY	2-port register file (1W/1R), bit write (BY)	32K	2	512	256
MN/BG	Dual-port CRAM, bit write (BG)	128K	32	4K	128
BC	CAM compiler	128K	2K	1024	128

Single-Port Clocked SRAM Compiler

The single-port clocked SRAM compiler creates speed-optimized RAM blocks based on user specifications.

Dual-Port Clocked SRAM Compiler

The dual-port clocked SRAM compiler creates area- and speed-optimized RAM based on user specifications.

Two-Port Register File

In the 2-port register file, the read and write ports are completely independent and can access any location simultaneously. Writing to the RegFile is controlled by the write clock input (WCLK) and the write enable input (WEN). On the positive (rising) edge of WCLK, the write address bus (AW) inputs, write data bus (D) inputs, and the value of the write enable (WEN) input are latched. If the latched value of WEN is high, data will be written to the memory location indexed by AW. If the latched value of WEN is low, no write will occur.

CAM

The Content Addressable Memory (CAM) is an all-level compiler function that supports three search modes. In search mode, the mask inputs determine which comparand inputs are masked in the search operation. The second search mode lets you sequentially retrieve all address locations containing matching data when multiple hits are present. The third search option performs a normal search operation and resets the valid bit of all matching locations.

Synthesizable Memories

For maximum flexibility, SR40 offers a number of memory options for use as “soft,” or synthesizable, memories. This compiler generates RTL (based on your specifications) as well as constraints for synthesis. Synopsys Design Compiler™ is then used to synthesize these memories to either flip-flop or latch-based implementation with support for multiple test methodologies. The compiler options, which are ideal for small RAM configurations, are:

- 1-port CRAM area optimized
- Dual-port CRAM

0.5 - 3.2 Gbps SERDES High-Speed Transceiver Core

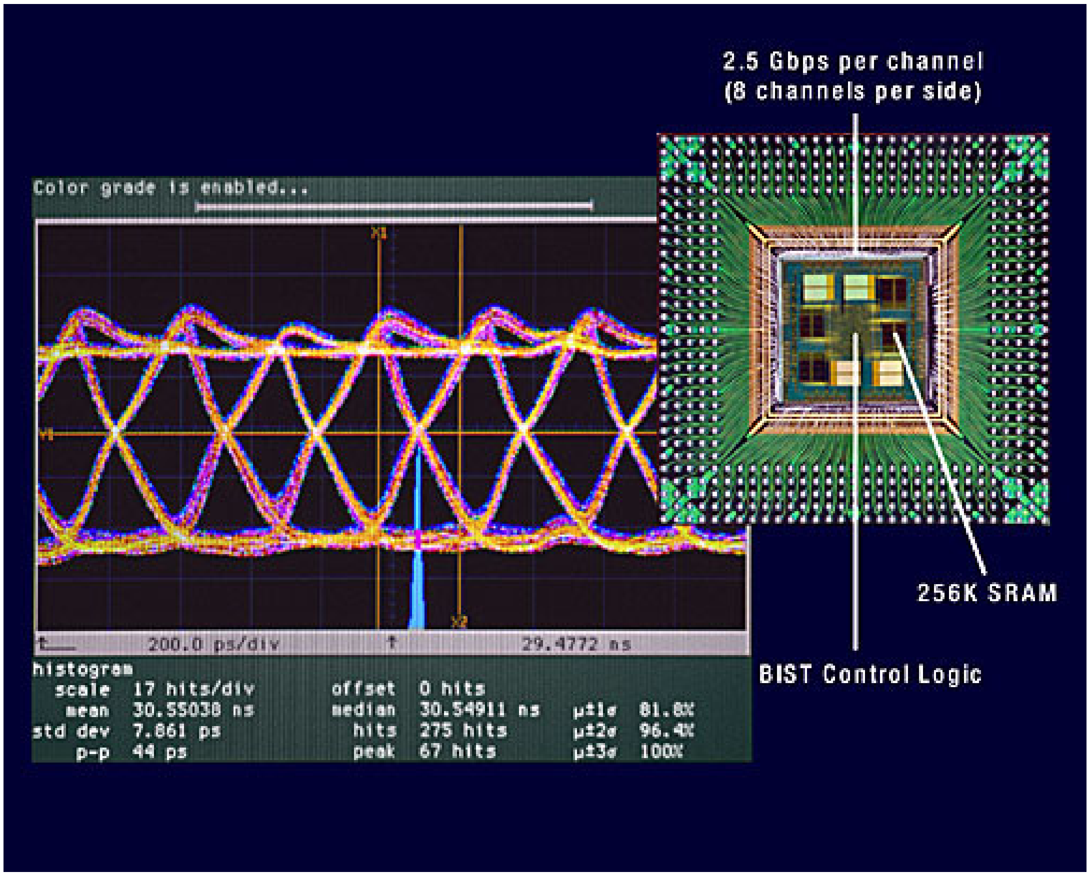
- 0.5 - 0.8 Gbps (half rate)
- 1.0 - 1.6 Gbps (full rate)
- 1.0 - 1.6 Gbps (half rate)
- 2.0 - 3.2 Gbsp (full rate)

The SERDES transceiver provides for ultra-high-speed bidirectional point-to-point data transmissions over 50Ω or 75Ω controlled impedence media such as printed circuit board, copper cables or fiber. A single SERDES port supports full-duplex data rates from 1.0 Gbps to more than 3.2 Gbps. Both 8-bit and 10-bit interfaces are supported under software control.

The SERDES transceiver core offers the possibility of building switch-routers with an order-of-magnitude increase in bandwidth over today’s high-performance switch-routers. It is also compatible with the many high-performance switching and routing systems that use 1.0 to 3.2 Gbps catalog products such as TI’s TLK2201. SERDES macros can be used to replace slower parallel data transmission architectures, providing a reduction in the number of traces, connector pins and transmit/receive pins. This solution offers significant power and cost savings over conventional solutions, as well as scalability for higher data rates in the future.

A SERDES port performs the clock generation, data serialization and deserialization, and clock extraction functions of a physical layer interface device. Parallel data loaded into the transmitter is serialized and transmitted differentially at a rate controlled by the supplied reference clock. The maximum rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the level of noise coupling from the environment. At the receiver, the data stream is deserialized and reconstructed into parallel format. in 10-bit mode, a comma detect feature can be used to properly byte align the reconstructed parallel data. In 8-bit mode, byte alignment, if required, must be performed outside the macro.

Figure 1: SERDES Transceiver Core



```
histogram
   scale  17 hits/div          offset  0 hits
    mean  30.55038 ns          median  30.54911 ns   µ±1σ  81.8%
 std dev  7.861 ps               hits  275 hits      µ±2σ  96.4%
     p-p  44 ps                  peak  67 hits       µ±3σ  100%
```

The SERDES macros provide several built-in self-test (BIST) features, including internal Pseudo Random Bit Stream (PRBS) generation and verification, and both external and internal loopback capabilities. The internal loopback feature allows at-speed testing of the complete serialization and deserialization paths with the exception of the analog receive and transmit front-ends. This enables in-system functional testing of parts after installation in customer systems. Moreover, special phase ramping logic allows loopback tests to be carried out both in synchronous and asynchronous modes, ensuring proper coverage of the clock recovery loop.

Packaging

Table 3: Supported Packages

Package	Pins	TI Suffix Code	Body Size (mm)	Lead Spacing (mm)
Thin Quad Flatpack (TQFP)	32	VF	7x 7x1.4	0.80
	48	PFB	7x 7x1.0	0.50
	52	PAH	10x10x1.0	0.65
	64	PAG	10x10x1.0	0.50
	80	PET	10x10x1.0	0.40
	80	PFC	12x12x1.0	0.50
	100	PZT	14x14x1.0	0.50
	128	PDT	14x14x1.0	0.40
	144	PGE	20x20x1.4	0.50
	176	PBL	20x20x1.4	0.40
	176	PGF	24x24x1.4	0.50
	208	PDV	28x28x1.4	0.50
	216	PDQ	24x24x1.4	0.40
	256	PEF	24x24x1.4	0.40
MicroStar Ball Grid Array (USTARBGA)	64	GGV	8x 8x0.9	0.80
	80	GGM	10x10x0.9	0.80
	100	GGM	10x10x0.9	0.80
	100	GGT	11x11x0.9	0.80
	128	GGB	12x12x0.9	0.80
	144	GGU	12x12x0.9	0.80
	151	GHZ	10x10x0.9	0.50
	176	GGW	15x15x0.9	0.80
	196	GHC	15x15x0.9	1.00
	208	GGW	15x15x0.9	0.80
	240	GGW	15x15x0.9	0.80
	257	GHK	16x16x0.9	0.80
Generic BGA (GBGA) Cavity Down	352	GKN	27x27x1.7	1.00
	352	GPD	35x35x2.0	1.27
	432	GNP	40x40x1.9	1.27
	480	GNH	35x35x1.7	1.00
	520	GNP	40.x40x1.9	1.27

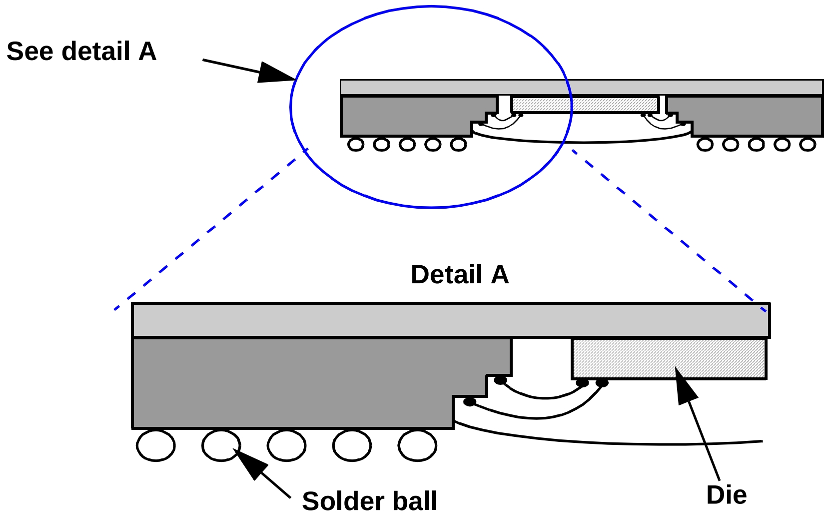
Package	Pins	TI Suffix Code	Body Size (mm)	Lead Spacing (mm)
	600	GNP	40x40x1.9	1.27
	672	GKP	40x40x1.6	1.27
	792	GKQ	40x40x1.4	1.00
	896	GKQ	40x40x1.4	1.00
Plastic Ball Grid Array	352	GFT	35x35x1.7	1.27
(PBGA)	388	GFW	35x35x1.7	1.27
PowerPAD	64	PAP	10x10x1.0	0.50
	80	PFP	12x12x1.0	0.50
	100	PZP	14x14x1.0	0.50
	208	PYP	28x28x1.4	0.50
	216	RBP	24x24x1.4	0.40
	256	PFK	28x28x1.4	0.40

Note: Body size is (length X widthX height) measured in millimeters. Body height is nominal thickness and does not include leads or balls. For overall package height, see individual package drawings.

Generic Ball Grid Array, Cavity Down

The Generic BGA has excellent thermal performance. This relatively low-cost package allows for two-tier bonding in order to achieve higher pin counts as well as four metal layers to provide package design flexibility. The figure below shows a cross-section of a GBGA, die-down package.

Figure 2: Cross-section of plastic BGA, cavity down

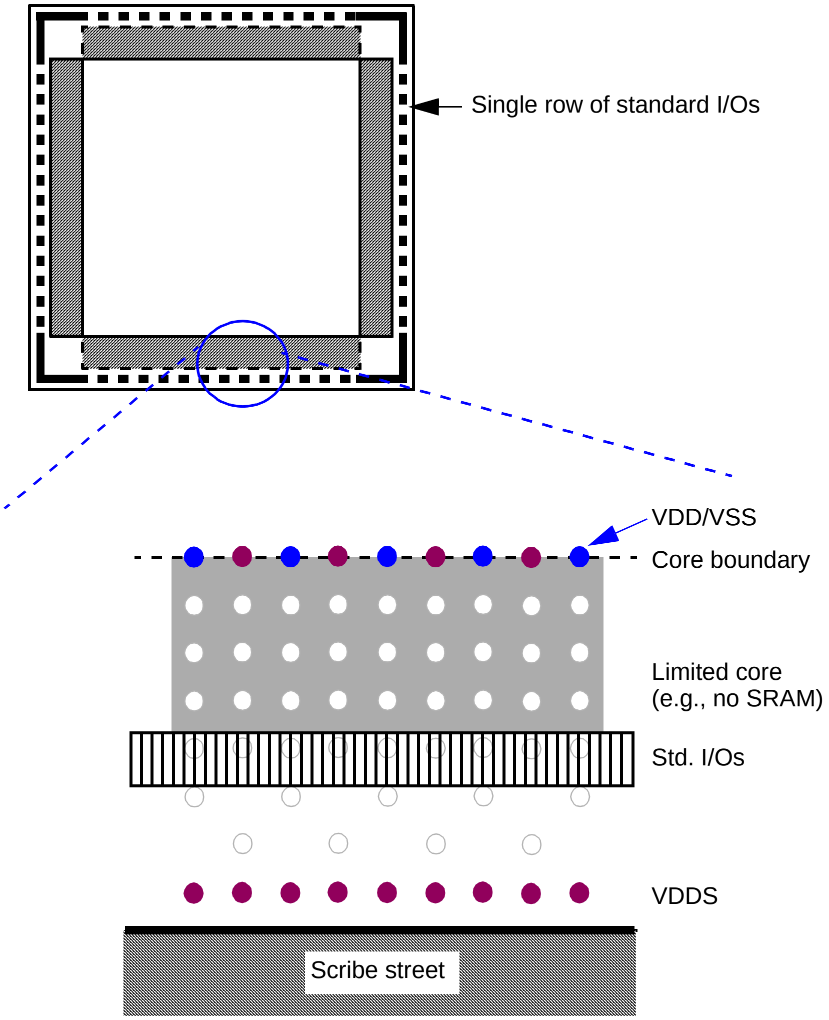


Flip-Chip Ball Grid Array

The flip-chip BGA package provides a high pin count and is highly customizable. It has the multi-channel, multi-function capability needed for communications applications requiring high-performance custom solutions.

SR40 supports both peripheral and full-array flip-chip packages.

Figure 3: Basic single-row peripheral flip-chip BGA



This design is the most basic. Signal/universal bumps are placed around the perimeter of the die/package. VDDS takes up the outermost row of bumps. The only bumps placed in the center of the die are power/ground. A single row of I/O buffers are placed around the perimeter of the die and bound the core (i.e., single-row peripheral flip chip). The innermost row of bumps handles power and ground for the core. In the middle runs a ring of I/Os. The bumps between the I/Os and the top row may be used as part of the core, though no complicated components like SRAM can be placed there.

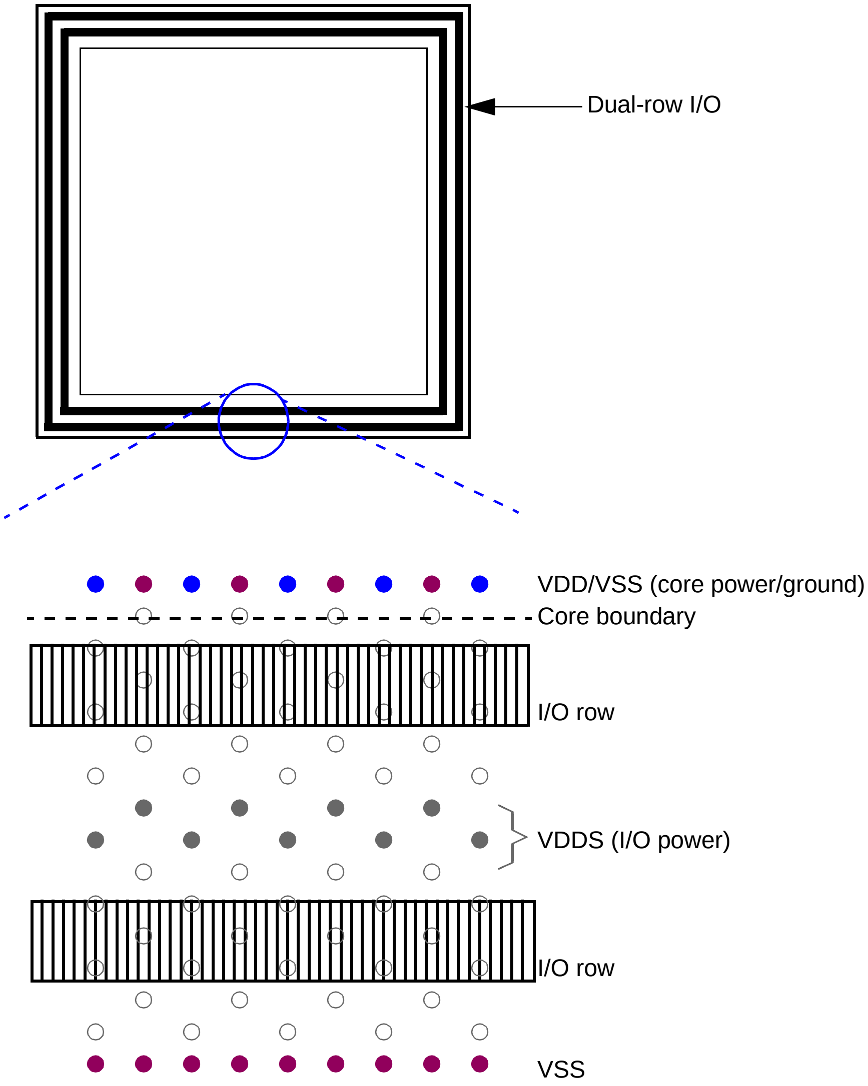
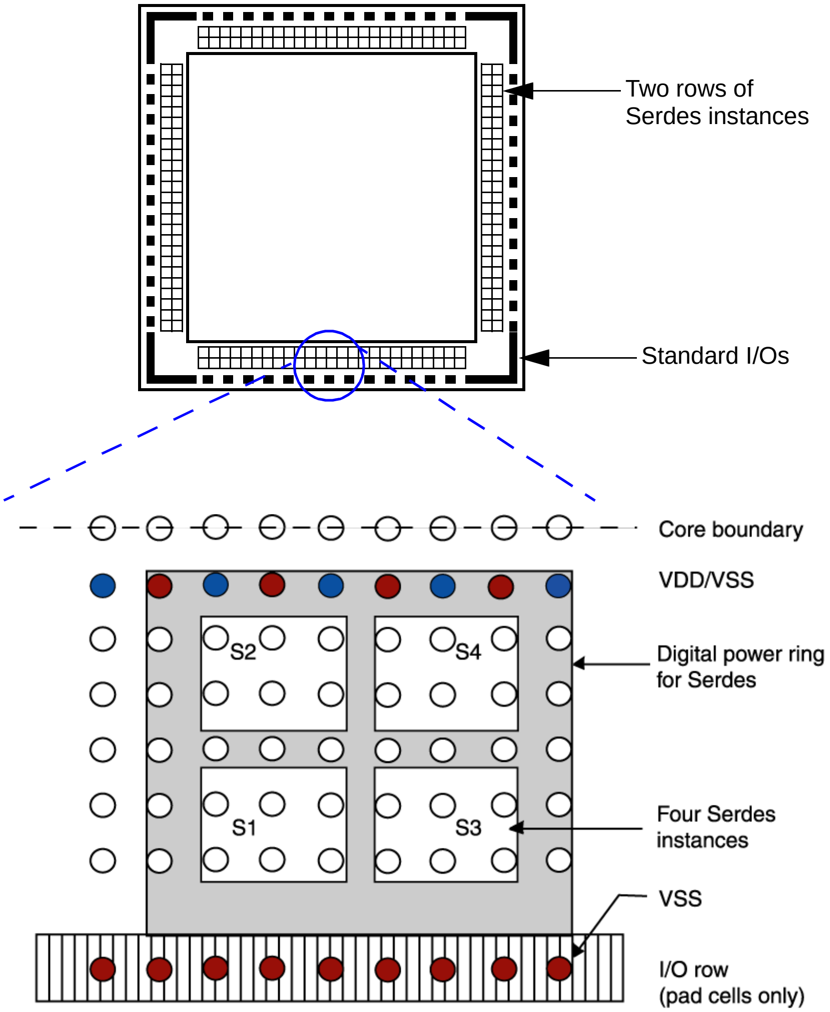


Figure 4: Basic double-row flip-chip BGA

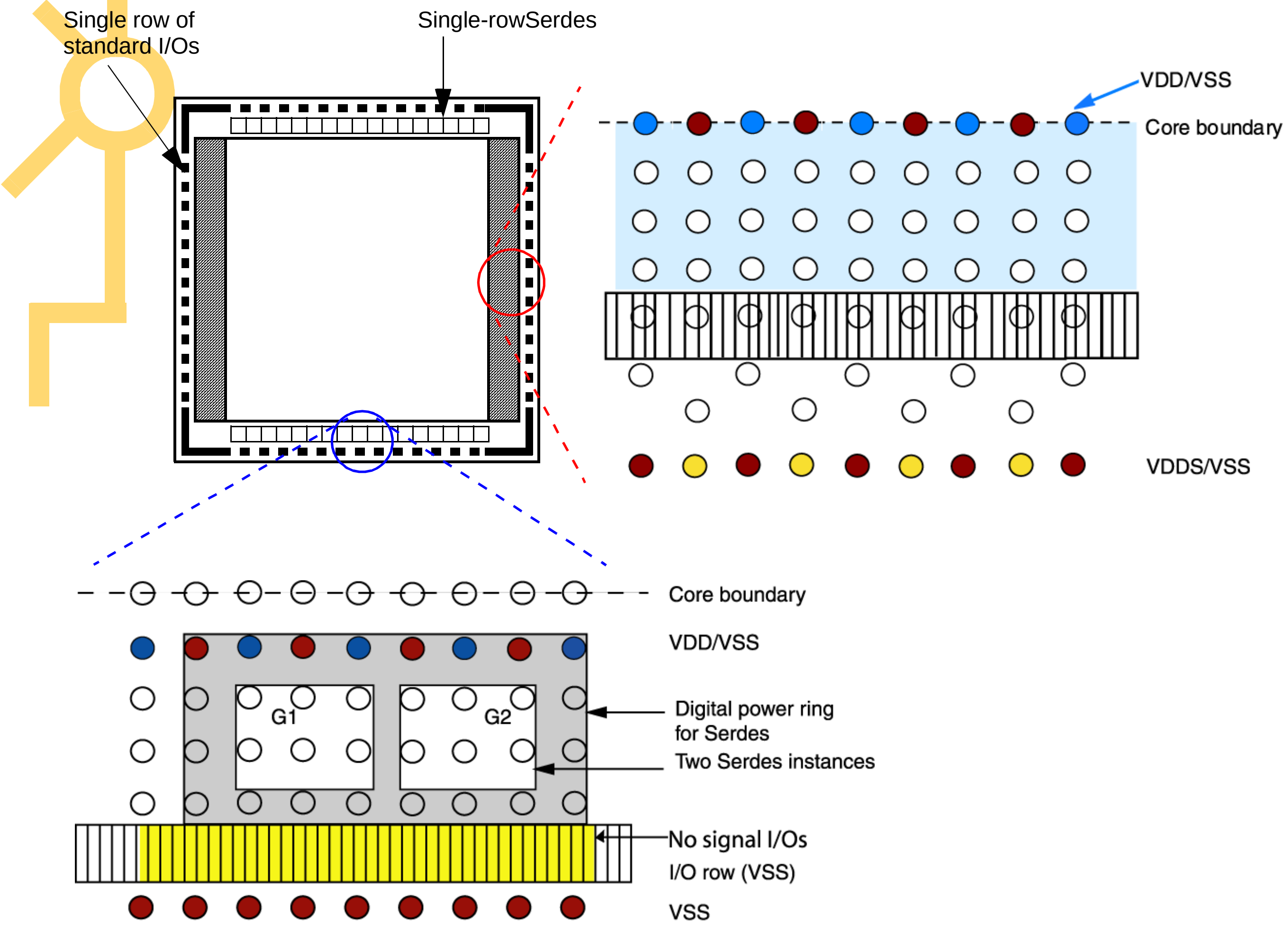
By staggering the bumps, more bumps can be placed in a given surface area. This design supports two rings of I/Os.

Figure 5: Double-row flip-chip packaging with Serdes transceivers on all sides



This design pushes most of the I/Os to the corners of the die and uses the sides for Serdes instances, placed in blocks of four. The Serdes instances require a dedicated ring of power pins, so only simple pad-cell I/Os may be placed in along the outside where Serdes cores are placed.

Figure 6: Double-row flip-chip packaging with Serdes and I/Os on at least one side



This design is a hybrid of the basic single-row design and the double-row with Serdes design, allowing for regular I/Os to be placed along one or more sides of a die that has Serdes cores on the other sides. I/Os running along the outside of a side that contains Serdes are limited to simple pad-cell only.

Clock Tree Synthesis (CTS)

Clock tree synthesis (CTS) is the primary method of clock distribution for SR40 family standard cell designs. The key capabilities of the CTS flow are:

- Consistently achieves 50 ps skew
- Insertion delay, skew, and power management
- Capability to handle more than 200 clocks
- Gated clock support for lower power
- Ability to balance multiple clocks together
- Easy to use in design flow
- Good prelayout to postlayout correlation
- Layout-centered approach for lowest skew and delay
- No customer netlist modifications
- Balancing into a SubChip
- One CTS macro
- Automatic clock buffer selection

With clock tree synthesis, the customer instantiates a single CTS buffer per clock tree. The CTS buffer is expanded at layout into a multistage clock tree. The configuration of the clock tree is optimized for size, delay, and power in accordance with the requirements of the application, and the clock tree is placed according to the location of its loads.

The postlayout timing of the clock tree is back annotated to the customer’s original netlist. The insertion delay is annotated as CTS buffer gate delay, and the clock skew is annotated to the input pin of the individual loads. Clock tree balancing and tuning are accomplished automatically by insertion of tuning buffers and loads at the root of the clock tree.

Flexible, Worldwide, Experienced Service

TI offers worldwide service and support with local Customer Design Centers (CDCs) committed to the timely success of the customer’s design. With service centers in time zones around the world, the support structure can take on the shape of a 24-hour virtual office.

The CDC partners take the design through the design process from system specification, through early evaluation, hierarchical design, layout, test and production. Flexible support includes foundry and turnkey design services.

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