Technical Article

EtherCAT Connectivity without DDR

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Other Parts Discussed in Post: AMIC110

No, I'm not talking about Dance Dance Revolution. Double data rate (DDR) is a very popular external memory interface, but the external random access memory (RAM) can take up valuable board space. TI has found a way to host the entire stack for the EtherCAT slave controller in internal memory on the Sitara™ AMIC110 processor, thus eliminating the need for an external memory. So when I say DDR-less EtherCAT, what I mean is an EtherCAT slave controller hosted entirely on internal memory.

Ethernet control automation technology (EtherCAT) is a real-time industrial Ethernet standard developed by Beckhoff Automation. It is among the most popular industrial communication protocols in the world. EtherCAT's key features are distributed clocking and a short cycle time with lower communication jitter. It is used in applications ranging from human machine interface (HMI) and programmable logic controllers (PLCs) to motor drives. End-equipment manufacturers are pushing to reduce the form factor and cost of their systems through integration, so TI has enabled a smaller, cheaper EtherCAT solution through a true DDR-less implementation on Sitara processors.

Removing DDR from the solution saves manufacturers cost in three areas. The first and most obvious is that there is no need to buy DDR memory. Second, reducing the number of printed circuit board (PCB) layers from six to four in some cases provides savings in manufacturing costs. Finally, reducing the size of the boards makes the entire enclosure smaller and thus cheaper.

In order to remove the need for DDR, TI used the internal memory size on Sitara processors and optimized the EtherCAT slave stack and its associated device drivers to fit entirely on the chip, which also greatly reduces latencies associated with external memory accesses. This solution is optimal for space and cost-sensitive applications such as remote input/output (I/O), motor drives, encoders and communication modules.

The DDR-less EtherCAT slave is now available on the AMIC110 processor. The AMIC110 device is an Arm® Cortex®-A8 processor with 300MHz performance, optimized for industrial communications. As with all other industrial communication protocols, this implementation of EtherCAT makes use of the programmable real-time unit industrial communication subsystem (PRU-ICSS). The PRU-ICSS consists of two 32-bit reduced instruction set computer (RISC) PRU cores dedicated for real-time processing, along with dedicated memories, Ethernet media access control (MAC) and other peripherals. TI will release a reference design later this quarter to help kickstart your development on DDR-less EtherCAT with the AMIC110.

Figure 1 illustrates the DDR-less EtherCAT slave solution on the AMIC110.

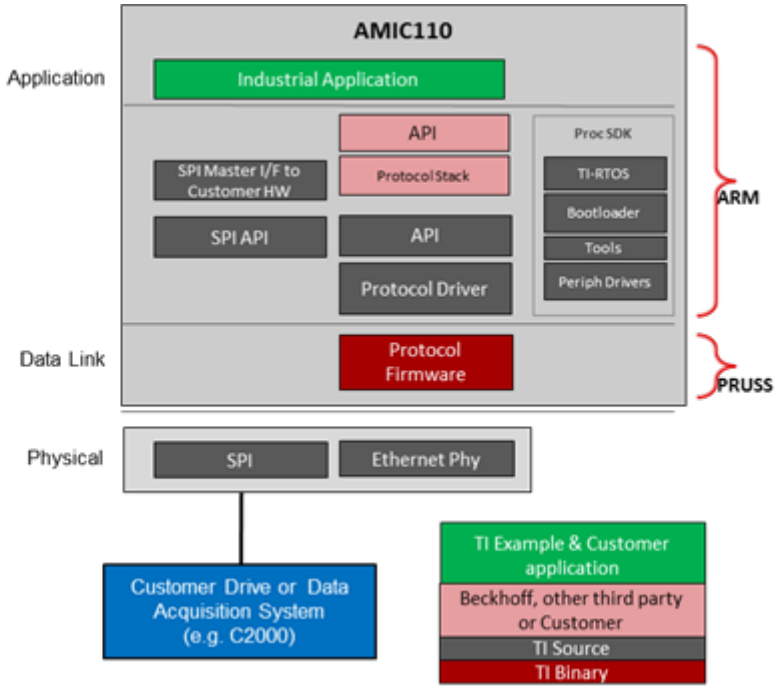

Figure 1. DDR-less EtherCAT Solution from TI

Sitara processors are designed with industrial applications in mind, with features like wide temperature support from -40°C to 105°C and 100,000 power-on hours (POH) at 105°C. These features help keep systems running for over 10 years. The Sitara portfolio is scalable from a single Cortex-A8 performing at 300MHz to dual Cortex-A15s at 1.5GHz, with integrated digital signal processors (DSPs), dual Cortex-M4s and graphics processing units (GPUs). The Processor SDK provides further scalability and flexibility by offering a single software platform for the entire Sitara portfolio so that you can easily port software developed for one processor to a different device. The Processor SDK contains many examples to help get your designs started and accelerate time to market.

Additional Resources

- If you're interested in going DDR-less for your EtherCAT slave, download the free evaluation version of the solution.
- Read the white paper, "EtherCAT on Sitara Processors."

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