Technical Article

The Effects of Gate-Driver Strength in Synchronous Buck Converters

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The peak voltage at phase node, V_{PH}, in a synchronous buck converter is one of the main specifications to determine converter reliability. Designers usually allow phase-node ringing to be as much as 85% to 90% of the MOSFET data sheet's absolute maximum rating. This margin is necessary for long-term reliability of the converter since the circuit needs to safely operate over a wide range of ambient temperature (-40^{0}C to + 85^{0}C).

From the driver side, the main factor contributing to phase-node ringing is the gate-driver strength during the turn-on process of the upper MOSFET, FET_{UPPER}. Let's analyze its effects in a converter with different gate-driver resistance values.

Figure 1 shows the top level of a synchronous buck converter with the upper MOSFET gate-driver section. The FET_{UPPER} requires a charge to turn on. This charge comes from the boot capacitor, C_{BOOT}. The charging path starts from C_{BOOT}, to R_{BOOT}, to the pull-up driver P-MOSFET (D_{UP}), the FET_{UPPER} input capacitor and back to C_{BOOT}.

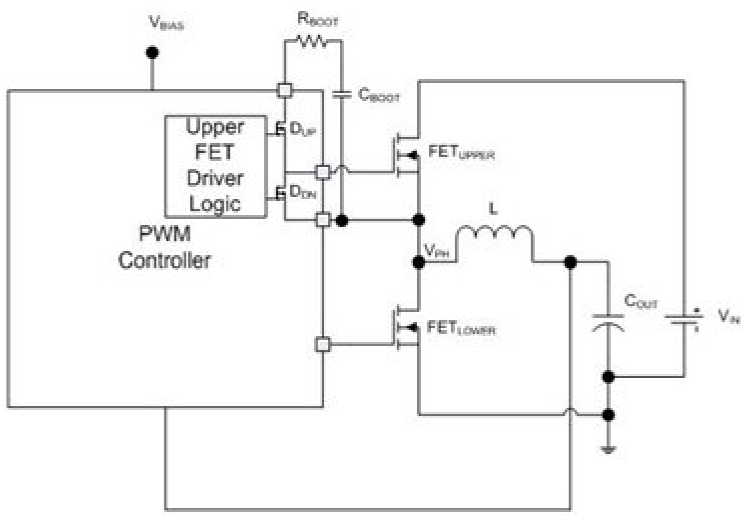

Figure 1. Top-level Synchronous Buck Converter

To simplify the comparison, treat R_{BOOT} as a short and assume MOSFET D_{UP} behavior as a linear resistance during the turn-on period of the FET_{UPPER}. A higher D_{UP} resistance value has a lower peak ringing voltage and lower converter efficiency due to higher switching power losses. A lower resistance value has both a higher peak-ringing voltage and better efficiency.

Figure 2 shows the rising edge of phase-node ringing with different gate-driver strength values. The waveforms are from the TPS543C20 evaluation board with V_{IN} =12V, V_{OUT} =1V, F_{SW} = 500 kHz, I_{LOAD} = 40A on. The peak ringing voltage of 6Ω D_{UP} is about 6V higher than 8Ω D_{UP}. The resistance value of D_{UP} inside the TPS543C20 can be program via an external communication interface such as an I^2C protocol. The waveforms are from the same device and same evaluation board to minimize variation from other components.

Now, let's compare a 6Ω D_{UP} along with different boot resistor values to an 8Ω D_{UP}. From the first order of the circuit analysis, a 6Ω D_{UP} along with a 2Ω boot resistor should have the same peak ringing voltage as the 8Ω D_{UP}. Figure 2 also compares the 6Ω D_{UP} value with 1Ω, 3Ω and 5Ω boot resistors. The peak ringing voltages of these configurations are higher than the 8Ω D_{UP} value.

You might ask why the 6Ω D_{UP} with a 2Ω boot resistor and the 8Ω D_{UP} values do not have the same peak ringing voltage results. This is because the D_{UP} behaves as a dynamic MOSFET, which requires time during the turn-on process, in comparison to pure resistance as R_{BOOT}. As a result, the rising slope of a phase node with a 6Ω D_{UP} and 6Ω D_{UP} plus boot resistors has the same ratio and is faster than the 8Ω D_{UP} slope.

Figure 2. Phase-node Ringing on the TPS543C20 Device

Figure 3 compares the efficiency of all configurations. The results clearly correlate our earlier assessment. 6Ω D_{UP} efficiency is the highest and has the highest peak voltage ringing. And, 8Ω D_{UP} efficiency is the lowest with the lowest peak voltage ringing.

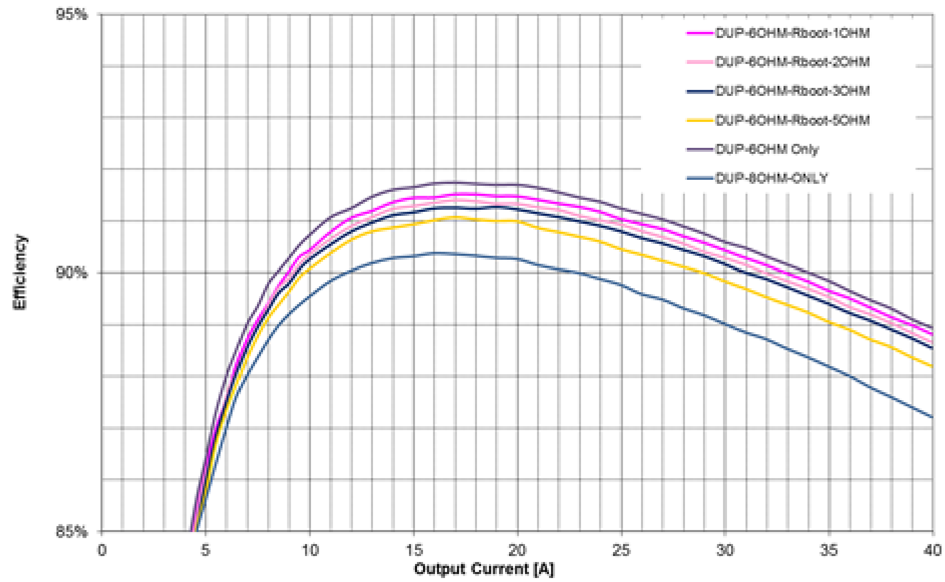

Figure 3. Efficiency Comparison with Gate-driver Strength Variation

It's critical to optimize the gate-driver strength with the main power-stage MOSFETs to ensure reliability and obtain the highest converter efficiency. A small variation in gate-driver strength can lead to wide variations in converter performance. Consider the TPS543C20 fixed frequency, non-compensation stackable synchronous buck converter for your next design.