Technical Article

Understanding Voltage References: Simple Current Sink

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Generating DC currents of arbitrary magnitude is a simple and straightforward process using operational amplifier feedback and a voltage reference. To this point, we have addressed several external opamp architectures for realizing individual or networks of current sources and sinks. In this final installment of the series, we will address an architecture which utilizes feedback from within the voltage reference itself. Let's begin by considering the voltage reference's symbol and its actual functional block diagram as displayed in Figure 1 below.

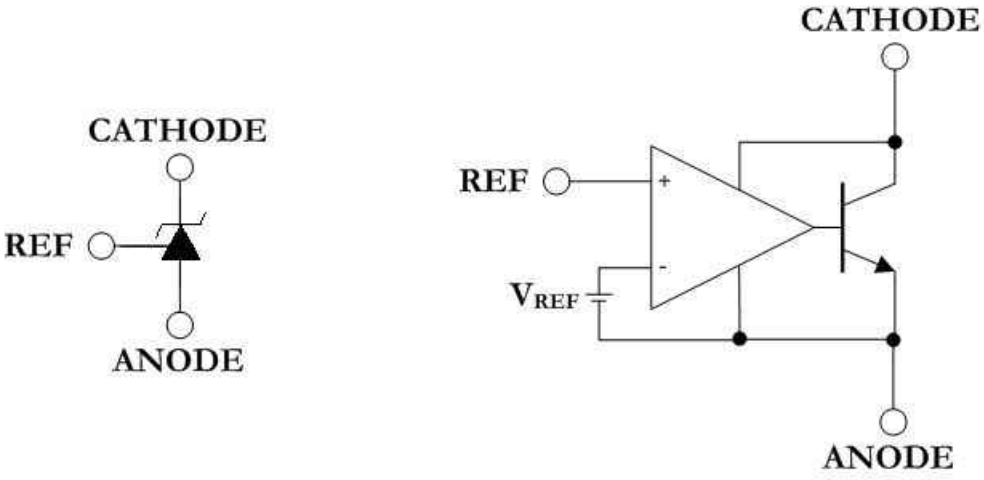

Figure 1. Voltage Reference and Its Functional Block Diagram

We have borrowed the symbol for the Zener diode because that's essentially how the voltage reference behaves; however, this behavior is achieved through clever design rather than simple device physics alone. Consider the self-referenced (cathode-reference-tied) configuration that was utilized in previous posts and shown in Figure 2 below.

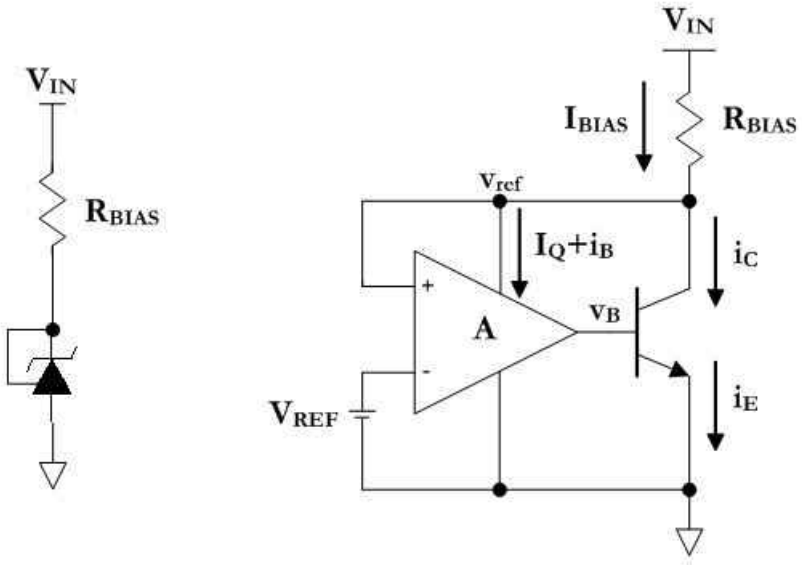

Figure 2. Voltage Reference Typical Operation

So, what can we say about this set up? First of all, we can greatly simplify and define the situation with all the currents in Figure 2 as shown in Equation 1.

$$I_{BIAS} = I_Q + i_B + i_C = I_Q + i_E \quad (1)$$

That is, I_{BIAS} is the summation of the opamp quiescent current, I_Q, and the emitter current, i_E, of the bipolar junction transistor (BJT). Equation 2 further simplifies this by acknowledging that the opamp quiescent current will be negligible compared to the emitter current during normal operation.

$$I_{BIAS} \approx i_E \quad (2)$$

Equations 3 and 4 define the emitter current beginning with the diode equation for the base-emitter junction and assuming forward bias operation with nominal ideality factor.

$$i_E = I_S \cdot \left(e^{\frac{v_{BE}}{n \cdot V_T}} - 1\right) \approx I_S \cdot e^{\frac{v_{BE}}{V_T}} \quad (3)$$

$$I_{BIAS} \approx I_S \cdot e^{\frac{v_{BE}}{V_T}} \quad (4)$$

As indicated by Equation 4 above, there must be some base-emitter voltage present to maintain I_{BIAS}. This of course implies that there is a non-zero difference between v_{ref} and V_{REF} in Figure 2; we will account for this by defining v_{ref} in Equation 5 in terms of V_{REF} and a small perturbation voltage, ε_v.

$$v_{ref} = V_{REF} + \varepsilon_v \quad (5)$$

We can now define ε_v in terms of the base-emitter voltage and opamp gain as shown in Equations 6 and 7.

$$v_{BE} = A \cdot (V_{REF} + \varepsilon_v - V_{REF}) = A \cdot \varepsilon_v \quad (6)$$

$$\varepsilon_v = \frac{v_{BE}}{A} \quad (7)$$

Clearly ε_v drops to zero in the ideal opamp case; however, let's consider some very conservative values. Equation 8 below solves Equation 7 assuming the v_{BE} required to maintain I_{BIAS} is 0.5V and the gain of the opamp is a mediocre 10^4.

$$\varepsilon_v = \frac{0.5V}{10^4} = 50\mu V \quad (8)$$

For a 1.25V voltage reference, this represents an error of some four thousandths of a percent or 40ppm—that is, such an error can be safely regarded as negligible.

Now consider what happens to ε_v when we increase the input voltage, and therefore I_{BIAS}; specifically, suppose we double I_{BIAS} from some arbitrary operating point as illustrated by Equations 9 and 10.

$$I_{BIAS1} = I_S \cdot e^{\frac{v_{BE1}}{V_T}} \quad (9)$$

$$I_{BIAS2} = I_S \cdot e^{\frac{v_{BE2}}{V_T}} = 2 \cdot I_{BIAS1} \quad (10)$$

The change in V_{BE} required to support doubling I_{BIAS} can now be derived by dividing Equation 10 by Equation 9 and simplifying terms as follows in Equations 11 through 13.

$$\frac{I_{BIAS2}}{I_{BIAS1}} = \frac{I_S \cdot e^{\frac{v_{BE2}}{V_T}}}{I_S \cdot e^{\frac{v_{BE1}}{V_T}}} = \frac{e^{\frac{v_{BE2}}{V_T}}}{e^{\frac{v_{BE1}}{V_T}}} = 2 \quad (11)$$

$$\frac{v_{BE2}}{V_T} - \frac{v_{BE1}}{V_T} = \ln(2) \quad (12)$$

$$\Delta v_{BE} = V_T \cdot \ln(2) \quad (13)$$

Finally, we can derive an equation for the change in ε_v required to support doubling I_{BIAS} as shown in Equations 14 and 15.

$$\Delta v_{BE} = A \cdot \varepsilon_{v2} - A \cdot \varepsilon_{v1} = A \cdot \Delta\varepsilon_v \quad (14)$$

$$\Delta\varepsilon_v = \frac{\Delta v_{BE}}{A} = \frac{V_T \cdot \ln(2)}{A} \quad (15)$$

Substituting in the room temperature value of the thermal voltage, V_T, and assuming (again) the mediocre opamp gain of 10^4 we can solve Equation 15 for a conservative value of $\Delta\varepsilon_v$ required for doubling I_{BIAS}, resulting in Equation 16 below.

$$\Delta\varepsilon_v = \frac{V_T \cdot \ln(2)}{A} = \frac{17.92mV}{10^4} = 1.792\mu V \qquad (16)$$

In this case, every time I_{BIAS} is doubled the voltage at v_{ref} increases by only 1.792µV. It is this multiplication of opamp gain with the exponential IV characteristic of the base-emitter diode which mimics Zener breakdown behavior.

Connecting the voltage reference differently we can leverage its internal opamp to generate a simple current sink as shown in Figure 3 below.

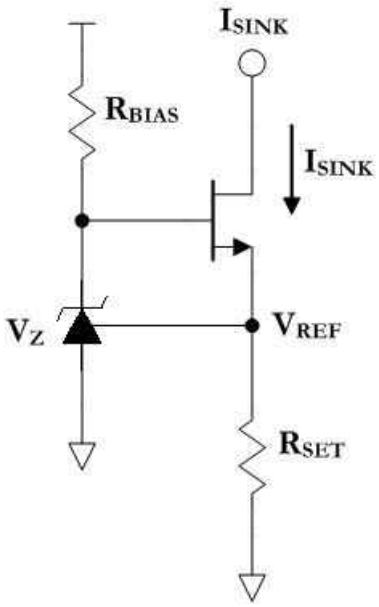

Figure 3. Simple Voltage Reference Derived Current Sink

To visualize what's going on here, consider the functional diagram inserted in place of the symbol as shown in Figure 4 below.

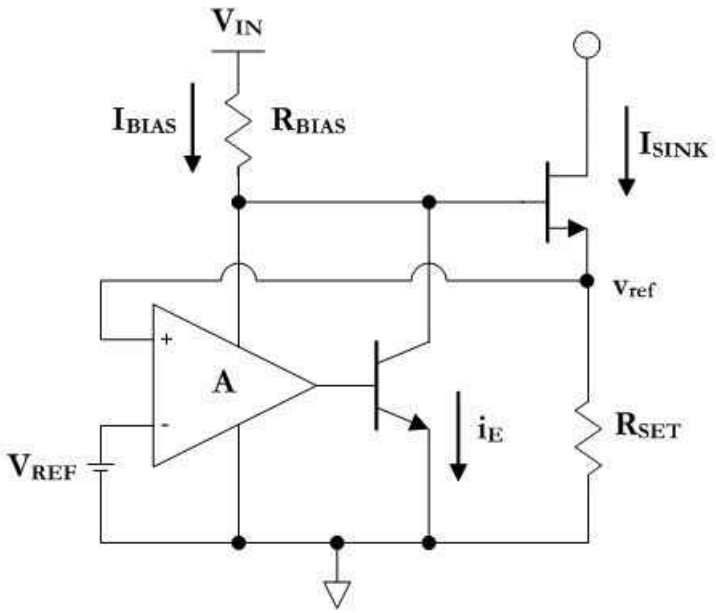

Figure 4. Simple Current Sink Functional Diagram

Notice that the V_{IN}, R_{BIAS}, and BJT circuit essentially acts as an inverting output stage for the opamp. Therefore, we can collapse the total combination into a new opamp symbol with a new gain, A_T, and reversed input polarity as shown below in Figure 5.

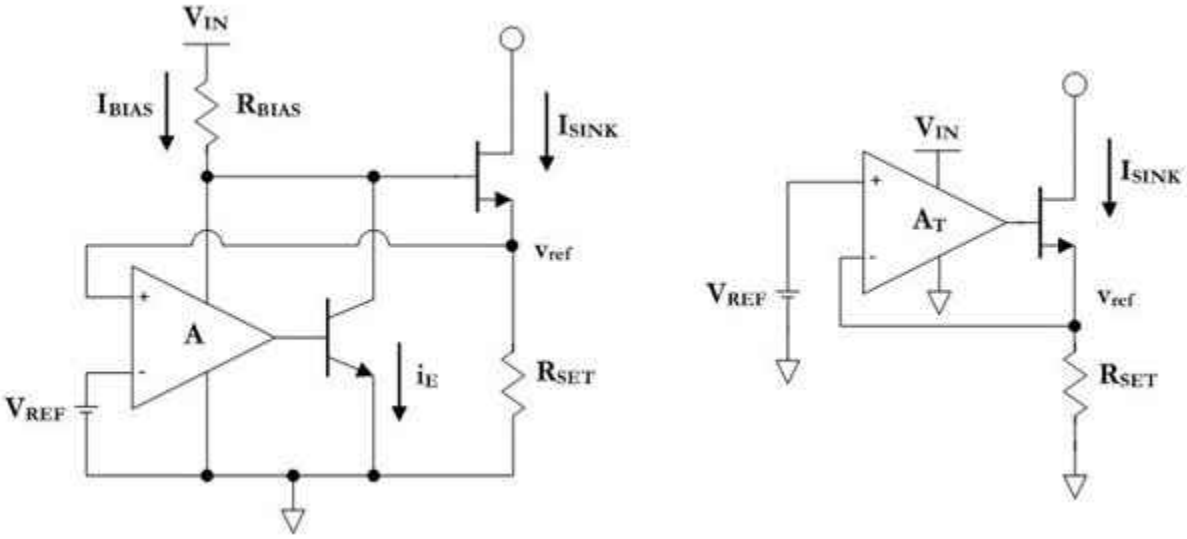

Figure 5. Simple Current Sink Functional Diagram and Equivalent Circuit

Thus, we have arrived at the same current sink circuit discussed in the first post in this series.

Throughout this series we have investigated the important topic of generating current references from voltage references. The first post covers precision, single sources and sinks of arbitrary magnitude (which can, of course, be used to implement bias networks); the second and third posts discuss a method by which bias networks might be derived with a single feedback device if a tradeoff of precision and component count is workable; and finally, this post discusses a greatly simplified method of implementing the current sink (specifically) discussed in the first post. The architectures discussed throughout this series are a handy addition to any design toolbox, and Texas Instruments has a wide variety of voltage references which can be used to realize these designs.

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