Technical Article

Waveform Audit: My Boost Converter Has an Off-ramp!

As an applications engineer, I often get inquiries about voltage and current flows in switching regulators. And I often realize that the basic theory I learned in college doesn't always tell the whole story. A recent case with the asynchronous boost converter in the TPS65150 LCD bias device is a good example of what I mean.

Let's start with the basic theory of how the switching node of a boost converter should look. Figure 1 shows the basic structure of an asynchronous boost converter.

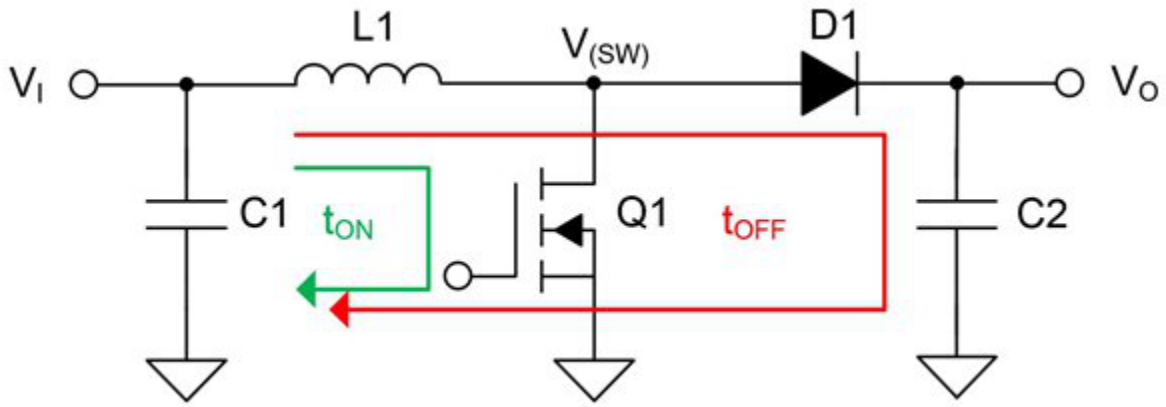

Figure 1. Simplified Boost Converter Block Diagram

When transistor Q1 turns on, the switch node pulls to ground and inductor L1 charges. The voltage on the switch node is approximately equal to 0V during the on time. During the off time, Q1 turns off, L1 discharges to the output, and the voltage on the switch node equals the output voltage (V_O) plus the forward voltage (V_F) across diode D1.

Figure 2 shows the switch-node waveform under typical operating conditions. As expected, the voltage on the switch node is rectangular and alternates between ground and V_O + V_F.

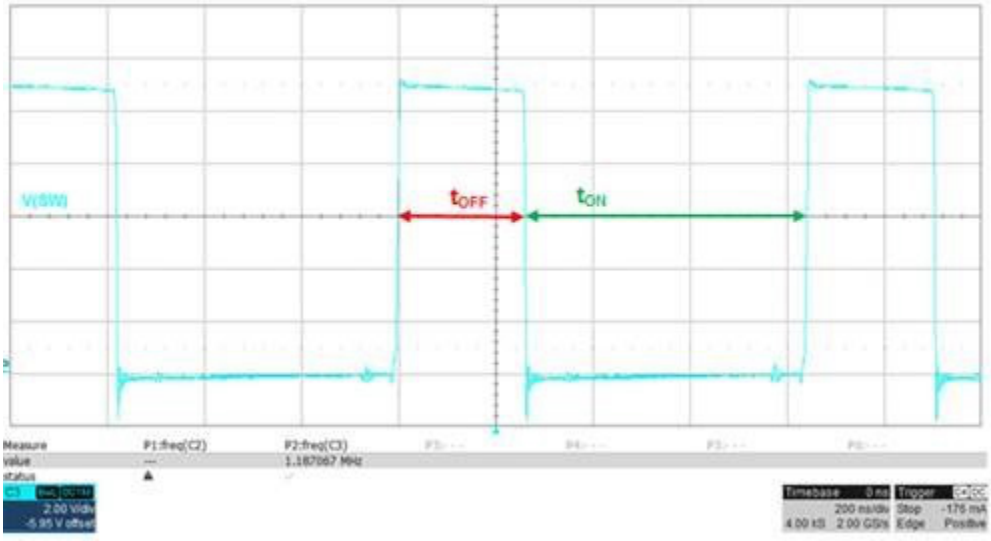

Figure 2. Switch-node Waveform

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But under low-output current conditions, the switch-node waveform shape changes and looks like Figure 3. At the start of the off time the switch-node voltage is $V_O + V_F$ (as before), but then it ramps down linearly. What's causing this behavior and what's the difference to the basic theory?

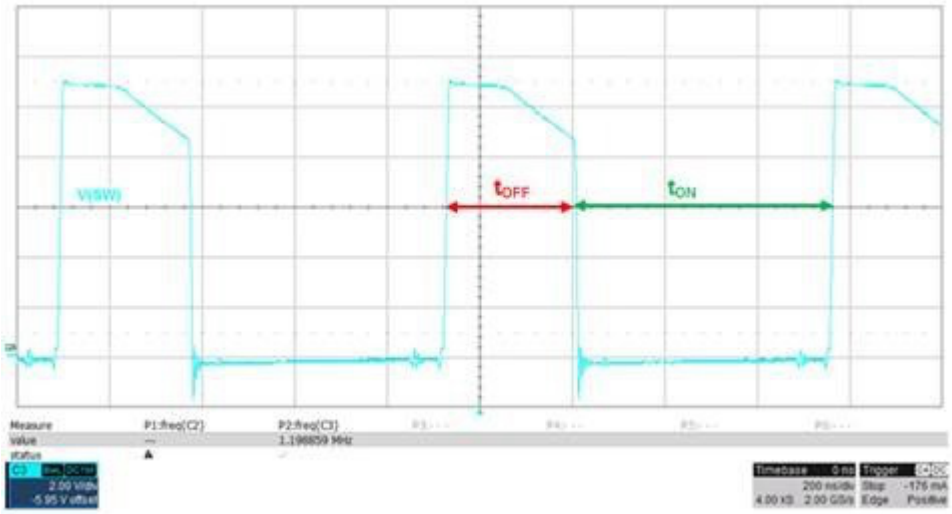

Figure 3. Switch-node Waveform at Low-output Currents

The internal block diagram shown in Figure 4 reveals the reason for the sloping waveform: an additional PMOS transistor (Q2) connected across the diode rectifier. This transistor is a synchronous rectifier that lets the converter operate in continuous conduction mode (CCM) under all operating conditions. It is on when the inductor current is negative and off at all other times. Because it is not the main rectifier, the $Rds_{(on)}$ of Q2 can be relatively high (a few ohms) without decreasing efficiency much, but the high $Rds_{(on)}$ causes a voltage drop on the switch node when the negative inductor current flows through it. And because the inductor current is linearly increasing, the voltage drop also increases, causing the slope shown in Figure 3.

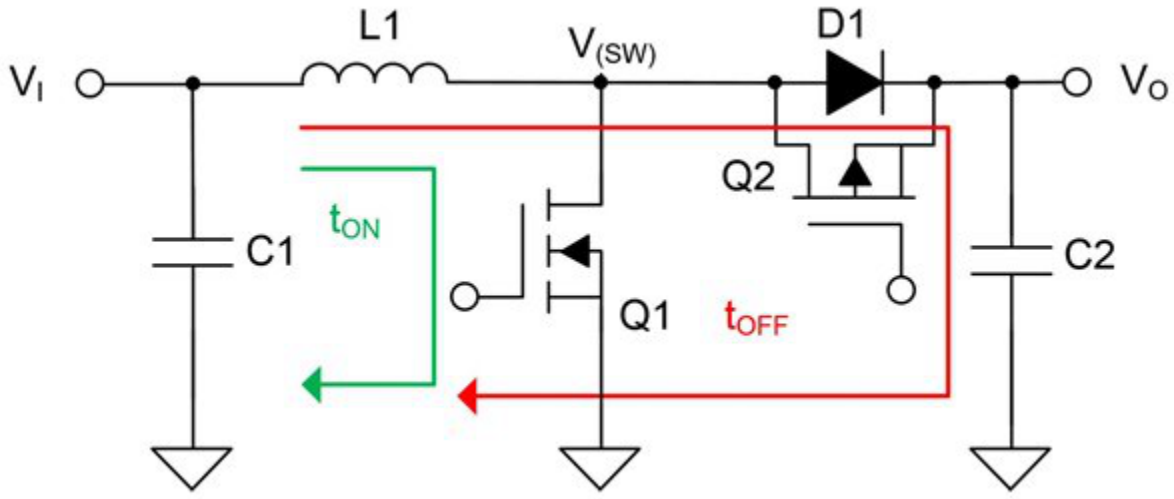

Figure 4. Internal Block Diagram Showing Synchronous Rectifier

Figure 5 shows the inductor current as well as the switch-node voltage and confirms that the ramp on the switch-node voltage starts when the inductor current goes negative, and increases as the inductor current increases.

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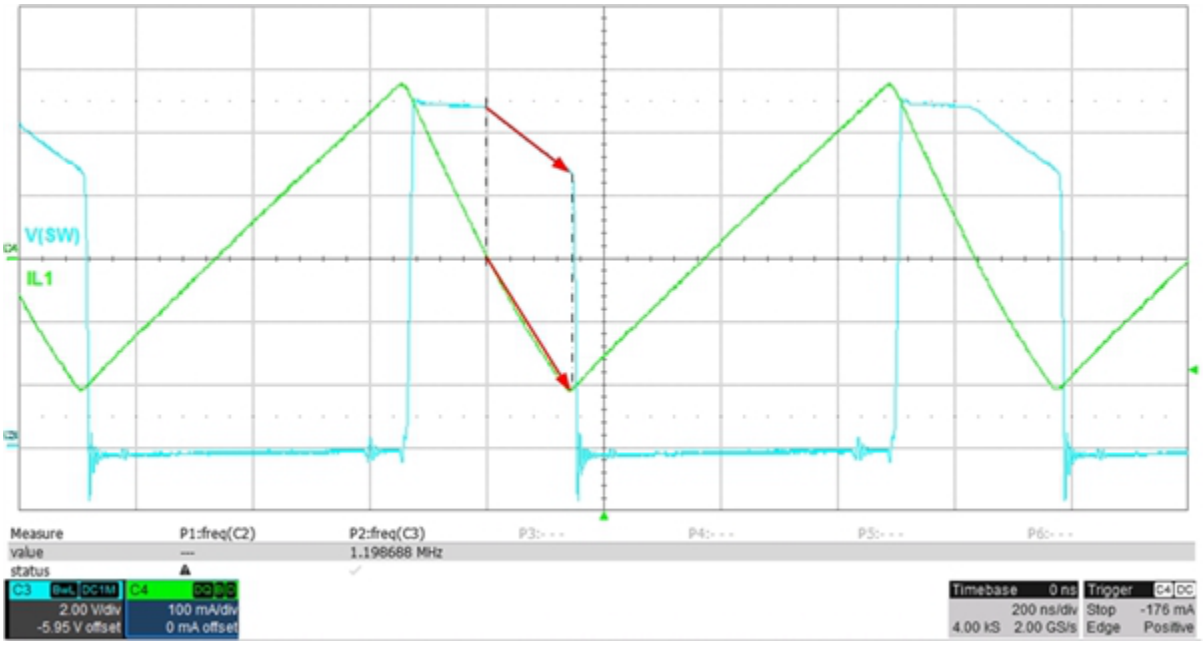

Figure 5. Switch-node Voltage and Inductor-current Waveforms

Be aware that the ramp starts for all output currents below the critical conduction point. You can calculate the critical conduction current with Equation Figure 6:

$$I_{O(crit)} = \frac{V_O(D(1-D)^2)}{2Lf_{SW}} \qquad (1)$$

Figure 6. (1)

where D is the duty cycle (boost: $D = \frac{V_O - V_I}{V_O}$), L is the inductance and is the switching frequency.

If you want get a deeper understanding of voltage and current flows in switching regulators, download the tool, "Power Stage Designer of Most Commonly Used Switch-Mode Power Supplies.

If you have experienced similar waveforms in your power-supply design of power supplies that you cannot explain – but would like to know the reason for, – just add a comment below.

Additional Resources:

- Learn more about LCD bias solutions.

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