Technical Article

RF Sampling: Interleaving Builds Faster ADCs

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There is an increasing demand in modern receiver systems for higher capacity and more data throughput. We must have high-sample-rate data converters and high-dynamic-range systems. Some analog-to-digital converter (ADC) architectures do achieve very high sampling rates but don't have the best signal-to-noise ratio (SNR). Other devices achieve very good SNR but their sampling rate is limited. Not one core ADC device simultaneously achieves the requirements for both a high sampling rate and dynamic range.

Interleaving solves the problem. Interleaving combines multiple lower-sampling-rate converters together to create one higher-sampling-rate converter. The clock source to each of the converters is delayed so that the signal is sampled at slightly different times. The samples combine into one data stream at the output.

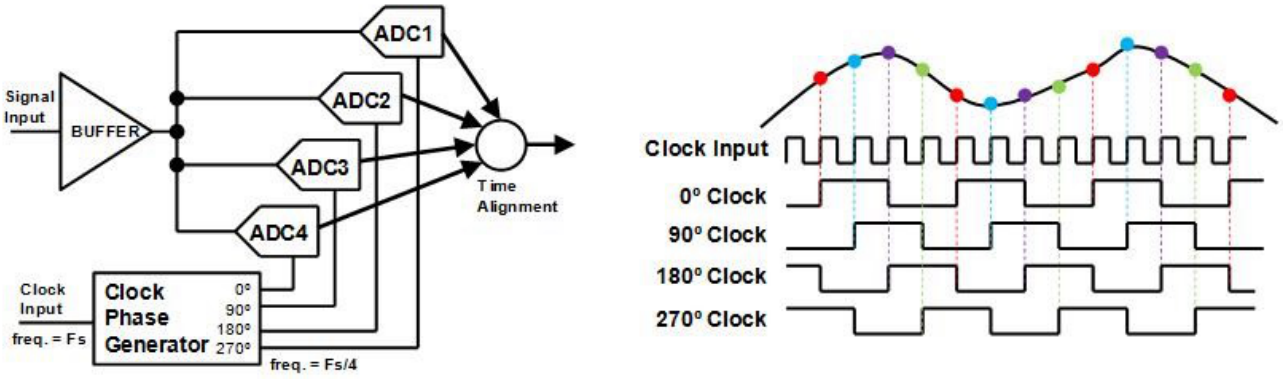

Figure 1. Four-way Interleaving Block Diagram and Timing Chart

Figure 1 shows an example four-way interleaved ADC. Each of the four converters is clocked at the same rate. The phase of the clock is shifted by 90 degrees with respect to each converter. The timing chart illustrates how the delay in the clock edges samples the analog signal at a different time. Once the data combines at the output, the data stream has four times as many samples as one converter. This looks like a converter that is sampling four times as fast. The composite SNR performance is roughly equivalent to that of the individual core.

There is a catch: using multiple converters increases power consumption. Also, because of imperfections in the analog circuits, small errors will result in interleaving spurs. These interleaving spurs impact the overall spurious-free dynamic range (SFDR).

The analog errors manifest in three primary areas, as shown in Figure 2. DC offset mismatch shifts the relative common mode between the converters, while gain and clock-phase-alignment errors result in sampling the signal at imprecise locations.

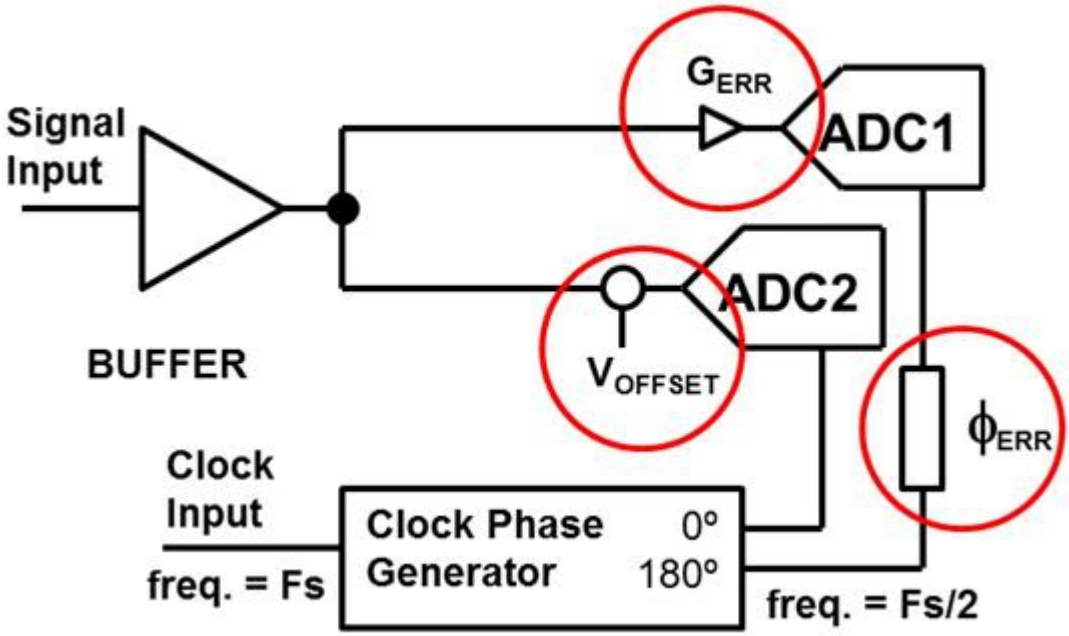

Figure 2. Sources of Error in an Interleaved ADC

These errors translate to spurious products in the captured spectrum. The offset error introduces a discrete spurious tone. The number of spurs is dependent on the number of interleaved cores (N). The discrete interleaving spur (ILS) frequency location is found relative to the sampling rate (Fs), expressed as Equation 1:

$ILS_n = Fs*n/N$ where n = 1, 2, …N-1 (1)

For a four-way interleaved ADC, interleaving spurs are located at Fs/4 and Fs/2. The signal-dependent errors of gain and clock phase yield images centered around the discrete frequency locations found above. Figure 3 illustrates the spectrum performance with interleaving spurious for a four-way interleaving device.

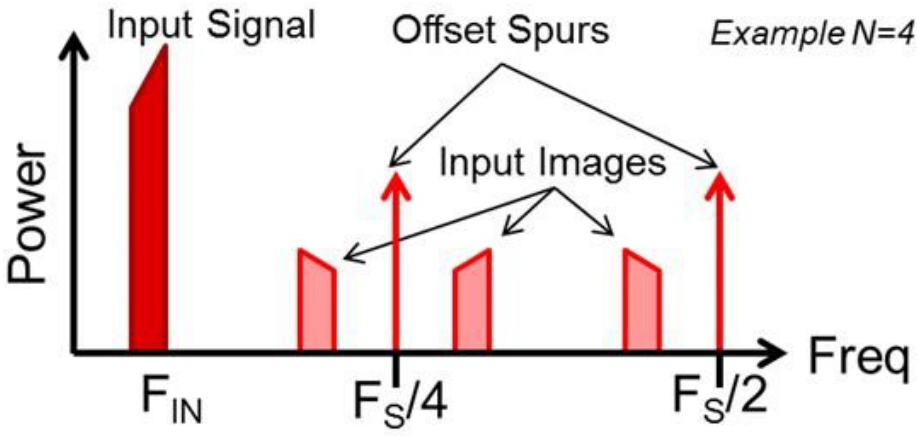

Figure 3. Interleaving Spurious for a Four-core Device

Of course, these spurious products are undesirable. ADC cores fabricated on the same die will be inherently well matched, but they will not be perfect. Calibration is required to get good SFDR performance, implemented with analog trims or with digital adjustments in the foreground or background. Foreground calibration requires that the device cease processing data while the calibration routine optimizes the performance. Background calibration continually updates the adjustment while the ADC is running so that it never goes offline.

The ADC12J4000 ADC uses four interleaved cores to achieve a 4GSPS output sampling rate. This device offers two options for interleaving correction. The foreground calibration disengages the sampling and holds the output data static while the cores are trimmed. Depending on the calibration mode and sampling rate, this process can take tens of milliseconds to complete. If going offline is not acceptable, the device has a background calibration mode where a fifth core is inserted to the mix. While one core is calibrating offline, the other four are proceeding normally. Then the freshly calibrated core seamlessly goes online while another core turns off for calibration. This process repeats, without disrupting the output.

Foreground correction can generally keep interleaving spurs better than -70 dBc at room temperature. The ADS54J60 is a dual ADC that uses four interleaved cores per channel to achieve a 1GSPS output sampling rate. This converter employs a proprietary digital interleaving correction block to adjust for the core imbalances. This correction scheme always works in the background so there is never an interruption to the output data stream. This scheme achieves better than -80 dBc correction.

Next month, I will discuss proper frequency planning to get around troublesome spurious products in radio frequency (RF) sampling data converters.

Additional Resources

- Learn more about designing with data converters in TI's Data Converter Learning Center.
- Watch and learn more about digital-mixer usage in this RF sampling: managing data rates video.
- Read other blog posts in the RF sampling series.

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