Technical Article

How to enhance power and signal integrity with low noise and low ripple design techniques

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Improving accuracy and precision, and minimizing system noise is a common challenge for engineers designing a power supply for noise-sensitive systems for medical applications, test and measurement, and wireless infrastructure that use clocks, data converters or amplifiers. Although the term “noise” can mean different things to different people, in this article I’ll define noise as low-frequency thermal noise generated by resistors and transistors in the circuit. You can identify noise through a spectral noise-density curve in microvolts per square-root hertz, and as integrated output noise in root-mean-square microvolts, typically over a specific range from 10 Hz to 100 kHz. Noise in the power supply can degrade the analog-to-digital converter’s performance and introduce clock jitter.

The traditional setup for powering a clock, data converter or amplifier is to use a DC/DC converter (or module), followed by a low-dropout regulator (LDO) such as the TPS7A94, TPS7A82, TPS7A84, TPS7A52, TPS7A53 or TPS7A54, followed by a ferrite-bead filter, as shown in Figure 1. This design approach minimizes both noise and ripple from the power supply and works well for load currents below approximately 2 A. As loads increase, however, the power loss in the LDO introduces issues in efficiency and thermal management; for example, a post-regulation LDO can add 1.5 W of power loss in a typical analog front-end application. Are those of you looking for low noise and efficiency in your design out of options? Not quite.

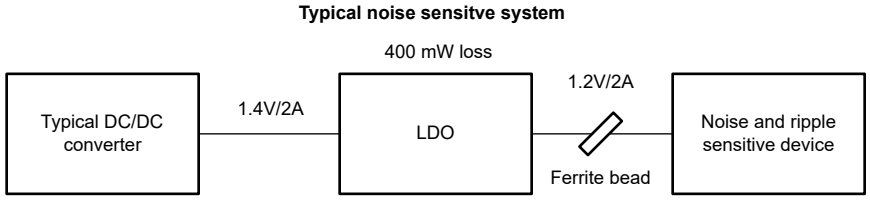

Figure 1. A typical low-noise architecture using a DC/DC converter, LDO and ferrite-bead filter

Using a low-noise buck converter or module in place of an LDO

One way to keep the power loss in check is to minimize the dropout through the LDO. However, this approach will have a negative impact on noise performance. Additionally, higher-current LDOs are typically larger, which can increase design footprints and cost. A more effective way to ensure low noise while controlling the power loss is to eliminate the LDO from the design altogether and use a low-noise DC/DC buck converter or module, as shown in Figure 2.

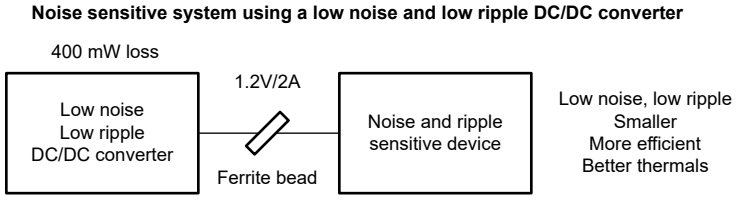

Figure 2. Using a low-noise buck converter without an LDO

I know what you're thinking: How does removing the primary device that reduces noise still provide a low-noise supply? Many LDOs have a low-pass filter on the bandgap reference to minimize the noise into the error amplifier. The TPS62912 and TPS62913 family of low-noise buck converters, as well as the TPSM82912 and TPSM82913 modules, implement a noise-reduction/soft-start pin for connecting a capacitor, forming a low-pass resistor-capacitor filter using the integrated R_f and externally connected $C_{NR/SS}$, as shown in Figure 3. This implementation essentially mimics the behavior of the bandgap low-pass filter in an LDO. If you still need lower noise than the TPS62913 or TPSM82913 can provide, you can use a low noise LDO like the TPS7A94 with a reduced dropout, lower power dissipation, and still achieve extremely low noise. This is explained in more detail in App Brief SBVA099.

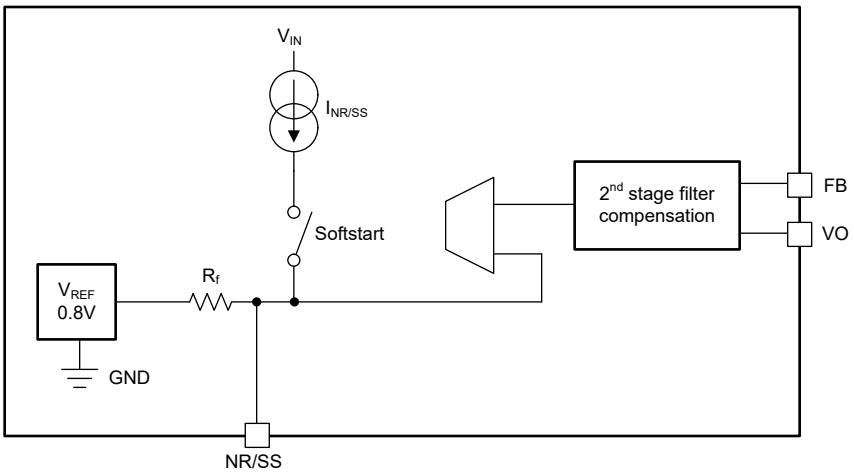

Figure 3. Low-noise buck block diagram with bandgap noise filtering

What about the output voltage ripple?

Every DC/DC converter generates an output voltage ripple at its switching frequency. Noise-sensitive analog rails in precision systems need the lowest supply voltage ripple to minimize frequency spurs in the spectrum, which typically depend on the switching frequency of the DC/DC converter, inductor value, output capacitance, equivalent series resistance and equivalent series inductance. To mitigate the ripple from these components, engineers often use an LDO and/or a small ferrite bead and capacitors to create a pi filter to minimize ripple at the load. A low-ripple buck converter such as the TPS62912 and TPS62913, as well as the TPSM82913 module, leverage this ferrite-bead filter by integrating ferrite-bead compensation and remote-sense feedback. Using the inductance of the ferrite bead in combination with an additional output capacitor removes the high-frequency components in the output voltage ripple and reduces the ripple by approximately 30 dB, as shown in Figure 4.

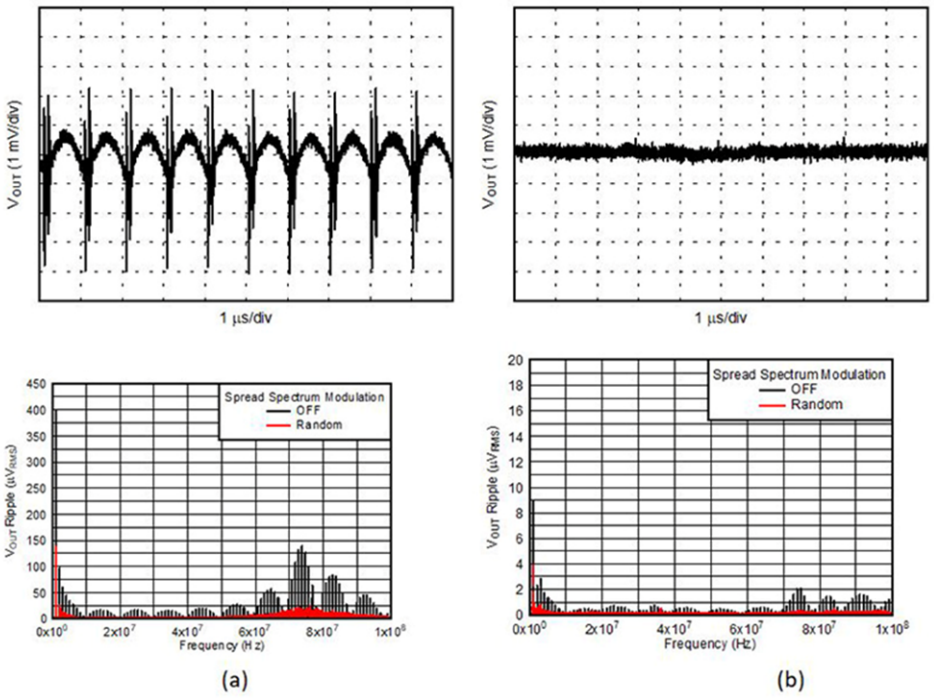

Figure 4. Output voltage ripple before the ferrite-bead filter (a); and after the ferrite-bead filter (b)

Conclusion

By integrating features that mitigate system noise and ripple, low-noise buck converters can help engineers achieve a low-noise power-supply solution without the need for an LDO. Of course, the noise levels required by different applications will vary, as will the performance for different output voltages, so only you can determine the best low-noise architecture for your design. But if you're looking to simplify the design of noise-sensitive analog power supplies, reduce power losses, and shrink the overall design footprint, consider using a low-noise buck converter.

Additional resources

- "Powering Sensitive ADC Designs with the TPS62913 Low-Ripple and Low-Noise Buck Converter."
- "Powering the AFE7920 with the TPS62913 Low-Ripple and Low-Noise Buck Converter."
- For details about the output voltage ripple contribution when using a DC/DC converter, read the technical article, "Understanding and managing buck regulator output ripple."
- To learn more about lowering noise and ripple with the TPS62913 and the TPS62913, watch the video training: " Low ripple & Low Iq DC/DC point-of-load buck converters."
- To see other ways of reducing output voltage ripple from a buck converter, read the whitepaper Low-noise and low-ripple techniques for a high-efficiency, low-loss supply without an LDO.

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