# Maximizing power for Level 3 EV charging stations

**Sang Chon,**
*C2000™ MCU Automotive Marketing Manager*
*Texas Instruments*

**Manish Bhardwaj,**
*C2000 MCU Digital Power Applications Engineer*
*Texas Instruments*

**Hrishi Nene,**
*C2000 MCU Digital Power Applications Engineer*
*Texas Instruments*

**With increasing battery capacity and decreasing battery cost, electric vehicles (EVs) are becoming more commonplace. Just as traditional internal combustion engine (ICE) automobiles spawned the need for more gas stations, EVs will also drive the demand for more public charging options.**

To maximize the deployment of as many charging stations as possible, the technology that goes into a charging station must be efficient and cost-effective, and provide an overall positive customer experience. Another challenge involves deploying a charging infrastructure that not only supports today's use cases of mostly short local trips, but also supports faster charging compared to home-based chargers to ease concerns about charge times when users have a need to go on longer trips.

## EV charger types

You'll find charging stations installed in a number of settings: at residential homes, public parking lots adjacent to a restaurant or office building, or commercial outlets like a convenience store. Currently, the Society of Automotive Engineers (SAE) defines three different levels of charging stations, also known as electric vehicle supply equipment (EVSE):

- Level 1 EVSE uses a standard AC line current in the U.S., or single-phase 120V at 12 to 16A elsewhere. AC-to-DC power conversion takes place in the vehicle. These relatively inexpensive stations will recharge a completely discharged EV battery with a capacity of 24kWh in approximately 17 hours.
- Level 2 EVSE are based on a similar technology as Level 1, but can accept a more powerful 208V-240V polyphase AC input line at 15A-80A. This reduces the charge time for a completely drained battery to 7 hours.
- Level 3 EVSE differs from Level 1 and 2 in that AC-to-DC power conversion takes place in the charging station, so it's possible to supply a high-voltage DC line to the battery to shorten the charging time. As a result, the cost and complexity of a Level 3 station is significantly greater. They can supply anywhere from 300V up to ~920V at a maximum of ~500A. The approximate charging time will be around 10- to 30 minutes dependent on energy level in the battery. Unlike Levels 1 and 2, which are more typical of residential installations where EVs recharge overnight, the more expensive Level 3 DC fast charging stations are usually found in public, shared settings and eventually likely even into gas stations.

## Power stage

Efficiency in converting the AC power of the grid into the DC power that charges an EV battery is one of the most critical aspects of a charging station. Consequently, it's important to select the most

| EVSE Type | Power Supply | Charger Power | Charging time Battery EV (BEV) |
|---|---|---|---|
| Level 1 (AC Charging) | 120VAC 12 A to 16 A (Single Phase) | ~1.44 kW to ~1.92 kW | ~17 Hours |
| Level 2 (AXC Charging) | 208 ~ 240 VAC 15 A ~ 80 A (Single/Split Phase) | ~3.1 kW to ~19.2 kW | ~7 Hours (3.3 kW on-board charger) ~3.5 Hours (6.6 kW on-board charger) |
| Level 3 (Combo Charging System or DC Charging | 200 to 920 VDC (Max 500 A) (Poly Phase) | From 120 kW up to 350 kW | ~10 to 30 Minutes |

***Table 1**. Classification of EV chargers.*

effective conversion topology for a charging station's typical use case. The power module in a DC fast charger typically comprises of an AC-to-DC rectifier converter and an isolated DC/DC converter, both of which we'll discuss below.

To support the high power levels of fast chargers, the AC-to-DC rectifier is a three phase AC input power factor correction (PFC) stage. Popular topologies for implementing three phase PFC are either a three phase totem pole PFC converter or a Vienna rectifier based PFC converter. Amongst these two topologies, Vienna rectifier based converters are gaining more popularity due to its three level switching implementation, higher efficiency, reduced voltage stresses on components, and higher power density.

Similarly for the isolated DC-DC converters, there are a number of options to consider. Resonant converters such as LLC are popular because of their ability to achieve Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS). Additionally,there are multiple variants of LLC converters such as half bridge LLC and full bridge LLC topologies. For high power and high voltage applications, a full bridge LLC is typically used because of its better utilization of the magnetic core and reduction in current stress/rating of the components. An interleaved LLC approach can also be applied to reduce the filtering requirements for higher power at the output of the converter.

To optimize the LLC operation for a wide range of battery voltages, a variable-link PFC voltage is desired. However the challenge is when a variable voltage is present at the output of the PFC, the stress on the power devices will increase. The advantage of the Vienna rectifier for PFC here is that it is a three-level topology and therefore the stress increase is proportionately less on the power switches. Therefore, high-end and high-power Level 3 DC fast charging systems often use the combination of a Vienna rectifier and interleaved (IL) full-bridge resonant converter (LLC). The reason for this topology combination is because it's important to consider how quickly power can be drawn from the grid and transferred into the battery, which typically requires a three-phase approach to power conversion. Below is a diagram of such a charger (**Figure 1**).

## Vienna rectifier (for Level 3 charging)

As discussed in the previous section, in many cases the topology for Level 3 EVSE is a three-phase Vienna rectifier. This type of rectifier is a unidirectional, three-phase pulse-width modulation (PWM) rectifier. When compared to a boost-type PWM rectifier, the Vienna topology uses multilevel switching (three levels), which reduces the inductance value requirement and reduces the voltage stress on the switches by half. This improves efficiency and power density.

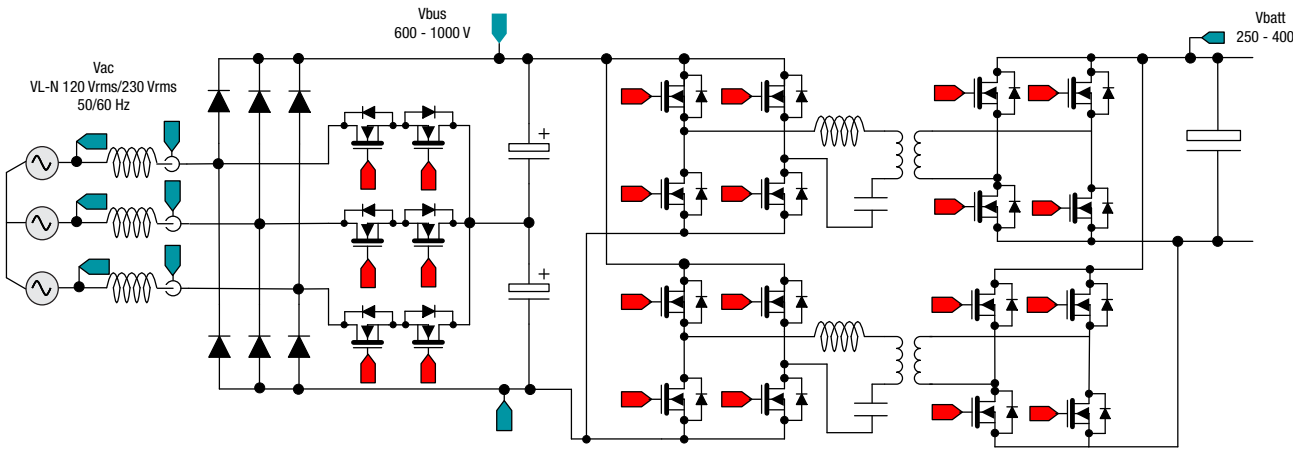


***Figure 1**. Commonly used topologies for EV charging stations (three-phase Vienna rectifier plus full-bridge LLC)*

This converter has been shown to be capable of achieving 99% or more in efficiency.

Traditionally, Vienna rectifiers have used hysteresis-based controllers which are more complex to design. Only recently has sine triangle-based PWM been shown to work for Vienna rectifier control. Furthermore, with the development of an average current control model the adoption of the rectifier in industrial and automotive applications has accelerated. Still, this type of control can be quite challenging to design because of the need to execute multiple loops, fine tuning and switching at higher frequencies.

There are several types of Vienna rectifiers, but the most popular for Level 3 charging stations is the Y-connection variant shown in **Figure 2**.

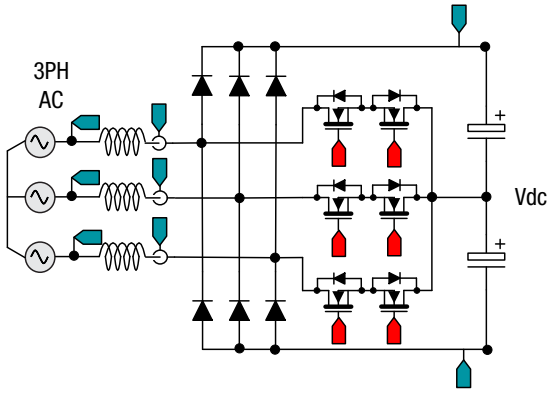


***Figure 2**. Vienna rectifier (Y-connection) topology for EV charging stations.*

## C2000™ real-time MCUs for Vienna rectifiers

C2000 real-time MCUs are controllers designed specifically for power electronics applications. The TMS320F28004x is a good fit for Vienna rectifier topologies shown in **Figure 3** below, with built-in device features and software libraries that make development of a Vienna rectifier topology smaller, lower cost and easier. For example:

- Actuating the signals for the control of the power devices on the Vienna rectifier can be challenging, especially when due to size constraints the switching frequencies are > 100kHz. The flexibility in the PWM module on the C2000 MCU allow designers to generate these signals easily.
- Sensing the signals is an important aspect for good control and the fast and precise Analog to Digital converter on the C2000 MCU enables highly accurate sampling and measurement resulting in better THDi which is a key specification for PFC converters to meet.
- Protection is another aspect in the design of the converter. The integrated comparator subsystem (CMPSS) integrates protection for overcurrent and overvoltage without the use of any external

circuitry, thus making the board smaller and lower in cost. The flexible X-Bar architecture enables combining trip events from multiple sources such as CMPSS and GPIOs that signal gate driver faults in a quick and easy manner again without the need of external logic or circuitry.

- An optimized central processing unit (CPU) enables fast execution of the control loop. The on-chip trigonometric math unit (TMU) accelerates trigonometric operations, which imparts additional speed in control-loop execution and reduces the overall MIPS requirement.

- The Control Law Accelerator (CLA) is a secondary core that is available to offload control type tasks from the main CPU (C28x) thus freeing up bandwidth on the C28x MCU for other operations and tasks. Additionally, the CLA can be used as a parallel processing unit to run the control loop faster, therefore enabling higher switching frequency control of the Vienna rectifier.

- As AC signals are sensed for the voltage and current, the first step in using these values for control is removal of the DC-offset. Even for non-AC signals removal of DC-offset can be an important first step to meet system voltage regulation requirements. The ADC Post Processing Block (PPB) enables automatic removal of the offset from the sensed signal in hardware. This allows the control loop to directly read a signed register value, therefore saving on cycles used to load offsets and subtract offsets from the critical path in the Interrupt Service Routine (ISR).

- Tuning of control loops is another challenge that a system designer must face and can be a time consuming task. TI has developed a tool called the software frequency response analyzer (SFRA) and the compensation designer tool to ease the tuning of control loops and accelerate the design process.

## Analog integration

Most power electronic converters need protection from an overcurrent event. A typical way to implement this for a single channel is shown in **Figure 4**. As the Vienna rectifier is a three phase power topology, it requires multiple comparators, and references. For example, just to implement current protection, 2 op-amps, 6 comparators, and additional resistors and capacitors may be needed to implement a simple over current trip for all three phases.

C2000 MCUs such as the TMS320F280049 can avoid all of this extra circuitry. This MCU has on-chip windowed comparators as part of the CMPSS

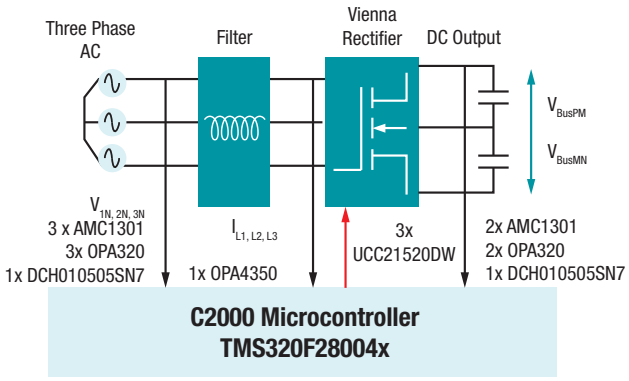


***Figure 3**. Vienna rectifier block diagram controlled by the C2000 TMS320F28004x real-time MCU.*

that are internally connected to the PWM module and can enable fast tripping of the PWM. The TMS320F280049 saves board space and is cost-efficient in the end application because you can use these on-chip resources and avoid adding extra components; see **Figure 6**.

When developing a Vienna rectifier design, it can take up to five CMPSSs on the TMS320F280049 MCU: three for current sensing each of the three phases and two for sensing on the DC bus.

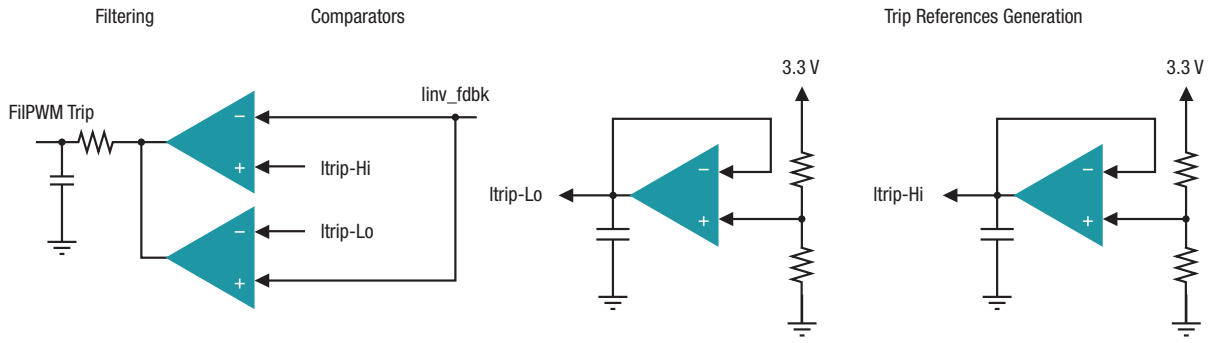


***Figure 4**. Trip generation for PWM using comparators and reference generators*

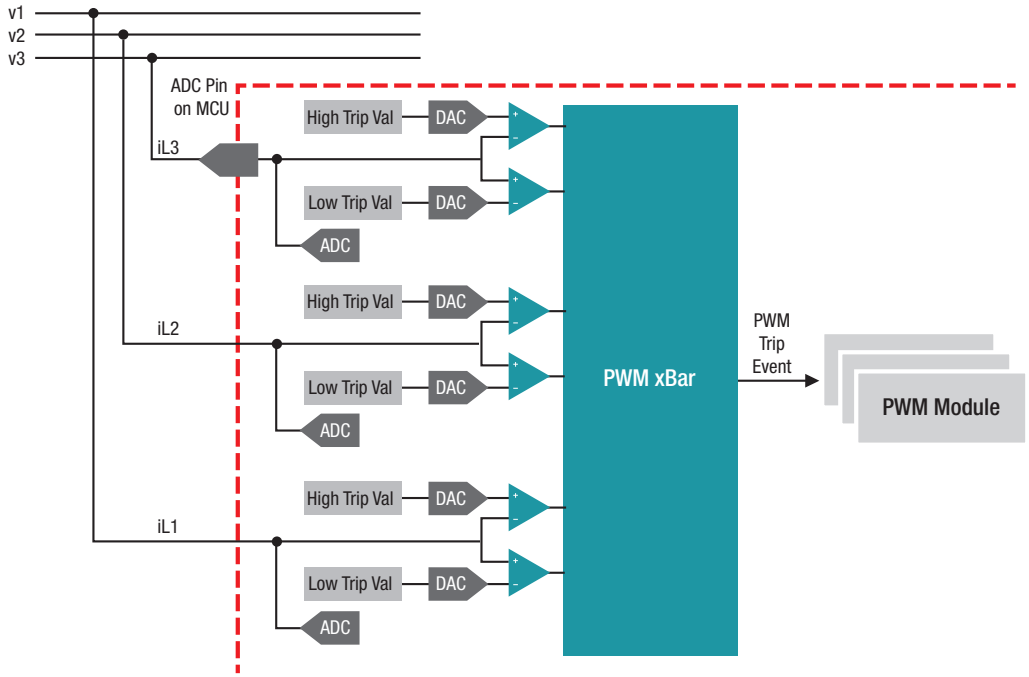


***Figure 5.** Over current protection scheme on Vienna rectifier*

## Accelerating control-loop execution

The F280049 TMU is an enhanced instruction set of the C28x™ digital signal processor (DSP) core that helps efficiently execute trigonometric and arithmetic operations commonly used in control system applications. Similar to a floating-point instruction set, the TMU is an Institute of Electrical and Electronics Engineers (IEEE)-754 floating-point math accelerator tightly

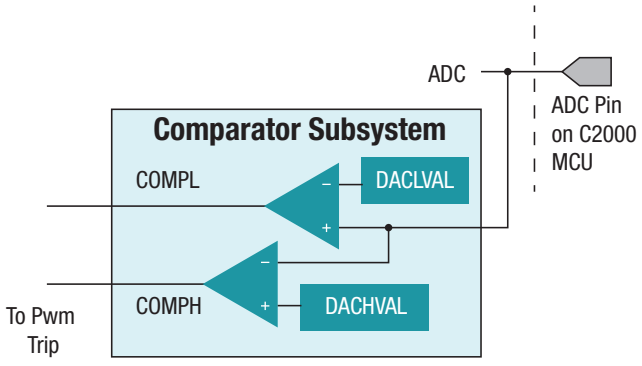


***Figure 6.** The CMPSS used for overcurrent protection.*

coupled with the CPU. However, where the floating-point unit provides general-purpose floating-point

math support, the TMU focuses on accelerating several specific trigonometric math operations that would otherwise be quite cycle-intensive. These operations include sine, cosine, arctangent, divide and square root, as shown in **Figure 7**.

Multiple control schemes are possible for the Vienna rectifier. In many of these schemes a rotating reference frame type of control structure is used. These schemes use transforms such as ABC to DQ0, and rely heavily on computation of "sine" and "cosine" values. With the faster switching frequencies in Vienna rectifiers, it's even more important to compute these routines quickly. For example, compared to MCUs that only have a floating-point unit, the sine instruction with the TMU instruction set can execute a "sine" instruction in 4 pipelined cycles, compared to up to 41 cycles. That is a ~10x performance improvement for such operations thus making TMU a significant impact on Vienna rectifier control algorithms. Furthermore, the ADC PPB block can save cycles by incorporating offset subtraction in hardware. For example on the Vienna rectifier, a minimum of 8 signals are needed to be sensed with offsets subtracted (3 voltages for ac input, 3 currents for ac input and 2 output bus voltages). Operations to read a single signal requires reading the ADC, reading the offset, subtracting the offset, scaling the result and storing in memory. This can take up-to 12 cycles even with optimized assembly code. With the PPB it can be reduced to 8 cycles, which imparts a 33% improvement in execution of these operations.

The CPU load for computing a Vienna rectifier control loop can also be extensive involving reading of 8 signals (in addition oversampling may require even more CPU bandwidth), execution of 4 controllers, and updating the PWM. For example, even with the TMU and the ADC PPB for a 50kHz control loop on a 100MHz device: the CPU load (C28x) is ~47%, out of which ~37% is for the main control ISR (50kHz) and ~8.5% is for the instrumentation ISR (10kHz).

The CLA can enable offloading of these ISRs from the C28x core. The CLA (type1) on the TMS320F2837x series can offload the faster ISR and CLA (type 2) on the F28004x can offload both the ISRs thus reducing the C28x CPU utilization to zero.

The CLA can enable control loops for Vienna rectifiers of up to 200kHz using parallel processing on 100MHz devices such as F280049. With a >200MHz device such as the TMS320F2837x series, up to 400kHz control loop frequencies are feasible with control algorithm code still in C. And furthermore, with assembly code, even higher control loop frequencies can be achieved with C2000 real-time MCUs.

| Operation | C Equivalent Operation |
|---|---|
| Multiply by 2*pi | a = b * 2pi |
| Divide by 2*pi | a = b / 2pi |
| Divide | a = b / c |
| Square root | a = sqrt(b) |
| Sin per unit | a sin(b*2pi) |
| Cos per unit | a = cos(b*2pi) |
| Arc tangent per unit | a = atan(b)/2pi |
| Art tangent 2 and quadrant operation | Operation to assist in calculating ATANPU2 |

***Figure 7**. TMU-supported instructions summary.*

## Ease tuning of control loops

The software frequency response analyzer (SFRA) is one of three tools included in the powerSUITE digital power-supply design software tools for

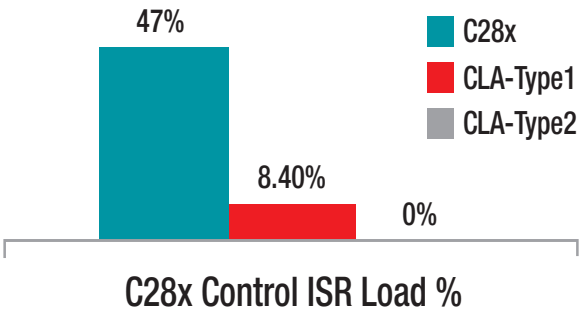


***Figure 8**. C28x CPU load for Vienna Control Algorithm, without CLA, with CLA-1, with CLA-2*

C2000 MCUs. The SFRA includes a software library that enables you to quickly measure the frequency response of your digital power converter's voltage and current control loops. The SFRA library contains software functions that inject a frequency into the control loop and measure the response of the system using the C2000 MCU's on-chip analog-to-digital converter (ADC). This process provides frequency-response characteristics and the open-loop-gain frequency response of the Vienna rectifier's closed-loop system.

You can then view the open-loop-gain frequency response on a PC-based graphical user interface (GUI). All of the frequency response data is exported into a comma-separated values (CSV) file, or optionally an Excel spreadsheet, which you can then use to design the compensation loop using Compensation Designer. The benefit here is that you don't need to use a hardware response analyzer that requires extra time to set up and take measurements. You can tune the Vienna rectifier completely via software. Below, **Figure 9** shows the graphical interface for the Software Frequency Response Analyzer GUI where you can measure the bandwidth, gain margin and phase margin from a frequency sweep.

## Two-phase interleaved resonant LLC (for Level 3 charging)

In many cases, the topology for the isolated DC/DC for Level 3 EVSE is a two-phase interleaved full-bridge resonant LLC. The full-bridge LLC's high performance (efficiency, power density, etc.) meets the requirements of various combined charging system (CCS) power classes ranging from 300V to 1000V, making these converters a good choice for high-power applications. Below is a diagram of full bridge LLC stage.

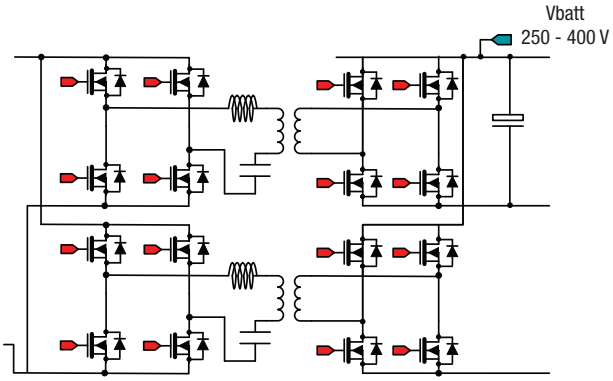


***Figure 9**. Resonant full-bridge LLC topology.*

## C2000 real-time MCUs for resonant full-bridge interleaved LLC

You can also use the TMS320F28004x MCUs for resonant full-bridge interleaved LLC topologies with the C2000 MCU's latest (fourth) generation PWM module, which has two primary features that can help to improve the efficiency of a full-bridge LLC:

- Global one-shot reload for variable-frequency interleaved PWM waveform generation.
- Current balancing between the interleaved phases

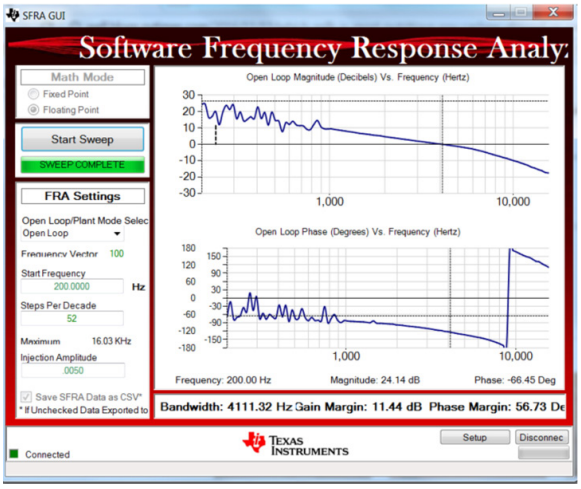


***Figure 10**. The SFRA run on a closed current loop.*

## PWM waveform generation for variable frequency

LLC resonant converters are variable-frequency converters, where the PWM switching frequency of operation frequently changes during runtime. For reliable operation, the changing frequencies must not produce any glitches or irregular PWM behavior. For applications with high-output currents that require input-output isolation, it is common practice to use synchronous rectification (SR) on the secondary side of the isolation transformer. SR uses additional power electronic devices that switch with changing frequencies.

Level 3 charging stations will require multiphase interleaved converters. These interleaved converters have even more devices switching with variable frequencies and require fixed-phase relationships between various phases under all operating frequencies. Guaranteeing correct PWM waveform generation with changing frequencies under all operating conditions is a big challenge for the controller because the safe time to update the PWM parameters becomes smaller as switching frequencies increase or number of interleaved phases increases. Furthermore, when interleaving multiple phases of resonant converters, it is critical to ensure that high accuracy phase current balancing is comprehended in the design. Inadequate or improperly implemented current balancing or incorrect PWM waveform generation can lead to converter failure and significant system or component damage.

**Figure 11** shows how a PWM period update can be missed and can cause a converter failure. The C2000 implementation of a global one-shot reload is a key mechanism to help make sure the PWM waveform generation is done correctly. Global one-shot reload ensures that all duty, phase, and dead-band updates take effect within the switching cycle where the new frequency is needed. This provides a clean transition from one frequency to the other for all phases. In contrast, using a general purpose timer without a one-shot and global reload function, the max switching frequency will be limited due to more cycles needed to be spent to avoid phase sync issues. This also becomes increasingly difficult as more phases are added.

To give an example, if we assume that all PWM modules need to always be in-phase with each other and if there are 16 PWM outputs, and all global reload registers are used, a potential time-critical cycle savings of 142 cycles can be realized. The exact number of cycles saved will depend on the usage. This cycle savings enables higher switching frequencies to be realized.

## Phase Current Balancing

When interleaving two or more identical full-bridge LLC converters, any differences in their tank circuits will lead to unequal balancing of the load current between individual phases. Unequal load balancing is a major problem in interleaved resonant converters because it decreases system efficiency, reliability and thermal stability. This can lead to high-circulating currents, higher ripple current in the output capacitor and even converter failure with significant system damage. Because even small differences from component tolerances can lead to considerable

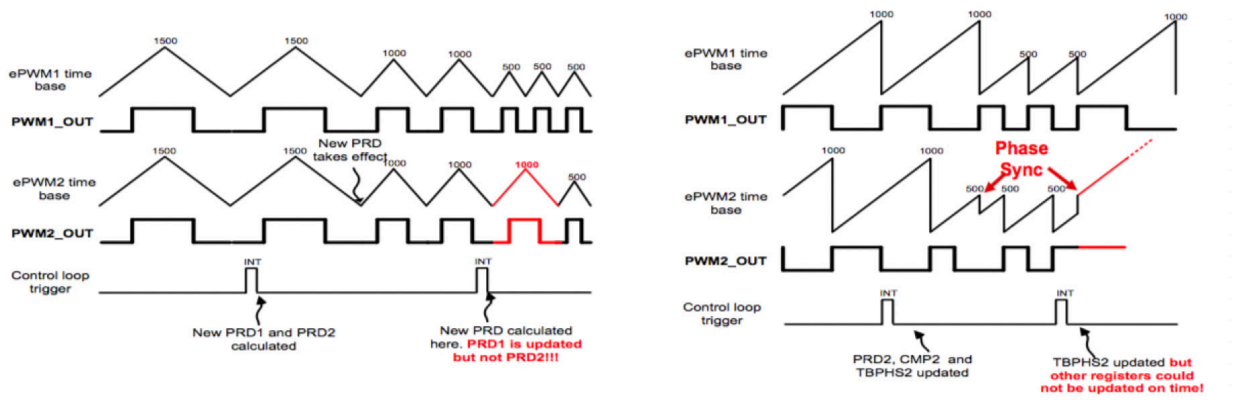


***Figure 11**. Challenges for variable-frequency PWM waveform generation.*

imbalances between phases, all interleaved resonant converters must have a way to share and balance current between individual phases to deliver safe, reliable and efficient operation.

One solution is to design the tank circuit with extremely tight tolerances; however, this design ends up increasing system costs considerably. Moreover, as mentioned above, even the slightest differences from tolerances can still lead to imbalances between phases. Although this solution may work for some applications, it is impractical for most systems. Some solutions try to match the tank circuits in different phases by adding more reactive components to the tank circuits in some or all of the phases, but this also comes with its downsides. In addition to increasing system cost and size, this solution may also increase manufacturing costs if further trimming is required on the assembly line. Recent proposals take this approach a step further by trying to match the tank circuits during operation, adding more power electronic switches to switch additional inductance or capacitance in and out of the tank circuit for some or all of the phases. This approach provides a good way to precisely adjust the tank circuits, but at the expense of increased system cost, size, complexity and a possible reduction in system efficiency.

Other proposals add extra converters based on an additional secondary winding on some or all of the LLC transformers. The operation of this additional converter is then controlled in a way to compensate for the extra current being carried by the other phases. This method suffers the same drawbacks as those discussed above and also increases complexity in the transformer design.

The TMSF28004x MCU can implement current or phase balancing techniques in software without the need for additional external components or circuits. This new design is yet another example of the benefits enabled by the C2000 MCU's highly configurable PWM modules. In this implementation, a current-balancing loop in the software appropriately decreases the PWM duty cycle for those switches in the phase carrying a higher load current. The controller also adjusts PWM timing for corresponding SR switches in that phase.

## The C2000 TMS320F280049 MCU

The F28004x is a new series in the C2000 MCU family (**Figure 12**) designed specifically for power-control applications. The F28004x series includes:

- 100MHz CPU performance with the option of an additional latest generation 100MHz parallel control law accelerator (CLA) co-processor.
- Advanced, Real-Time Control accelerators including TMU, floating-point unit, and Viterbi complex-unit.

- Up to seven integrated CMPSS modules.
- Three high-performance ADCs with a post-processing block, programmable gain amplifiers and a flexible comparator subsystem.
- Flexible timers: fourth-generation enhanced pulse-width modulator (ePWM) modules with 150ps resolution, complex waveform generation and advanced synchronization capability.
- Up to 256KB of integrated flash memory
- 100KB of full-speed random access memory (RAM).

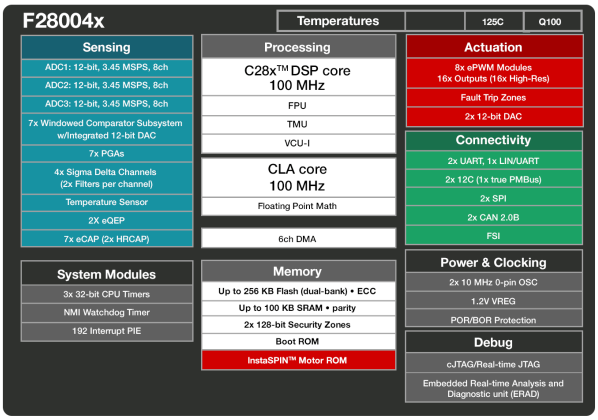


***Figure 12**. The new C2000 F28004x series*

## C2000 MCU-based Vienna rectifier and interleaved LLC DC/DC reference design

For more information on implementing a Vienna rectifier and Interleaved LLC resonant isolated DC/DC converter in charging station power modules based on C2000 real-time MCUs, see the Vienna Rectifier-Based Three-Phase Power Factor Correction Reference Design Using C2000 MCU(s) and Two Phase Interleaved LLC Resonant Converter Reference Design Using C2000 MCUs. The latter design is based on a half bridge, but you can apply many techniques used in that reference design to a full-bridge implementation.

## Conclusion

As the demand for higher power Level 3 DC charging stations increases, topologies such as the Vienna Rectifier with interleaved LLC DC/DC to implement 3 phase AC to DC power conversion at high efficiencies will become increasely more critical.  C2000's new F28004x real-time microcontroller series builds on C2000's rich portfolio of optimal solutions that help engineers solve design challenges related to these designs highlighted in this paper and other advanced power topologies.

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