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Application Report
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TPS65950/30/20 32-kHz Oscillator Schematic and PCB Layout Guide

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ABSTRACT

This application note explains the layout guidelines for the 32-kHz oscillator for the TPS65950 power-management and audio code integrated circuit. Because PCB layout is always a compromise based on different system designs, use this application note as a reference for layout guidelines.

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1 Purpose

The objective of this document is to provide application engineers with PCB design guidelines that can be applied to improve the performance of the TPS659xx 32-kHz oscillator, and to prevent ramp-up production issues. Most recommendations provided by this document are specific to the TPS659xx 32-kHz oscillator and may not be best practices for other devices. PCB rules can differ depending on the design option, the die layout, and packaging.

2 Equivalent Circuit of the Oscillator and External Components

2.1 32-kHz Oscillator Block Diagram

Figure 1 is a block diagram of the 32-kHz cell. The oscillator cell contains the oscillator circuitry, the biasing generator, and the startup circuit. It also contains a shaper stage to generate the internal 32-kHz logic signal, and two internal crystal load capacitors, Cxi and Cxo.

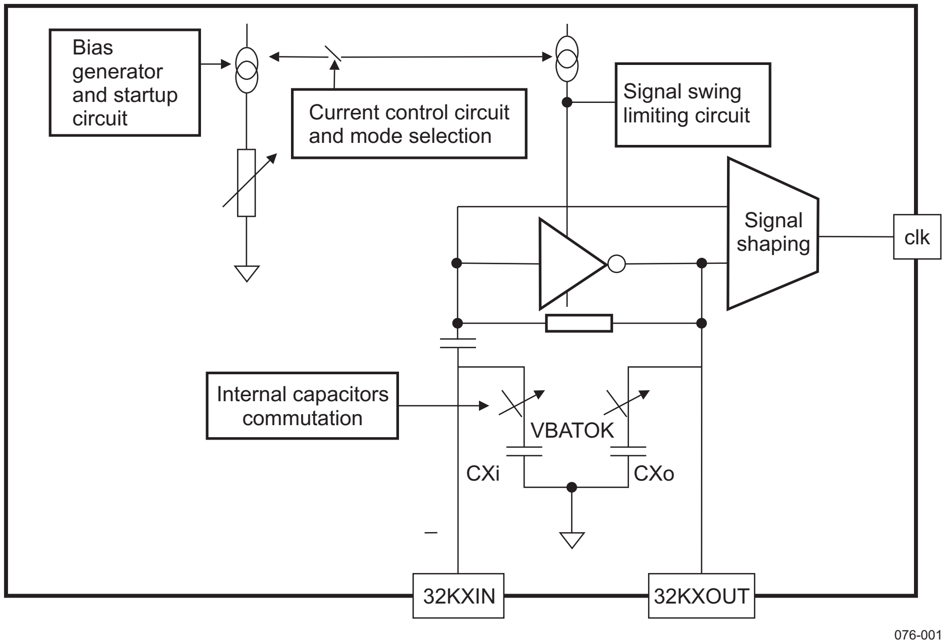

Figure 1. TPS659xx 32-kHz Internal Block Diagram

2.2 *Equivalent Circuit and External Components*

Figure 2 shows the equivalent circuit of the oscillator with additional required components. The oscillator is based on a CMOS inverter; crystal and phasing capacitors (C1, C2) are connected between input and output of the oscillator to provide the additional phase lag required to satisfy the oscillation criteria. The 1-µF capacitor is the tank load capacitor of the VRRTC supply; resistor R and capacitor C3 prevent the oscillator from starting in a parasitic mode. An additional filter (R, C3) is required if a crystal model is used with a potential start of oscillation at the sixth harmonic frequency (200 kHz).

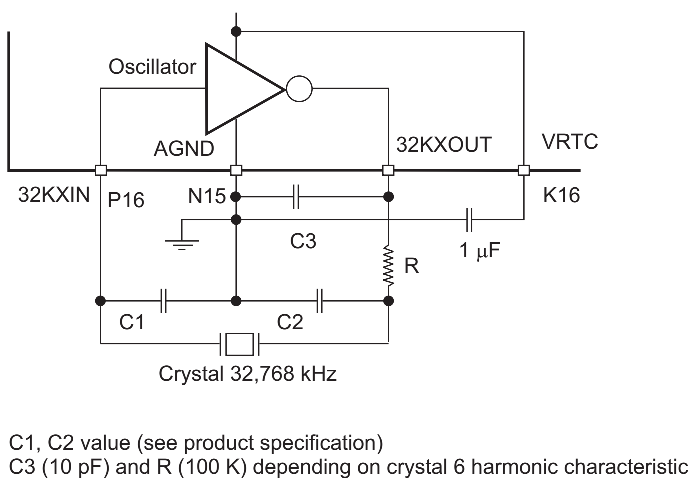

Figure 2. 32-kHz Equivalent Circuit and External Components With Recommended Values

3 PCB Layout Recommendations

3.1 Basic Information

Attention must be paid to the low-frequency oscillator and to the way the external components are placed and interconnected. Because of the oscillator gain characteristics and slow signal rise and fall times (quasi sine wave signal), the low-frequency oscillator is extremely sensitive to power supply noise and to electromagnetic coupling to fast surrounding signals. Noise coupling can significantly degrade the frequency stability of the oscillations. The objective of this section is to present general guidelines that can be applied to improve the performance of the oscillator and to prevent any critical issues.

3.2 Placement of Components

To avoid excessive noise sensitivity caused by spurious coupling or parasitic antenna phenomena on the PCB, the connections of the crystal to oscillator input and output and to other components must be as short as possible. The best practice is to place the crystal and phasing capacitors as close as possible to the TPS65950 part. This helps to minimize the length of connections. Figure 3 shows the closest possible position.

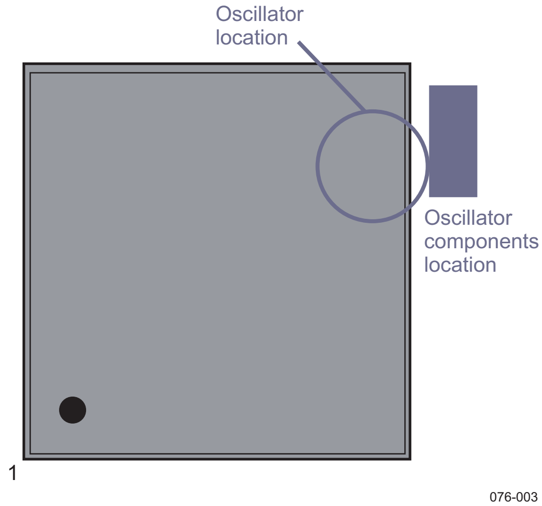

Figure 3. Best Placement for Crystal and Components

If the crystal and its associated components cannot be placed close to the package because of other critical compromises, all connections must be routed carefully to avoid passing under the package with long traces or making critical loops that could create spurious coupling with the logic activity.

3.3 Crystal Phasing Capacitors and Ground Return Current

Because the phase lag between the currents flowing through the two load capacitors (C1 and C2) are in opposition, the best practice is to connect close to the crystal, the two capacitors before connecting to the ground reference. At that time the current back to the ground is significantly reduced. There is no isolated GND on the oscillator.

The common point of the two capacitors must be connected to the reference ground, AGND. The connections must be as short as possible and of identical lengths. Avoid long connections from these capacitors that make a large loop on the PCB, because this behaves like an antenna and can collect surrounding high-frequency radiation.

3.4 Ground Plane Reference and Cross-Coupling

The reference ground of the oscillator must be as quiet as possible; otherwise, high-frequency noise is transmitted directly to the oscillator input and output, resulting in degradation of the oscillator performance. To prevent cross-coupling to fast signals with high-level harmonic content, do not route signal traces through the crystal area. Both oscillator pin connections are critical.

Putting a separate ground under the crystal and the oscillator connected to the reference ground plane generally causes a worse situation. The separate plane must have the same potential as the principal ground plane for all frequency ranges. A separate plane connected by one point can behave like an antenna.

3.5 Spurious Oscillation Mode

If the gain of the oscillator is greater than one at 200 kHz and the condition is satisfied on a spurious tortional mode, the tuning fork crystal model currently used for the 32-kHz crystal oscillator can oscillate at a frequency near 200 kHz, instead of oscillating at the fundamental longitudinal mode (32 kHz).

A good protection against this phenomenon is to put in series with the crystal a resistor that creates an additional phase lag with crystal capacitor C2 so that the criteria for oscillation at 200 kHz cannot be reached. This series resistor also limits current in the crystal during startup.

An additional filtering effect versus high-frequency noise is provided by capacitor C3 (10 pF) connected to the REFGND pin. If the series resistor is not used, capacitor C3 must not be mounted.

The best strategy is to implement the footprint on the PCB for the resistor and capacitor C3.

4 Summary of PCB Layout Guidelines

For the best performance, observe the following guidelines:

1. Place the crystal and its components close to the oscillator side and the oscillator pins.
2. Ensure that the ground plane under the oscillator and its components are of good quality.
3. Avoid placing a separate ground under the oscillator and connecting it to the general ground through a single point.
4. Avoid long connections to the crystal and to the load capacitor that create a large loop on the PCB or that pass under the uBGA package.
5. Use a short connection between the two crystal load capacitors and route the common connection to the oscillator ground reference.
6. Place a ceramic capacitor for noise filtering from VRRTC to REFGND with short connections.
7. Place the 32KCLK_out (logic output signal) output so that the return ground current runs back to REFGND. Do not route the trace close to the oscillator input.
8. Add a series resistor between the output of the oscillator and the crystal to suppress a spurious tortional oscillation mode of the crystal (depending on the crystal model used). If using this resistor, place a filtering capacitor for high-frequency noise at the slicer input.

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