TPS65921 PCB Layout Guidelines

Application Report

Literature Number: SWCA091A
October 2010–Revised March 2012

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TPS65921 PCB Layout Guidelines

ABSTRACT

This document describes how to connect the TPS65921 features during board layout.

1 Introduction

Some TPS65921 features need specific attention during board layout. This document describes how to connect each ball on the PCB and what to do when functions are not used.

2 TPS65921 Layout Recommendations

2.1 PCB Recommendation for Each Pin

Table 1. PCB Recommendation for Each Pin

Name	Ball	Type	I/O (1)	Description	PCB Recommendation	Not Used Features (2)
JTAG.TDO/GPIO	L9	Digital	I/O	JTAG® test output or GPIO0/card detection 1	--	Floating
ADCIN0	F2	Analog	I/O	General-purpose ADC input	--	Floating
STAR.ADC/JTAG.TDI	H7	Digital	I	ADC conversion request/JTAG test data input	--	GND
SDA	C4	Digital	I/O	General-purpose inter-integrated circuit (I^2C™) bidirectional data signal	--	N/A (3)
SCL	B3	Digital	I/O	General-purpose I^2C bidirectional clock signal	--	N/A
SRI2C_SDA	D4	Digital	I/O	SmartReflex™ I^2C bidirectional data signal	--	Floating
SRI2C_SCL	A3	Digital	I/O	SmartReflex I^2C bidirectional clock signal	--	GND
PWRON	D5	Digital	I	Input detects a control command to start or stop the system.	--	VBAT
REGEN	G3	Digital	O	Enable signal for external low-dropout (LDO) regulator.	--	Floating
MSECURE	G8	Digital	I	Security and digital rights management	--	IO.1P8
BOOT0	E5	Digital	I	Power-up sequence selection	--	N/A
BOOT1	F6	Digital	I	Power-up sequence selection	--	N/A
NRESPWRON	E7	Digital	O	Output control the NRESETN of the application processor	--	Floating
NRESWARM	H8	Digital	I	Warm reset signal	--	GND
NSLEEP	K4	Digital	I	ACTIVE-SLEEP state transition control signal	--	GND

(1) I = Input, O = Output
(2) This column provides the connection when the associated feature is not used or not connected.
(3) N/A = Not applicable

Table 1. PCB Recommendation for Each Pin (continued)

Name	Ball	Type	I/O [1]	Description	PCB Recommendation	Not Used Features [2]
INT	A9	Digital	O	Interrupt line output	--	Floating
SYSEN	B9	Digital	O	System enable output	--	Floating
CLKEN	F10	Digital	O	Clock enable	--	Floating
CLK32KOUT	G6	Digital	O	32-kHz clock output	--	Floating
32KXOUT	G11	Analog	O	32-kHz crystal oscillator	Sensitive balls. Route as differential pair. Place crystal as close as possible to balls.	Floating
32KXIN	H11	Analog	I			N/A
HFCLKIN	C8	Analog	I	Sine wave or square wave input	High-speed (HS) clock. Keep away from sensitive signals.	N/A
HFCLKOUT	K8	Digital	O	50% duty cycle square wave output	HS clock. Keep away from sensitive signals.	Floating
VREF	G10	Analog	O	Reference voltage	Very sensitive, connect capacitor close ball	N/A
GND_AGND	K7	Analog	I/O	Substrate ground	Connect to a clean ground.	GND
AGND	H10	Analog	I/O	Reference ground	Connect to a clean ground same as 32-kHz oscillator foot capacitor ground and VREF capacitor ground.	GND
DGND	B8	Power	I/O	Digital ground	Do not connect with DCDC/charge pump ground.	GND
IO.1P8	A10	Power	I	Supply for input/output (I/O) buffers (VDDIO)	--	N/A
VBACKUP	G9	Power	I	Must be shorted to GND	--	GND
VDD1.IN	E9, E10, E11	Power	I	VDD1 DCDC input	High current (≈2.5-A peak) and noisy balls. Place input capacitor close to balls. Connect input capacitor ground to VDD1.GND.	VBAT
VDD1.GND	A11, B10, B11	Power	I/O	VDD1 DCDC power ground	High current (≈2.5-A peak) pin. Connect to separate GND plane. Connect separate plane to main plane in a single point to avoid GND loop.	GND
VDD1.L	C10, C11, D10	Power	O	VDD1 DCDC switched output	High current (≈2.5-A peak) and noisy balls. Connect with shortest shape to inductor.	Floating
VDD1.FDBK	D11	Analog	I	VDD1 feedback voltage (output)	Sensitive signal. Keep away from noisy signals as VDD1.L. Connect output capacitor ground to VDD1.GND.	GND
VDD2.IN	K10,L10	Power	I	VDD2 DCDC input	High current (≈1.2-A peak) and noisy balls. Place input capacitor close to balls. Connect input capacitor ground to VDD2.GND.	VBAT
VDD2.GND	J10, J11	Power	I/O	VDD2 DCDC power ground	High current (≈1.2-A peak) pin. Connect to separate GND plane. Connect separate plane to main plane in a single point to avoid GND loop.	GND

Table 1. PCB Recommendation for Each Pin (continued)

Name	Ball	Type	I/O [1]	Description	PCB Recommendation	Not Used Features [2]
VDD2.L	K11, L11	Power	O	VDD2 DCDC switched output	High current (≈1.2-A peak) and noisy balls. Connect with shortest shape to inductor.	Floating
VDD2.FDBK	H9	Analog	I	VDD2 feedback voltage (output)	Sensitive signal. Keep away from noisy signals as VDD2.L. Connect output capacitor ground to VDD2.GND.	GND
VIO.IN	K2, L2	Power	I	VIO DCDC input	High current (≈1.4-A peak) and noisy balls. Place input capacitor close to balls. Connect input capacitor ground to VIO.GND.	VBAT
VIO.GND	J1, J2	Power	I/O	VIO DCDC power ground	High current pin (≈1.4-A peak). Connect to separate GND plane. Connect with main plane in a single point to avoid GND loop.	GND
VIO.L	K1, L1	Power	O	VIO DCDC switched output	High current (≈1.4-A peak) and noisy balls. Connect with shortest shape to inductor.	Floating
VIO.FDBK	H1	Analog	I	VIO feedback voltage (output)	Sensitive signal. Keep away from noisy signals as VIO.L. No current, route with thin net. Connect output capacitor ground to VIO.GND.	GND
VAUX12S.IN	F1	Power	I	VAUX LDO input	100-mA trace. Place capacitor close to ball.	VBAT
VAUX.OUT	G1	Power	O	VAUX regulator output	100-mA trace. Place capacitor close to ball.	Floating
VPLLA3R.IN	A6	Power	I	VPLL//VRTC LDO input	70-mA trace. Place capacitor close to ball.	VBAT
VPLL1.OUT	A8	Power	O	VPLL LDO output	40-mA trace. Place capacitor close to ball.	Floating
VRTC.OUT	B5	Power	O	VRTC internal LDO output (internal use only)	Place capacitor close to ball.	N/A
VINT.IN	A7	Power	I	VINTDIG LDO input	100-mA trace. Place capacitor close to ball.	VBAT
VINTANA1	D1	Power	O	VINTANA1 internal LDO output (internal use only)	Place capacitor close to ball.	N/A
VINTANA2	A2	Power	O	VINTANA2 internal LDO output (internal use only)	Place capacitor close to ball.	N/A
VDAC.IN	C1	Power	I	VDAC/VINTANA1/VINTAN2 LDO input	370-mA trace. Place capacitor close to ball.	VBAT
VDAC.OUT	E1	Power	O	VDAC LDO output	70-mA trace. Place capacitor close to ball.	Floating
VINTDIG.OUT	B7	Power	O	VINTDIG internal LDO output (internal use only)	Place capacitor close to ball.	N/A
VMMC.IN	B1	Power	I	VMMC Input LDO	220-mA trace. Place capacitor close to ball.	VBAT
VMMC1.OUT	A1	Power	O	VMMC LDO output	220-mA trace. Place capacitor close to ball.	Floating
VBAT.USB	K6	Power	I	VUSB1P8, VUSB1P5, and VUSB3P1 regulators input	Place capacitor close to ball.	VBAT

Table 1. PCB Recommendation for Each Pin (continued)

Name	Ball	Type	I/O [1]	Description	PCB Recommendation	Not Used Features [2]
VUSB.3P1	L6	Power	O	VUSB.3P1 LDO output	Place capacitor close to ball.	N/A
VUSB1P8.OUT	J6	Power	O	VUSB1P8 LDO output (internal use only)	Place capacitor close to ball.	Floating
VUSB1P5.OUT	J5	Power	O	VUSB1P5 LDO output (internal use only)	Place capacitor close to ball.	Floating
TESTV1	H2	Analog	IO	Analog test pin 1	--	Floating
TESTV2	C9	Analog	IO	Analog test pin 2	--	Floating
TEST	D3	Digital	IO	Selection between JTAG mode and application mode	--	Floating
AVSS1	F3	Power	I/O	Analog ground	--	GND
AVSS2	H6	Power	I/O	Analog ground	--	GND
AVSS3	F9	Power	I/O	Analog ground	--	GND
AVSS4	A4	Power	I/O	Analog ground	--	GND
VBUS	K5	Power		VBUS power rail	100-mA trace	N/A
DP	L7	Analog	I/O	USB differential data line	See Section 2.2 of the USB PCB recommendation.	N/A
DM	L8	Analog	I/O	USB differential data line		N/A
ID	J7	Digital	I/O	USB ID		Floating
UCLK	D6	Digital	I/O	HS USB clock		Floating
STP	E6	Digital	I/O	HS USB stop		Floating
DIR	A5	Digital	I/O	HS USB direction		Floating
NXT	C5	Digital	I/O	HS USB next		Floating
DATA0	B6	Digital	I/O	HS USB Data0		Floating
DATA1	C6	Digital	I/O	HS USB Data1		Floating
DATA2	C7	Digital	I/O	HS USB Data2		Floating
DATA3	D7	Digital	I/O	HS USB Data3		Floating
DATA4	F8	Digital	I/O	HS USB Data4		Floating
DATA5	F11	Digital	I/O	HS USB Data5		Floating
DATA6	E8	Digital	I/O	HS USB Data6		Floating
DATA7	D9	Digital	I/O	HS USB Data7		Floating
CP_IN	L4	Power	I/O	Charge pump input voltage	200-mA trace. Noisy ball. Place input capacitor close to balls. Connect input capacitor ground to CP_GND.	VBAT
CP_GND	J3	Power GND	I/O	Charge pump ground	Connect to separate GND plane. Connect separate plane to main plane in a single point to avoid GND loop.	GND
CP_CAPP	L5	Analog	I/O	Charge pump flying capacitor P	Place fly capacitor as close as possible to balls.	Floating
CP_CAPM	L3	Analog	I/O	Charge pump flying capacitor M		
KPD.C0	B4	Open-drain	O	Keypad column 0	--	Floating
KPD.C1	D2	Open-drain	O	Keypad column 1	--	Floating
KPD.C2	E2	Open-drain	O	Keypad column 2	--	Floating
KPD.C3	B2	Open-drain	O	Keypad column 3	--	Floating
KPD.C4	C2	Open-drain	O	Keypad column 4	--	Floating
KPD.C5	E4	Open-drain	O	Keypad column 5	--	Floating
KPD.C6	E3	Open-drain	O	Keypad column 6	--	Floating

Table 1. PCB Recommendation for Each Pin (continued)

Name	Ball	Type	I/O [1]	Description	PCB Recommendation	Not Used Features [2]
KPD.C7	F4	Open-drain	O	Keypad column 7	--	Floating
KPD.R0	H5	Digital	I	Keypad row 0	--	Floating
KPD.R1	G4	Digital	I	Keypad row 1	--	Floating
KPD.R2	H4	Digital	I	Keypad row 2	--	Floating
KPD.R3	G5	Digital	I	Keypad row 3	--	Floating
KPD.R4	J4	Digital	I	Keypad row 4	--	Floating
KPD.R5	J8	Digital	I	Keypad row 5	--	Floating
KPD.R6	G7	Digital	I	Keypad row 6	--	Floating
KPD.R7	F5	Digital	I	Keypad row 7	--	Floating
VBAT	K3	Power	I/O	Battery input voltage	Battery sense pin, very sensitive. Connect to a clean Vsystem.	VBAT
CLKREQ	D8	Digital	I	Clock request	--	GND
TEST.RESET	J9	Digital	I	Reserved	--	GND
VPROG	H3	Analog	I	Reserved	--	GND
JTAG.TCK	F7	Digital	I	JTAG clock input	--	GND
JTAG.TMS/GPIO	K9	Digital	I/O	JTAG test mode state or GPIO1/card detection 2	--	Floating
TEST2/GPIO2	G2	Digital	I	Digital test pin/GPIO2	--	Floating

2.2 USB-Specific Recommendation

2.2.1 General Considerations

- USB design requires symmetrical termination and symmetrical components placement along DP and DM paths.
- Place the USB host controller and major components on the unrouted board first.
- Place the USB host controller as close as possible to the transceiver device; for example, ULPI traces as short as possible.
- Route the HS clock and HS USB. Route differential pairs first.
- Maintain the maximum possible distance between HS clocks/periodic signals to the HS USB differential pairs and any connector leaving the PCB (such as I/O connectors, control and signal headers, and power connectors).
- The maximum TI-recommended external capacitance on DP (or DM) lines is 4 pF.
  - This capacitance is the sum of all external discrete components; that is, the total capacitance on DP/DM lines, including trace capacitance, can be larger than 4 pF.
  - All discrete components must be placed as close as possible to the USB receptacle.
- Place low-capacitance ESD protections as close as possible to the USB receptacle, with no other external devices in between.
- Common mode chokes degrade signal quality; thus, they must be used only if EMI performance enhancement is necessary.
- Place common mode chokes (if required to improve EMI performance) as close as possible to the USB receptacle, but after the ESD device(s).

2.2.2 USB Interface (DP/DM)

- Route the USB receptacle ground pin to the analog ground plane of the device with multiple vias connections.
- Route the DP/DM trace pair together.
- For HS-capable devices, route the DP/DM signals from the device to the USB receptacle with the optimum trace length of 5 cm, and the maximum trace length 1-way delay of 0.5 ns (7.5 cm for 67 ps/cm in FR-3).
- Match DP/DM trace lengths. The maximum mismatch allowed is 150 mils (~0.4 cm).
- Route DP/DM signals with 90-Ω differential impedance, and 22.5~30-Ω common-mode impedance (the objective is to have Zodd ~= Z0 = Zdiff/2 = 45 Ω)
- Use an impedance calculator to determine the trace width and spacing required for the specific board stackup being used.
- Keep the maximum possible distance between DP/DM signals from other platform clocks, power sources, and digital/analog signals.
- Do not route DP/DM signals over/under crystals, oscillators, clock synthesizers, magnetic devices, and ICs that use clocks.
- Avoid changing the routing layer for DP/DM traces; if unavoidable, use multiple vias.
- Minimize bends and corners on DP/DM traces.
- When it becomes necessary to turn 90 degrees, use two 45-degree turns or an arc instead of one 90-degree turn. This reduces reflections on the signal by minimizing impedance discontinuities.
- Avoid creating stubs on DP/DM traces, because stubs cause signal reflections and affect global signal quality.
- If stubs are unavoidable, they must be lower than 200 mils (~0.5 cm).
- Route DP/DM signals over continuous VCC or GND planes without interruption, avoiding crossing anti-etch (plane splits), which increases inductance and radiation levels by introducing a greater loop area.
- Route DP/DM signals at least 25 mils (~0.65 mm) away from any plane splits.
- Follow the 20 * h rule of thumb by keeping traces at least 20 * (height above the plane) away from the edge of the plane (VCC or GND, depending on the plane the trace is over).
- Changing signal layers is preferable to crossing plane splits if a choice must be made.
- If crossing a plane split is unavoidable, proper placement of stitching caps can minimize the adverse effects on EMI and signal quality performance caused by crossing the split.
- Avoid anti-etch on the ground plane.

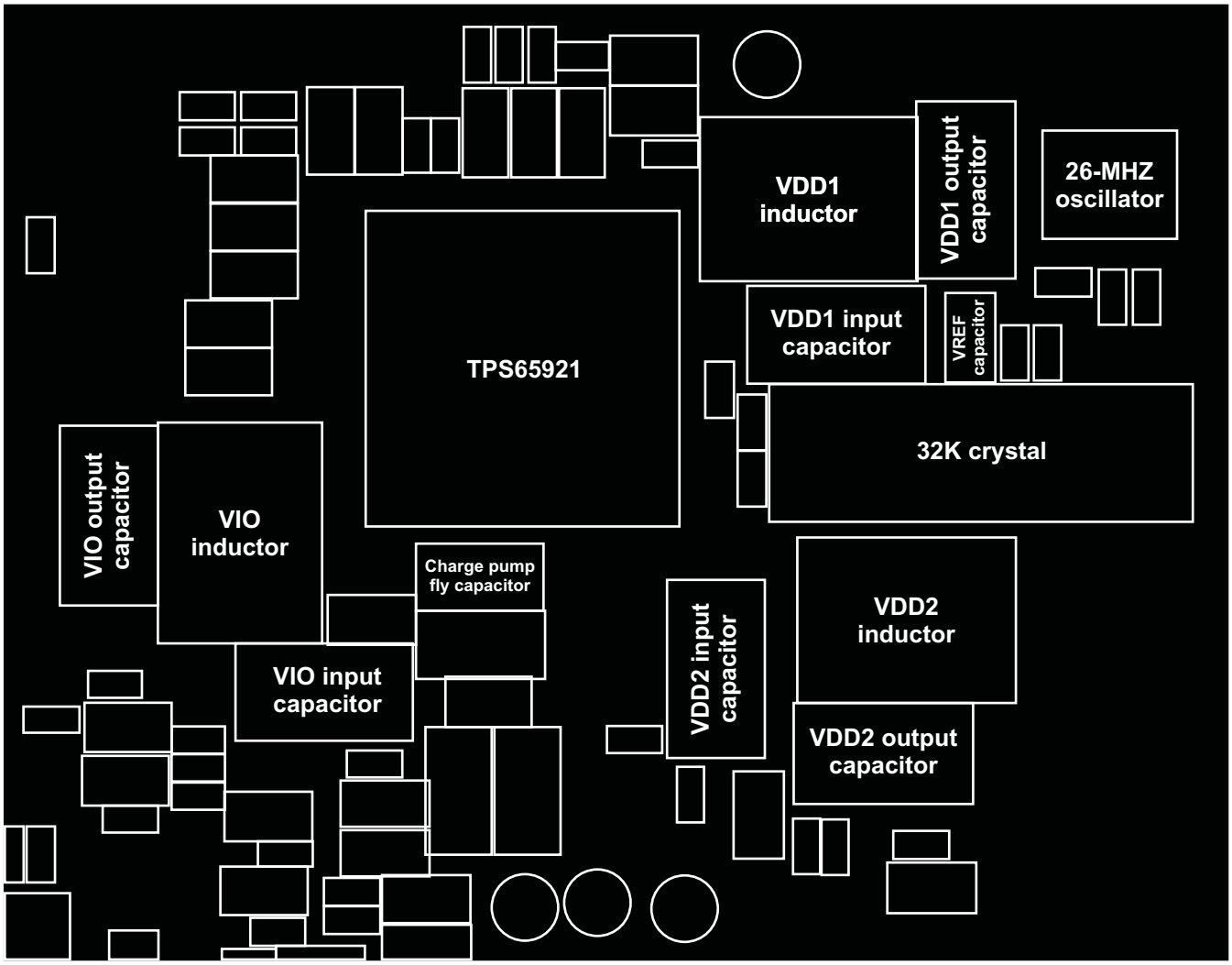
2.2.3 ULPI Interface

- Route the ULPI 12-pin bus as a 50-Ω single-ended nonterminated adapted bus.
- Route the ULPI 12-pin bus with minimum trace lengths and a strict maximum of 50 mm, to ensure timing. Match 12 ULPI signal trace lengths.
- Route the ULPI 12-pin bus as clock signals and set a minimum spacing of three times the trace width (S < 3W).

2.3 Layout Examples

2.3.1 Critical Component Placement

Figure 1. Critical Component Placement



2.3.2 DCDC Layout:VIO

Figure 2. VIO DCDC Layout Top

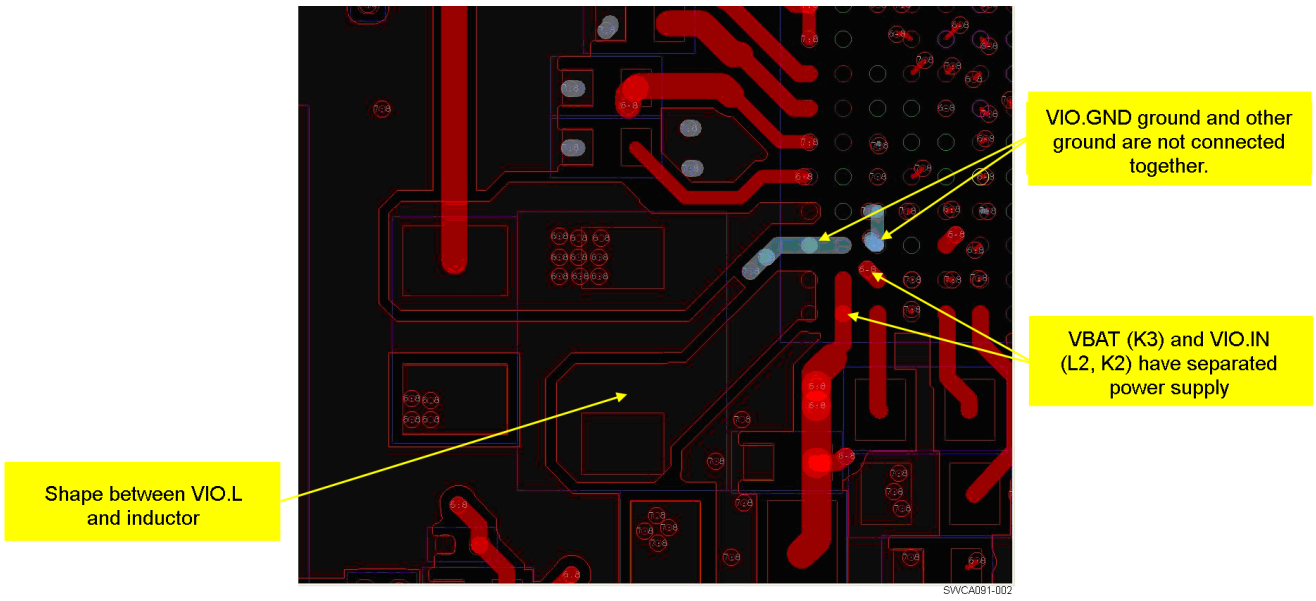
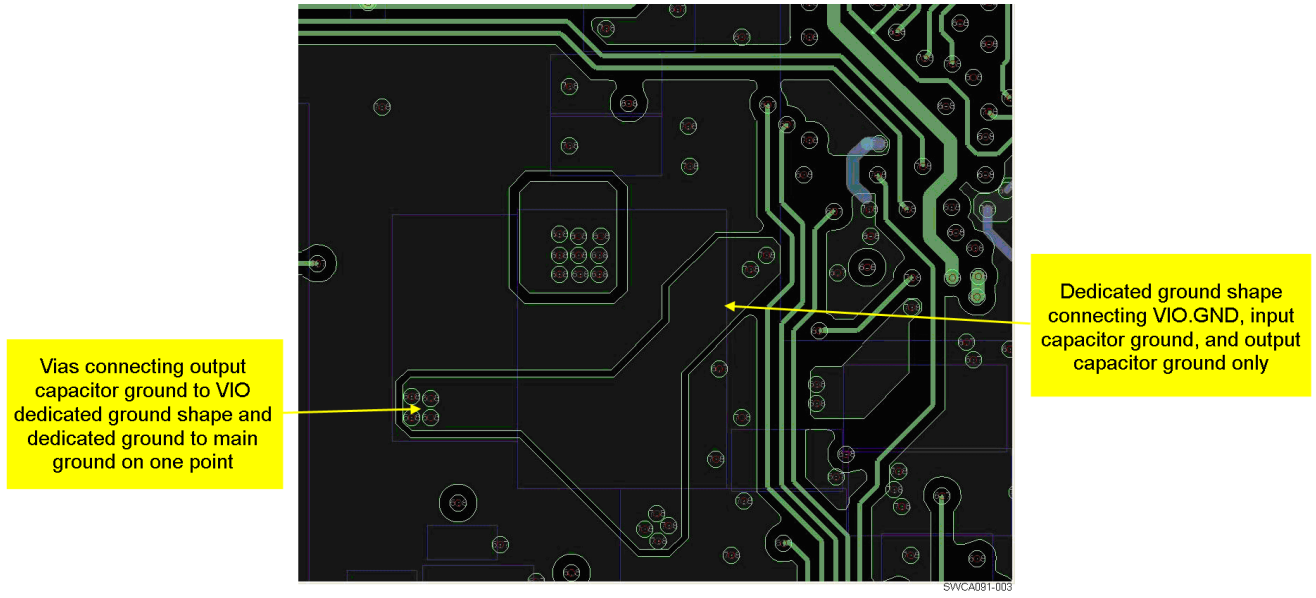


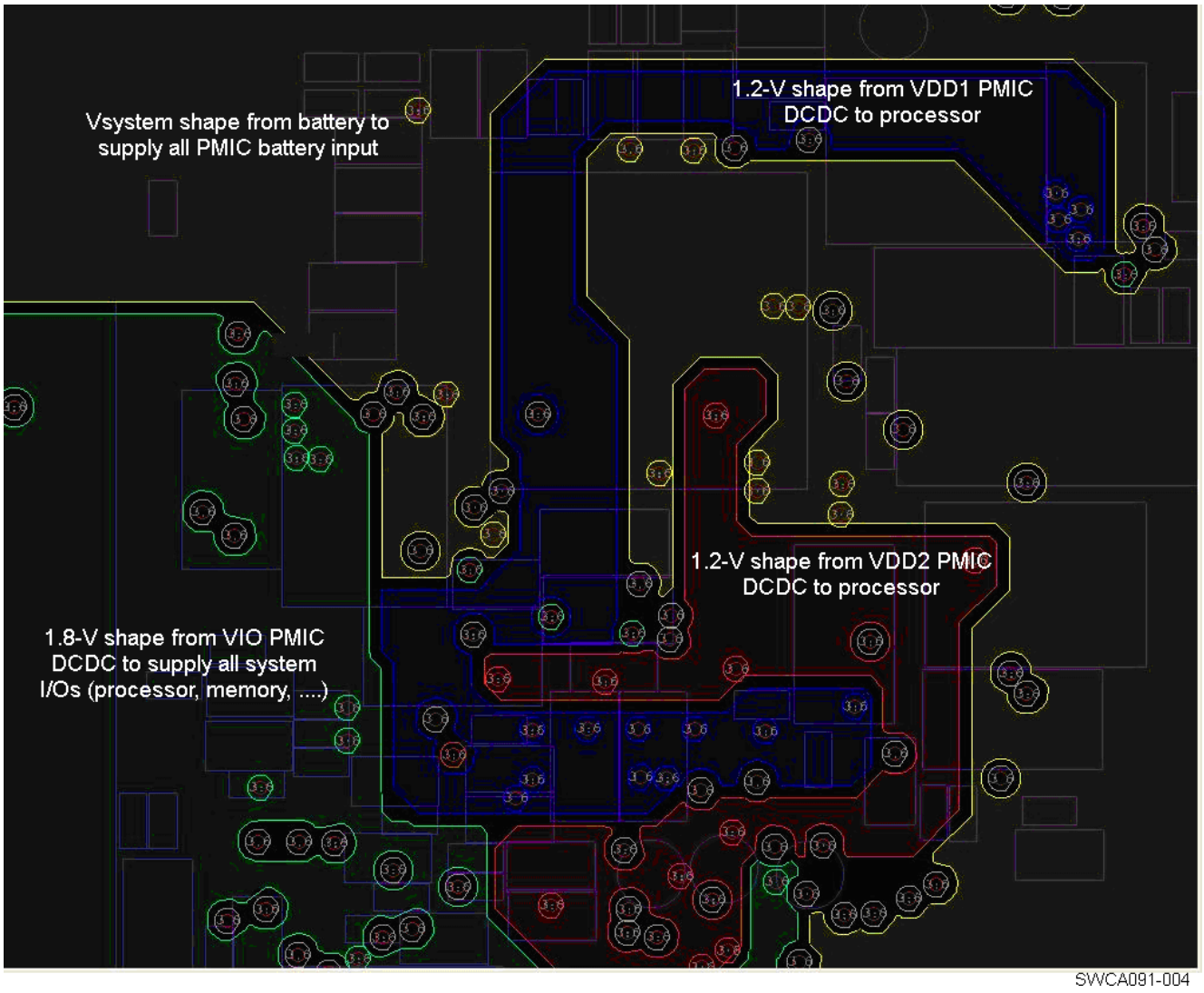
Figure 3. VIO DCDC Layout IN1



2.3.3 Power Supply Layout

A layer must be used for system power. Use shape for Vsystem and a DCDC-to-processor connection to minimize the loss of power in the PCB (see Figure 4).

Figure 4. Power Layer Layout on PMIC Side



2.3.4 USB Connector Layout

Figure 5. USB Board Layout Bottom Side

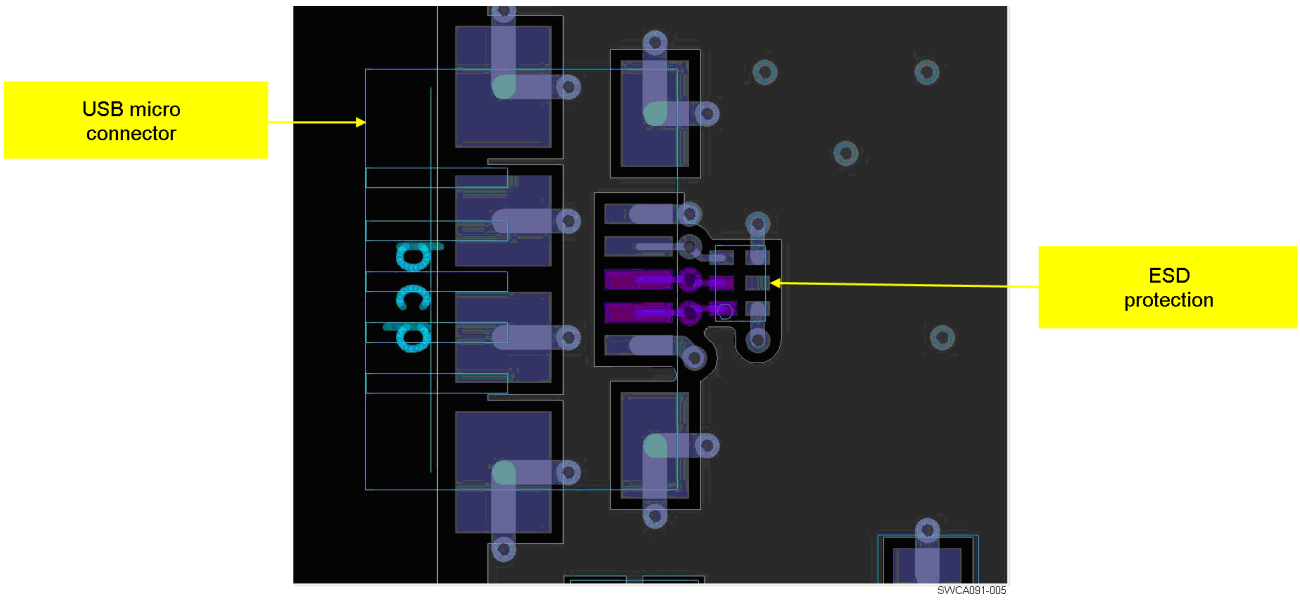
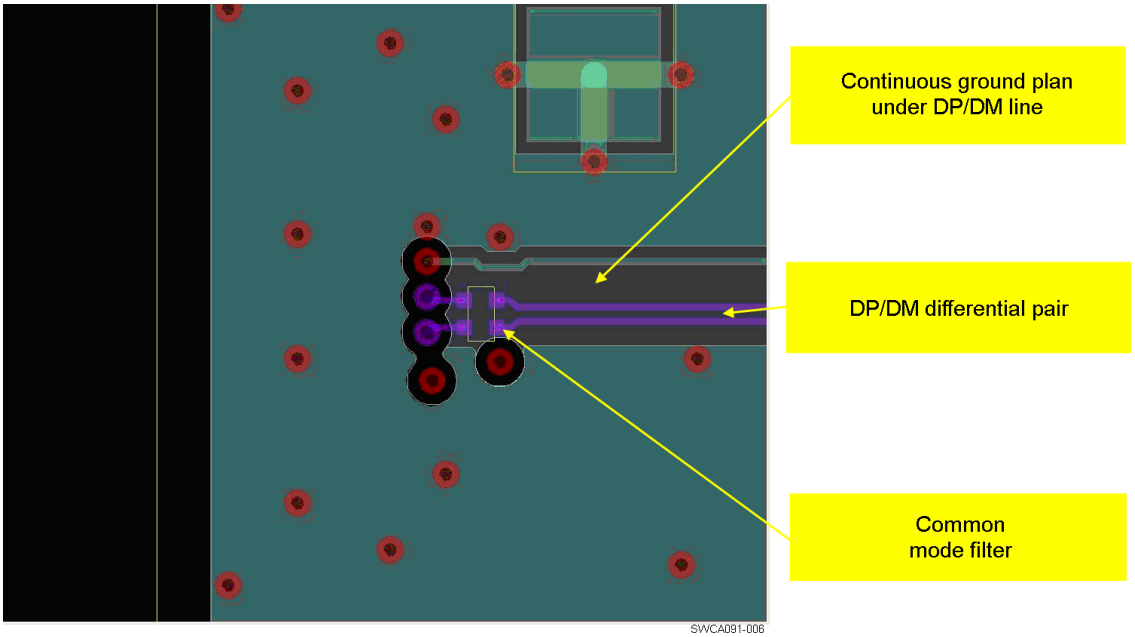


Figure 6. USB Board Layout TOP/IN1 Side



2.3.5 32-kHz and Reference Layout

Figure 7. Reference and 32-kHz Oscillator Layout Top

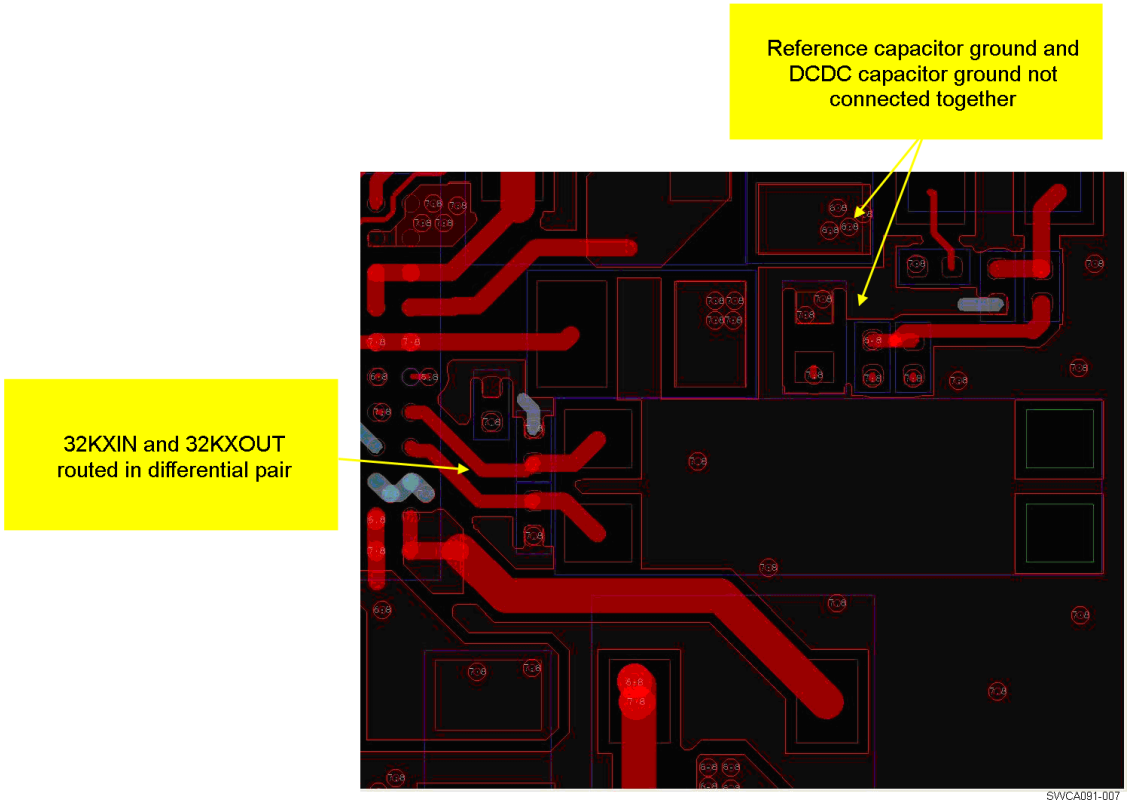
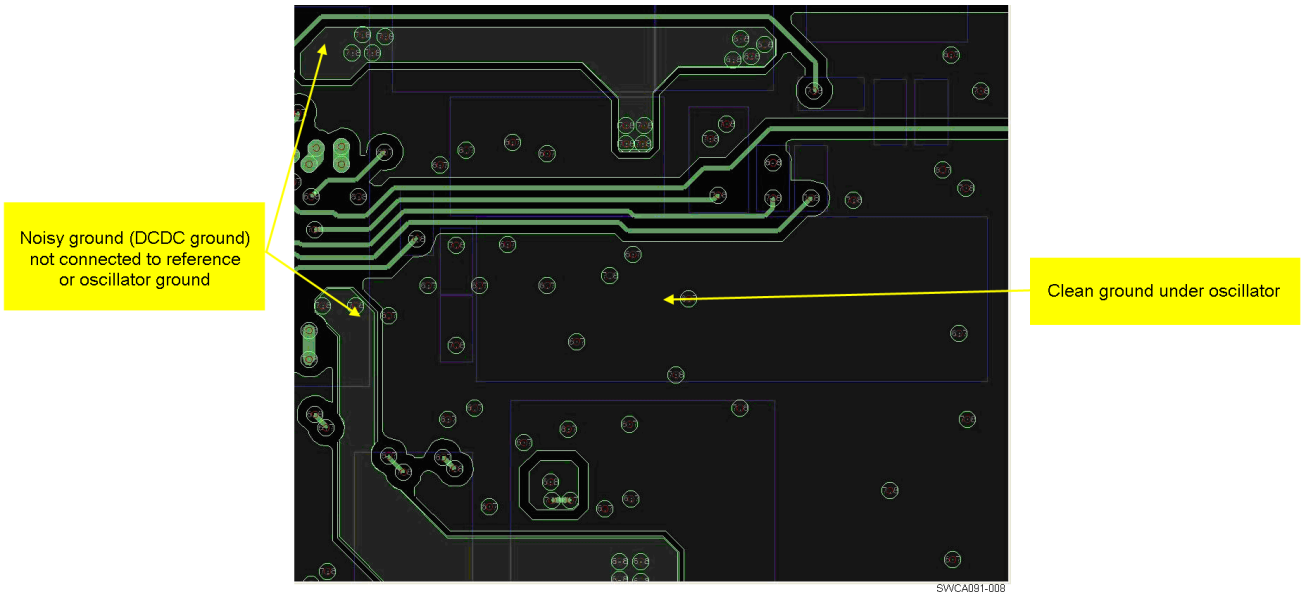


Figure 8. Reference and 32-kHz Oscillator Layout IN1



3 Revision History

Table 2. REVISION HISTORY

Version	Literature Number	Date	Notes
*	SWCA091	October 2010	See (1).
A	SWCA091	March 2012	See (2)

(1) *TPS65921 PCB Layout Guidelines*, SWCA091 - Initial release.
(2) *TPS65921 PCB Layout Guidelines*, SWCA091A - Table 1: Swap and update ground desctions

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