TPS65921 Register Manual

1 TPS65921 Instance Summary

The table below shows the I2C bus and I2C address for all TPS65921 module instances.

Table 1. TPS65921 Instance Summary

Module Name	Used I2C bus	I2C Address
USB	General Purpose	0x48
INT	General Purpose	0x49
AUX	General Purpose	0x4A
POWER	General Purpose	0x4B
POWER_SR	Smart Reflex	0x12

2 USB

This section provides information on the USB module instances within this product. Each of the registers within the different USB module instances is described separately below.

2.1 USB Sub Chip Instance Summary

The table below shows the base address USB module instances.

Table 2. USB Instance Summary

Module Name	Base Address
USB	0x00

2.2 USB Registers Mapping Summary

Table 3. USB Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	Address Offset	Physical Address
VENDOR_ID_LO	RO	8	0x51	0x00	0x00
VENDOR_ID_HI	RO	8	0x04	0x01	0x01
PRODUCT_ID_LO	RO	8	0x02	0x02	0x02
PRODUCT_ID_HI	RO	8	0xC0	0x03	0x03
FUNC_CTRL	RW	8	0x41	0x04	0x04
FUNC_CTRL_SET	RW	8	0x41	0x05	0x05
FUNC_CTRL_CLR	RW	8	0x41	0x06	0x06
IFC_CTRL	RW	8	0x18	0x07	0x07
IFC_CTRL_SET	RW	8	0x18	0x08	0x08
IFC_CTRL_CLR	RW	8	0x18	0x09	0x09
OTG_CTRL	RW	8	0x06	0x0A	0x0A

Table 3. USB Register Summary (continued)

Register Name	Type	Register Width (Bits)	Register Reset	Address Offset	Physical Address
OTG_CTRL_SET	RW	8	0x06	0x0B	0x0B
OTG_CTRL_CLR	RW	8	0x06	0x0C	0x0C
USB_INT_EN_RISE	RW	8	0x1F	0x0D	0x0D
USB_INT_EN_RISE_SET	RW	8	0x1F	0x0E	0x0E
USB_INT_EN_RISE_CLR	RW	8	0x1F	0x0F	0x0F
USB_INT_EN_FALL	RW	8	0x1F	0x10	0x10
USB_INT_EN_FALL_SET	RW	8	0x1F	0x11	0x11
USB_INT_EN_FALL_CLR	RW	8	0x1F	0x12	0x12
USB_INT_STS	RO	8	0x01	0x13	0x13
USB_INT_LATCH	RO	8	0x01	0x14	0x14
DEBUG	RO	8	0x00	0x15	0x15
SCRATCH_REG	RW	8	0x00	0x16	0x16
SCRATCH_REG_SET	RW	8	0x00	0x17	0x17
SCRATCH_REG_CLR	RW	8	0x00	0x18	0x18
CARKIT_CTRL	RW	8	0x00	0x19	0x19
CARKIT_CTRL_SET	RW	8	0x00	0x1A	0x1A
CARKIT_CTRL_CLR	RW	8	0x00	0x1B	0x1B
CARKIT_INT_DELAY	RW	8	0x52	0x1C	0x1C
CARKIT_INT_EN	RW	8	0x00	0x1D	0x1D
CARKIT_INT_EN_SET	RW	8	0x00	0x1E	0x1E
CARKIT_INT_EN_CLR	RW	8	0x00	0x1F	0x1F
CARKIT_INT_STS	RO	8	0x00	0x20	0x20
CARKIT_INT_LATCH	RO	8	0x00	0x21	0x21
TRANS_POS_WIDTH	RW	8	0x1B	0x25	0x25
TRANS_NEG_WIDTH	RW	8	0x0C	0x26	0x26
OTHER_FUNC_CTRL	RW	8	0x00	0x80	0x80
OTHER_FUNC_CTRL_SET	RW	8	0x00	0x81	0x81
OTHER_FUNC_CTRL_CLR	RW	8	0x00	0x82	0x82
OTHER_IFC_CTRL	RW	8	0x80	0x83	0x83
OTHER_IFC_CTRL_SET	RW	8	0x80	0x84	0x84
OTHER_IFC_CTRL_CLR	RW	8	0x80	0x85	0x85
OTHER_INT_EN_RISE	RW	8	0x00	0x86	0x86
OTHER_INT_EN_RISE_SET	RW	8	0x00	0x87	0x87
OTHER_INT_EN_RISE_CLR	RW	8	0x00	0x88	0x88
OTHER_INT_EN_FALL	RW	8	0x00	0x89	0x89
OTHER_INT_EN_FALL_SET	RW	8	0x00	0x8A	0x8A
OTHER_INT_EN_FALL_CLR	RW	8	0x00	0x8B	0x8B
OTHER_INT_STS	RO	8	0x00	0x8C	0x8C
OTHER_INT_LATCH	RO	8	0x00	0x8D	0x8D
ID_INT_EN_RISE	RW	8	0x00	0x8E	0x8E
ID_INT_EN_RISE_SET	RW	8	0x00	0x8F	0x8F
ID_INT_EN_RISE_CLR	RW	8	0x00	0x90	0x90
ID_INT_EN_FALL	RW	8	0x00	0x91	0x91
ID_INT_EN_FALL_SET	RW	8	0x00	0x92	0x92
ID_INT_EN_FALL_CLR	RW	8	0x00	0x93	0x93
ID_INT_STS	RO	8	0x00	0x94	0x94

Table 3. USB Register Summary (continued)

Register Name	Type	Register Width (Bits)	Register Reset	Address Offset	Physical Address
ID_INT_LATCH	RO	8	0x00	0x95	0x95
ID_STATUS	RO	8	0x00	0x96	0x96
POWER_CTRL	RW	8	0x00	0xAC	0xAC
POWER_CTRL_SET	RW	8	0x00	0xAD	0xAD
POWER_CTRL_CLR	RW	8	0x00	0xAE	0xAE
OTHER_IFC_CTRL2	RW	8	0x00	0xAF	0xAF
OTHER_IFC_CTRL2_SET	RW	8	0x00	0xB0	0xB0
OTHER_IFC_CTRL2_CLR	RW	8	0x00	0xB1	0xB1
REG_CTRL_EN	RW	8	0x00	0xB2	0xB2
REG_CTRL_EN_SET	RW	8	0x00	0xB3	0xB3
REG_CTRL_EN_CLR	RW	8	0x00	0xB4	0xB4
REG_CTRL_ERROR	RO	8	0x00	0xB5	0xB5
OTHER_FUNC_CTRL2	RW	8	0x04	0xB8	0xB8
OTHER_FUNC_CTRL2_SET	RW	8	0x04	0xB9	0xB9
OTHER_FUNC_CTRL2_CLR	RW	8	0x04	0xBA	0xBA
VBUS_DEBOUNCE	RW	8	0x1F	0xC0	0xC0
ID_DEBOUNCE	RW	8	0x34	0xC1	0xC1
VBAT_TIMER	RW	8	0x06	0xD3	0xD3
PHY_PWR_CTRL	RW	8	0x00	0xFD	0xFD
PHY_CLK_CTRL	RW	8	0x02	0xFE	0xFE
PHY_CLK_CTRL_STS	RO	8	0x00	0xFF	0xFF

2.3 USB Register Descriptions

Table 4. VENDOR_ID_LO

I2C Address	0x48		
Physical Address	0x00	**Instance**	USB
Description	Lower byte of vendor ID supplied by USB-IF (Texas-Instruments Vendor ID = 0x0451)		
Type	RO		

7	6	5	4	3	2	1	0
VENDOR_ID							

Bits	Field Name	Description	Type	Reset
7:0	VENDOR_ID		RO	0x51

Table 5. VENDOR_ID_HI

I2C Address	0x48		
Physical Address	0x01	**Instance**	USB
Description	Upper byte of Vendor ID supplied by USB-IF (Texas-Instruments Vendor ID = 0x0451).		
Type	RO		

7	6	5	4	3	2	1	0
VENDOR_ID							

Bits	Field Name	Description	Type	Reset
7:0	VENDOR_ID		RO	0x04

Table 6. PRODUCT_ID_LO

I2C Address	0x48		
Physical Address	0x02	**Instance**	USB
Description	Lower byte of Product ID supplied by Vendor (TWL4030 Product ID is 0xC002).		
Type	RO		

7	6	5	4	3	2	1	0
PRODUCT_ID							

Bits	Field Name	Description	Type	Reset
7:0	PRODUCT_ID		RO	0x02

Table 7. PRODUCT_ID_HI

I2C Address	0x48		
Physical Address	0x03	**Instance**	USB
Description	Upper byte of Product ID supplied by Vendor (TWL4030 Product ID is 0xC002).		
Type	RO		

7	6	5	4	3	2	1	0
PRODUCT_ID							

Bits	Field Name	Description	Type	Reset
7:0	PRODUCT_ID		RO	0xC0

Table 8. FUNC_CTRL

I2C Address	0x48		
Physical Address	0x04	**Instance**	USB
Description	Controls UTMI function settings of the PHY.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	SUSPENDM	RESET	OPMODE		TERMSELECT	XCVRSELECT	

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	SUSPENDM	Active low PHY suspend. Put PHY into low-power mode. In low-power mode the PHY powers down all blocks except the full speed receiver, OTG comparators, and the ULPI interface pins. The PHY automatically set this bit to 1 when low-power mode is exited.	RW	1
5	RESET	Active high transceiver reset. Does not reset the ULPI interface or ULPI register set.Once set, the PHY asserts the DIR signal and reset the UTMI core. When the reset is completed, the PHY de-asserts DIR and clears this bit. After de-asserting DIR, the PHY re-assert DIR and send an RX command update.Note: This bit is auto-cleared, this explain why it can't be read at 1.	RW	0
4:3	OPMODE	Select the required bit encoding style during transmit 0x0: Normal operation 0x1: Non-driving 0x2: Disable bit-stuff and NRZI encoding 0x3: Reserved	RW	0x0
2	TERMSELECT	Controls the internal 1.5Kohms pull-up resistor and 45ohms HS terminations. Control over bus resistors changes depending on XcvrSelect, OpMode, DpPulldown and DmPulldown.	RW	0
1:0	XCVRSELECT	Select the required transceiver speed. 0x0: Enable HS transceiver 0x1: Enable FS transceiver 0x2: Enable LS transceiver 0x3: Enable FS transceiver for LS packets(FS preamble is automatically pre-pended)	RW	0x1

Table 9. FUNC_CTRL_SET

I2C Address	0x48		
Physical Address	0x05	**Instance**	USB
Description	This register doesn't physically exist. It is the same as the func_ctrl register with read/set-only property (write 1 to set a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	SUSPENDM	RESET	OPMODE		TERMSELECT	XCVRSELECT	

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	SUSPENDM		RW	1
5	RESET		RW	0
4:3	OPMODE		RW	0x0
2	TERMSELECT		RW	0
1:0	XCVRSELECT		RW	0x1

Table 10. FUNC_CTRL_CLR

I2C Address	0x48		
Physical Address	0x06	**Instance**	USB
Description	This register doesn't physically exist. It is the same as the func_ctrl register with read/clear-only property (write 1 to clear a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	SUSPENDM	RESET	OPMODE		TERMSELECT	XCVRSELECT	

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	SUSPENDM		RW	1
5	RESET		RW	0
4:3	OPMODE		RW	0x0
2	TERMSELECT		RW	0
1:0	XCVRSELECT		RW	0x1

Table 11. IFC_CTRL

I2C Address	0x48		
Physical Address	0x07	**Instance**	USB
Description	Enables alternative interfaces and PHY features.		
Type	RW		

7	6	5	4	3	2	1	0
INTERFACE_PROTECT_DISABLE	RESERVED	RESERVED	AUTORESUME	CLOCKSUSPENDM	CARKITMODE	FSLSSERIALMODE_3PIN	RESERVED

Bits	Field Name	Description	Type	Reset
7	INTERFACE_PROTECT_DISABLE	Controls circuitry built into the PHY for protecting the ULPI interface when the link tri-states stp and data.0b: Enables the interface protect circuit1b: Disables the interface protect circuit	RW	0
6	Reserved		RO	0
5	Reserved		RO	0
4	AUTORESUME	Enables the PHY to automatically transmit resume signaling.Refer to USB specification 7.1.7.7 and 7.9 for more details. 0 = AutoResume disabled1 = AutoResume enabled (default)	RW	1
3	CLOCKSUSPENDM	Active low clock suspend. Valid only in Serial Modes. Powers down the internal clock circuitry only. Valid only when SuspendM = 1b. The PHY must ignore ClockSuspend when SuspendM = 0b. By default, the clock will not be powered in Serial and Carkit Modes.0b: Clock will not be powered in Serial and Carkit Modes.1b: Clock will be powered in Serial and Carkit Modes.Note: By default the clock will not be powered down in serial or carkit mode.	RW	1
2	CARKITMODE	Changes the ULPI interface to carkit interface. The PHY automatically clear this field when carkit mode is exited. 0b: Carkit disabled.1b: Enable serial carkit mode.	RW	0
1	FSLSSERIALMODE_3PIN	Changes the ULPI interface to 3-pin Serial Mode using DAT/SE0 encoding . Alternatively, changes the ULPI interface to 4-pin Serial Mode using VP/VM encoding if theFsLsSerialMode_4pin bit in the Other_Interface_Control register is also set.The PHY automatically clear this field when serial mode is exited. 0b: FS/LS packets are sent using the parallel interface1b: FS/LS packets are sent using the serial interface	RW	0
0	Reserved		RO	0

Table 12. IFC_CTRL_SET

I2C Address	0x48		
Physical Address	0x08	**Instance**	USB
Description	This register doesn't physically exist. It is the same as the ifc_ctrl register with read/set-only property (write 1 to set a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
INTERFACE_PROTECT_DISABLE	RESERVED	RESERVED	AUTORESUME	CLOCKSUSPENDM	CARKITMODE	FSLSSERIALMODE_3PIN	RESERVED

Bits	Field Name	Description	Type	Reset
7	INTERFACE_PROTECT_DISABLE		RW	0
6	Reserved		RO	0
5	Reserved		RO	0
4	AUTORESUME		RW	1
3	CLOCKSUSPENDM		RW	1
2	CARKITMODE		RW	0
1	FSLSSERIALMODE_3PIN		RW	0
0	Reserved		RO	0

Table 13. IFC_CTRL_CLR

I2C Address	0x48		
Physical Address	0x09	**Instance**	USB
Description	This register doesn't physically exist. It is the same as the ifc_ctrl register with read/clear-only property (write 1 to clear a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
INTERFACE_PROTECT_DISABLE	RESERVED	RESERVED	AUTORESUME	CLOCKSUSPENDM	CARKITMODE	FSLSSERIALMODE_3PIN	RESERVED

Bits	Field Name	Description	Type	Reset
7	INTERFACE_PROTECT_DISABLE		RW	0
6	Reserved		RO	0
5	Reserved		RO	0
4	AUTORESUME		RW	1
3	CLOCKSUSPENDM		RW	1
2	CARKITMODE		RW	0
1	FSLSSERIALMODE_3PIN		RW	0
0	Reserved		RO	0

Table 14. OTG_CTRL

I2C Address	0x48						
Physical Address	0x0A	**Instance**	USB				
Description	Controls UTMI+ OTG functions of the PHY.						
Type	RW						

7	6	5	4	3	2	1	0
RESERVED	RESERVED	DRVVBUS	CHRGVBUS	DISCHRGVBUS	DMPULLDOWN	DPPULLDOWN	IDPULLUP

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	DRVVBUS	Signals the internal charge pump to drive 5V on VBUS. 0b: do not drive VBUS1b: drive 5V on VBUS	RW	0
4	CHRGVBUS	Charge VBUS through a resistor. Used for VBUS pulsing SRP. The Link must first check that VBUS has been discharged (see DischrgVbus register bit), and that both D+ and D- data lines have been low (SE0) for 2 ms. 0b: do not charge VBUS. 1b: charge VBUS	RW	0
3	DISCHRGVBUS	Discharge VBUS through a resistor. If the Link sets this bit to 1, it waits for an RX CMD indicating SessEnd has transitioned from 0 to 1, and then resets this bit to 0 to stop the discharge. 0b: do not discharge VBUS1b : discharge VBUS	RW	0
2	DMPULLDOWN	Enables the 15-kΩ pull-down resistor on D-. 0b: Pull-down resistor not connected to D-. 1b: Pull-down resistor connected to D-.	RW	1
1	DPPULLDOWN	Enables the 15-kΩ pull-down resistor on D+. 0b: Pull-down resistor not connected to D+. 1b: Pull-down resistor connected to D+.	RW	1
0	IDPULLUP	Connects a pull-up to the ID line and enables sampling of the signal level. 0b: Disable sampling of ID line. 1b: Enable sampling of ID line.	RW	0

Table 15. OTG_CTRL_SET

I2C Address	0x48		
Physical Address	0x0B	**Instance**	USB
Description	This register doesn't physically exist. It is the same as the otg_ctrl register with read/set-only property (write 1 to set a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	DRVVBUS	CHRGVBUS	DISCHRGVBUS	DMPULLDOWN	DPPULLDOWN	IDPULLUP

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	DRVVBUS		RW	0
4	CHRGVBUS		RW	0
3	DISCHRGVBUS		RW	0
2	DMPULLDOWN		RW	1
1	DPPULLDOWN		RW	1
0	IDPULLUP		RW	0

Table 16. OTG_CTRL_CLR

I2C Address	0x48		
Physical Address	0x0C	**Instance**	USB
Description	This register doesn't physically exist. It is the same as the otg_ctrl register with read/Clear-only property (write 1 to clear a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	DRVVBUS	CHRGVBUS	DISCHRGVBUS	DMPULLDOWN	DPPULLDOWN	IDPULLUP

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	DRVVBUS		RW	0
4	CHRGVBUS		RW	0
3	DISCHRGVBUS		RW	0
2	DMPULLDOWN		RW	1
1	DPPULLDOWN		RW	1
0	IDPULLUP		RW	0

Table 17. USB_INT_EN_RISE

I2C Address	0x48		
Physical Address	0x0D	**Instance**	USB
Description	If set, the bits in this register cause an interrupt event notification to be generated when the corresponding PHY signal changes from low to high. By default, all transitions are enabled.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	IDGND_RISE	SESSEND_RISE	SESSVALID_RISE	VBUSVALID_RISE	HOSTDISCONNECT_RISE

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	Reserved		RO	0
4	IDGND_RISE	Generate an interrupt event notification when IdGnd changes from low to high. Event is automatically masked if IdPullup bit is clear to 0 and for 50ms after IdPullup is set to 1.	RW	1
3	SESSEND_RISE	Generate an interrupt event notification when SessEnd changes from low to high.	RW	1
2	SESSVALID_RISE	Generate an interrupt event notification when SessValid changes from low to high. SessValid is the same as UTMI+ AValid.	RW	1
1	VBUSVALID_RISE	Generate an interrupt event notification when VbusValid changes from low to high.	RW	1
0	HOSTDISCONNECT_RISE	Generate an interrupt event notification when Hostdisconnect changes from low to high. Applicable only in host mode (DpPulldown and DmPulldown both set to 1b).	RW	1

Table 18. USB_INT_EN_RISE_SET

I2C Address	0x48		
Physical Address	0x0E	**Instance**	USB
Description	This register doesn't physically exist. It is the same as the usb_int_en_rise register with read/set-only property (write 1 to set a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	IDGND_RISE	SESSEND_RISE	SESSVALID_RISE	VBUSVALID_RISE	HOSTDISCONNECT_RISE

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	Reserved		RO	0
4	IDGND_RISE		RW	1
3	SESSEND_RISE		RW	1
2	SESSVALID_RISE		RW	1
1	VBUSVALID_RISE		RW	1
0	HOSTDISCONNECT_RISE		RW	1

Table 19. USB_INT_EN_RISE_CLR

I2C Address	0x48		
Physical Address	0x0F	**Instance**	USB
Description	This register doesn't physically exist. It is the same as the usb_int_en_rise register with read/clear-only property (write 1 to clear a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	IDGND_RISE	SESSEND_RISE	SESSVALID_RISE	VBUSVALID_RISE	HOSTDISCONNECT_RISE

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	Reserved		RO	0
4	IDGND_RISE		RW	1
3	SESSEND_RISE		RW	1
2	SESSVALID_RISE		RW	1
1	VBUSVALID_RISE		RW	1
0	HOSTDISCONNECT_RISE		RW	1

Table 20. USB_INT_EN_FALL

I2C Address	0x48		
Physical Address	0x10	**Instance**	USB
Description	If set, the bits in this register cause an interrupt event notification to be generated when the corresponding PHY signal changes from low to high. By default, all transitions are enabled.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	IDGND_FALL	SESSEND_FALL	SESSVALID_FALL	VBUSVALID_FALL	HOSTDISCONNECT_FALL

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	Reserved		RO	0
4	IDGND_FALL	Generate an interrupt event notification when IdGnd changes from high to low.Event is automatically masked if IdPullup bit is clear to 0 and for 50 ms after IdPullup is set to 1.	RW	1
3	SESSEND_FALL	Generate an interrupt event notification when SessEnd changes from high to low.	RW	1
2	SESSVALID_FALL	Generate an interrupt event notification when SessValid changes from high to low. SessValid is the same as UTMI+ AValid.	RW	1
1	VBUSVALID_FALL	Generate an interrupt event notification when VbusValid changes from high to low.	RW	1
0	HOSTDISCONNECT_FALL	Generate an interrupt event notification when Hostdisconnect changes from high to low. Applicable only in host mode (DpPulldown and DmPulldown both set to 1b).	RW	1

Table 21. USB_INT_EN_FALL_SET

I2C Address	0x48		
Physical Address	0x11	**Instance**	USB
Description	This register doesn't physically exist. It is the same as the usb_int_en_fall register with read/set-only property (write 1 to set a particular bit, a write 0 has no-action)		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	IDGND_FALL	SESSEND_FALL	SESSVALID_FALL	VBUSVALID_FALL	HOSTDISCONNECT_FALL

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	Reserved		RO	0
4	IDGND_FALL		RW	1
3	SESSEND_FALL		RW	1
2	SESSVALID_FALL		RW	1
1	VBUSVALID_FALL		RW	1
0	HOSTDISCONNECT_FALL		RW	1

Table 22. USB_INT_EN_FALL_CLR

I2C Address	0x48		
Physical Address	0x12	**Instance**	USB
Description	This register doesn't physically exist. It is the same as the usb_int_en_fall register with read/clear-only property (write 1 to clear a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	IDGND_FALL	SESSEND_FALL	SESSVALID_FALL	VBUSVALID_FALL	HOSTDISCONNECT_FALL

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	Reserved		RO	0
4	IDGND_FALL		RW	1
3	SESSEND_FALL		RW	1
2	SESSVALID_FALL		RW	1
1	VBUSVALID_FALL		RW	1
0	HOSTDISCONNECT_FALL		RW	1

Table 23. USB_INT_STS

I2C Address	0x48		
Physical Address	0x13	**Instance**	USB
Description	Indicates the current value of the interrupt source signal.		
Type	RO		

7	6	5	4	3	2	1	0
RESERVED			IDGND	SESSEND	SESSVALID	VBUSVALID	HOSTDISCONNECT

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4	IDGND	Current value of UTMI+ IdGnd output. This bit is not updated if IdPullup bit is reset to 0 and for 50 ms after IdPullup is set to 1.	RO	0
3	SESSEND	Current value of UTMI+ SessEnd output.	RO	0
2	SESSVALID	Current value of UTMI+ SessValid output. SessValid is the same as UTMI+ AValid.	RO	0
1	VBUSVALID	Current value of UTMI+ VbusValid output.	RO	0
0	HOSTDISCONNECT	Current value of UTMI+ Hostdisconnect output. Applicable only in host mode. Automatically reset to 0 when low-power mode is entered. NOTE: Reset value is 0 when host is connected. Reset value is 1 when host is disconnected.	RO	1

Table 24. USB_INT_LATCH

I2C Address	0x48		
Physical Address	0x14	**Instance**	USB
Description	These bits are set by the PHY when an unmasked change occurs on the corresponding internal signal. The PHY will automatically clear all bits when the Link reads this register, or when low-power mode is entered. The PHY also clears this register when Serial Mode or Carkit Mode is entered regardless of the value of ClockSuspendM. The PHY follows the rules defined in Table 26 of the ULPI spec for setting any latch register bit. It is important to note that if register read data is returned to the Link in the same cycle that a USB Interrupt Latch bit is to be set, the interrupt condition is given immediately in the register read data and the Latch bit is not set. Note that it is optional for the Link to read the USB Interrupt Latch register in Synchronous Mode because the RX CMD byte already indicates the interrupt source directly.		
Type	RO		

7	6	5	4	3	2	1	0
RESERVED			IDGND_LATCH	SESSEND_LATCH	SESSVALID_LATCH	VBUSVALID_LATCH	HOSTDISCONNECT_LATCH

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4	IDGND_LATCH	Set to 1 by the PHY when an unmasked event occurs on IdGnd. Cleared when this register is read.	RO	0
3	SESSEND_LATCH	Set to 1 by the PHY when an unmasked event occurs on SessEnd. Cleared when this register is read.	RO	0
2	SESSVALID_LATCH	Set to 1 by the PHY when an unmasked event occurs on SessValid. Cleared when this register is read. SessValid is the same as UTMI+ AValid.	RO	0
1	VBUSVALID_LATCH	Set to 1 by the PHY when an unmasked event occurs on VbusValid. Cleared when this register is read.	RO	0
0	HOSTDISCONNECT_LATCH	Set to 1 by the PHY when an unmasked event occurs on Hostdisconnect. Cleared when this register is read. Applicable only in host mode. NOTE: As this IT is enabled by default, the reset value depends on the host status Reset value is 0 when host is connected. Reset value is 1 when host is disconnected.	RO	1

Table 25. DEBUG

I2C Address	0x48		
Physical Address	0x15	**Instance**	USB
Description	Indicates the current value of various signals useful for debugging.		
Type	RO		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	LINESTATE	

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	Reserved		RO	0
4	Reserved		RO	0
3	Reserved		RO	0
2	Reserved		RO	0
1:0	LINESTATE	These signals reflect the current state of the single ended receivers. They directly reflect the current state of the DP (LineState[0]) and DM (LineState[1]) signals. Read 0x0: SE0 (LS/FS), Squelch (HS/Chirp) Read 0x1: LS: 'K' State, FS: 'J' State, HS: !Squelch, Chirp: !Squelch & HS_Differential_Receiver_Output Read 0x2: LS: 'J' State, FS: 'K' State, HS: Invalid, Chirp: !Squelch & !HS_Differential_Receiver_Output Read 0x3: SE1 (LS/FS), Invalid (HS/Chirp)	RO	0x0

Table 26. SCRATCH_REG

I2C Address	0x48		
Physical Address	0x16	**Instance**	USB
Description	Empty register byte for testing purposes. Software can read, write, set, and clear this register and the PHY functionality will not be affected.		
Type	RW		

7	6	5	4	3	2	1	0
SCRATCH							

Bits	Field Name	Description	Type	Reset
7:0	SCRATCH	Scratch data.	RW	0x00

Table 27. SCRATCH_REG_SET

I2C Address	0x48		
Physical Address	0x17	**Instance**	USB
Description	This register doesn't physically exist. It is the same as the scratch_reg register with read/set-only property (write 1 to set a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
SCRATCH							

Bits	Field Name	Description	Type	Reset
7:0	SCRATCH		RW	0x00

Table 28. SCRATCH_REG_CLR

I2C Address	0x48		
Physical Address	0x18	**Instance**	USB
Description	This register doesn't physically exist. It is the same as the scratch_reg with read/clear-only property (write 1 to clear a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
SCRATCH							

Bits	Field Name	Description	Type	Reset
7:0	SCRATCH		RW	0x00

Table 29. CARKIT_CTRL

I2C Address	0x48		
Physical Address	0x19	**Instance**	USB
Description	Controls the operation of the carkit circuitry within the PHY. Only valid if CarkitMode in the Interface_Control register is set to 1.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	SPARE1			RXDEN	TXDEN	IDGNDDRV	SPARE

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6:4	SPARE1	SPARE REGISTER	RW	0x0
3	RXDEN	Routes RXD signal from D+ pin to DATA[1] pin.	RW	0
2	TXDEN	Routes TXD signal from DATA[0] pin onto D- pin.	RW	0
1	IDGNDDRV	Drives ID pin to ground.	RW	0
0	SPARE	SPARE REGISTER	RW	0

Table 30. CARKIT_CTRL_SET

I2C Address	0x48		
Physical Address	0x1A	**Instance**	USB
Description	This register doesn't physically exist. It is the same as the carkit_ctrl register with read/set-only property (write 1 to set a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	SPARE1			RXDEN	TXDEN	IDGNDDRV	SPARE

Bits	Field Name	Description	Type	Reset
7	RESERVED		RW	0
6:4	SPARE1	SPARE REGISTER	RW	0x0
3	RXDEN		RW	0
2	TXDEN		RW	0
1	IDGNDDRV		RW	0
0	SPARE	SPARE REGISTER	RW	0

Table 31. CARKIT_CTRL_CLR

I2C Address	0x48		
Physical Address	0x1B	**Instance**	USB
Description	This register doesn't physically exist. It is the same as the carkit_ctrl register with read/clear-only property (write 1 to clear a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	SPARE1			RXDEN	TXDEN	IDGNDDRV	SPARE

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6:4	SPARE1	SPARE REGISTER	RW	0
3	RXDEN		RW	0
2	TXDEN		RW	0
1	IDGNDDRV		RW	0
0	SPARE	SPARE REGISTER	RW	0

Table 32. CARKIT_INT_DELAY

I2C Address	0x48		
Physical Address	0x1C	**Instance**	USB
Description	SPARE REGISTER		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	SPARE						

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6:0	SPARE	SPARE REGISTER	RW	0x52

Table 33. CARKIT_INT_EN

I2C Address	0x48		
Physical Address	0x1D	**Instance**	USB
Description	If set, the bits in this register cause an interrupt event notification to be generated when the corresponding PHY signal changes.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED			SPARE			IDFLOAT_FALL_EN	IDFLOAT_RISE_EN

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4:2	SPARE	SPARE REGISTER	RW	0x0
1	IDFLOAT_FALL_EN	Generate an interrupt event notification when the ID pin changes from floating to not floating. The IdPullup bit in the OTG Control register must be set.	RW	0
0	IDFLOAT_RISE_EN	Generate an interrupt event notification when the ID pin changes from not floating to floating. The IdPullup bit in the OTG Control register must be set.	RW	0

Table 34. CARKIT_INT_EN_SET

I2C Address	0x48		
Physical Address	0x1E	**Instance**	USB
Description	This register doesn't physically exist. It is the same as the carkit_int_en register with read/set-only property (write 1 to set a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED			SPARE			IDFLOAT_FALL_EN	IDFLOAT_RISE_EN

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4:2	SPARE	SPARE REGISTER	RW	0x0
1	IDFLOAT_FALL_EN		RW	0
0	IDFLOAT_RISE_EN		RW	0

Table 35. CARKIT_INT_EN_CLR

I2C Address	0x48		
Physical Address	0x1F	**Instance**	USB
Description	This register doesn't physically exist. It is the same as the carkit_int_en register with read/clear-only property (write 1 to clear a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED			SPARE			IDFLOAT_FALL_EN	IDFLOAT_RISE_EN

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4:2	SPARE	SPARE REGISTER	RW	0x0
1	IDFLOAT_FALL_EN		RW	0
0	IDFLOAT_RISE_EN		RW	0

Table 36. CARKIT_INT_STS

I2C Address	0x48		
Physical Address	0x20	**Instance**	USB
Description	When a carkit interrupt event notification occurs, the link can read this register to determine which event triggered the interrupt.		
Type	RO		

7	6	5	4	3	2	1	0
RESERVED							IDFLOAT

Bits	Field Name	Description	Type	Reset
7:1	Reserved		RO	0x00
0	IDFLOAT	Asserted when the ID pin is floating.	RO	0

Table 37. CARKIT_INT_LATCH

I2C Address	0x48		
Physical Address	0x21	**Instance**	USB
Description	These bits are set by the PHY when an unmasked carkit event occurs. The PHY will automatically clear all bits when the Link reads this register, or when low-power mode is entered. It is important to note that if register read data is returned to the Link in the same cycle that a Carkit Interrupt Latch bit is to be set, the interrupt condition is given immediately in the register read data and the latch bit is not set.		
Type	RO		

7	6	5	4	3	2	1	0
RESERVED							IDFLOAT_LATCH

Bits	Field Name	Description	Type	Reset
7:1	Reserved		RO	0x00
0	IDFLOAT_LATCH	Asserted if the IdFloat Rise bit in the Carkit Interrupt Enable register is set, and the ID line changes from not floating to floating. Also asserted if the IdFloat Fall bit in the Carkit Interrupt Enable register is set, and the ID line changes from floating to not floating.	RO	0

Table 38. TRANS_POS_WIDTH

I2C Address	0x48		
Physical Address	0x25	**Instance**	USB
Description	SPARE REGISTER		
Type	RW		

7	6	5	4	3	2	1	0
SPARE							

Bits	Field Name	Description	Type	Reset
7:0	SPARE	SPARE REGISTER	RW	0x1B

Table 39. TRANS_NEG_WIDTH

I2C Address	0x48		
Physical Address	0x26	**Instance**	USB
Description	SPARE REGISTER		
Type	RW		

7	6	5	4	3	2	1	0
SPARE							

Bits	Field Name	Description	Type	Reset
7:0	SPARE	SPARE REGISTER	RW	0x0C

Table 40. OTHER_FUNC_CTRL

I2C Address	0x48		
Physical Address	0x80	**Instance**	USB
Description	Provides additional control for carkit support.		
Type	RW		

7	6	5	4	3	2	1	0
SPARE		RESERVED2	BDIS_ACON_EN	RESERVED1	SPARE1	RESERVED	

Bits	Field Name	Description	Type	Reset
7:6	SPARE	SPARE REGISTER	RW	0x0
5	RESERVED2		RO	0
4	BDIS_ACON_EN	Enables A-device to connect if B-device disconnect detected. Conditions: detect a continuous SE0 on the line for > 2.5 µs. A USB reset from the A-device is ignored. 0b: No-action 1b: Automatically asserts a pull-up on D+ to connect after B-device disconnect.	RW	0
3	RESERVED1		RO	0
2	SPARE1	SPARE REGISTER	RW	0
1:0	RESERVED		RO	0x0

Table 41. OTHER_FUNC_CTRL_SET

I2C Address	0x48		
Physical Address	0x81	**Instance**	USB
Description	This register doesn't physically exist. It is the same as the other_func_ctrl register with read/set-only property (write 1 to set a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED		RESERVED	BDIS_ACON_EN	RESERVED	SPARE1	RESERVED	

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RW	0x0
5	Reserved		RORreturns0s	0
4	BDIS_ACON_EN		RW	0
3	Reserved		RO	0
2	SPARE1	SPARE REGISTER	RW	0
1:0	Reserved		RO	0x0

Table 42. OTHER_FUNC_CTRL_CLR

I2C Address	0x48		
Physical Address	0x82	**Instance**	USB
Description	This register doesn't physically exist. It is the same as the other_func_ctrl register with read/clear-only property (write 1 to clear a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
SPARE		RESERVED	BDIS_ACON_EN	RESERVED	SPARE1	RESERVED	

Bits	Field Name	Description	Type	Reset
7:6	SPARE	SPARE REGISTER	RW	0x0
5	Reserved		RORreturns0s	0
4	BDIS_ACON_EN		RW	0
3	Reserved		RO	0
2	SPARE1		RW	0
1:0	Reserved		RO	0x0

Table 43. OTHER_IFC_CTRL

I2C Address	0x48		
Physical Address	0x83	**Instance**	USB
Description	This register is used to re-route the module interrupts to TWL4030 instead to ULPI and to optionnaly tristate the ULPI I/F.It can be access only via I2C.		
Type	RW		

7	6	5	4	3	2	1	0
DATAPOLARITY	OE_INT_EN	CEA2011_MODE	FSLSSERIALMODE_4PIN	HIZ_ULPI_60MHZ_OUT	HIZ_ULPI	SPARE	ALT_INT_REROUTE

Bits	Field Name	Description	Type	Reset
7	DATAPOLARITY	Control data polarity on dp/dm	RW	1
6	OE_INT_EN	oe_int_en enable	RW	0
5	CEA2011_MODE	Compatibility mode with legacy with USB FS/UART interconnect based on CEA-2011 specification. 0b: ULPI mode 1b: CEA-2011 mode	RW	0
4	FSLSSERIALMODE_4PIN	Modify the behavior of the 3pin_FsLsSerialMode bit in the Interface_Control register. 0b: No action 1b: Use VP/VM encoding instead of DAT/SE0.	RW	0
3	HIZ_ULPI_60MHZ_OUT	Tristate 11-pin of the ULPI interface. The clock pin output a 60-MHz clock. 0b: Normal operation 1b: Output 60-MHz clock + Hiz the other 11 ULPI pins	RW	0
2	HIZ_ULPI	Tristate the 12-pin of the ULPI interface including the clock pin. 0b: Normal operation 1b: Hiz the 12-pin ULPI bus	RW	0
1	SPARE	SPARE REGISTER	RW	0
0	ALT_INT_REROUTE	Routes interrupt as a TWL4030 interrupt instead of using an ULPI RX command (alt_int bit remains unasserted if any other RX command are sent by the PHY). 0b: Interrupts are signaled using a RX command (ULPI) with alt_int bit set. 1b: Interrupts are signaled as a TWL4030 interrupt.	RW	0

Table 44. OTHER_IFC_CTRL_SET

I2C Address	0x48		
Physical Address	0x84	**Instance**	USB
Description	This register doesn't physically exist. It is the same as the other_ifc_ctrl register with read/set-only property (write 1 to set a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
DATAPOLARITY	OE_INT_EN	CEA2011_MODE	FSLSSERIALMODE_4PIN	HIZ_ULPI_60MHZ_OUT	HIZ_ULPI	SPARE	ALT_INT_REROUTE

Bits	Field Name	Description	Type	Reset
7	DATAPOLARITY		RW	1
6	OE_INT_EN		RW	0
5	CEA2011_MODE		RW	0
4	FSLSSERIALMODE_4PIN		RW	0
3	HIZ_ULPI_60MHZ_OUT		RW	0
2	HIZ_ULPI		RW	0
1	SPARE	SPARE REGISTER	RW	0
0	ALT_INT_REROUTE		RW	0

Table 45. OTHER_IFC_CTRL_CLR

I2C Address	0x48		
Physical Address	0x85	**Instance**	USB
Description	This register doesn't physically exist. It is the same as the other_ifc_ctrl register with read/clear-only property (write 1 to clear a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
DATAPOLARITY	OE_INT_EN	CEA2011_MODE	FSLSSERIALMODE_4PIN	HIZ_ULPI_60MHZ_OUT	HIZ_ULPI	SPARE	ALT_INT_REROUTE

Bits	Field Name	Description	Type	Reset
7	DATAPOLARITY		RW	1
6	OE_INT_EN		RW	0
5	CEA2011_MODE		RW	0
4	FSLSSERIALMODE_4PIN		RW	0
3	HIZ_ULPI_60MHZ_OUT		RW	0
2	HIZ_ULPI		RW	0
1	SPARE	SPARE REGISTER	RW	0
0	ALT_INT_REROUTE		RW	0

Table 46. OTHER_INT_EN_RISE

I2C Address	0x48		
Physical Address	0x86	**Instance**	USB
Description	If set, the bits in this register cause an interrupt event notification to be generated when the corresponding PHY signal changes.		
Type	RW		

7	6	5	4	3	2	1	0
VB_SESS_VLD_RISE_EN	DM_HI_RISE_EN	DP_HI_RISE_EN	RESERVED	BDIS_ACON_RISE_EN	RESERVED	SPARE	ABNORMAL_STRESS_RISE_EN

Bits	Field Name	Description	Type	Reset
7	VB_SESS_VLD_RISE_EN	If this bit is set, it generates an interrupt event notification when the VB_SESS_VLD pin changes from low to high.	RW	0
6	DM_HI_RISE_EN	If this bit is set, it generates an interrupt event notification when the DM_HI pin changes from low to high.	RW	0
5	DP_HI_RISE_EN	If this bit is set, it generates an interrupt event notification when the DP_HI pin changes from low to high.	RW	0
4	Reserved		RO	0
3	BDIS_ACON_RISE_EN	If this bit is set, it generates an interrupt event notification when pull-up is automaticaly asserted on D+ after B Device disconnect.	RW	0
2	Reserved		RO	0
1	SPARE	SPARE REGISTER	RW	0
0	ABNORMAL_STRESS_RISE_EN	If this bit is set, it generates an interrupt event notification if the stress protection circuit has been activated.	RW	0

Table 47. OTHER_INT_EN_RISE_SET

I2C Address	0x48		
Physical Address	0x87	**Instance**	USB
Description	This register doesn't physically exist. It is the same as the other_int_en_rise register with read/set-only property (write 1 to set a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
VB_SESS_VLD_RISE_EN	DM_HI_RISE_EN	DP_HI_RISE_EN	RESERVED	BDIS_ACON_RISE_EN	RESERVED	SPARE	ABNORMAL_STRESS_RISE_EN

Bits	Field Name	Description	Type	Reset
7	VB_SESS_VLD_RISE_EN		RW	0
6	DM_HI_RISE_EN		RW	0
5	DP_HI_RISE_EN		RW	0
4	Reserved		RO	0
3	BDIS_ACON_RISE_EN		RW	0
2	Reserved		RO	0
1	SPARE	SPARE REGISTER	RW	0
0	ABNORMAL_STRESS_RISE_EN		RW	0

Table 48. OTHER_INT_EN_RISE_CLR

I2C Address	0x48		
Physical Address	0x88	**Instance**	USB
Description	This register doesn't physically exist. It is the same as the other_int_en_rise register with read/clear-only property (write 1 to clear a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
VB_SESS_VLD_RISE_EN	DM_HI_RISE_EN	DP_HI_RISE_EN	RESERVED	BDIS_ACON_RISE_EN	RESERVED	SPARE	ABNORMAL_STRESS_RISE_EN

Bits	Field Name	Description	Type	Reset
7	VB_SESS_VLD_RISE_EN		RW	0
6	DM_HI_RISE_EN		RW	0
5	DP_HI_RISE_EN		RW	0
4	Reserved		RO	0
3	BDIS_ACON_RISE_EN		RW	0
2	Reserved		RO	0
1	SPARE	SPARE REGISTER	RW	0
0	ABNORMAL_STRESS_RISE_EN		RW	0

Table 49. OTHER_INT_EN_FALL

I2C Address	0x48		
Physical Address	0x89	**Instance**	USB
Description	If set, the bits in this register cause an interrupt event notification to be generated when the corresponding PHY signal changes.		
Type	RW		

7	6	5	4	3	2	1	0
VB_SESS_VLD_FALL_EN	DM_HI_FALL_EN	DP_HI_FALL_EN	RESERVED	RESERVED	RESERVED	SPARE	ABNORMAL_STRESS_FALL_EN

Bits	Field Name	Description	Type	Reset
7	VB_SESS_VLD_FALL_EN	If this bit is set, it generates an interrupt event notification when the VB_SESS_VLD pin changes from low to high.	RW	0
6	DM_HI_FALL_EN	If this bit is set, it generates an interrupt event notification when the DM_HI pin changes from low to high.	RW	0
5	DP_HI_FALL_EN	If this bit is set, it generates an interrupt event notification when the DP_HI pin changes from low to high.	RW	0
4	Reserved		RO	0
3	Reserved		RO	0
2	Reserved		RO	0
1	SPARE	SPARE REGISTER	RW	0
0	ABNORMAL_STRESS_FALL_EN	If this bit is set, it generates an interrupt event notification if the stress protection circuit has been activated.	RW	0

Table 50. OTHER_INT_EN_FALL_SET

I2C Address	0x48		
Physical Address	0x8A	**Instance**	USB
Description	This register doesn't physically exist. It is the same as the other_int_en_fall register with read/set-only property (write 1 to set a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
VB_SESS_VLD_FALL_EN	DM_HI_FALL_EN	DP_HI_FALL_EN	RESERVED	RESERVED	RESERVED	SPARE	ABNORMAL_STRESS_FALL_EN

Bits	Field Name	Description	Type	Reset
7	VB_SESS_VLD_FALL_EN		RW	0
6	DM_HI_FALL_EN		RW	0
5	DP_HI_FALL_EN		RW	0
4	Reserved		RO	0
3	Reserved		RO	0
2	Reserved		RO	0
1	SPARE	SPARE REGISTER	RW	0
0	ABNORMAL_STRESS_FALL_EN		RW	0

Table 51. OTHER_INT_EN_FALL_CLR

I2C Address	0x48		
Physical Address	0x8B	**Instance**	USB
Description	This register doesn't physically exist. It is the same as the other_int_en_fall register with read/clear-only property (write 1 to clear a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
VB_SESS_VLD_FALL_EN	DM_HI_FALL_EN	DP_HI_FALL_EN	RESERVED	RESERVED	RESERVED	SPARE	ABNORMAL_STRESS_FALL_EN

Bits	Field Name	Description	Type	Reset
7	VB_SESS_VLD_FALL_EN		RW	0
6	DM_HI_FALL_EN		RW	0
5	DP_HI_FALL_EN		RW	0
4	Reserved		RO	0
3	Reserved		RO	0
2	Reserved		RO	0
1	SPARE	SPARE REGISTER	RW	0
0	ABNORMAL_STRESS_FALL_EN		RW	0

Table 52. OTHER_INT_STS

I2C Address	0x48		
Physical Address	0x8C	**Instance**	USB
Description	Indicates the current value of the interrupt source signal.		
Type	RO		

7	6	5	4	3	2	1	0
VB_SESS_VLD	DM_HI	DP_HI	RESERVED	BDIS_ACON	RESERVED	SPARE	ABNORMAL_STRESS

Bits	Field Name	Description	Type	Reset
7	VB_SESS_VLD	Same as VB_SESS_VLD pin	RO	0
6	DM_HI	Same as DM_HI pin	RO	0
5	DP_HI	Same as DP_HI pin	RO	0
4	Reserved		RO	0
3	BDIS_ACON	Asserted when the bdis_acon bit in the Other_Interrupt_Latch register is set.	RO	0
2	Reserved		RO	0
1	SPARE	SPARE REGISTER	RO	0
0	ABNORMAL_STRESS	An abnormal condition has caused the short withstand protection circuit to be activated. This may be the result of the attachement of a defective cable or a defective device.	RO	0

Table 53. OTHER_INT_LATCH

I2C Address	0x48		
Physical Address	0x8D	**Instance**	USB
Description	These bits are set by the PHY when an unmasked specific event occurs. The PHY will automatically clear all bits when the Link reads this register, or when low-power mode is entered. It is important to note that if register read data is returned to the Link in the same cycle that a Other_Interrupt_Latch bit is to be set, the interrupt condition is given immediately in the register read data and the latch bit is not set.		
Type	RO		

7	6	5	4	3	2	1	0
VB_SESS_VLD	DM_HI	DP_HI	RESERVED	BDIS_ACON	RESERVED	SPARE	ABNORMAL_STRESS_LATCH

Bits	Field Name	Description	Type	Reset
7	VB_SESS_VLD	Set once VB_SESS_VLD changes level and the event is unmasked.	RO	0
6	DM_HI	Set once DM_HI changes level and the event is unmasked.	RO	0
5	DP_HI	Set once DP_HI changes level and the event is unmasked.	RO	0
4	Reserved		RO	0
3	BDIS_ACON	Set once when bdis_acon_en is set, and transceiver asserts dp_pullup after detecting B-device disconnect.	RO	0
2	Reserved		RO	0
1	SPARE	SPARE REGISTER	RO	0
0	ABNORMAL_STRESS_LATCH	Asserted if the Abnormal_stress bit in the Other_Interrupt_Enable register is set, and a stress conditions has been detected (ex: shorts).	RO	0

Table 54. ID_INT_EN_RISE

I2C Address	0x48		
Physical Address	0x8E	**Instance**	USB
Description	If set, the bits in this register cause an interrupt event notification to be generated when the corresponding PHY signal changes from low to high.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	ID_RES_FLOAT	RESERVED	RESERVED	RESERVED

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	Reserved		RO	0
4	Reserved		RO	0
3	ID_RES_FLOAT		RW	0
2	Reserved		RW	0
1	Reserved		RW	0
0	Reserved		RW	0

Table 55. ID_INT_EN_RISE_SET

I2C Address	0x48		
Physical Address	0x8F	**Instance**	USB
Description	This register doesn't physically exist. It is the same as the id_int_en_rise register with read/set-only property (write 1 to set a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	ID_RES_FLOAT	RESERVED	RESERVED	RESERVED

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	Reserved		RO	0
4	Reserved		RO	0
3	ID_RES_FLOAT		RW	0
2	Reserved		RW	0
1	Reserved		RW	0
0	Reserved		RW	0

Table 56. ID_INT_EN_RISE_CLR

I2C Address	0x48		
Physical Address	0x90	**Instance**	USB
Description	This register doesn't physically exist. It is the same as the id_int_en_rise register with read/clear-only property (write 1 to clear a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	ID_RES_FLOAT	RESERVED	RESERVED	RESERVED

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	Reserved		RO	0
4	Reserved		RO	0
3	ID_RES_FLOAT		RW	0
2	Reserved		RW	0
1	Reserved		RW	0
0	Reserved		RW	0

Table 57. ID_INT_EN_FALL

I2C Address	0x48		
Physical Address	0x91	**Instance**	USB
Description	If set, the bits in this register cause an interrupt event notification to be generated when the corresponding PHY signal changes from high to low.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	ID_RES_FLOAT	RESERVED	RESERVED	RESERVED

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	Reserved		RO	0
4	Reserved		RO	0
3	ID_RES_FLOAT		RW	0
2	Reserved		RW	0
1	Reserved		RW	0
0	Reserved		RW	0

Table 58. ID_INT_EN_FALL_SET

I2C Address	0x48		
Physical Address	0x92	**Instance**	USB
Description	This register doesn't physically exist. It is the same as the id_int_en_fall register with read/set-only property (write 1 to set a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	ID_RES_FLOAT	RESERVED	RESERVED	RESERVED

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	Reserved		RO	0
4	Reserved		RO	0
3	ID_RES_FLOAT		RW	0
2	Reserved		RW	0
1	Reserved		RW	0
0	Reserved		RW	0

Table 59. ID_INT_EN_FALL_CLR

I2C Address	0x48		
Physical Address	0x93	**Instance**	USB
Description	This register doesn't physically exist. It is the same as the id_int_en_fall register with read/clear-only property (write 1 to clear a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	ID_RES_FLOAT	RESERVED	RESERVED	RESERVED

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	Reserved		RO	0
4	Reserved		RO	0
3	ID_RES_FLOAT		RW	0
2	Reserved		RW	0
1	Reserved		RW	0
0	Reserved		RW	0

Table 60. ID_INT_STS

I2C Address	0x48		
Physical Address	0x94	**Instance**	USB
Description	Indicates the current value of the interrupt source signal.		
Type	RO		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	ID_RES_FLOAT	RESERVED	RESERVED	RESERVED

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	Reserved		RO	0
4	Reserved		RO	0
3	ID_RES_FLOAT	Same as ID_RES_FLOAT pin	RO	0
2	Reserved		RO	0
1	Reserved		RO	0
0	Reserved		RO	0

Table 61. ID_INT_LATCH

I2C Address	0x48		
Physical Address	0x95	**Instance**	USB
Description	These bits are set by the PHY when an unmasked specific event occurs. The PHY will automatically clear all bits when the Link reads this register, or when low-power mode is entered.		
Type	RO		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	ID_RES_FLOAT	RESERVED	RESERVED	RESERVED

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	Reserved		RO	0
4	Reserved		RO	0
3	ID_RES_FLOAT		RO	0
2	Reserved		RO	0
1	Reserved		RO	0
0	Reserved		RO	0

Table 62. ID_STATUS

I2C Address	0x48		
Physical Address	0x96	**Instance**	USB
Description	Indicates the resistor value connected on the ID pin.These bits will read as 0 while IdPullUp=0b in the OTG_Control register. The link shall wait at least 50ms after setting Idpullup to 1b before reading this register.		
Type	RO		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	ID_RES_FLOAT	RESERVED	RESERVED	RESERVED	ID_RES_GND

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	Reserved		RO	0
4	ID_RES_FLOAT	Set if there is the ID pin has no resistor to ground (open connection).	RO	0
3	Reserved		RO	0
2	Reserved		RO	0
1	Reserved		RO	0
0	ID_RES_GND	Set if the ID pin is grounded.	RO	0

Table 63. POWER_CTRL

I2C Address	0x48		
Physical Address	0xAC	**Instance**	USB
Description	Controlling OTG power section of the USB.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	OTG_EN	RESERVED	OTG_BIAS_VRUSB_EN	ID_RES_EN	VBUS_RES_EN	VBUS_BIAS_EN

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	OTG_EN	Enable complete OTG block (i.e., enable all OTG comparators, and reference circuitry in VRUSB_3V1 supply domain). It is recommended to set IDPULLUP (OTG_CTRL 0x0A) before enabling OTG_EN, to avoid extra consumption.	RW	0
4	Reserved		RO	0
3	OTG_BIAS_VRUSB_EN	Test-mode: When this bit is 1, and OTG_EN=0, enable the OTG biasing current mirror.	RW	0
2	ID_RES_EN	Test-mode: When this bit is 1, and OTG_EN=0, enable the OTG ID resistor string.	RW	0
1	VBUS_RES_EN	Test-mode: When this bit is 1, and OTG_EN=0, enable the OTG VBUS resistor string.	RW	0
0	VBUS_BIAS_EN	Test-mode: When this bit is 1, and OTG_EN=0, enable the OTG VRUSB_3V1 domain reference current mirror.	RW	0

Table 64. POWER_CTRL_SET

I2C Address	0x48		
Physical Address	0xAD	**Instance**	USB
Description	This register doesn't physically exist. It is the same as the power_ctrl register with read/set-only property (write 1 to set a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	OTG_EN	RESERVED	OTG_BIAS_VRUSB_EN	ID_RES_EN	VBUS_RES_EN	VBUS_BIAS_EN

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	OTG_EN		RW	0
4	Reserved		RO	0
3	OTG_BIAS_VRUSB_EN		RW	0
2	ID_RES_EN		RW	0
1	VBUS_RES_EN		RW	0
0	VBUS_BIAS_EN		RW	0

Table 65. POWER_CTRL_CLR

I2C Address	0x48		
Physical Address	0xAE	**Instance**	USB
Description	This register doesn't physically exist. It is the same as the power_ctrl register with read/clear-only property (write 1 to clear a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	OTG_EN	RESERVED	OTG_BIAS_VRUSB_EN	ID_RES_EN	VBUS_RES_EN	VBUS_BIAS_EN

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	OTG_EN		RW	0
4	Reserved		RO	0
3	OTG_BIAS_VRUSB_EN		RW	0
2	ID_RES_EN		RW	0
1	VBUS_RES_EN		RW	0
0	VBUS_BIAS_EN		RW	0

Table 66. OTHER_IFC_CTRL2

I2C Address	0x48		
Physical Address	0xAF	**Instance**	USB
Description	This register is used to control an optional ULPI serial mode and to re-route the interrupts.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	ULPI_STP_LOW	ULPI_TXEN_POL	ULPI_4PIN_2430	USB_INT_OUTSEL	

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	Reserved		RO	0
4	ULPI_STP_LOW	0b: ULPI state is controlled by OTHER_IFC_CTRL1b: Force low the STP input line when it is multiplexed with GPIO	RW	0
3	ULPI_TXEN_POL	Controls the TXEN active level when the ULPI interface is set in ULPI serial mode. 0b: TXEN is active high. 1b: TXEN is active low.	RW	0
2	ULPI_4PIN_2430	Changes the ULPI interface to a 4-pin Serial Mode based on 2430C port map. 0b: ULPI interface is defined by OTHER_IFC_CONTROL and IFC_CTRL register. 1b: FS/LS packets are sent using 4-pin ULPI serial interface based on 2430C port map.	RW	0
1:0	USB_INT_OUTSEL	Re-route interrupts. Valid only if ALT_INT_REROUTE bit of OTHER_IFC_CTRL is asserted. 00b: Re-route interrupt to the processor1 (INT1N line) 01b: Re-route interrupt to the processor2 (INT2N line) Others: reserved.	RW	0x0

Table 67. OTHER_IFC_CTRL2_SET

I2C Address	0x48		
Physical Address	0xB0	**Instance**	USB
Description	This register doesn't physically exist. It is the same as the other_ifc_ctrl2 register with read/set-only property (write 1 to set a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	ULPI_STP_LOW	ULPI_TXEN_POL	ULPI_4PIN_2430	USB_INT_OUTSEL	

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	Reserved		RO	0
4	ULPI_STP_LOW		RW	0
3	ULPI_TXEN_POL		RW	0
2	ULPI_4PIN_2430		RW	0
1:0	USB_INT_OUTSEL		RW	0x0

Table 68. OTHER_IFC_CTRL2_CLR

I2C Address	0x48		
Physical Address	0xB1	**Instance**	USB
Description	This register doesn't physically exist. It is the same as the other_ifc_ctrl2 register with read/clear-only property (write 1 to clear a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	ULPI_STP_LOW	ULPI_TXEN_POL	ULPI_4PIN_2430	USB_INT_OUTSEL	

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	Reserved		RO	0
4	ULPI_STP_LOW		RW	0
3	ULPI_TXEN_POL		RW	0
2	ULPI_4PIN_2430		RW	0
1:0	USB_INT_OUTSEL		RW	0x0

Table 69. REG_CTRL_EN

I2C Address	0x48		
Physical Address	0xB2	**Instance**	USB
Description	Interrupt enable to detect any conflcit when ULPI and I2C access occuring at the same time.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	ULPI_I2C_CONFLICT_INTEN

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	Reserved		RO	0
4	Reserved		RO	0
3	Reserved		RO	0
2	Reserved		RO	0
1	Reserved		RO	0
0	ULPI_I2C_CONFLICT_INTEN	If this bit is enabled, then any collisions between ULPI and I2C register access are reported as an interrupt event.	RW	0

Table 70. REG_CTRL_EN_SET

I2C Address	0x48		
Physical Address	0xB3	**Instance**	USB
Description	This register doesn't physically exist. It is the same as the reg_ctrl_en register with read/set-only property (write 1 to set a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	ULPI_I2C_CONFLICT_INTEN

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	Reserved		RO	0
4	Reserved		RO	0
3	Reserved		RO	0
2	Reserved		RO	0
1	Reserved		RO	0
0	ULPI_I2C_CONFLICT_INTEN		RW	0

Table 71. REG_CTRL_EN_CLR

I2C Address	0x48		
Physical Address	0xB4	**Instance**	USB
Description	This register doesn't physically exist. It is the same as the reg_ctrl_en register with read/clear-only property (write 1 to clear a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	ULPI_I2C_CONFLICT_INTEN

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	Reserved		RO	0
4	Reserved		RO	0
3	Reserved		RO	0
2	Reserved		RO	0
1	Reserved		RO	0
0	ULPI_I2C_CONFLICT_INTEN		RW	0

Table 72. REG_CTRL_ERROR

I2C Address	0x48		
Physical Address	0xB5	**Instance**	USB
Description	An interrupt latch which reports if a conflict has occurred beween ULPI and I2C register access.		
Type	RO		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	ULPI_I2C_CONFLICT_ERROR

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	Reserved		RO	0
4	Reserved		RO	0
3	Reserved		RO	0
2	Reserved		RO	0
1	Reserved		RO	0
0	ULPI_I2C_CONFLICT_ERROR	If this bit is set, it means a collision has occurred between ULPI and I2C access. To clear this interrupt latch, the software has to make a read access. **NOTE:** This interrupt has to be enabled first, writing 0x01 in REG_CTRL_EN(@B2)	RO	0

Table 73. OTHER_FUNC_CTRL2

I2C Address	0x48		
Physical Address	0xB8	**Instance**	USB
Description	Provides additional control for carkit support. It can be accessed only via I2C.		
Type	RW		

7	6	5	4	3	2	1	0
ZHSTX		ISHTX				RESERVED	VBAT_TIMER_EN

Bits	Field Name	Description	Type	Reset
7:6	ZHSTX	High speed output impedance configuration for eye diagram tuning : 00: 45.455 Ω 01: 43.779 Ω 10: 42.793 Ω 11: 42.411 Ω	RW	0x0
5:2	ISHTX	High speed output drive strength configuration for eye diagram tuning : 0000: 17.928 mA 0001: 18.117 mA 0010: 18.306 mA 0011: 18.495 mA 0100: 18.683 mA 0101: 18.872 mA 0110: 19.061 mA 0111: 19.249 mA 1000: 19.438 mA 1001: 19.627 mA 1010: 19.816 mA 1011: 20.004 mA 1100: 20.193 mA 1101: 20.382 mA 1110: 20.570 mA 1111: 20.759 mA IHSTX[0] is also the AC BOOST enable IHSTX[0] = 0 if AC BOOST is disabled IHSTX[0] = 1 if AC BOOST is enabled	RW	0x1
1	Reserved	Charge Pump enable	RO	0
0	VBAT_TIMER_EN	Enable the vbat function for BCI.	RW	0

Table 74. OTHER_FUNC_CTRL2_SET

I2C Address	0x48		
Physical Address	0xB9	**Instance**	USB
Description	This register doesn't physically exist. It can be accessed only via I2C. It is the same as the other_func_ctrl2 register with read/set-only property (write 1 to set a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
ZHSTX		IHSTX				RESERVED	VBAT_TIMER_EN

Bits	Field Name	Description	Type	Reset
7:6	ZHSTX	High speed output impedance configuration for eye diagram tuning	RW	0x0
5:2	IHSTX	High speed output drive strength configuration for eye diagram tuning	RW	0x1
1	Reserved	Charge pump enable	RO	0
0	VBAT_TIMER_EN	Enable the vbat function for BCI.	RW	0

Table 75. OTHER_FUNC_CTRL2_CLR

I2C Address	0x48		
Physical Address	0xBA	**Instance**	USB
Description	This register doesn't physically exist. It can be accessed only via I2C. It is the same as the other_func_ctrl2 register with read/clear-only property (write 1 to clear a particular bit, a write 0 has no-action).		
Type	RW		

7	6	5	4	3	2	1	0
ZHTX		ISHTX				RESERVED	VBAT_TIMER_EN

Bits	Field Name	Description	Type	Reset
7:6	ZHTX	High speed output impedance configuration for eye diagram tuning	RW	0x0
5:2	ISHTX	High speed output drive strength configuration for eye diagram tuning	RW	0x1
1	Reserved	Charge Pump enable	RO	0
0	VBAT_TIMER_EN		RW	0

Table 76. VBUS_DEBOUNCE

I2C Address	0x48		
Physical Address	0xC0	**Instance**	USB
Description	Programmable counter value for VBUS debouncing.counter period = [vbus_debounce - 1 : vbus_debounce] * (32/32768) seconds		
Type	RW		

7	6	5	4	3	2	1	0
VBUS_DEBOUNCE							

Bits	Field Name	Description	Type	Reset
7:0	VBUS_DEBOUNCE	Debouncing duration value in 1.024-kHz periods. Reset value is 30 ms	RW	0x1F

Table 77. ID_DEBOUNCE

I2C Address	0x48		
Physical Address	0xC1	**Instance**	USB
Description	Programmable counter value for ID debouncing.counter period = [id_debounce - 1 : id_debounce] * (32/32768) seconds		
Type	RW		

7	6	5	4	3	2	1	0
ID_DEBOUNCE							

Bits	Field Name	Description	Type	Reset
7:0	ID_DEBOUNCE	Debouncing duration value in 1.024-kHz periods. Reset value is 50 ms. **Note:** The default value fit with the ULPI requirements.	RW	0x34

Table 78. VBAT_TIMER

I2C Address	0x48		
Physical Address	0xD3	**Instance**	USB
Description	Counter value for VBAT function.It can be accessed only via I2C. This register can only be modified when vbat_timer_en_rg = 0		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	VBAT_TIMER_VALUE			

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	Reserved		RO	0
4	Reserved		RO	0
3:0	VBAT_TIMER_VALUE	Programmable counter value for vbat_timer for BCI.	RW	0x6

Table 79. PHY_PWR_CTRL

I2C Address	0x48		
Physical Address	0xFD	**Instance**	USB
Description	Controls the PHY state. It can be access only via I2C.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	PHYPWD

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	Reserved		RO	0
4	Reserved		RO	0
3	Reserved		RO	0
2	Reserved		RO	0
1	Reserved		RO	0
0	PHYPWD	Power down entire PHY. 0b: Normal state. 1b: Power down.	RW	0

Table 80. PHY_CLK_CTRL

I2C Address	0x48		
Physical Address	0xFE	**Instance**	USB
Description	Control the DPLL clock state. It can be accessed only via I2C.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	CLOCKGATING_EN	CLK32K_EN	REQ_PHY_DPLL_CLK

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	Reserved		RO	0
4	Reserved		RO	0
3	Reserved		RO	0
2	CLOCKGATING_EN	Enable automatic clock gating of the ulpi register clock. 0b: Gating is disabled 1b: Gating is enabled	RW	0
1	CLK32K_EN	32-kHz clock enable 0b: 32-kHz clock is disabled 1b: 32-kHz clock is enabled	RW	1
0	REQ_PHY_DPLL_CLK	Active high DPLL clock request. 0b: PHY state depend on the bit SuspendM in the FUNC_CTRL register. 1b: Powered the PHY and wake-up the clock.	RW	0

Table 81. PHY_CLK_CTRL_STS

I2C Address	0x48		
Physical Address	0xFF	**Instance**	USB
Description	Indicates the current state of the PHY DPLL. It can be access only via I2C.		
Type	RO		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	PHY_DPLL_CLK

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	Reserved		RO	0
4	Reserved		RO	0
3	Reserved		RO	0
2	Reserved		RO	0
1	Reserved		RO	0
0	PHY_DPLL_CLK	Asserted when the PHY DPLL is locked. **NOTE:** Read value is 0 when DPLL is OFF Read value is 1 when DPLL is ON	RO	0

3 INT

This section provides information on the INT module instances within this product. Each of the registers within the different INT module instances is described separately below.

3.1 INT Sub-Chip Instance Summary

The table below shows the base address for the INT module instances.

Table 82. INT_SC Instance Summary

Module Name	Base Address
PIH	0x81
INTBR	0x85
GPIO	0x98

3.2 PIH

This section provides information on the PIH module instances within INT. Each of the registers within the different PIH module instances is described separately below.

3.2.1 PIH Registers Mapping Summary

Table 83. PIH Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	Address Offset	Physical Address
PIH_ISR_P1	RW	8	0x00	0x0	0x81

3.2.2 PIH Register Descriptions

Table 84. PIH_ISR_P1

I2C Address	0x49		
Physical Address	0x81	**Instance**	PIH
Description	This register stores the currently active block number (in hexa) generating the current interrupt. Reading this register will not clear any bits, but inform the host on which subsystem SIH_ISRx register to read.		
Type	RW		

7	6	5	4	3	2	1	0
PIH_ISR7	PIH_ISR6	PIH_ISR5	PIH_ISR4	PIH_ISR3	PIH_ISR2	PIH_ISR1	PIH_ISR0

Bits	Field Name	Description	Type	Reset
7	PIH_ISR7	Read 0: No interrupt set 1: Interrupt set	RW	0
6	PIH_ISR6	Read 0: No interrupt set 1: Interrupt set	RW	0
5	PIH_ISR5	POWER Management dedicated Interrupt line status Read 0: No interrupt set 1: Interrupt set	RW	0
4	PIH_ISR4	USB dedicated Interrupt line status Read 0: No interrupt set 1: Interrupt set	RW	0
3	PIH_ISR3	MADC dedicated Interrupt line status Read 0: No interrupt set 1: Interrupt set	RW	0
2	PIH_ISR2	ACCESSORY dedicated Interrupt line status Read 0: No interrupt set 1: Interrupt set	RW	0
1	PIH_ISR1	Keypad dedicated Interrupt line status Read 0: No interrupt set 1: Interrupt set	RW	0
0	PIH_ISR0	GPIO dedicated Interrupt line status Read 0: No interrupt set 1: Interrupt set	RW	0

3.3 INTBR

This section provides information on the INTBR module instances within INT. Each of the registers within the different INTBR module instances is described separately below.

3.3.1 INTBR Registers Mapping Summary

Table 85. INTBR Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	Address Offset	Physical Address
IDCODE_7_0	RO	8	0x2F	0x00	0x85
IDCODE_15_8	RO	8	0x80	0x01	0x86
IDCODE_23_16	RO	8	0x77	0x02	0x87
IDCODE_31_24	RO	8	0x0B	0x03	0x88
DIEID_7_0	RO	8	0x00	0x04	0x89
DIEID_15_8	RO	8	0x00	0x05	0x8A
DIEID_23_16	RO	8	0x00	0x06	0x8B
DIEID_31_24	RO	8	0x00	0x07	0x8C
DIEID_39_32	RO	8	0x00	0x08	0x8D
DIEID_47_40	RO	8	0x00	0x09	0x8E
DIEID_55_48	RO	8	0x00	0x0A	0x8F
DIEID_63_56	RO	8	0x00	0x0B	0x90
GPBR1	RW	8	0x90	0x0C	0x91
PMBR1	RW	8	0x00	0x0D	0x92
PMBR2	RW	8	0x00	0x0E	0x93
GPPUPDCTR1	RW	8	0x55	0x0F	0x94
GPPUPDCTR2	RW	8	0x00	0x10	0x95
GPPUPDCTR3	RW	8	0x00	0x11	0x96
UNLOCK_TEST_REG	RW	8	0x00	0x12	0x97

3.3.2 INTBR Register Descriptions

Table 86. IDCODE_7_0

I2C Address	0x49		
Physical Address	0x85	**Instance**	INTBR
Description	This register reflect the value of IDcode [7:0] values issued from TAP/JTAG test modules. Cf DFT specification for details.The purpose of this register is to acces to IDCODE throught I2c IF.		
Type	RO		

7	6	5	4	3	2	1	0
IDCODE_7	IDCODE_6	IDCODE_5	IDCODE_4	IDCODE_3	IDCODE_2	IDCODE_1	IDCODE_0

Bits	Field Name	Description	Type	Reset
7	IDCODE_7	IDcode bit field 7	RO	0
6	IDCODE_6	IDcode bit field 6	RO	0
5	IDCODE_5	IDcode bit field 5	RO	1
4	IDCODE_4	IDcode bit field 4	RO	0
3	IDCODE_3	IDcode bit field 3	RO	1
2	IDCODE_2	IDcode bit field 2	RO	1
1	IDCODE_1	IDcode bit field 1	RO	1

Bits	Field Name	Description	Type	Reset
0	IDCODE_0	IDcode bit field 0	RO	1

Table 87. IDCODE_15_8

I2C Address	0x49		
Physical Address	0x86	Instance	INTBR
Description	This register reflect the value of IDcode [15:8] values issued from TAP/JTAG test modules. Cf DFT specification for details.The purpose of this register is to acces to IDCODE throught I2c IF.		
Type	RO		

7	6	5	4	3	2	1	0
IDCODE_15	IDCODE_14	IDCODE_13	IDCODE_12	IDCODE_11	IDCODE_10	IDCODE_9	IDCODE_8

Bits	Field Name	Description	Type	Reset
7	IDCODE_15	IDcode bit field 15	RO	1
6	IDCODE_14	IDcode bit field 14	RO	0
5	IDCODE_13	IDcode bit field 13	RO	0
4	IDCODE_12	IDcode bit field 12	RO	0
3	IDCODE_11	IDcode bit field 11	RO	0
2	IDCODE_10	IDcode bit field 10	RO	0
1	IDCODE_9	IDcode bit field 9	RO	0
0	IDCODE_8	IDcode bit field 8	RO	0

Table 88. IDCODE_23_16

I2C Address	0x49		
Physical Address	0x87	Instance	INTBR
Description	This register reflect the value of IDcode [23:16] values issued from TAP/JTAG test modules. Cf DFT specification for details. The purpose of this register is to acces to IDCODE throught I2c IF.		
Type	RO		

7	6	5	4	3	2	1	0
IDCODE_23	IDCODE_22	IDCODE_21	IDCODE_20	IDCODE_19	IDCODE_18	IDCODE_17	IDCODE_16

Bits	Field Name	Description	Type	Reset
7	IDCODE_23	IDcode bit field 23	RO	0
6	IDCODE_22	IDcode bit field 22	RO	1
5	IDCODE_21	IDcode bit field 21	RO	1
4	IDCODE_20	IDcode bit field 20	RO	1
3	IDCODE_19	IDcode bit field 19	RO	0
2	IDCODE_18	IDcode bit field 18	RO	1
1	IDCODE_17	IDcode bit field 17	RO	1
0	IDCODE_16	IDcode bit field 16	RO	1

Table 89. IDCODE_31_24

I2C Address	0x49		
Physical Address	0x88	**Instance**	INTBR
Description	This register reflect the value of IDcode [31:24] values issued from TAP/JTAG test modules. Cf DFT specification for details. The purpose of this register is to acces to IDCODE throught I2C IF.		
Type	RO		

7	6	5	4	3	2	1	0
IDCODE_31	IDCODE_30	IDCODE_29	IDCODE_28	IDCODE_27	IDCODE_26	IDCODE_25	IDCODE_24

Bits	Field Name	Description	Type	Reset
7	IDCODE_31	IDcode bit field 31	RO	0
6	IDCODE_30	IDcode bit field 30	RO	0
5	IDCODE_29	IDcode bit field 29	RO	0
4	IDCODE_28	IDcode bit field 28	RO	1
3	IDCODE_27	IDcode bit field 27	RO	1
2	IDCODE_26	IDcode bit field 26	RO	0
1	IDCODE_25	IDcode bit field 25	RO	1
0	IDCODE_24	IDcode bit field 24	RO	1

Table 90. DIEID_7_0

I2C Address	0x49		
Physical Address	0x89	**Instance**	INTBR
Description	This register reflect the value of DIEID EEprom [7:0] values. This register is protected by UNLOCK_TEST_REG register as DIEID is in EEPROM.		
Type	RO		

7	6	5	4	3	2	1	0
DIEID_7	DIEID_6	DIEID_5	DIEID_4	DIEID_3	DIEID_2	DIEID_1	DIEID_0

Bits	Field Name	Description	Type	Reset
7	DIEID_7	DIEID bit field 7	RO	0
6	DIEID_6	DIEID bit field 6	RO	0
5	DIEID_5	DIEID bit field 5	RO	0
4	DIEID_4	DIEID bit field 4	RO	0
3	DIEID_3	DIEID bit field 3	RO	0
2	DIEID_2	DIEID bit field 2	RO	0
1	DIEID_1	DIEID bit field 1	RO	0
0	DIEID_0	DIEID bit field 0	RO	0

Table 91. DIEID_15_8

I2C Address	0x49		
Physical Address	0x8A	**Instance**	INTBR
Description	This register reflect the value of DIEID EEprom [15:8] values. This register is protected by UNLOCK_TEST_REG register as DIEID is in EEPROM.		
Type	RO		

7	6	5	4	3	2	1	0
DIEID_15	DIEID_14	DIEID_13	DIEID_12	DIEID_11	DIEID_10	DIEID_9	DIEID_8

Bits	Field Name	Description	Type	Reset
7	DIEID_15	DIEID bit field 15	RO	0
6	DIEID_14	DIEID bit field 14	RO	0
5	DIEID_13	DIEID bit field 13	RO	0
4	DIEID_12	DIEID bit field 12	RO	0
3	DIEID_11	DIEID bit field 11	RO	0
2	DIEID_10	DIEID bit field 10	RO	0
1	DIEID_9	DIEID bit field 9	RO	0
0	DIEID_8	DIEID bit field 8	RO	0

Table 92. DIEID_23_16

I2C Address	0x49		
Physical Address	0x8B	**Instance**	INTBR
Description	This register reflect the value of DIEID EEprom [23:16] values. This register is protected by UNLOCK_TEST_REG register as DIEID is in EEPROM.		
Type	RO		

7	6	5	4	3	2	1	0
DIEID_23	DIEID_22	DIEID_21	DIEID_20	DIEID_19	DIEID_18	DIEID_17	DIEID_16

Bits	Field Name	Description	Type	Reset
7	DIEID_23	DIEID bit field 23	RO	0
6	DIEID_22	DIEID bit field 22	RO	0
5	DIEID_21	DIEID bit field 21	RO	0
4	DIEID_20	DIEID bit field 20	RO	0
3	DIEID_19	DIEID bit field 19	RO	0
2	DIEID_18	DIEID bit field 18	RO	0
1	DIEID_17	DIEID bit field 17	RO	0
0	DIEID_16	DIEID bit field 16	RO	0

Table 93. DIEID_31_24

I2C Address	0x49		
Physical Address	0x8C	**Instance**	INTBR
Description	This register reflect the value of DIEID EEprom [31:24] values. This register is protected by UNLOCK_TEST_REG register as DIEID is in EEPROM.		
Type	RO		

7	6	5	4	3	2	1	0
DIEID_31	DIEID_30	DIEID_29	DIEID_28	DIEID_27	DIEID_26	DIEID_25	DIEID_24

Bits	Field Name	Description	Type	Reset
7	DIEID_31	DIEID bit field 31	RO	0
6	DIEID_30	DIEID bit field 30	RO	0
5	DIEID_29	DIEID bit field 29	RO	0
4	DIEID_28	DIEID bit field 28	RO	0
3	DIEID_27	DIEID bit field 27	RO	0
2	DIEID_26	DIEID bit field 26	RO	0
1	DIEID_25	DIEID bit field 25	RO	0
0	DIEID_24	DIEID bit field 24	RO	0

Table 94. DIEID_39_32

I2C Address	0x49		
Physical Address	0x8D	**Instance**	INTBR
Description	This register reflect the value of DIEID EEprom [39:32] values. This register is protected by UNLOCK_TEST_REG register as DIEID is in EEPROM.		
Type	RO		

7	6	5	4	3	2	1	0
DIEID_39	DIEID_38	DIEID_37	DIEID_36	DIEID_35	DIEID_34	DIEID_33	DIEID_32

Bits	Field Name	Description	Type	Reset
7	DIEID_39	DIEID bit field 39	RO	0
6	DIEID_38	DIEID bit field 38	RO	0
5	DIEID_37	DIEID bit field 37	RO	0
4	DIEID_36	DIEID bit field 36	RO	0
3	DIEID_35	DIEID bit field 35	RO	0
2	DIEID_34	DIEID bit field 34	RO	0
1	DIEID_33	DIEID bit field 33	RO	0
0	DIEID_32	DIEID bit field 32	RO	0

Table 95. DIEID_47_40

I2C Address	0x49		
Physical Address	0x8E	**Instance**	INTBR
Description	This register reflect the value of DIEID EEprom [47:40] values. This register is protected by UNLOCK_TEST_REG register as DIEID is in EEPROM.		
Type	RO		

7	6	5	4	3	2	1	0
DIEID_47	DIEID_46	DIEID_45	DIEID_44	DIEID_43	DIEID_42	DIEID_41	DIEID_40

Bits	Field Name	Description	Type	Reset
7	DIEID_47	DIEID bit field 47	RO	0
6	DIEID_46	DIEID bit field 46	RO	0
5	DIEID_45	DIEID bit field 45	RO	0
4	DIEID_44	DIEID bit field 44	RO	0
3	DIEID_43	DIEID bit field 43	RO	0
2	DIEID_42	DIEID bit field 42	RO	0
1	DIEID_41	DIEID bit field 41	RO	0
0	DIEID_40	DIEID bit field 40	RO	0

Table 96. DIEID_55_48

I2C Address	0x49		
Physical Address	0x8F	**Instance**	INTBR
Description	This register reflect the value of DIEID EEprom [55:48] values. This register is protected by UNLOCK_TEST_REG register as DIEID is in EEPROM.		
Type	RO		

7	6	5	4	3	2	1	0
DIEID_55	DIEID_54	DIEID_53	DIEID_52	DIEID_51	DIEID_50	DIEID_49	DIEID_48

Bits	Field Name	Description	Type	Reset
7	DIEID_55	DIEID bit field 55	RO	0
6	DIEID_54	DIEID bit field 54	RO	0
5	DIEID_53	DIEID bit field 53	RO	0
4	DIEID_52	DIEID bit field 52	RO	0
3	DIEID_51	DIEID bit field 51	RO	0
2	DIEID_50	DIEID bit field 50	RO	0
1	DIEID_49	DIEID bit field 49	RO	0
0	DIEID_48	DIEID bit field 48	RO	0

Table 97. DIEID_63_56

I2C Address	0x49		
Physical Address	0x90	**Instance**	INTBR
Description	This register reflect the value of DIEID EEprom [63:56] values. This register is protected by UNLOCK_TEST_REG register as DIEID is in EEPROM.		
Type	RO		

7	6	5	4	3	2	1	0
DIEID_63	DIEID_62	DIEID_61	DIEID_60	DIEID_59	DIEID_58	DIEID_57	DIEID_56

Bits	Field Name	Description	Type	Reset
7	DIEID_63	DIEID bit field 63	RO	0
6	DIEID_62	DIEID bit field 62	RO	0
5	DIEID_61	DIEID bit field 61	RO	0
4	DIEID_60	DIEID bit field 60	RO	0
3	DIEID_59	DIEID bit field 59	RO	0
2	DIEID_58	DIEID bit field 58	RO	0
1	DIEID_57	DIEID bit field 57	RO	0
0	DIEID_56	DIEID bit field 56	RO	0

Table 98. GPBR1

I2C Address	0x49		
Physical Address	0x91	**Instance**	INTBR
Description	General purpose Bank Register. This register include MADC default clock switch off bit (default madc clock is enabled by default). Three others fields are dedicated to HFCLK/3MHz software MADC clock switching if Vbat Monitoring function is needed in sleep mode.		
Type	RW		

7	6	5	4	3	2	1	0
MADC_HFCLK_EN	MADC_3Mhz_EN	VBAT_MON_EN	DEFAULT_MADC_CLK_EN	RESERVED	RESERVED	RESERVED	RESERVED

Bits	Field Name	Description	Type	Reset
7	MADC_HFCLK_EN	When set to 1 (default) MADC 1-MHz clock divider based on HFCLK (26 MHz) clock (Not available in sleep mode) is switched on. 'when 0 MADC 1-MHz clock divider based on HFCLK is switched off	RW	1
6	MADC_3MHZ_EN	When set to 1 MADC 1-MHz clock divider based on 3-MHz clock (available even when TPS65921 is in sleep mode) is witched on. when 0 (default) MADC 1-MHz clock divider based on 3-MHz clock is switched off	RW	0
5	VBAT_MON_EN	When 1 Vbat monitoring function is Enabled in sleep mode → meaning that if enabled (MADC_3Mhz_EN=1), MADC 1-MHz clock based on 3-MHz clock dividers is connected to MADC. When 0 (default) then feature is not enabled in Sleep → meaning that if enabled (MADC_HFCLK_EN=1), MADC 1-MHz clock based on HFCLK clock dividers is connected to MADC.	RW	0
4	DEFAULT_MADC_CLK_EN	When this Bit is 1 (by default) default MADC clock is on and is equal to HFCLK divided by 26. That means that if HFCLK is 26 MHz then MADC default clock will be 1 MHz. Then If HFCLK is other than 26 MHz so either 38.4 MHz or 19.2 MHz then MADC frequency will be 38.4/26 = 1.47 MHz or 19.2/26 =7.36 MHz. When this bit is cleared, MADC clock is based on what is described inside CFG_BOOT registers bits HFCLK_FREQ related to hfclk frequency value (meaning that no MADC clock generated when HFCLK_FREQ is default to "00"). Note that when this bit is set any mechanism of clock gating regarding madc clock request will by bypassed. That means that power consumption will be upper than if madc_default_clk_en is cleared, as the clock is always provided to MADC even if no requested.	RW	1
3	Reserved		RW	0
2	Reserved		RW	0
1	Reserved		RW	0
0	Reserved		RW	0

Table 99. PMBR1

I2C Address	0x49		
Physical Address	0x92	**Instance**	INTBR
Description	Pad Muxing Bank Register 1 is used to select GPIO mode functionality versus USB Mode, or other TPS65921 features. By default USB is selected, in case of USB muxing, otherwise GPIO is the default selected feature.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED		RESERVED		RESERVED		GPIO_USB	

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RW	0x0
5:4	Reserved		RW	0x0
3:2	Reserved		RW	0x0
1:0	GPIO_USB	GPIO 3/4/5/9/10/11/12/14 and USB functions pad muxing control register 0x0: (default) Full USB ULPI 8D Function is enabled 0x1: GPIO Function is enabled on 9/10/11/12/14/3/4/5 and USB 3 Pin on DATA0/DATA1/DATA2 0x2: GPIO Function is enabled on GPIO 9/10/11/14/3/4/5 and USB 4 Pin on DATA0/DATA1/DATA2/DATA3 0x3: GPIO Function is enabled on GPIO 9/10/11/12/14/3/5 and USB 4 Pin on DATA0/DATA1/DATA2/DATA6 This mode is a 4 pin USB mode with Receive mapped on DATA6.	RW	0x0

Table 100. PMBR2

I2C Address	0x49		
Physical Address	0x93	**Instance**	INTBR
Description	Pad Muxing Bank Register2 is used to select GPIO8 versus UART1 functionality (GPIO8 is default). By default GPIO is selected.Reserved spare Field are read/write [can be used for spare].		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED_S6	RESERVED_S5	RESERVED_S4	RESERVED_S3	RESERVED		GPIO8_UART1_RXD	RESERVED

Bits	Field Name	Description	Type	Reset
7	RESERVED_S6	Reserved for spare	RW	0
6	RESERVED_S5	Reserved for spare	RW	0
5	RESERVED_S4	Reserved for spare	RW	0
4	RESERVED_S3	Reserved for spare	RW	0
3:2	Reserved		RW	0x0
1	GPIO8_UART1_RXD	GPIO8/UART1_RXD functions pad muxing control register 0: (Default) GPIO8 function is enabled 1: UART1 function is enabled	RW	0
0	Reserved	GPIO13/LEDSYNC functions pad muxing control register	RW	0

Table 101. GPPUPDCTR1

I2C Address	0x49		
Physical Address	0x94	**Instance**	INTBR
Description	This register is the generic pullup/pulldown control register for I2Cs PAD (both Smart Reflex I2C and TPS65921 internal common register I2C buses). By default, the external PU resistor should be connected. But as a 3.3-KΩ resistor is available inside pad, this can be connected, as the default is VMODE2/POWEROK2 on the I2C_SR Line. This pad muxing is controlled by the power module register.The default value is pullup.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED_S4	SR_I2C_SDA_CTRL_PU	RESERVED_S3	SR_I2C_SCL_CTRL_PU	RESERVED_S2	I2C_SDA_CTRL_PU	RESERVED_S1	I2C_SCL_CTRL_PU

Bits	Field Name	Description	Type	Reset
7	RESERVED_S4	Reserved for spare	RW	0
6	SR_I2C_SDA_CTRL_PU	0: Pullup is disabled 1: Pullup is enabled	RW	1
5	RESERVED_S3	Reserved for spare	RW	0
4	SR_I2C_SCL_CTRL_PU	0: Pullup is disabled 1: Pullup is enabled	RW	1
3	RESERVED_S2	Reserved for spare	RW	0
2	I2C_SDA_CTRL_PU	0: Pullup is disabled 1: Pullup is enabled	RW	1
1	RESERVED_S1	Reserved for spare	RW	0
0	I2C_SCL_CTRL_PU	0: Pullup is disabled 1: Pullup is enabled	RW	1

Table 102. GPPUPDCTR2

I2C Address	0x49		
Physical Address	0x95	Instance	INTBR
Description	General purpose pullup/pulldown control register (May be updated).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED_S8	RESERVED_S7	RESERVED_S6	RESERVED_S5	RESERVED_S4	RESERVED_S3	RESERVED_S2	RESERVED_S1

Bits	Field Name	Description	Type	Reset
7	RESERVED_S8	Reserved for spare	RW	0
6	RESERVED_S7	Reserved for spare	RW	1
5	RESERVED_S6	Reserved for spare	RW	0
4	RESERVED_S5	Reserved for spare	RW	1
3	RESERVED_S4	Reserved for spare	RW	0
2	RESERVED_S3	Reserved for spare	RW	0
1	RESERVED_S2	Reserved for spare	RW	0
0	RESERVED_S1	Reserved for spare	RW	0

Table 103. GPPUPDCTR3

I2C Address	0x49		
Physical Address	0x96	Instance	INTBR
Description	General purpose pullup/pulldown control register (May be updated).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED_S8	RESERVED_S7	RESERVED_S6	RESERVED_S5	RESERVED_S4	RESERVED_S3	RESERVED_S2	RESERVED_S1

Bits	Field Name	Description	Type	Reset
7	RESERVED_S8	Reserved for spare	RW	0
6	RESERVED_S7	Reserved for spare	RW	0
5	RESERVED_S6	Reserved for spare	RW	0
4	RESERVED_S5	Reserved for spare	RW	0
3	RESERVED_S4	Reserved for spare	RW	0
2	RESERVED_S3	Reserved for spare	RW	0
1	RESERVED_S2	Reserved for spare	RW	0
0	RESERVED_S1	Reserved for spare	RW	0

Table 104. UNLOCK_TEST_REG

I2C Address	0x49		
Physical Address	0x97	**Instance**	INTBR
Description	Writing "01001001" to this register allows to unlock TPS65921 EEPROM SW READ access through OCP		
Type	RW		

7	6	5	4	3	2	1	0
TEST_RESERVED_8	TEST_RESERVED_7	TEST_RESERVED_6	TEST_RESERVED_5	TEST_RESERVED_4	TEST_RESERVED_3	TEST_RESERVED_2	TEST_RESERVED_1

Bits	Field Name	Description	Type	Reset
7	TEST_RESERVED_8	Reserved for test registers access	RW	0
6	TEST_RESERVED_7	Reserved for test registers access	RW	0
5	TEST_RESERVED_6	Reserved for test registers access	RW	0
4	TEST_RESERVED_5	Reserved for test registers access	RW	0
3	TEST_RESERVED_4	Reserved for test registers access	RW	0
2	TEST_RESERVED_3	Reserved for test registers access	RW	0
1	TEST_RESERVED_2	Reserved for test registers access	RW	0
0	TEST_RESERVED_1	Reserved for test registers access 0: (Default) GPIO13 Function is enabled 1: LEDSYNC Function is enabled	RW	0

3.4 GPIO

This section provides information on the GPIO module instances within INT. Each of the registers within the different GPIO module instances is described separately below.

3.4.1 GPIO Registers Mapping Summary

Table 105. GPIO Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	Address Offset	Physical Address
GPIODATAIN1	RO	8	0x00	0x00	0x98
GPIODATAIN2	RO	8	0x00	0x01	0x99
GPIODATADIR1	RW	8	0x00	0x03	0x9B
GPIODATADIR2	RW	8	0x00	0x04	0x9C
GPIODATAOUT1	RW	8	0x00	0x06	0x9E
GPIODATAOUT2	RW	8	0x00	0x07	0x9F
CLEARGPIODATAOUT1	RW	8	0x00	0x09	0xA1
CLEARGPIODATAOUT2	RW	8	0x00	0x0A	0xA2
SETGPIODATAOUT1	RW	8	0x00	0x0C	0xA4
SETGPIODATAOUT2	RW	8	0x00	0x0D	0xA5
GPIO_DEBEN1	RW	8	0x00	0x0F	0xA7
GPIO_DEBEN2	RW	8	0x00	0x10	0xA8
GPIO_CTRL	RW	8	0x04	0x12	0xAA
GPIOPUPDCTR1	RW	8	0x15	0x13	0xAB
GPIOPUPDCTR2	RW	8	0x00	0x14	0xAC
GPIOPUPDCTR3	RW	8	0x01	0x15	0xAD
GPIOPUPDCTR4	RW	8	0x00	0x16	0xAE
GPIO_ISR1A	RW	8	0x00	0x19	0xB1
GPIO_ISR2A	RW	8	0x00	0x1A	0xB2
GPIO_IMR1A	RW	8	0x3F	0x1C	0xB4
GPIO_IMR2A	RW	8	0x5F	0x1D	0xB5
GPIO_EDR1	RW	8	0x00	0x28	0xC0
GPIO_EDR2	RW	8	0x00	0x29	0xC1
GPIO_EDR3	RW	8	0x00	0x2A	0xC2
GPIO_EDR4	RW	8	0x00	0x2B	0xC3
GPIO_SIH_CTRL	RW	8	0x01	0x2D	0xC5

3.4.2 GPIO Register Descriptions

Table 106. GPIODATAIN1

I2C Address	0x49		
Physical Address	0x98	**Instance**	GPIO
Description	The DATA INPUT REGISTER GPIODATAIN1 is used to register the data that is read from the GPIO[0:7] pins. The DATA INPUT REGISTER is a read-only register. The input data is sampled synchronously with the interface clock and then captured in the DATA INPUT REGISTER synchronously with the OCP bus clock.		
Type	RO		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	GPIO5IN	GPIO4IN	GPIO3IN	GPIO2IN	GPIO1IN	GPIO0IN

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RO	0
5	GPIO5IN	Read 0: GPIO Input is 0 Read 1: GPIO Input is 1	RO	0
4	GPIO4IN	Read 0: GPIO Input is 0 Read 1: GPIO Input is 1	RO	0
3	GPIO3IN	Read 0: GPIO Input is 0 Read 1: GPIO Input is 1	RO	0
2	GPIO2IN	Read 0: GPIO Input is 0 Read 1: GPIO Input is 1	RO	0
1	GPIO1IN	Read 0: GPIO Input is 0 Read 1: GPIO Input is 1	RO	0
0	GPIO0IN	Read 0: GPIO Input is 0 Read 1: GPIO Input is 1	RO	0

Table 107. GPIODATAIN2

I2C Address	0x49		
Physical Address	0x99	**Instance**	GPIO
Description	The DATA INPUT REGISTER GPIODATAIN2 is used to register the data that is read from the GPIO[8:15] pins. The DATA INPUT REGISTER is a read-only register. The input data is sampled synchronously with the interface clock and then captured in the DATA INPUT REGISTER synchronously with the OCP bus clock.		
Type	RO		

7	6	5	4	3	2	1	0
RESERVED	GPIO14IN	RESERVED	GPIO12IN	GPIO11IN	GPIO10IN	GPIO9IN	RESERVED

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	GPIO14IN	Read 0: GPIO Input is 0 Read 1: GPIO Input is 1	RO	0
5	Reserved		RO	0
4	GPIO12IN	Read 0: GPIO Input is 0 Read 1: GPIO Input is 1	RO	0
3	GPIO11IN	Read 0: GPIO Input is 0 Read 1: GPIO Input is 1	RO	0
2	GPIO10IN	Read 0: GPIO Input is 0 Read 1: GPIO Input is 1	RO	0
1	GPIO9IN	Read 0: GPIO Input is 0 Read 1: GPIO Input is 1	RO	0
0	Reserved		RO	0

Table 108. GPIODATADIR1

I2C Address	0x49		
Physical Address	0x9B	**Instance**	GPIO
Description	The DATA DIRECTION REGISTER GPIODATADIRA is used to enable the pin's input/output capabilities by setting the direction GPIOdir. At reset, all the GPIO[0:7] related pins are configured as input and output capabilities are disabled. This register is not used within the module. Its only function is to carry the pads configuration.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	GPIO5DIR	GPIO4DIR	GPIO3DIR	GPIO2DIR	GPIO1DIR	GPIO0DIR

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	0
6	Reserved		RW	0
5	GPIO5DIR	0: GPIO direction is input 1: GPIO direction is output	RW	0
4	GPIO4DIR	0: GPIO direction is input 1: GPIO direction is output	RW	0
3	GPIO3DIR	0: GPIO direction is input 1: GPIO direction is output	RW	0
2	GPIO2DIR	0: GPIO direction is input 1: GPIO direction is output	RW	0
1	GPIO1DIR	0: GPIO direction is input 1: GPIO direction is output	RW	0
0	GPIO0DIR	0: GPIO direction is input 1: GPIO direction is output	RW	0

Table 109. GPIODATADIR2

I2C Address	0x49		
Physical Address	0x9C	**Instance**	GPIO
Description	The DATA DIRECTION REGISTER GPIODATADIR2 is used to enable the pin's input/output capabilities by setting the direction GPIOdir. At reset, all the GPIO[8:15] related pins are configured as input and output capabilities are disabled. This register is not used within the module. Its only function is to carry the pads configuration.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	GPIO14DIR	RESERVED	GPIO12DIR	GPIO11DIR	GPIO10DIR	GPIO9DIR	RESERVED

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	0
6	GPIO14DIR	0: GPIO direction is input 1: GPIO direction is output	RW	0
5	Reserved		RW	0
4	GPIO12DIR	0: GPIO direction is input 1: GPIO direction is output	RW	0
3	GPIO11DIR	0: GPIO direction is input 1: GPIO direction is output	RW	0
2	GPIO10DIR	0: GPIO direction is input 1: GPIO direction is output	RW	0
1	GPIO9DIR	0: GPIO direction is input 1: GPIO direction is output	RW	0
0	Reserved		RW	0

Table 110. GPIODATAOUT1

I2C Address	0x49		
Physical Address	0x9E	**Instance**	GPIO
Description	The DATA OUTPUT REGISTER GPIODATAOUT1 is used for setting the value to the GPIO[0:7] output pins. Data is written to the DATA OUTPUT REGISTER synchronously with the OCP clock. The data loaded in the DATA OUTPUT REGISTER is set at the output GPIO pins synchronously with the rising edge of the OCP clock.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	GPIO5OUT	GPIO4OUT	GPIO3OUT	GPIO2OUT	GPIO1OUT	GPIO0OUT

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	0
6	Reserved		RW	0
5	GPIO5OUT	0: GPIO output is set to 0 1: GPIO output is set to 1	RW	0
4	GPIO4OUT	0: GPIO output is set to 0 1: GPIO output is set to 1	RW	0
3	GPIO3OUT	0: GPIO output is set to 0 1: GPIO output is set to 1	RW	0
2	GPIO2OUT	0: GPIO output is set to 0 1: GPIO output is set to 1	RW	0
1	GPIO1OUT	0: GPIO output is set to 0 1: GPIO output is set to 1	RW	0
0	GPIO0OUT	0: GPIO output is set to 0 1: GPIO output is set to 1	RW	0

Table 111. GPIODATAOUT2

I2C Address	0x49		
Physical Address	0x9F	**Instance**	GPIO
Description	The DATA OUTPUT REGISTER GPIODATAOUT2 is used for setting the value to the GPIO[8:15] output pins. Data is written to the DATA OUTPUT REGISTER synchronously with the OCP clock. The data loaded in the DATA OUTPUT REGISTER is set at the output GPIO pins synchronously with the rising edge of the OCP clock.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	GPIO14OUT	RESERVED	GPIO12OUT	GPIO11OUT	GPIO10OUT	GPIO9OUT	RESERVED

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	0
6	GPIO14OUT	0: GPIO output is set to 0 1: GPIO output is set to 1	RW	0
5	Reserved		RW	0
4	GPIO12OUT	0: GPIO output is set to 0 1: GPIO output is set to 1	RW	0
3	GPIO11OUT	0: GPIO output is set to 0 1: GPIO output is set to 1	RW	0
2	GPIO10OUT	0: GPIO output is set to 0 1: GPIO output is set to 1	RW	0
1	GPIO9OUT	0: GPIO output is set to 0 1: GPIO output is set to 1	RW	0
0	Reserved		RW	0

Table 112. CLEARGPIODATAOUT1

I2C Address	0x49		
Physical Address	0xA1	**Instance**	GPIO
Description	A write operation in the CLEAR DATA OUTPUT REGISTER clears the corresponding bit in the DATA OUTPUT REGISTER when the written bit is 1, whereas a written bit at 0 has no effect (see the Clear Instruction example). A read of the CLEAR DATA OUTPUT REGISTER returns the value of the DATA OUTPUT REGISTER.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	GPIO5OUT	GPIO4OUT	GPIO3OUT	GPIO2OUT	GPIO1OUT	GPIO0OUT

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	0
6	Reserved		RW	0
5	GPIO5OUT	0: No action 1: GPIO output is set to 0	RW	0
4	GPIO4OUT	0: No action 1: GPIO output is set to 0	RW	0
3	GPIO3OUT	0: No action 1: GPIO output is set to 0	RW	0
2	GPIO2OUT	0: No action 1: GPIO output is set to 0	RW	0
1	GPIO1OUT	0: No action 1: GPIO output is set to 0	RW	0
0	GPIO0OUT	0: No action 1: GPIO output is set to 0	RW	0

Table 113. CLEARGPIODATAOUT2

I2C Address	0x49		
Physical Address	0xA2	**Instance**	GPIO
Description	A write operation in the CLEAR DATA OUTPUT REGISTER clears the corresponding bit in the DATA OUTPUT REGISTER when the written bit is 1, whereas a written bit at 0 has no effect (see the Clear Instruction example). A read of the CLEAR DATA OUTPUT REGISTER returns the value of the DATA OUTPUT REGISTER.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	GPIO14OUT	RESERVED	GPIO12OUT	GPIO11OUT	GPIO10OUT	GPIO9OUT	RESERVED

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	0
6	GPIO14OUT	0: No action 1: GPIO output is set to 0	RW	0
5	Reserved		RW	0
4	GPIO12OUT	0: No action 1: GPIO output is set to 0	RW	0
3	GPIO11OUT	0: No action 1: GPIO output is set to 0	RW	0
2	GPIO10OUT	0: No action 1: GPIO output is set to 0	RW	0
1	GPIO9OUT	0: No action 1: GPIO output is set to 0	RW	0
0	Reserved		RW	0

Table 114. SETGPIODATAOUT1

I2C Address	0x49		
Physical Address	0xA4	**Instance**	GPIO
Description	A write operation in the SETDATAOUTPUT REGISTER sets the corresponding bit in the DATA OUTPUT REGISTER when the written bit is1, whereas a written bit at 0 has no effect (see the Set instruction example). A read of the SET DATA OUTPUT REGISTER returns the value of the DATA OUTPUT REGISTER.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	GPIO5OUT	GPIO4OUT	GPIO3OUT	GPIO2OUT	GPIO1OUT	GPIO0OUT

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	0
6	Reserved		RW	0
5	GPIO5OUT	0: No action 1: GPIO output is set to 1	RW	0
4	GPIO4OUT	0: No action 1: GPIO output is set to 1	RW	0
3	GPIO3OUT	0: No action 1: GPIO output is set to 1	RW	0
2	GPIO2OUT	0: No action 1: GPIO output is set to 1	RW	0
1	GPIO1OUT	0: No action 1: GPIO output is set to 1	RW	0
0	GPIO0OUT	0: No action 1: GPIO output is set to 1	RW	0

Table 115. SETGPIODATAOUT2

I2C Address	0x49		
Physical Address	0xA5	**Instance**	GPIO
Description	A write operation in the SET DATA OUTPUT REGISTER sets the corresponding bit in the DATA OUTPUT REGISTER when the written bit is1, whereas a written bit at 0 has no effect (see the Set instruction example). A read of the SET DATA OUTPUT REGISTER returns the value of the DATA OUTPUT REGISTER.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	GPIO14OUT	RESERVED	GPIO12OUT	GPIO11OUT	GPIO10OUT	GPIO9OUT	RESERVED

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	0
6	GPIO14OUT	0: No action 1: GPIO output is set to 1	RW	0
5	Reserved		RW	0
4	GPIO12OUT	0: No action 1: GPIO output is set to 1	RW	0
3	GPIO11OUT	0: No action 1: GPIO output is set to 1	RW	0
2	GPIO10OUT	0: No action 1: GPIO output is set to 1	RW	0
1	GPIO9OUT	0: No action 1: GPIO output is set to 1	RW	0
0	Reserved		RW	0

Table 116. GPIO_DEBEN1

I2C Address	0x49		
Physical Address	0xA7	**Instance**	GPIO
Description	The DEBOUNCING ENABLE REGISTER is used to enable/disable the debouncing feature for each input lines.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	GPIO5DEB	GPIO4DEB	GPIO3DEB	GPIO2DEB	GPIO1DEB	GPIO0DEB

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	0
6	Reserved		RW	0
5	GPIO5DEB	0: GPIO debounce not set 1: GPIO debounce set	RW	0
4	GPIO4DEB	0: GPIO debounce not set 1: GPIO debounce set	RW	0
3	GPIO3DEB	0: GPIO debounce not set 1: GPIO debounce set	RW	0
2	GPIO2DEB	0: GPIO debounce not set 1: GPIO debounce set	RW	0
1	GPIO1DEB	0: GPIO debounce not set 1: GPIO debounce set	RW	0
0	GPIO0DEB	0: GPIO debounce not set 1: GPIO debounce set	RW	0

Table 117. GPIO_DEBEN2

I2C Address	0x49		
Physical Address	0xA8	**Instance**	GPIO
Description	The DEBOUNCING ENABLE REGISTER is used to enable/disable the debouncing feature for each input lines.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	GPIO14DEB	RESERVED	GPIO12DEB	GPIO11DEB	GPIO10DEB	GPIO9DEB	RESERVED

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	0
6	GPIO14DEB	0: GPIO debounce not set 1: GPIO debounce set	RW	0
5	Reserved		RW	0
4	GPIO12DEB	0: GPIO debounce not set 1: GPIO debounce set	RW	0
3	GPIO11DEB	0: GPIO debounce not set 1: GPIO debounce set	RW	0
2	GPIO10DEB	0: GPIO debounce not set 1: GPIO debounce set	RW	0
1	GPIO9DEB	0: GPIO debounce not set 1: GPIO debounce set	RW	0
0	Reserved		RW	0

Table 118. GPIO_CTRL

I2C Address	0x49		
Physical Address	0xAA	**Instance**	GPIO
Description	The GPIO CONTROL REGISTER GPIO_CTRL is used to control the card detect feature behavior, and to power on/off GPIO Module GPIO_ON Field.Reserved field are Read/Write [can be used for spare]		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED_S5	RESERVED_S4	RESERVED_S3	RESERVED_S2	RESERVED_S1	GPIO_ON	GPIO1CD2	GPIO0CD1

Bits	Field Name	Description	Type	Reset
7	RESERVED_S5	Reserved for spare	RW	0
6	RESERVED_S4	Reserved for spare	RW	0
5	RESERVED_S3	Reserved for spare	RW	0
4	RESERVED_S2	Reserved for spare	RW	0
3	RESERVED_S1	Reserved for spare	RW	0
2	GPIO_ON	0: GPIO module is disabled. 1: GPIO module is enabled.	RW	1
1	GPIO1CD2	0: Card detect 2 feature disabled 1: Card detect 2 feature enabled	RW	0
0	GPIO0CD1	0: Card detect 1 feature disabled 1: Card detect 1 feature enabled	RW	0

Table 119. GPIOPUPDCTR1

I2C Address	0x49		
Physical Address	0xAB	**Instance**	GPIO
Description	GPIO pullup/pulldown control Register 1. By default, pulldowns are enabled in order to avoid leakage if GPIO are not externaly connected. Therefore, as GPIO3 is muxed with DATA5 Pin of USB ULPI and as this functionality is default, then default for this GPIO is no pullup and pulldown enabled.		
Type	RW		

7	6	5	4	3	2	1	0
GPIO3PU	GPIO3PD	GPIO2PU	GPIO2PD	GPIO1PU	GPIO1PD	GPIO0PU	GPIO0PD

Bits	Field Name	Description	Type	Reset
7	GPIO3PU	0: GPIO pullup is disabled 1: GPIO pullup is enabled	RW	0
6	GPIO3PD	0: GPIO pulldown is disabled 1: GPIO pulldown is enabled	RW	0
5	GPIO2PU	0: GPIO pullup is disabled 1: GPIO pullup is enabled	RW	0
4	GPIO2PD	0: GPIO pulldown is disabled 1: GPIO pulldown is enabled	RW	1
3	GPIO1PU	0: GPIO pullup is disabled 1: GPIO pullup is enabled	RW	0
2	GPIO1PD	0: GPIO pulldown is disabled 1: GPIO pulldown is enabled	RW	1
1	GPIO0PU	0: GPIO pullup disabled 1: GPIO pullup enabled	RW	0
0	GPIO0PD	0: GPIO pulldown is disabled 1: GPIO pulldown is enabled	RW	1

Table 120. GPIOPUPDCTR2

I2C Address	0x49		
Physical Address	0xAC	**Instance**	GPIO
Description	GPIO pullup/pulldown control register 2. By default, pulldowns are anebled in order to avoid leakage if GPIO are not externaly connected. Therefore, as GPIO4/GPIO5 are muxed respectively with DATA6/DATA7 Pin of USB ULPI and as USB/ULPI functionality is default, then default for these GPIOs is no pullup and pulldown enabled.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	GPIO5PU	GPIO5PD	GPIO4PU	GPIO4PD

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	0
6	Reserved		RW	1
5	Reserved		RW	0
4	Reserved		RW	1
3	GPIO5PU	0: GPIO pullup is disabled 1: GPIO pullup is enabled	RW	0
2	GPIO5PD	0: GPIO pulldown is disabled 1: GPIO pulldown is enabled	RW	0
1	GPIO4PU	0: GPIO pullup disabled 1: GPIO pullup enabled	RW	0
0	GPIO4PD	0: GPIO pulldown is disabled 1: GPIO pulldown is enabled	RW	0

Table 121. GPIOPUPDCTR3

I2C Address	0x49		
Physical Address	0xAD	**Instance**	GPIO
Description	GPIO pullup/pulldown control Register 3. By default, pulldowns are anebled in order to avoid leakage if GPIO are not externaly connected. Therefore, as GPIO9/GPIO10/GPIO11 are muxed respectively with STP/DIR/NXT Pin of USB ULPI and as USB/ULPI functionality is default, then default for these GPIOs is no pullup and pulldown enabled.		
Type	RW		

7	6	5	4	3	2	1	0
GPIO11PU	GPIO11PD	GPIO10PU	GPIO10PD	GPIO9PU	GPIO9PD	RESERVED	RESERVED

Bits	Field Name	Description	Type	Reset
7	GPIO11PU	0: GPIO pullup is disabled 1: GPIO pullup is enabled	RW	0
6	GPIO11PD	0: GPIO pulldown is disabled 1: GPIO pulldown is enabled	RW	0
5	GPIO10PU	0: GPIO pullup is disabled 1: GPIO pullup is enabled	RW	0
4	GPIO10PD	0: GPIO pulldown is disabled 1: GPIO pulldown is enabled	RW	0
3	GPIO9PU	0: GPIO pullup is disabled 1: GPIO pullup is enabled	RW	0
2	GPIO9PD	0: GPIO pulldown is disabled 1: GPIO pulldown is enabled	RW	0
1	Reserved		RW	0
0	Reserved		RW	1

Table 122. GPIOPUPDCTR4

I2C Address	0x49		
Physical Address	0xAE	**Instance**	GPIO
Description	GPIO pullup/pulldown control Register 4. By default, pulldowns are enabled in order to avoid leakage if GPIO are not externaly connected. Therefore, as GPIO12/GPIO14 are muxed respectively with DATA3/DATA4 Pin of USB ULPI and as this functionality is default, then default for these GPIOs is no pullup and pulldown enabled.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	GPIO14PU	GPIO14PD	RESERVED	RESERVED	GPIO12PU	GPIO12PD

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	0
6	Reserved		RW	1
5	GPIO14PU	0: GPIO pullup is disabled 1: GPIO pullup is enabled	RW	0
4	GPIO14PD	0: GPIO pulldown is disabled 1: GPIO pulldown is enabled	RW	0
3	Reserved		RW	0
2	Reserved		RW	1
1	GPIO12PU	0: GPIO pullup disabled 1: GPIO pullup enabled	RW	0
0	GPIO12PD	0: GPIO pulldown is disabled 1: GPIO pulldown is enabled	RW	0

Table 123. GPIO_ISR1A

I2C Address	0x49		
Physical Address	0xB1	**Instance**	GPIO
Description	The INTERRUPT STATUS ISR1A REGISTERs ise used to determine which of the input GPIO[0:7] pins trigged the interrupt line gpio_int1_n request. As illustrated here below, bit 0 corresponds to po_pad_gpio[0], bit 1 to po_pad_gpio[1], etc. When a bit in this register is set to 1, it indicates that the corresponding GPIO pin is requesting the interrupt. However, the user cannot generate an interrupt by writing a 1 to the INTERRUPT STATUS ISR1 REGISTER. If the user writes a 0 to a bit in this register,the value will remain unchanged when in COR mode. The INTERRUPT STATUS ISR1A REGISTER is synchronous with the interface OCP clockA read of a 1 in any bifield means that the corresponding interrupt event is active on interrupt request line 1.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	GPIO5ISR1	GPIO4ISR1	GPIO3ISR1	GPIO2ISR1	GPIO1ISR1	GPIO0ISR1

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	0
6	Reserved		RW	0
5	GPIO5ISR1	0: GPIO hardware interrupt inactive on processor 1 request line 1: GPIO hardware interrupt active on processor 1 request line	RW	0
4	GPIO4ISR1	0: GPIO hardware interrupt inactive on processor 1 request line 1: GPIO hardware interrupt active on processor 1 request line	RW	0
3	GPIO3ISR1	0: GPIO hardware interrupt inactive on processor 1 request line 1: GPIO hardware interrupt active on processor 1 request line	RW	0
2	GPIO2ISR1	0: GPIO hardware interrupt inactive on processor 1 request line 1: GPIO hardware interrupt active on processor 1 request line	RW	0
1	GPIO1ISR1	0: GPIO hardware interrupt inactive on processor 1 request line 1: GPIO hardware interrupt active on processor 1 request line	RW	0
0	GPIO0ISR1	0: GPIO hardware interrupt inactive on processor 1 request line 1: GPIO hardware interrupt active on processor 1 request line	RW	0

Table 124. GPIO_ISR2A

I2C Address	0x49		
Physical Address	0xB2	**Instance**	GPIO
Description	The INTERRUPT STATUS ISR2A REGISTERs ise used to determine which of the input GPIO[8:15] pins trigged the interrupt line gpio_int1_n request. As illustrated here below, bit 0 corresponds to po_pad_gpio[8], bit 1 to po_pad_gpio[9], etc. When a bit in this register is set to 1, it indicates that the corresponding GPIO pin is requesting the interrupt. However, the user cannot generate an interrupt by writing a 1 to the INTERRUPT STATUS ISR2 REGISTER. If the user writes a 0 to a bit in this register, the value will remain unchanged when in COR mode. The INTERRUPT STATUS ISR2A REGISTER is synchronous with the interface OCP clockA read of a 1 in any bifield means that the corresponding interrupt event is active on interrupt request line 1.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	GPIO14ISR2	RESERVED	GPIO12ISR2	GPIO11ISR2	GPIO10ISR2	GPIO9ISR2	RESERVED

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	0
6	GPIO14ISR2	0: GPIO hardware interrupt inactive on processor 1 request line 1: GPIO hardware interrupt active on processor 1 request line	RW	0
5	Reserved		RW	0
4	GPIO12ISR2	0: GPIO hardware interrupt inactive on processor 1 request line 1: GPIO hardware interrupt active on processor 1 request line	RW	0
3	GPIO11ISR2	0: GPIO hardware interrupt inactive on processor 1 request line 1: GPIO hardware interrupt active on processor 1 request line	RW	0
2	GPIO10ISR2	0: GPIO hardware interrupt inactive on processor 1 request line 1: GPIO hardware interrupt active on processor 1 request line	RW	0
1	GPIO9ISR2	0: GPIO hardware interrupt inactive on processor 1 request line 1: GPIO hardware interrupt active on processor 1 request line	RW	0
0	Reserved		RW	0

Table 125. GPIO_IMR1A

I2C Address	0x49		
Physical Address	0xB4	**Instance**	GPIO
Description	The INTERRUPT MASK IMR1A REGISTER allows the user to mask/unmask the expected transition on input GPIO[0:7] from generating an interrupt request on gpio_int1_n. The INTERRUPT MASK REGISTERS are programmed synchronously with the interface OCP clock. Writing 0 in any bit field unmask the corresponding gpio interrupt event on interrupt request line 1. By default, all interrupts are masked.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	GPIO5IMR1	GPIO4IMR1	GPIO3IMR1	GPIO2IMR1	GPIO1IMR1	GPIO0IMR1

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	1
6	Reserved		RW	1
5	GPIO5IMR1	0: GPIO event not masked on processor 1 request line 1: GPIO event masked on processor 1 request line	RW	1
4	GPIO4IMR1	0: GPIO event not masked on processor 1 request line 1: GPIO event masked on processor 1 request line	RW	1
3	GPIO3IMR1	0: GPIO event not masked on processor 1 request line 1: GPIO event masked on processor 1 request line	RW	1
2	GPIO2IMR1	0: GPIO event not masked on processor 1 request line 1: GPIO event masked on processor 1 request line	RW	1
1	GPIO1IMR1	0: GPIO event not masked on processor 1 request line 1: GPIO event masked on processor 1 request line	RW	1
0	GPIO0IMR1	0: GPIO event not masked on processor 1 request line 1: GPIO event masked on processor 1 request line	RW	1

Table 126. GPIO_IMR2A

I2C Address	0x49		
Physical Address	0xB5	**Instance**	GPIO
Description	The INTERRUPT MASK IMR2A REGISTER allows the user to mask/unmask the expected transition on input GPIO[8:15] from generating an interrupt request on gpio_int1_n. The INTERRUPT MASK REGISTERS are programmed synchronously with the interface OCP clock. Writing 0 in any bit field unmask the corresponding gpio interrupt event on interrupt request line 1. By default, all interrupts are masked.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	GPIO14IMR2	RESERVED	GPIO12IMR2	GPIO11IMR2	GPIO10IMR2	GPIO9IMR2	RESERVED

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	1
6	GPIO14IMR2	0: GPIO event not masked on processor 1 request line 1: GPIO event masked on processor 1 request line	RW	1
5	Reserved		RW	1
4	GPIO12IMR2	0: GPIO event not masked on processor 1 request line 1: GPIO event masked on processor 1 request line	RW	1
3	GPIO11IMR2	0: GPIO event not masked on processor 1 request line 1: GPIO event masked on processor 1 request line	RW	1
2	GPIO10IMR2	0: GPIO event not masked on processor 1 request line 1: GPIO event masked on processor 1 request line	RW	1
1	GPIO9IMR2	0: GPIO event not masked on processor 1 request line 1: GPIO event masked on processor 1 request line	RW	1
0	Reserved		RW	1

Table 127. GPIO_EDR1

I2C Address	0x49		
Physical Address	0xC0	**Instance**	GPIO
Description	The INTERRUPT EDGE DETECTION REGISTER GPIO_EDR1 allows the user to define, for each external GPIO[0:3] pin configured as input, the expected edge to trigger an interrupt request. The interrupt request can be either generated from a High-to-Low transition (bits are 01), a Low-to-High transition (bits are 10) or both transitions (bits are 11) accruing. To disable the edge detection capability, the relevant bits corresponding to the GPIO need to be reset (00).		
Type	RW		

7	6	5	4	3	2	1	0
GPIO3RISING	GPIO3FALLING	GPIO2RISING	GPIO2FALLING	GPIO1RISING	GPIO1FALLING	GPIO0RISING	GPIO0FALLING

Bits	Field Name	Description	Type	Reset
7	GPIO3RISING	0: GPIO rising detection disabled 1: GPIO rising detection enabled	RW	0
6	GPIO3FALLING	0: GPIO falling detection disabled 1: GPIO falling detection enabled	RW	0
5	GPIO2RISING	0: GPIO rising detection disabled 1: GPIO rising detection enabled	RW	0
4	GPIO2FALLING	0: GPIO falling detection disabled 1: GPIO falling detection enabled	RW	0
3	GPIO1RISING	0: GPIO rising detection disabled 1: GPIO rising detection enabled	RW	0
2	GPIO1FALLING	0: GPIO falling detection disabled 1: GPIO falling detection enabled	RW	0
1	GPIO0RISING	0: GPIO rising detection disabled 1: GPIO rising detection enabled	RW	0
0	GPIO0FALLING	0: GPIO falling detection disabled 1: GPIO falling detection enabled	RW	0

Table 128. GPIO_EDR2

I2C Address	0x49		
Physical Address	0xC1	**Instance**	GPIO
Description	The INTERRUPT EDGE DETECTION REGISTER GPIO_EDR2 allows the user to define, for each external GPIO[4:7] pin configured as input, the expected edge to trigger an interrupt request The interrupt request can be either generated from a High to Low transition (bits are 01), a low to High transition (bits are 10) or both transitions (bits are 11) accruing. To disable the edge detection capability, the relevant bits corresponding to the GPIO need to be reset (00).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	GPIO5RISING	GPIO5FALLING	GPIO4RISING	GPIO4FALLING

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	0
6	Reserved		RW	0
5	Reserved		RW	0
4	Reserved		RW	0
3	GPIO5RISING	0: GPIO rising detection disabled 1: GPIO rising detection enabled	RW	0
2	GPIO5FALLING	0: GPIO falling detection disabled 1: GPIO falling detection enabled	RW	0
1	GPIO4RISING	0: GPIO rising detection disabled 1: GPIO rising detection enabled	RW	0
0	GPIO4FALLING	0: GPIO falling detection disabled 1: GPIO falling detection enabled	RW	0

Table 129. GPIO_EDR3

I2C Address	0x49		
Physical Address	0xC2	**Instance**	GPIO
Description	The INTERRUPT EDGE DETECTION REGISTER GPIO_EDR3 allows the user to define, for each external GPIO[8:1] pin configured as input, the expected edge to trigger an interrupt request The interrupt request can be either generated from a High-to-Low transition (bits are 01), a Low-to-High transition (bits are 10) or both transitions (bits are 11) accruing. To disable the edge detection capability, the relevant bits corresponding to the GPIO need to be reset (00).		
Type	RW		

7	6	5	4	3	2	1	0
GPIO11RISING	GPIO11FALLING	GPIO10RISING	GPIO10FALLING	GPIO9RISING	GPIO9FALLING	RESERVED	RESERVED

Bits	Field Name	Description	Type	Reset
7	GPIO11RISING	0: GPIO rising detection disabled 1: GPIO rising detection enabled	RW	0
6	GPIO11FALLING	0: GPIO falling detection disabled 1: GPIO falling detection enabled	RW	0
5	GPIO10RISING	0: GPIO rising detection disabled 1: GPIO rising detection enabled	RW	0
4	GPIO10FALLING	0: GPIO falling detection disabled 1: GPIO falling detection enabled	RW	0
3	GPIO9RISING	0: GPIO rising detection disabled 1: GPIO rising detection enabled	RW	0
2	GPIO9FALLING	0: GPIO falling detection disabled 1: GPIO falling detection enabled	RW	0
1	Reserved		RW	0
0	Reserved		RW	0

Table 130. GPIO_EDR4

I2C Address	0x49		
Physical Address	0xC3	**Instance**	GPIO
Description	The INTERRUPT EDGE DETECTION REGISTER GPIO_EDR4 allows the user to define, for each external GPIO[13:15] pin configured as input, the expected edge to trigger an interrupt request The interrupt request can be either generated from a High-to-Low transition (bits are 01), a Low-to-High transition (bits are 10) or both transitions (bits are 11) accruing. To disable the edge detection capability, the relevant bits corresponding to the GPIO need to be reset (00). 2		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	GPIO14RISING	GPIO14FALLING	RESERVED	RESERVED	GPIO12RISING	GPIO12FALLING

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	0
6	Reserved		RW	0
5	GPIO14RISING	0: GPIO rising detection disabled 1: GPIO rising detection enabled	RW	0
4	GPIO14FALLING	0: GPIO falling detection disabled 1: GPIO falling detection enabled	RW	0
3	Reserved		RW	0
2	Reserved		RW	0
1	GPIO12RISING	0: GPIO rising detection disabled 1: GPIO rising detection enabled	RW	0
0	GPIO12FALLING	0: GPIO falling detection disabled 1: GPIO falling detection enabled	RW	0

Table 131. GPIO_SIH_CTRL

I2C Address	0x49		
Physical Address	0xC5	**Instance**	GPIO
Description	The GPIO SIH CONTROL REGISTER GPIO_SIH_CTRL allow the user to disable a pending event incoming during SW interrupt latency by programming 1 in PENDDIS field..The ClearOnRead bit field enable Clear on Read feature. That mean that any read access to the ISR clear this register and release the interrupt line associated (default value). If disabled a read access to a specific address value will clear all ISR within the SIHH.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED					COR	PENDDIS	RESERVED

Bits	Field Name	Description	Type	Reset
7:3	Reserved	Reads return 0s.	RO	0x00
2	COR	0: Clear ISR specific bit field when write access mode 1: Clear ISR when read mode	RW	0
1	PENDDIS	0: Pending event feature is enabled 1: Pending event feature is disabled	RW	0
0	Reserved		RW	1

4 AUX

This section provides information on the AUX module instances within this product. Each of the registers within the different AUX module instances is described separately below.

4.1 Aux Sub-Chip Instance Summary

The table below shows the base address for the AUX_SC module instances.

Table 132. AUX_SC Instance Summary

Module Name	Base Address
MADC	0x00
ACCESSORY_VINTDIG	0x74
keypad	0xD2

4.2 MADC

This section provides information on the MADC module instances within AUX. Each of the registers within the different MADC module instances is described separately below.

4.2.1 MADC Registers Mapping Summary

Table 133. MADC Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	Address Offset	Physical Address
CTRL1	RW	8	0x00	0x00	0x00
CTRL2	RW	8	0x01	0x01	0x01
RTSELECT_LSB	RW	8	0x00	0x02	0x02
RTSELECT_MSB	RW	8	0x00	0x03	0x03
RTAVERAGE_LSB	RW	8	0x00	0x04	0x04
RTAVERAGE_MSB	RW	8	0x00	0x05	0x05
SW1SELECT_LSB	RW	8	0x00	0x06	0x06
SW1SELECT_MSB	RW	8	0x00	0x07	0x07
SW1AVERAGE_LSB	RW	8	0x00	0x08	0x08
SW1AVERAGE_MSB	RW	8	0x00	0x09	0x09
SW2SELECT_LSB	RW	8	0x00	0x0A	0x0A
SW2SELECT_MSB	RW	8	0x00	0x0B	0x0B
SW2AVERAGE_LSB	RW	8	0x00	0x0C	0x0C
SW2AVERAGE_MSB	RW	8	0x00	0x0D	0x0D
BCI_USBAVERAGE	RW	8	0x00	0x0E	0x0E
ACQUISITION	RW	8	0x07	0x0F	0x0F
USBREF_LSB	RW	8	0xC0	0x10	0x10
USBREF_MSB	RW	8	0x8C	0x11	0x11
CTRL_SW1	RW	8	0xDE	0x12	0x12
CTRL_SW2	RW	8	0xDE	0x13	0x13
RTCH0_LSB	RO	8	0x00	0x17	0x17
RTCH0_MSB	RO	8	0x00	0x18	0x18
RTCH8_LSB	RO	8	0x00	0x27	0x27
RTCH8_MSB	RO	8	0x00	0x28	0x28
RTCH12_LSB	RO	8	0x00	0x2F	0x2F
RTCH12_MSB	RO	8	0x00	0x30	0x30
GPCH0_LSB	RO	8	0x00	0x37	0x37

Table 133. MADC Register Summary (continued)

Register Name	Type	Register Width (Bits)	Register Reset	Address Offset	Physical Address
GPCH0_MSB	RO	8	0x00	0x38	0x38
GPCH8_LSB	RO	8	0x00	0x47	0x47
GPCH8_MSB	RO	8	0x00	0x48	0x48
GPCH12_LSB	RO	8	0x00	0x4F	0x4F
GPCH12_MSB	RO	8	0x00	0x50	0x50
BCICH1_LSB	RO	8	0x00	0x59	0x59
BCICH1_MSB	RO	8	0x00	0x5A	0x5A
BCICH4_LSB	RO	8	0x00	0x5F	0x5F
BCICH4_MSB	RO	8	0x00	0x60	0x60
MADC_ISR1	RW	8	0x00	0x61	0x61
MADC_IMR1	RW	8	0x0F	0x62	0x62
MADC_EDR	RW	8	0x55	0x66	0x66
MADC_SIH_CTRL	RW	8	0x07	0x67	0x67

4.2.2 MADC Register Descriptions

Table 134. CTRL1

I2C Address	0x4A		
Physical Address	0x00	**Instance**	MADC
Description	USBREF/VBAT comparator status bit. When 1 measured Vbat is greater than USBREF value programmed inside USBREF_LSB and USBREF_MSB registers, else status is 0.		
Type	RW		

7	6	5	4	3	2	1	0
VBATREF_LSB					RESERVED	RESERVED	MADCON

Bits	Field Name	Description	Type	Reset
7:3	VBATREF_LSB	LSB of the VBAT compared value (5 LSBs)	RW	0x00
2	Reserved	Reserved for spare	RW	0
1	Reserved	Reserved for spare	RW	0
0	MADCON	MADC software power on. When set to 1 MADC is powered.	RW	0

Table 135. CTRL2

I2C Address	0x4A		
Physical Address	0x01	**Instance**	MADC
Description	Control register: STARTADCRF is used to control STARTADC detection polarity, and is write protected when MADCON active.USB_INT_MODE is used to configure the way an interrupt is generated from MADC after a VBATMEAS channel conversion when occurs an USB conversion request.VBATREF_MSB register is associated to VBAT Monitoring function (linked with VBATREF Vbat comparator) VBATREF_LSB fields are part of CTRL1 register.		
Type	RW		

7	6	5	4	3	2	1	0
VBATREF_MSB					RESERVED	USB_INT_MODE	STARTADCRF

Bits	Field Name	Description	Type	Reset
7:3	VBATREF_MSB	LSB of the VBAT compared value (5 MSBs) VBATREF_MSB register is associated to VBAT Monitoring function (linked with VBATREF Vbat comparator) VBATREF_LSB field is part of CTRL1 register.	RW	0x00
2	Reserved	reserved for spare	RW	0
1	USB_INT_MODE	Default is 0 meaning that the MADC will sent an interrupt when the value resulting from VBATMEAS channel is under USBREF register value. When 1 then an interrupt is sent every time the conversion value is either going upper or under USBREF value. This is used only in case of USB conversion request.	RW	0
0	STARTADCRF	STARDADC Rising/Falling edge detection bit field. When set to 1 STARDADC is active High (default value)	RW	1

Table 136. RTSELECT_LSB

I2C Address	0x4A		
Physical Address	0x02	**Instance**	MADC
Description	Real time conversion channel selection register for channel 0 to 7. These bits become read-only bits during real time conversion. When the bit CHi is set MADC channel i is inserted in the conversion sequence started by a real time request through STARTADC.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	CH0

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	0
6	Reserved		RW	0
5	Reserved		RW	0
4	Reserved		RW	0
3	Reserved		RW	0
2	Reserved		RW	0
1	Reserved		RW	0
0	CH0	Real-time conversion channel selection register for channel 0	RW	0

Table 137. RTSELECT_MSB

I2C Address	0x4A		
Physical Address	0x03	**Instance**	MADC
Description	Real time conversion channel selection register for channel 8 to 15. These bits become read-only bits during real time conversion. When the bit CHi is set MADC channel i is inserted in the conversion sequence started by a real time request through STARTADC.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	CH12	RESERVED	RESERVED	RESERVED	CH8

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	0
6	Reserved		RW	0
5	Reserved		RW	0
4	CH12	Real-time conversion channel selection register for channel 12	RW	0
3	Reserved		RW	0
2	Reserved		RW	0
1	Reserved		RW	0
0	CH8	Real-time conversion channel selection register for channel 8	RW	0

Table 138. RTAVERAGE_LSB

I2C Address	0x4A		
Physical Address	0x04	**Instance**	MADC
Description	Real time conversion averaging function selection register for channel 0 to 7. These bits become read-only bits during real time conversion. When the bit AV_CHi is set MADC will make an averaging measurement during real time conversion of channel i (i.e., it will measure 4 times consecutively the value and store the average).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	AV_CH0

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	0
6	Reserved		RW	0
5	Reserved		RW	0
4	Reserved		RW	0
3	Reserved		RW	0
2	Reserved		RW	0
1	Reserved		RW	0
0	AV_CH0	Real time conversion averaging function selection register for channel 0	RW	0

Table 139. RTAVERAGE_MSB

I2C Address	0x4A		
Physical Address	0x05	**Instance**	MADC
Description	Real time conversion averaging function selection register for channel 8 to 15. These bits become read-only bits during real time conversion. When the bit AV_CHi is set MADC will make an averaging measurement during real time conversion of channel i (i.e., it will measure 4 times consecutively the value and store the average).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	AV_CH12	RESERVED	RESERVED	RESERVED	AV_CH8

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	0
6	Reserved		RW	0
5	Reserved		RW	0
4	AV_CH12	Real time conversion averaging function selection register for channel 12	RW	0
3	Reserved		RW	0
2	Reserved		RW	0
1	Reserved		RW	0
0	AV_CH8	Real time conversion averaging function selection register for channel 8	RW	0

Table 140. SW1SELECT_LSB

I2C Address	0x4A		
Physical Address	0x06	**Instance**	MADC
Description	S/W1 conversion channel selection register for channel 0 to 7. These bits become Read only bits during S/W conversion initiated by SW1 bit. When the bit CHi is set MADC channel i is inserted in the conversion sequence.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	CH0

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	0
6	Reserved		RW	0
5	Reserved		RW	0
4	Reserved		RW	0
3	Reserved		RW	0
2	Reserved		RW	0
1	Reserved		RW	0
0	CH0	S/W1 conversion channel selection register for channel 0	RW	0

Table 141. SW1SELECT_MSB

I2C Address	0x4A		
Physical Address	0x07	**Instance**	MADC
Description	S/W1 conversion channel selection register for channel 8 to 15. These bits become read-only bits during S/W conversion initiated by SW1 bit. When the bit CHi is set MADC channel i is inserted in the conversion sequence.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	CH12	RESERVED	RESERVED	RESERVED	CH8

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	0
6	Reserved		RW	0
5	Reserved		RW	0
4	CH12	S/W1 conversion channel selection register for channel 12	RW	0
3	Reserved		RW	0
2	Reserved		RW	0
1	Reserved		RW	0
0	CH8	S/W1 conversion channel selection register for channel 8	RW	0

Table 142. SW1AVERAGE_LSB

I2C Address	0x4A		
Physical Address	0x08	**Instance**	MADC
Description	S/W1 conversion averaging function selection register for channel 0 to 7. These bits become read-only bits during S/W 1 conversion. When the bit AV_CHi is set MADC will make an averaging measurement during S/W 1 conversion of channel i i.e. it will measure 4 times consecutively the value and store the average.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	AV_CH0

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	0
6	Reserved		RW	0
5	Reserved		RW	0
4	Reserved		RW	0
3	Reserved		RW	0
2	Reserved		RW	0
1	Reserved		RW	0
0	AV_CH0	S/W1 conversion averaging function selection register for channel 0	RW	0

Table 143. SW1AVERAGE_MSB

I2C Address	0x4A		
Physical Address	0x09	Instance	MADC
Description	S/W1 conversion averaging function selection register for channel 8 to 15. These bits become read-only bits during S/W 1 conversion. When the bit AV_CHi is set MADC will make an averaging measurement during S/W 1 conversion of channel i (i.e., it will measure 4 times consecutively the value and store the average).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	AV_CH12	RESERVED	RESERVED	RESERVED	AV_CH8

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	0
6	Reserved		RW	0
5	Reserved		RW	0
4	AV_CH12	S/W1 conversion averaging function selection register for channel 12	RW	0
3	Reserved		RW	0
2	Reserved		RW	0
1	Reserved		RW	0
0	AV_CH8	S/W1 conversion averaging function selection register for channel 8	RW	0

Table 144. SW2SELECT_LSB

I2C Address	0x4A		
Physical Address	0x0A	Instance	MADC
Description	S/W2 conversion channel selection register for channel 0 to 7. These bits become read-only bits during S/W conversion initiated by SW2 bit. When the bit CHi is set MADC channel i is inserted in the conversion sequence.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	CH0

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	0
6	Reserved		RW	0
5	Reserved		RW	0
4	Reserved		RW	0
3	Reserved		RW	0
2	Reserved		RW	0
1	Reserved		RW	0
0	CH0	S/W2 conversion channel selection register for channel 0	RW	0

Table 145. SW2SELECT_MSB

I2C Address	0x4A		
Physical Address	0x0B	**Instance**	MADC
Description	S/W2 conversion channel selection register for channel 8 to 15. These bits become read-only bits during S/W conversion initiated by SW2 bit. When the bit CHi is set MADC channel i is inserted in the conversion sequence.		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	CH12	RESERVED	RESERVED	RESERVED	CH8

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	0
6	Reserved		RW	0
5	Reserved		RW	0
4	CH12	S/W2 conversion channel selection register for channel 12	RW	0
3	Reserved		RW	0
2	Reserved		RW	0
1	Reserved		RW	0
0	CH8	S/W2 conversion channel selection register for channel 8	RW	0

Table 146. SW2AVERAGE_LSB

I2C Address	0x4A		
Physical Address	0x0C	**Instance**	MADC
Description	S/W2 conversion averaging function selection register for channel 0 to 7. These bits become read-only bits during S/W 2 conversion. When the bit AV_CHi is set MADC will make an averaging measurement during S/W 2 conversion of channel i (i.e., it will measure 4 times consecutively the value and store the average).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	AV_CH0

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	0
6	Reserved		RW	0
5	Reserved		RW	0
4	Reserved		RW	0
3	Reserved		RW	0
2	Reserved		RW	0
1	Reserved		RW	0
0	AV_CH0	S/W2 conversion averaging function selection register for channel 0	RW	0

Table 147. SW2AVERAGE_MSB

I2C Address	0x4A		
Physical Address	0x0D	**Instance**	MADC
Description	S/W2 conversion averaging function selection register for channel 8 to 15. These bits become read-only bits during S/W 2 conversion. When the bit AV_CHi is set MADC will make an averaging measurement during S/W 2 conversion of channel i (i.e. it will measure 4 times consecutively the value and store the average).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	AV_CH12	RESERVED	RESERVED	RESERVED	AV_CH8

Bits	Field Name	Description	Type	Reset
7	Reserved		RW	0
6	Reserved		RW	0
5	Reserved		RW	0
4	AV_CH12	S/W2 conversion averaging function selection register for channel 12	RW	0
3	Reserved		RW	0
2	Reserved		RW	0
1	Reserved		RW	0
0	AV_CH8	S/W2 conversion averaging function selection register for channel 8	RW	0

Table 148. BCI_USBAVERAGE

I2C Address	0x4A		
Physical Address	0x0E	**Instance**	MADC
Description	BCI and USB conversion averaging function selection register for BCI and USB channels. These bits become read-only bits during BCI and USB conversion. When the bit AV_CHi is set MADC will make an averaging measurement during BCI or USB conversion of channel i (i.e., it will measure 4 times consecutively the value and store the average).		
Type	RW		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	AV_USB_CH0	AV_BCI_CH4	RESERVED2	RESERVED	AV_BCI_CH1	RESERVED

Bits	Field Name	Description	Type	Reset
7	Reserved	reserved-reads return 0s	RO	0
6	Reserved	reserved-reads return 0s	RO	0
5	AV_USB_CH0	USB conversion averaging function selection register for channel 0	RW	0
4	AV_BCI_CH4	BCI conversion averaging function selection register for channel 4	RW	0
3	RESERVED2		RW	0
2	Reserved		RW	0
1	AV_BCI_CH1	BCI conversion averaging function selection register for channel 1	RW	0
0	Reserved		RW	0

Table 149. ACQUISITION

I2C Address	0x4A		
Physical Address	0x0F	**Instance**	MADC
Description	Acquisition Time Control Register bit fields.These bits are used to program the analog input settling time. The settling time is programmable from 5us to 20us with 1us steps with BIT_7DT0[3:0] and up to 1 ms with BIT_7DT0[7:4]. The default value is 12 µs (SW1, SW2 and RT). For BCI and USB use, the value is hard coded at 20 µs. These bits need to be written before the MADC set ON. To be able to change the value, no conversion should be running. This value is used for SW1, SW2, and RT conversion modes. This register access (new settling value update) will be effective only if CTRL_SW1 and CTRL_SW2 busy bits is 0 (no conversions running) . That mean that before writing to this register in order to change settling value, first SW need to read CTRL_SW1 or CTRL_SW2 busy bits to 0.		
Type	RW		

7	6	5	4	3	2	1	0
BIT_7DT0							

Bits	Field Name	Description	Type	Reset
7:0	BIT_7DT0	Acquisition Time Control Register. These bits become Read only bits when the BUSY signal is set (on going conversion). These bits are used to program the analog input settling time. The settling time is programmable from 5 µs to 20 µs with 1-µs steps. The default value is 12 µs. These bit need to be written before the MADC set ON. To be able to change the value, no conversion should be running. This value is used for SW1, SW2 and RT conversion modes.	RW	0x07

Table 150. USBREF_LSB

I2C Address	0x4A		
Physical Address	0x10	**Instance**	MADC
Description	LSB of the Reference value to be compared to the conversion result asked by the USB for VBAT conversion.		
Type	RW		

7	6	5	4	3	2	1	0
BIT_1DT0		RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	LSB of the VBAT compared value (2 LSBs)	RW	0x3
5	Reserved	Reserved-reads return 0s	RO	0
4	Reserved	Reserved-reads return 0s	RO	0
3	Reserved	Reserved-reads return 0s	RO	0
2	Reserved	Reserved-reads return 0s	RO	0
1	Reserved	Reserved-reads return 0s	RO	0
0	Reserved	Reserved-reads return 0s	RO	0

Table 151. USBREF_MSB

I2C Address	0x4A		
Physical Address	0x11	**Instance**	MADC
Description	MSB of the Reference value to be compared to the conversion result asked by the USB for VBAT conversion.		
Type	RW		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	MSB of the VBAT compared value (8 MSB's)	RW	0x8C

Table 152. CTRL_SW1

I2C Address	0x4A		
Physical Address	0x12	**Instance**	MADC
Description	MADC Busy signal. When this bit is at 1, the MADC is running its sequence of conversions. It is the same bit as the BUSY bit in the CTRL_SW2 register.USBREF_STS and VBATREF_STS fields are status bit (read only) that give status of respectively USBREF and VBATREF Vbat monitoring output comparator, the same two duplicated status bits are also included inside CTRL_SW12 register.		
Type	RW		

7	6	5	4	3	2	1	0
VBATREF_STS	USBREF_STS	SW1	EOC_USB	RESERVED	EOC_RT	EOC_SW1	BUSY

Bits	Field Name	Description	Type	Reset
7	VBATREF_STS	VBATREF/VBAT comparator status bit. When 1 measured Vbat is greater than VBATREF value programmed in VBATREF_LSB and VBATREF_MSB fields inside CTRL1/CTRL2 registers, else status is 0. It is the same bit as the VBATREF_STS bit in the CTRL_SW2 register.	RO	1
6	USBREF_STS	USBREF/VBAT comparator status bit. When 1 measured Vbat is greater than USBREF value programmed inside USBREF_LSB and USBREF_MSB registers, else status is 0. It is the same bit as the USBREF_STS bit in the CTRL_SW2 register.	RO	1
5	SW1	S/W 1.Toggle bit used by the host processor to start an all channel conversion. Writing logical 0 in this bit has no effect.	WO	0
4	EOC_USB	End Of Conversion USB. When this bit is set MADC indicates that conversion required by USB bit is terminated. An interrupt has been sent at the end of required conversion sequence to the interrupts controller. Default state is logic 1 indicating that the conversion is terminated. While associated conversion sequence is running this bit is at logical 0. This bit is the same as the EOC_USB bit in the CTRL_SW2 register.	RO	1
3	Reserved		RO	1
2	EOC_RT	End Of Conversion Real Time. When this bit is set MADC indicates that conversion with real time constraints is terminated. An interrupt has been sent at the end of required conversion sequence to the interrupts controller. Default state is logic 1 indicating that the conversion is terminated. While associated conversion sequence is running this bit is at logical 0. It is the same bit as the EOC_RT bit in the CTRL_SW2 register.	RO	1
1	EOC_SW1	End Of Conversion S/W 1. When this bit is set MADC indicates that conversion required by SW1 bit is terminated. An interrupt has been sent at the end of required conversion sequence to the interrupts controller. Default state is logic 1 indicating that the conversion is terminated. While associated conversion sequence is running this bit is at logical 0.	RO	1
0	BUSY	MADC Busy signal. When this bit is at 1, the MADC is running its sequence of conversions. It is the same bit as the BUSY bit in the CTRL_SW2 register.	RO	0

Table 153. CTRL_SW2

I2C Address	0x4A		
Physical Address	0x13	**Instance**	MADC
Description	End Of Conversion BCI. When this bit is set MADC indicates that BCI conversion is terminated. A data ready signal has been sent at the end of required conversion sequence to the BCI. Default state is logic 1 indicating that the conversion is terminated. While associated conversion sequence is running this bit is at logical 0. It is the same bit as the EOC_BCI bit in the CTRL_SW1 register.USBREF_STS and VBATREF_STS fields are status bit (read only) that give status of respectively USBREF and VBATREF Vbat monitoring output comparator, the same two duplicated status bits are also included inside CTRL1 register.		
Type	RW		

7	6	5	4	3	2	1	0
VBATREF_STS	USBREF_STS	SW2	EOC_USB	RESERVED	EOC_RT	EOC_SW2	BUSY

Bits	Field Name	Description	Type	Reset
7	VBATREF_STS	VBATREF/VBAT comparator status bit. When 1 measured Vbat is greater than VBATREF value programmed in VBATREF_LSB and VBATREF_MSB fields inside CTRL1/CTRL2 registers, else status is 0. It is the same bit as the VBATREF_STS bit in the CTRL_SW1 register.	RO	1
6	USBREF_STS	USBREF/VBAT comparator status bit. When 1 measured Vbat is greater than USBREF value programmed inside USBREF_LSB and USBREF_MSB registers, else status is 0. It is the same bit as the USBREF_STS bit in the CTRL_SW1 register.	RO	1
5	SW2	S/W 2.Toggle bit used by the host processor to start an all channel conversion. Writing logical 0 in this bit has no effect.	WO	0
4	EOC_USB	End Of Conversion USB. When this bit is set MADC indicates that conversion required by USB bit is terminated. An interrupt has been sent at the end of required conversion sequence to the interrupts controller. Default state is logic 1 indicating that the conversion is terminated. While associated conversion sequence is running this bit is at logical 0. This bit is the same as the EOC_USB bit in the CTRL_SW1 register.	RO	1
3	Reserved		RO	1
2	EOC_RT	End Of Conversion Real Time. When this bit is set MADC indicates that conversion with real time constraints is terminated. An interrupt has been sent at the end of required conversion sequence to the interrupts controller. Default state is logic 1 indicating that the conversion is terminated. While associated conversion sequence is running this bit is at logical 0. This bit is the same as the EOC_RT bit in the CTRL_SW1 register.	RO	1
1	EOC_SW2	End Of Conversion S/W 2. When this bit is set MADC indicates that conversion required by SW2 bit is terminated. An interrupt has been sent at the end of required conversion sequence to the interrupts controller. Default state is logic 1 indicating that the conversion is terminated. While associated conversion sequence is running this bit is at logical 0.	RO	1
0	BUSY	MADC Busy signal. When this bit is at 1, the MADC is running its sequence of conversions. It is the same bit as the BUSY bit in the CTRL_SW1 register.	RO	0

Table 154. RTCH0_LSB

I2C Address	0x4A		
Physical Address	0x17	**Instance**	MADC
Description	Channel 0 RT Conversion Result Register (ADIN0 = BTYPE).		
Type	RO		

7	6	5	4	3	2	1	0
BIT_1DT0		RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 0 result of conversion (2 LSBs).	RO	0x0
5	Reserved	Reserved-reads return 0s	RO	0
4	Reserved	Reserved-reads return 0s	RO	0
3	Reserved	Reserved-reads return 0s	RO	0
2	Reserved	Reserved-reads return 0s	RO	0
1	Reserved	Reserved-reads return 0s	RO	0
0	Reserved	Reserved-reads return 0s	RO	0

Table 155. RTCH0_MSB

I2C Address	0x4A		
Physical Address	0x18	**Instance**	MADC
Description	Channel 0 RT Conversion Result Register (ADIN0 = BTYPE).		
Type	RO		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 0 result of conversion (8 MSBs).	RO	0x00

Table 156. RTCH8_LSB

I2C Address	0x4A		
Physical Address	0x27	**Instance**	MADC
Description	Channel 8 RT Conversion Result Register (USBVBUS).		
Type	RO		

7	6	5	4	3	2	1	0
BIT_1DT0		RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 8 result of conversion (2 LSBs).	RO	0x0
5	Reserved	Reserved-reads return 0s	RO	0
4	Reserved	Reserved-reads return 0s	RO	0
3	Reserved	Reserved-reads return 0s	RO	0
2	Reserved	Reserved-reads return 0s	RO	0
1	Reserved	Reserved-reads return 0s	RO	0
0	Reserved	Reserved-reads return 0s	RO	0

Table 157. RTCH8_MSB

I2C Address	0x4A		
Physical Address	0x28	Instance	MADC
Description	Channel 8 RT Conversion Result Register (USBVBUS).		
Type	RO		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 8 result of conversion (8 MSBs).	RO	0x00

Table 158. RTCH12_LSB

I2C Address	0x4A		
Physical Address	0x2F	Instance	MADC
Description	Channel 12 RT Conversion Result Register (VBAT).		
Type	RO		

7	6	5	4	3	2	1	0
BIT_1DT0		RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 12 result of conversion (2 LSBs).	RO	0x0
5	Reserved	Reserved-reads return 0s	RO	0
4	Reserved	Reserved-reads return 0s	RO	0
3	Reserved	Reserved-reads return 0s	RO	0
2	Reserved	Reserved-reads return 0s	RO	0
1	Reserved	Reserved-reads return 0s	RO	0
0	Reserved	Reserved-reads return 0s	RO	0

Table 159. RTCH12_MSB

I2C Address	0x4A		
Physical Address	0x30	Instance	MADC
Description	Channel 12 RT Conversion Result Register (VBAT).		
Type	RO		

7	6	5	4	3	2	1	0
BIT_9DT2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 12 result of conversion (8 MSBs).	RO	0x00

Table 160. GPCH0_LSB

I2C Address	0x4A		
Physical Address	0x37	**Instance**	MADC
Description	Channel 0 GP Conversion Result Register (ADIN0 = BTYPE).		
Type	RO		

7	6	5	4	3	2	1	0
BIT_1DT0		RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 0 result of conversion (2 LSBs).	RO	0x0
5	Reserved	Reserved-reads return 0s	RO	0
4	Reserved	Reserved-reads return 0s	RO	0
3	Reserved	Reserved-reads return 0s	RO	0
2	Reserved	Reserved-reads return 0s	RO	0
1	Reserved	Reserved-reads return 0s	RO	0
0	Reserved	Reserved-reads return 0s	RO	0

Table 161. GPCH0_MSB

I2C Address	0x4A		
Physical Address	0x38	**Instance**	MADC
Description	Channel 0 GP Conversion Result Register (ADIN0 = BTYPE).		
Type	RO		

7	6	5	4	3	2	1	0
BIT_9dt2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 0 result of conversion (8 MSBs).	RO	0x00

Table 162. GPCH8_LSB

I2C Address	0x4A		
Physical Address	0x47	**Instance**	MADC
Description	Channel 8 GP Conversion Result Register (USBVBUS).		
Type	RO		

7	6	5	4	3	2	1	0
BIT_1dt0		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 8 result of conversion (2 LSBs).	RO	0x0
5	Reserved	Reserved-reads return 0s	RO	0
4	Reserved	Reserved-reads return 0s	RO	0
3	Reserved	Reserved-reads return 0s	RO	0
2	Reserved	Reserved-reads return 0s	RO	0
1	Reserved	Reserved-reads return 0s	RO	0
0	Reserved	Reserved-reads return 0s	RO	0

Table 163. GPCH8_MSB

I2C Address	0x4A			
Physical Address	0x48	Instance	MADC	
Description	Channel 8 GP Conversion Result Register (USBVBUS).			
Type	RO			

7	6	5	4	3	2	1	0
BIT_9dt2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 8 result of conversion (8 MSBs).	RO	0x00

Table 164. GPCH12_LSB

I2C Address	0x4A			
Physical Address	0x4F	Instance	MADC	
Description	Channel 12 GP Conversion Result Register (VBAT).			
Type	RO			

7	6	5	4	3	2	1	0
BIT_1dt0		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 12 result of conversion (2 LSBs).	RO	0x0
5	Reserved	Reserved-reads return 0s	RO	0
4	Reserved	Reserved-reads return 0s	RO	0
3	Reserved	Reserved-reads return 0s	RO	0
2	Reserved	Reserved-reads return 0s	RO	0
1	Reserved	Reserved-reads return 0s	RO	0
0	Reserved	Reserved-reads return 0s	RO	0

Table 165. GPCH12_MSB

I2C Address	0x4A			
Physical Address	0x50	Instance	MADC	
Description	Channel 12 GP Conversion Result Register (VBAT).			
Type	RO			

7	6	5	4	3	2	1	0
BIT_9dt2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 12 result of conversion (8 MSBs).	RO	0x00

Table 166. BCICH1_LSB

I2C Address	0x4A			
Physical Address	0x59	Instance	MADC	
Description	Channel 1 BCI Conversion Result Register ("ADCIN8=USBVBUS").			
Type	RO			

7	6	5	4	3	2	1	0
BIT_1dt0		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 1 result of conversion (2 LSBs).	RO	0x0
5	Reserved	Reserved-reads return 0s	RO	0
4	Reserved	Reserved-reads return 0s	RO	0
3	Reserved	Reserved-reads return 0s	RO	0
2	Reserved	Reserved-reads return 0s	RO	0
1	Reserved	Reserved-reads return 0s	RO	0
0	Reserved	Reserved-reads return 0s	RO	0

Table 167. BCICH1_MSB

I2C Address	0x4A			
Physical Address	0x5A	Instance	MADC	
Description	Channel 1 BCI Conversion Result Register ("ADCIN8=USBVBUS")..			
Type	RO			

7	6	5	4	3	2	1	0
BIT_9dt2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 1 result of conversion (8 MSBs).	RO	0x00

Table 168. BCICH4_LSB

I2C Address	0x4A			
Physical Address	0x5F	Instance	MADC	
Description	Channel 4 BCI Conversion Result Register ("ADCIN12 = VBAT").			
Type	RO			

7	6	5	4	3	2	1	0
BIT_1dt0		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Bits	Field Name	Description	Type	Reset
7:6	BIT_1DT0	Channel 4 result of conversion (2 LSBs).	RO	0x0
5	Reserved	Reserved-reads return 0s	RO	0
4	Reserved	Reserved-reads return 0s	RO	0
3	Reserved	Reserved-reads return 0s	RO	0
2	Reserved	Reserved-reads return 0s	RO	0
1	Reserved	Reserved-reads return 0s	RO	0
0	Reserved	Reserved-reads return 0s	RO	0

Table 169. BCICH4_MSB

I2C Address	0x4A			
Physical Address	0x60	Instance	MADC	
Description	Channel 4 BCI Conversion Result Register ("ADCIN12 = VBAT").			
Type	RO			

7	6	5	4	3	2	1	0
BIT_9dt2							

Bits	Field Name	Description	Type	Reset
7:0	BIT_9DT2	Channel 4 result of conversion (8 MSBs).	RO	0x00

Table 170. MADC_ISR1

I2C Address	0x4A		
Physical Address	0x61	Instance	MADC
Description	The INTERRUPT STATUS ISR1 REGISTERs is used to determine which of the end of sequences (RT, SW1, SW2, and USB) triggered the interrupt line po_madc_p1_n request. When a bit in this register is set to 1, it indicates that the corresponding end of sequence is requesting the interrupt. However, the user cannot generate an interrupt by writing a 1 to the INTERRUPT STATUS ISR1 REGISTER. When a bit in this register is set to 1 then the corresponding interrupt line is released. If the user writes a 0 to a bit in this register, the value will remain unchanged. The INTERRUPT STATUS ISR1 REGISTER is synchronous with the interface OCP clock.		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	USB_ISR1	SW2_ISR1	SW1_ISR1	RT_ISR1

Bits	Field Name	Description	Type	Reset
7	Reserved	Reserved-reads return 0s	RO	0
6	Reserved	Reserved-reads return 0s	RO	0
5	Reserved	Reserved-reads return 0s	RO	0
4	Reserved	Reserved-reads return 0s	RO	0
3	USB_ISR1	0: Interrupt not set 1: Interrupt set	RW	0
2	SW2_ISR1	0: Interrupt not set 1: Interrupt set	RW	0
1	SW1_ISR1	0: Interrupt not set 1: Interrupt set	RW	0
0	RT_ISR1	0: Interrupt not set 1: Interrupt set	RW	0

Table 171. MADC_IMR1

I2C Address	0x4A		
Physical Address	0x62	**Instance**	MADC
Description	The INTERRUPT MASK IMR1 REGISTER allows the user to mask the expected transition on end of sequence from generating an interrupt request on po_madc_p1_n. The INTERRUPT MASK REGISTERS are programmed synchronously with the interface OCP clock.		
Type	RW		

7	6	5	4	3	2	1	0
RSVD4	RSVD3	RSVD2	RSVD1	USB_IMR1	SW2_IMR1	SW1_IMR1	RT_IMR1

Bits	Field Name	Description	Type	Reset
7	RSVD4	Reserved-reads return 0s	RO	0
6	RSVD3	Reserved-reads return 0s	RO	0
5	RSVD2	Reserved-reads return 0s	RO	0
4	RSVD1	Reserved-reads return 0s	RO	0
3	USB_IMR1	0: Interrupt is not masked 1: Interrupt is masked	RW	1
2	SW2_IMR1	0: Interrupt is not masked 1: Interrupt is masked	RW	1
1	SW1_IMR1	0: Interrupt is not masked 1: Interrupt is masked	RW	1
0	RT_IMR1	0: Interrupt is not masked 1: Interrupt is masked	RW	1

Table 172. MADC_EDR

I2C Address	0x4A		
Physical Address	0x66	**Instance**	MADC
Description	The INTERRUPT EDGE DETECTION REGISTER MADC_EDR allows the user to define, for all signals 'end of real time sequence', 'end of SW1 sequence', 'end of SW2 sequence' and 'end of USB sequence' the expected edge to trigger an interrupt request. The interrupt request can be either generated from a High to Low transition (bits are 01), a Low to High transition (bits are 10) or both transitions (bits are 11) accruing. To get the falling edge detection capability, the relevant bits corresponding to the MADC need to be reset (55).		
Type	RW		

7	6	5	4	3	2	1	0
USB_EDRRISING	USB_EDRFALLING	SW2_EDRRISING	SW2_EDRFALLING	SW1_EDRRISING	SW1_EDRFALLING	RT_EDRRISING	RT_EDRFALLING

Bits	Field Name	Description	Type	Reset
7	USB_EDRRISING	USB rising-edge interrupt event detection control register.	RW	0
6	USB_EDRFALLING	USB falling-edge interrupt event detection control register.	RW	1
5	SW2_EDRRISING	SW2 rising-edge interrupt event detection control register.	RW	0
		0: Rising detection disabled		
		1: Rising detection enabled		
4	SW2_EDRFALLING	SW2 falling-edge interrupt event detection control register.	RW	1
		0: Falling detection disabled		
		1: Falling detection enabled		
3	SW1_EDRRISING	SW1 rising-edge interrupt event detection control register.	RW	0
		0: Rising detection disabled		
		1: Rising detection enabled		
2	SW1_EDRFALLING	SW1 falling-edge interrupt event detection control register.	RW	1
		0: Falling detection disabled		
		1: Falling detection enabled		
1	RT_EDRRISING	RT rising-edge interrupt event detection control register.	RW	0
		0: Rising detection disabled		
		1: Rising detection enabled		
0	RT_EDRFALLING	RT falling-edge interrupt event detection control register.	RW	1
		0: Falling detection disabled		
		1: Falling detection enabled		

Table 173. MADC_SIH_CTRL

I2C Address	0x4A		
Physical Address	0x67	**Instance**	MADC
Description	The MADC SIH CONTROL REGISTER allow the user to disable a pending event incoming during SW interrupt latency by programming 1 in PENDDIS field.The ClearOnRead bit field enable Clear on Read feature. That mean that any read access to the ISR clear this register and release the interrupt line associated (default value). If disabled a read access to a specific address value will clear all ISR within the SIH.		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	COR	PENDDIS	Reserved

Bits	Field Name	Description	Type	Reset
7	Reserved	Reads return 0s.	RO	0
6	Reserved	Reads return 0s.	RO	0
5	Reserved	Reads return 0s.	RO	0
4	Reserved	Reads return 0s.	RO	0
3	Reserved	Reads return 0s.	RO	0
2	COR	1 : Clear ISR on read 0 : Clear ISR specific bit field when write access	RW	1
1	PENDDIS	0 : Pending event enabled 1 : Pending event disabled	RW	1
0	Reserved		RW	1

4.3 ACCESSORY_VINTDIG

This section provides information on the ACCESSORY_VINTDIG module instances within this product. Each of the registers within the different ACCESSORY_VINTDIG module instances is described separately below.

4.3.1 ACCESSORY_VINTDIG Registers Mapping Summary

Table 174. ACCESSORY_VINTDIG Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	Address Offset	Physical Address
USB_DTCT_CTRL	RW	8	0x00	0x02	0x76
USB_SW_CHRG_CTRL	RW	8	0x30	0x03	0x77
BCIA_CTRL	RW	8	0x00	0x04	0x78
ACCISR1	RW	8	0x00	0x05	0x79
ACCIMR1	RW	8	0x01	0x06	0x7A
ACCEDR1	RW	8	0x02	0x0A	0x7E
ACCSIHCTRL	RW	8	0x01	0x0B	0x7F
SPARE1	RO	8	0x00	0x0F	0x83
SPARE2	RW	8	0x00	0x10	0x84

4.3.2 ACCESSORY_VINTDIG Register Descriptions

Table 175. USB_DTCT_CTRL

I2C Address	0x4A			
Physical Address	0x76	**Instance**	ACCESSORY_VINTDIG	
Description	Battery Charger Controller (BCC) status bits			
Type	RW			

7	6	5	4	3	2	1	0
Reserved	USB_500	USB_100	USB_P_STS	USB_DET_STS		USB_SW_CHRG_CTRL_EN	USB_HW_CHRG_DET_EN

Bits	Field Name	Description	Type	Reset
7	Reserved		RORreturns0s	0
6	USB_500	Can be write only when USB_SW_CHRG_CTRL_EN is set to 1. Set USB500_P signal. Status of FSM USB500_P when USB_SW_CHRG_CTRL_EN is disabled and USB_HW_CHRG_DET_EN set to 1.	RW	0
5	USB_100	Can be write only when USB_SW_CHRG_CTRL_EN is set to 1. Set USB100_P signal. Status of FSM USB100_P when USB_SW_CHRG_CTRL_EN is disabled and USB_HW_CHRG_DET_EN set to 1.	RW	0
4	USB_P_STS	Status of USBVBUS_PRES signal with 10 ms debounce time. When set to 1, USB FSM is active according to enable bit setting.	RO	0
3:2	USB_DET_STS	Status of USB charger presence and USB charger type. Read 0x0: 00 => No USB charger detected. Read 0x1: 01 => 100 mA charger detected. Read 0x2: 10 => 500 mA charger detected. Read 0x3: 11 => Undefined.	RO	0x0
1	USB_SW_CHRG_CTRL_EN	Let the software control USB current sources and comparator outputs directly through register. USB dedicated FSM for detection is bypassed if this bit is set to 1.	RW	0
0	USB_HW_CHRG_DET_EN	SW enable of USB Hardware fsm for USB detection.Enable automatic Charger Detection (used to enable CHGD IBIAS block). Once enabled, Interrupt USB_CHG_TYPE is generated once detection has detected a USB100mA or USB 500mA charger.	RW	0

Table 176. USB_SW_CHRG_CTRL

I2C Address	0x4A		
Physical Address	0x77	Instance	ACCESSORY_VINTDIG
Description			
Type	RW		

7	6	5	4	3	2	1	0
USB_CHG_DET_EN_SW	VBUSOV_PRECH	CHGD_SERX_DM_LOWV	CHGD_SERX_DP_LOWV	CHGD_VDX_LOWV	CHGD_SERX_EN_LOWV	CHGD_VDX_SRC_EN_LOWV	CHGD_IDX_SRC_EN_LOWV

Bits	Field Name	Description	Type	Reset
7	USB_CHG_DET_EN_SW	This bit enable the USB analog charger detcetion module.This bit must be enabled once USB_SW_CHRG_CTRL_EN is set. Once USB_HW_CHRG_CTRL_EN is set, thsi bit is controlled by USB FSM and status only can be read here.	RW	0
6	VBUSOV_PRECH	Status of VBUSOVPRECH.	RO	0
5	CHGD_SERX_DM_LOWV	Dedicated CHGD SERX DM comparator output used in contact detect.	RO	1
4	CHGD_SERX_DP_LOWV	Dedicated CHGD SERX DP comparator output used in contact detect.	RO	1
3	CHGD_VDX_LOWV	VDAT_REF DM comparator output used in charger detect if DPDM_SWAP eeprom bit is 0.	RO	0
2	CHGD_SERX_EN_LOWV	Enable SERX comparators on DP & DM	RW	0
1	CHGD_VDX_SRC_EN_LOWV	Enable VDP_SRC buffer, IDM_SINK, and VDAT_REF_DM comp.	RW	0
0	CHGD_IDX_SRC_EN_LOWV	Enable IDP_SRC and RDM_DWN if DPDM_SWAP eeprom bit is 0.	RW	0

Table 177. BCIA_CTRL

I2C Address	0x4A		
Physical Address	0x78	Instance	ACCESSORY_VINTDIG
Description			
Type	RW		

7	6	5	4	3	2	1	0
Reserved							MESBAT_EN

Bits	Field Name	Description	Type	Reset
7:1	Reserved		RORreturns0s	0x00
0	MESBAT_EN	Must be set to 1 before battery measure through MADC.	RW	0

Table 178. ACCISR1

I2C Address	0x4A		
Physical Address	0x79	**Instance**	ACCESSORY_VINTDIG
Description	The INTERRUPT STATUS ISR1A REGISTERs is used to determine which monitoring function interrupt triggered the interrupt line PO_BCI_SIH_INT1_N request. When a bit in this register is set to 1, it indicates that the corresponding monitoring function is requesting the interrupt. However, the user cannot generate an interrupt by writing a 1 to the INTERRUPT STATUS ISR1 REGISTER. When a bit in this register is set to 1 then the corresponding interrupt line is released. If the user writes a 0 to a bit in this register, the value will remain unchanged. The INTERRUPT STATUS ISR1 REGISTER is synchronous with the interface OCP clock.		
Type	RW		

7	6	5	4	3	2	1	0
Reserved							USB_CHRG_TYPE_ISR1

Bits	Field Name	Description	Type	Reset
7:1	Reserved		RO	0x00
0	USB_CHRG_TYPE_ISR1	Interrupt USB_CHG_TYPE is generated once automatic detection has detected a USB100mA or USB 500mA charger.This interrupt is only available when Write 0: No impact. Register keeps its value. Read 0: No interrupt set. Read 1: Interrupt set. Write 1: When set to 1, then the corresponding interrupt line is released	RW	0

Table 179. ACCIMR1

I2C Address	0x4A		
Physical Address	0x7A	**Instance**	ACCESSORY_VINTDIG
Description	The INTERRUPT MASK IMR1 REGISTER allows the user to mask the expected transition on end of sequence from generating an interrupt request on PO_BCI_SIH_INT1_N. The INTERRUPT MASK REGISTERS are programmed synchronously with the interface OCP clock.		
Type	RW		

7	6	5	4	3	2	1	0
Reserved							USB_CHRG_TYPE_IMR1

Bits	Field Name	Description	Type	Reset
7:1	Reserved		RORreturns0s	0x00
0	USB_CHRG_TYPE_IMR1	0: Interrupt is not masked 1: Interrupt is masked	RW	1

Table 180. ACCEDR1

I2C Address	0x4A		
Physical Address	0x7E	**Instance**	ACCESSORY_VINTDIG
Description	The INTERRUPT EDGE DETECTION REGISTER ACC_EDR allows the user to define, for all incoming interrupt lines, the expected edge to trigger an interrupt request. The interrupt request can be either generated from a High to Low transition (bits are 01), a Low to High transition (bits are 10) or both transitions (bits are 11) accruing. To disable the edge detection capability, the relevant bits need to be reset (00).		
Type	RW		

7	6	5	4	3	2	1	0
Reserved						USB_CHRG_TYPE_EDRISING	USB_CHRG_TYPE_EDFALLING

Bits	Field Name	Description	Type	Reset
7:2	Reserved		RORreturns0s	0x00
1	USB_CHRG_TYPE_EDRISING	0: Rising detection disabled 1: Rising detection enabled	RW	1
0	USB_CHRG_TYPE_EDFALLING	0: Falling detection disabled 1: Falling detection enabled	RW	0

Table 181. ACCSIHCTRL

I2C Address	0x4A		
Physical Address	0x7F	**Instance**	ACCESSORY_VINTDIG
Description	The ACC SIH CONTROL REGISTER allows the user to disable a pending event incoming during SW interrupt latency by programming 1 in PENDDIS field.The ClearOnRead bit field enable Clear on Read feature. That mean that any read access to the ISR clear this register and release the interrupt line associated (default value). If disabled a read access to a specific address value will clear all ISR within the SIH.		
Type	RW		

7	6	5	4	3	2	1	0
Reserved					COR	PENDDIS	Reserved

Bits	Field Name	Description	Type	Reset
7:3	Reserved		RORreturns0s	0x00
2	COR	0: Clear ISR on write 1: Clear ISR specific bit field when read access	RW	0
1	PENDDIS	0: Pending event enabled 1: Pending event disabled	RW	0
0	Reserved		RW	1

Table 182. SPARE1

I2C Address	0x4A		
Physical Address	0x83	**Instance**	ACCESSORY_VINTDIG
Description			
Type	RO		

7	6	5	4	3	2	1	0
Reserved							

Bits	Field Name	Description	Type	Reset
7:0	Reserved		RO	0x00

Table 183. SPARE2

I2C Address	0x4A		
Physical Address	0x84	**Instance**	ACCESSORY_VINTDIG
Description			
Type	RW		

7	6	5	4	3	2	1	0
Reserved							

Bits	Field Name	Description	Type	Reset
7:0	Reserved		RW	0x00

4.4 Keypad

This section provides information on the keypad module instances within AUX. Each of the registers within the different keypad module instances is described separately below.

4.4.1 Keypad Registers Mapping Summary

Table 184. Keypad Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	Address Offset	Physical Address
KEYP_CTRL_REG	RW	8	0x03	0x00	0xD2
KEY_DEB_REG	RW	8	0x00	0x01	0xD3
LONG_KEY_REG1	RW	8	0x00	0x02	0xD4
LK_PTV_REG	RW	8	0xE0	0x03	0xD5
TIME_OUT_REG1	RW	8	0x00	0x04	0xD6
TIME_OUT_REG2	RW	8	0x00	0x05	0xD7
KBC_REG	RW	8	0xFF	0x06	0xD8
KBR_REG	RO	8	0xFF	0x07	0xD9
KEYP_SMS	RW	8	0x00	0x08	0xDA
FULL_CODE_7_0	RO	8	0x00	0x09	0xDB
FULL_CODE_15_8	RO	8	0x00	0x0A	0xDC
FULL_CODE_23_16	RO	8	0x00	0x0B	0xDD
FULL_CODE_31_24	RO	8	0x00	0x0C	0xDE
FULL_CODE_39_32	RO	8	0x00	0x0D	0xDF
FULL_CODE_47_40	RO	8	0x00	0x0E	0xE0
FULL_CODE_55_48	RO	8	0x00	0x0F	0xE1
FULL_CODE_63_56	RO	8	0x00	0x10	0xE2
KEYP_ISR1	RW	8	0x00	0x11	0xE3
KEYP_IMR1	RW	8	0x0F	0x12	0xE4
KEYP_EDR	RW	8	0x55	0x16	0xE8
KEYP_SIH_CTRL	RW	8	0x01	0x17	0xE9

4.4.2 Keypad Register Descriptions

Table 185. KEYP_CTRL_REG

I2C Address	0x4A		
Physical Address	0xD2	**Instance**	keypad
Description	Keypad control register is used to control keypad mode [software/hardware decoding mode] , event mode detection [long key/timeout/repeat].KBD ON is used to power keypad on by requesting the required functional clock.		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	KBD_ON	RP_EN	TOLE_EN	TOE_EN	LK_EN	SOFTMODEN	SOFT_NRST

Bits	Field Name	Description	Type	Reset
7	Reserved	Reads return 0s.	RO	0
6	KBD_ON	1: Enable keypad power on (clock is requested).	RW	0
5	RP_EN	1: Enable repeat mode detection	RW	0
4	TOLE_EN	1: Enable timeout long key detection	RW	0
3	TOE_EN	1: Enable timeout empty detection	RW	0
2	LK_EN	1: Enable long key process detection	RW	0
1	SOFTMODEN	0: Enable software mode using kbr_latch_reg and kbc_regConfigure SIH to receive kbr "and". 1: Hardware decoding using internal sequencer	RW	1
0	SOFT_NRST	0: Reset 1: Normal operation	RW	1

Table 186. KEY_DEB_REG

I2C Address	0x4A		
Physical Address	0xD3	**Instance**	keypad
Description	The value written to this register corresponds to the desired value of debouncing time.		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		KEYP_DEB					

Bits	Field Name	Description	Type	Reset
7:6	Reserved	Reads return 0s.	RO	0x0
5:0	KEYP_DEB	Debouncing time preset value	RW	0x00

Table 187. LONG_KEY_REG1

I2C Address	0x4A		
Physical Address	0xD4	**Instance**	keypad
Description	The value written to this register corresponds to the desired LSB value of the long key interrupt or repeat mode value		
Type	RW		

7	6	5	4	3	2	1	0
LSB_LK							

Bits	Field Name	Description	Type	Reset
7:0	LSB_LK	Long key LSB preset value	RW	0x00

Table 188. LK_PTV_REG

I2C Address	0x4A		
Physical Address	0xD5	**Instance**	keypad
Description	The value written to this register bit field 3:0 corresponds to the desired MSB value of the long key interrupt or repeat mode value.The value written to bifield 7:5 correspond to the prescaler timer value		
Type	RW		

7	6	5	4	3	2	1	0
PTV			Reserved	MSB_LK			

Bits	Field Name	Description	Type	Reset
7:5	PTV	Prescaler timer value	RW	0x7
4	Reserved	Reads return 0s.	RO	0
3:0	MSB_LK	Long key MSB preset value	RW	0x0

Table 189. TIME_OUT_REG1

I2C Address	0x4A		
Physical Address	0xD6	**Instance**	keypad
Description	The value written to this register corresponds to the desired LSB value of the timeout interrupt		
Type	RW		

7	6	5	4	3	2	1	0
LSB_TO							

Bits	Field Name	Description	Type	Reset
7:0	LSB_TO	Timeout LSB preset value	RW	0x00

Table 190. TIME_OUT_REG2

I2C Address	0x4A		
Physical Address	0xD7	**Instance**	keypad
Description	The value written to this register corresponds to the desired MSB value of the timeout interrupt		
Type	RW		

7	6	5	4	3	2	1	0
MSB_TO							

Bits	Field Name	Description	Type	Reset
7:0	MSB_TO	Timeout MSB preset value	RW	0x00

Table 191. KBC_REG

I2C Address	0x4A		
Physical Address	0xD8	**Instance**	keypad
Description	This register is used to manage the scanning sequence in software sequencing mode. The register values drives output column pins.		
Type	RW		

7	6	5	4	3	2	1	0
KBC7	KBC6	KBC5	KBC4	KBC3	KBC2	KBC1	KBC0

Bits	Field Name	Description	Type	Reset
7	KBC7	Drive KBC7 output pin	RW	1
6	KBC6	Drive KBC6 output pin	RW	1
5	KBC5	Drive KBC5 output pin	RW	1
4	KBC4	Drive KBC4 output pin	RW	1
3	KBC3	Drive KBC3 output pin	RW	1
2	KBC2	Drive KBC2 output pin	RW	1
1	KBC1	Drive KBC1 output pin	RW	1
0	KBC0	Drive KBC0 output pin	RW	1

Table 192. KBR_REG

I2C Address	0x4A		
Physical Address	0xD9	**Instance**	keypad
Description	This register is used to manage the decoding sequence in software sequencing mode and to sample the row input line in this mode.		
Type	RO		

7	6	5	4	3	2	1	0
KBR7	KBR6	KBR5	KBR4	KBR3	KBR2	KBR1	KBR0

Bits	Field Name	Description	Type	Reset
7	KBR7	Reflect KBR7 input pin	RO	1
6	KBR6	Reflect KBR6 input pin	RO	1
5	KBR5	Reflect KBR5 input pin	RO	1
4	KBR4	Reflect KBR4 input pin	RO	1
3	KBR3	Reflect KBR3 input pin	RO	1
2	KBR2	Reflect KBR2 input pin	RO	1
1	KBR1	Reflect KBR1 input pin	RO	1
0	KBR0	Reflect KBR0 input pin	RO	1

Table 193. KEYP_SMS

I2C Address	0x4A		
Physical Address	0xDA	**Instance**	keypad
Description	This test register indicate the current status of the sequencer state mahine, and enabled SIR test mode of the instantiated SIH.		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		MISS_EN	SIR_EN	STMSTS			

Bits	Field Name	Description	Type	Reset
7:6	Reserved	Reads return 0s.	RO	0x0
5	MISS_EN	1: Enable miss event detection	RW	0
4	SIR_EN	1: Enable SIH test mode (SIR)	RW	0
3:0	STMSTS	Read 0x0: Idle Read 0x1: scanning Read 0x2: Load timer debouncing Read 0x3: Test timer debouncing Read 0x4: Gen it event Read 0x6: Load timer long key Read 0x7: Test timer long key Read 0x8: Gen it long key Read 0xA: Test timer time out Read 0xB: Gen it time out Read 0xD: Load timer time out Read 0xF: Other	RO	0x0

Table 194. FULL_CODE_7_0

I2C Address	0x4A		
Physical Address	0xDB	**Instance**	keypad
Description	This register is updated when any key (in the range 0:7) is pressed.A bit at one indicates that the corresponding key is pressed		
Type	RO		

7	6	5	4	3	2	1	0
FULL_CODE_K7	FULL_CODE_K6	FULL_CODE_K5	FULL_CODE_K4	FULL_CODE_K3	FULL_CODE_K2	FULL_CODE_K1	FULL_CODE_K0

Bits	Field Name	Description	Type	Reset
7	FULL_CODE_K7	1: Indicates that key 7 is pressed	RO	0
6	FULL_CODE_K6	1: Indicates that key 6 is pressed	RO	0
5	FULL_CODE_K5	1: Indicates that key 5 is pressed	RO	0
4	FULL_CODE_K4	1: Indicates that key 4 is pressed	RO	0
3	FULL_CODE_K3	1: Indicates that key 3 is pressed	RO	0
2	FULL_CODE_K2	1: Indicates that key 2 is pressed	RO	0
1	FULL_CODE_K1	1: Indicates that key 1 is pressed	RO	0
0	FULL_CODE_K0	1: Indicates that key 0 is pressed	RO	0

Table 195. FULL_CODE_15_8

I2C Address	0x4A		
Physical Address	0xDC	**Instance**	keypad
Description	This register is updated when any key (in the range 8:15) is pressed.A bit at one indicates that the corresponding key is pressed		
Type	RO		

7	6	5	4	3	2	1	0
FULL_CODE_K15	FULL_CODE_K14	FULL_CODE_K13	FULL_CODE_K12	FULL_CODE_K11	FULL_CODE_K10	FULL_CODE_K9	FULL_CODE_K8

Bits	Field Name	Description	Type	Reset
7	FULL_CODE_K15	1: Indicates that key 15 is pressed	RO	0
6	FULL_CODE_K14	1: Indicates that key 14 is pressed	RO	0
5	FULL_CODE_K13	1: Indicates that key 13 is pressed	RO	0
4	FULL_CODE_K12	1: Indicates that key 12 is pressed	RO	0
3	FULL_CODE_K11	1: Indicates that key 11 is pressed	RO	0
2	FULL_CODE_K10	1: Indicates that key 10 is pressed	RO	0
1	FULL_CODE_K9	1: Indicates that key 9 is pressed	RO	0
0	FULL_CODE_K8	1: Indicates that key 8 is pressed	RO	0

Table 196. FULL_CODE_23_16

I2C Address	0x4A		
Physical Address	0xDD	**Instance**	keypad
Description	This register is updated when any key (in the range 16:23) is pressed.A bit at one indicates that the corresponding key is pressed		
Type	RO		

7	6	5	4	3	2	1	0
FULL_CODE_K23	FULL_CODE_K22	FULL_CODE_K21	FULL_CODE_K20	FULL_CODE_K19	FULL_CODE_K18	FULL_CODE_K17	FULL_CODE_K16

Bits	Field Name	Description	Type	Reset
7	FULL_CODE_K23	1: Indicates that key 23 is pressed	RO	0
6	FULL_CODE_K22	1: Indicates that key 22 Iis pressed	RO	0
5	FULL_CODE_K21	1: Indicates that key 21 is pressed	RO	0
4	FULL_CODE_K20	1: Indicates that key 20 is pressed	RO	0
3	FULL_CODE_K19	1: Indicates that key 19 is pressed	RO	0
2	FULL_CODE_K18	1: Indicates that key 18 is pressed	RO	0
1	FULL_CODE_K17	1: Indicates that key 17 is pressed	RO	0
0	FULL_CODE_K16	1: Indicates that key 16 is pressed	RO	0

Table 197. FULL_CODE_31_24

I2C Address	0x4A		
Physical Address	0xDE	**Instance**	keypad
Description	This register is updated when any key (in the range 24:31) is pressed.A bit at one indicates that the corresponding key is pressed		
Type	RO		

7	6	5	4	3	2	1	0
FULL_CODE_K31	FULL_CODE_K30	FULL_CODE_K29	FULL_CODE_K28	FULL_CODE_K27	FULL_CODE_K26	FULL_CODE_K25	FULL_CODE_K24

Bits	Field Name	Description	Type	Reset
7	FULL_CODE_K31	1: Indicates that key 31 is pressed	RO	0
6	FULL_CODE_K30	1: Indicates that key 30 is pressed	RO	0
5	FULL_CODE_K29	1: Indicates that key 29 is pressed	RO	0
4	FULL_CODE_K28	1: Indicates that key 28 is pressed	RO	0
3	FULL_CODE_K27	1: Indicates that key 27 is pressed	RO	0
2	FULL_CODE_K26	1: Indicates that key 26 is pressed	RO	0
1	FULL_CODE_K25	1: Indicates that key 25 Iis pressed	RO	0
0	FULL_CODE_K24	1: Indicates that key 24 is pressed	RO	0

Table 198. FULL_CODE_39_32

I2C Address	0x4A		
Physical Address	0xDF	**Instance**	keypad
Description	This register is updated when any key (in the range 32:39) is pressed.A bit at one indicates that the corresponding key is pressed		
Type	RO		

7	6	5	4	3	2	1	0
FULL_CODE_K39	FULL_CODE_K38	FULL_CODE_K37	FULL_CODE_K36	FULL_CODE_K35	FULL_CODE_K34	FULL_CODE_K33	FULL_CODE_K32

Bits	Field Name	Description	Type	Reset
7	FULL_CODE_K39	1: Indicates that key 39 is pressed	RO	0
6	FULL_CODE_K38	1: Indicates that key 38 is pressed	RO	0
5	FULL_CODE_K37	1: Indicates that key 37 is pressed	RO	0
4	FULL_CODE_K36	1: Indicates that key 36 is pressed	RO	0
3	FULL_CODE_K35	1: Indicates that key 35 is pressed	RO	0
2	FULL_CODE_K34	1: Indicates that key 34 is pressed	RO	0
1	FULL_CODE_K33	1: Indicates that key 33 Iis pressed	RO	0
0	FULL_CODE_K32	1: Indicates that key 32 is pressed	RO	0

Table 199. FULL_CODE_47_40

I2C Address	0x4A		
Physical Address	0xE0	**Instance**	keypad
Description	This register is updated when any key (in the range 40:47) is pressed.A bit at one indicates that the corresponding key is pressed		
Type	RO		

7	6	5	4	3	2	1	0
FULL_CODE_K47	FULL_CODE_K46	FULL_CODE_K45	FULL_CODE_K44	FULL_CODE_K43	FULL_CODE_K42	FULL_CODE_K41	FULL_CODE_K40

Bits	Field Name	Description	Type	Reset
7	FULL_CODE_K47	1: Indicates that key 47 is pressed	RO	0
6	FULL_CODE_K46	1: Indicates that key 46 is pressed	RO	0
5	FULL_CODE_K45	1: Indicates that key 45 is pressed	RO	0
4	FULL_CODE_K44	1: Indicates that key 44 is pressed	RO	0
3	FULL_CODE_K43	1: Indicates that key 43 is pressed	RO	0
2	FULL_CODE_K42	1: Indicates that key 42 is pressed	RO	0
1	FULL_CODE_K41	1: Indicates that key 41 Iis pressed	RO	0
0	FULL_CODE_K40	1: Indicates that key 40 is pressed	RO	0

Table 200. FULL_CODE_55_48

I2C Address	0x4A		
Physical Address	0xE1	**Instance**	keypad
Description	This register is updated when any key (in the range 48:55) is pressed.A bit at one indicates that the corresponding key is pressed		
Type	RO		

7	6	5	4	3	2	1	0
FULL_CODE_K55	FULL_CODE_K54	FULL_CODE_K53	FULL_CODE_K52	FULL_CODE_K51	FULL_CODE_K50	FULL_CODE_K49	FULL_CODE_K48

Bits	Field Name	Description	Type	Reset
7	FULL_CODE_K55	1: Indicates that key 55 is pressed	RO	0
6	FULL_CODE_K54	1: Indicates that key 54 is pressed	RO	0
5	FULL_CODE_K53	1: Indicates that key 53 is pressed	RO	0
4	FULL_CODE_K52	1: Indicates that key 52 is pressed	RO	0
3	FULL_CODE_K51	1: Indicates that key 51 is pressed	RO	0
2	FULL_CODE_K50	1: Indicates that key 50 is pressed	RO	0
1	FULL_CODE_K49	1: Indicates that key 49 Iis pressed	RO	0
0	FULL_CODE_K48	1: Indicates that key 48 is pressed	RO	0

Table 201. FULL_CODE_63_56

I2C Address	0x4A		
Physical Address	0xE2	**Instance**	keypad
Description	This register is updated when any key (in the range 56:63) is pressed.A bit at one indicates that the corresponding key is pressed		
Type	RO		

7	6	5	4	3	2	1	0
FULL_CODE_K63	FULL_CODE_K62	FULL_CODE_K61	FULL_CODE_K60	FULL_CODE_K59	FULL_CODE_K58	FULL_CODE_K57	FULL_CODE_K56

Bits	Field Name	Description	Type	Reset
7	FULL_CODE_K63	1: Indicates that key 63 is pressed	RO	0
6	FULL_CODE_K62	1: Indicates that key 62 is pressed	RO	0
5	FULL_CODE_K61	1: Indicates that key 61 is pressed	RO	0
4	FULL_CODE_K60	1: Indicates that key 60 is pressed	RO	0
3	FULL_CODE_K59	1: Indicates that key 59 is pressed	RO	0
2	FULL_CODE_K58	1: Indicates that key 58 is pressed	RO	0
1	FULL_CODE_K57	1: Indicates that key 57 lis pressed	RO	0
0	FULL_CODE_K56	1: Indicates that key 56 is pressed	RO	0

Table 202. KEYP_ISR1

I2C Address	0x4A		
Physical Address	0xE3	**Instance**	keypad
Description	The INTERRUPT STATUS ISR1 REGISTER is used to determine which of the input keypad event trigged the interrupt line kbd_int1_n request. As illustrated here below, bit 0 corresponds to a key pressed event (ITKP), bit 1 to long key pressed event (ITLK), bit 2 to a time out event (ITTO). When a bit in this register is set to 1, it indicates that the corresponding event is requesting the interrupt. However, the user cannot generate an interrupt by writing a 1 to the INTERRUPT STATUS ISR1 REGISTER. If the user writes a 0 to a bit in this register, the value will remain unchanged when in COR mode. The INTERRUPT STATUS ISR1 REGISTER is synchronous with the interface OCP clock		
Type	RW		

7	6	5	4	3	2	1	0
Reserved				ITMISR1	ITTOISR1	ITLKISR1	ITKPISR1

Bits	Field Name	Description	Type	Reset
7:4	Reserved	Reads return 0s.	RW	0x0
3	ITMISR1	0: Missing event hardware interrupt inactive on processor 1 request line. 1: Missing event hardware interrupt active on processor 1 request line in test mode only.	RW	0
2	ITTOISR1	0: Timeout hardware interrupt inactive on processor 1 request line 1: Timeout hardware interrupt active on processor 1 request line	RW	0
1	ITLKISR1	0: Long Key hardware interrupt inactive on processor 1 request line 1: Long Key hardware interrupt active on processor 1 request line	RW	0
0	ITKPISR1	0: Key pressed hardware interrupt inactive on processor 1 request line 1: Key pressed hardware interrupt active on processor 1 request line	RW	0

Table 203. KEYP_IMR1

I2C Address	0x4A		
Physical Address	0xE4	**Instance**	keypad
Description	The INTERRUPT MASK IMR1 REGISTER allows the user to mask the expected transition on Keypad event from generating an interrupt request on kbd_int1_n. The INTERRUPT MASK REGISTERS are programmed synchronously with the interface OCP clock.		
Type	RW		

7	6	5	4	3	2	1	0
Reserved				ITMISIMR1	ITTOIMR1	ITLKIMR1	ITKPIMR1

Bits	Field Name	Description	Type	Reset
7:4	Reserved	Reads return 0s.	RW	0x0
3	ITMISIMR1	0: Key pressed event not masked on processor 1 request line 1: Miss event masked on processor 1 request line (active in test mode only)	RW	1
2	ITTOIMR1	0: Timeout event not masked on processor 1 request line 1: Timeout event masked on processor 1 request line	RW	1
1	ITLKIMR1	0: Long key event not masked on processor 1 request line 1: Long key event masked on processor 1 request line	RW	1
0	ITKPIMR1	0: Key pressed event not masked on processor 1 request line 1: Key pressed event masked on processor 1 request line	RW	1

Table 204. KEYP_EDR

I2C Address	0x4A		
Physical Address	0xE8	**Instance**	keypad
Description	The INTERRUPT EDGE DETECTION REGISTER KEYP_EDR allows the user to define, for each external event (Key pressed, Long key, time out event), the expected edge to trigger an interrupt request The interrupt request can be either generated from a High to Low transition (bits are 01), a low to High transition (bits are 10) or both transitions (bits are 11) accruing. To disable the edge detection capability, the relevant bits corresponding to the Keypad event need to be reset (00).		
Type	RW		

7	6	5	4	3	2	1	0
ITMISRising	ITMISFalling	ITTORising	ITTOFalling	ITLKRising	ITLKFalling	ITKPRising	ITKPFalling

Bits	Field Name	Description	Type	Reset
7	ITMISRISING	0: Miss event rising detection disabled 1: Miss event rising detection enabled (test mode only)	RW	0
6	ITMISFALLING	0: Miss event falling detection disabled 1: Miss event falling detection enabled (test mode only)	RW	1
5	ITTORISING	0: Timeout event rising detection disabled 1: Timeout event rising detection enabled	RW	0
4	ITTOFALLING	0: Timeout event Falling detection Disabled 1: Timeout event Falling detection Enabled	RW	1
3	ITLKRISING	0: Long key event rising detection disabled 1: Long key event rising detection enabled	RW	0
2	ITLKFALLING	0: Long key event falling detection disabled 1: Long key event falling detection enabled	RW	1
1	ITKPRISING	0: key pressed event rising detection disabled 1: key pressed event rising detection enabled	RW	0
0	ITKPFALLING	0: key pressed event falling detection disabled 1: key pressed event falling detection enabled	RW	1

Table 205. KEYP_SIH_CTRL

I2C Address	0x4A		
Physical Address	0xE9	**Instance**	keypad
Description	The KEYP SIH CONTROL REGISTER KEYP_SIH_CTRL allow the user to disable a pending event incoming during SW interrupt latency by programming 1 in PENDDIS field.The ClearOnRead bit field enable Clear on Read feature. That mean that any read access to the ISR clear this register and release the interrupt line associated (default value). If disabled a read access to a specific address value will clear all ISR within the SIH.		
Type	RW		

7	6	5	4	3	2	1	0
Reserved					COR	PENDDIS	Reserved

Bits	Field Name	Description	Type	Reset
7:3	Reserved	Reads return 0s.	RO	0x00
2	COR	0: Clear ISR specific bit field when write access mode 1: Clear ISR when Read mode	RW	0
1	PENDDIS	0: Pending event feature is enabled 1: Pending event feature is disabled	RW	0
0	Reserved		RW	1

5 POWER

This section provides information on the POWER module instances within this product. Each of the registers within the different POWER module instances is described separately below.

5.1 POWER Sub-Chip Instance Summary

The table below shows the base address and address space for the POWER_SC module instances.

Table 206. POWER_SC Instance Summary

Module Name	Base Address	Size
SECURED_REG	0x00	20 Bytes
BACKUP_REG	0x14	8 Bytes
RTC	0x1C	18 Bytes
INT	0x2E	8 Bytes
PM_MASTER	0x36	37 Bytes
PM_RECEIVER	0x5B	151 Bytes

5.2 SECURED_REG

This section provides information on the SECURED_REG module instances within POWER. Each of the registers within the different SECURED_REG module instances is described separately below.

(Back-up domain)

5.2.1 SECURED_REG Registers Mapping Summary

Table 207. SECURED_REG Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	Address Offset	Physical Address
SECURED_REG_A	RW	8	0x00	0x00	0x00
SECURED_REG_B	RW	8	0x00	0x01	0x01
SECURED_REG_C	RW	8	0x00	0x02	0x02
SECURED_REG_D	RW	8	0x00	0x03	0x03
SECURED_REG_E	RW	8	0x00	0x04	0x04
SECURED_REG_F	RW	8	0x00	0x05	0x05
SECURED_REG_G	RW	8	0x00	0x06	0x06
SECURED_REG_H	RW	8	0x00	0x07	0x07
SECURED_REG_I	RW	8	0x00	0x08	0x08
SECURED_REG_J	RW	8	0x00	0x09	0x09
SECURED_REG_K	RW	8	0x00	0x0A	0x0A
SECURED_REG_L	RW	8	0x00	0x0B	0x0B
SECURED_REG_M	RW	8	0x00	0x0C	0x0C
SECURED_REG_N	RW	8	0x00	0x0D	0x0D
SECURED_REG_O	RW	8	0x00	0x0E	0x0E
SECURED_REG_P	RW	8	0x00	0x0F	0x0F
SECURED_REG_Q	RW	8	0x00	0x10	0x10
SECURED_REG_R	RW	8	0x00	0x11	0x11
SECURED_REG_S	RW	8	0x00	0x12	0x12
SECURED_REG_U	RW	8	0x00	0x13	0x13

5.2.2 SECURED_REG Register Descriptions

Table 208. SECURED_REG_A

I2C Address	0x4B						
Physical Address	0x00	**Instance**		SECURED_REG			
Description	(Back-up domain)						
Type	RW						

7	6	5	4	3	2	1	0
SECURED_DATA							

Bits	Field Name	Description	Type	Reset
7:0	SECURED_DATA		RW	0x00

Table 209. SECURED_REG_B

I2C Address	0x4B						
Physical Address	0x01	**Instance**		SECURED_REG			
Description	(Back-up domain)						
Type	RW						

7	6	5	4	3	2	1	0
SECURED_DATA							

Bits	Field Name	Description	Type	Reset
7:0	SECURED_DATA		RW	0x00

Table 210. SECURED_REG_C

I2C Address	0x4B						
Physical Address	0x02	**Instance**		SECURED_REG			
Description	(Back-up domain)						
Type	RW						

7	6	5	4	3	2	1	0
SECURED_DATA							

Bits	Field Name	Description	Type	Reset
7:0	SECURED_DATA		RW	0x00

Table 211. SECURED_REG_D

I2C Address	0x4B			
Physical Address	0x03	Instance	SECURED_REG	
Description	(Back-up domain)			
Type	RW			

7	6	5	4	3	2	1	0
SECURED_DATA							

Bits	Field Name	Description	Type	Reset
7:0	SECURED_DATA		RW	0x00

Table 212. SECURED_REG_E

I2C Address	0x4B			
Physical Address	0x04	Instance	SECURED_REG	
Description	(Back-up domain)			
Type	RW			

7	6	5	4	3	2	1	0
SECURED_DATA							

Bits	Field Name	Description	Type	Reset
7:0	SECURED_DATA		RW	0x00

Table 213. SECURED_REG_F

I2C Address	0x4B			
Physical Address	0x05	Instance	SECURED_REG	
Description	(Back-up domain)			
Type	RW			

7	6	5	4	3	2	1	0
SECURED_DATA							

Bits	Field Name	Description	Type	Reset
7:0	SECURED_DATA		RW	0x00

Table 214. SECURED_REG_G

I2C Address	0x4B			
Physical Address	0x06	Instance	SECURED_REG	
Description	(Back-up domain)			
Type	RW			

7	6	5	4	3	2	1	0
SECURED_DATA							

Bits	Field Name	Description	Type	Reset
7:0	SECURED_DATA		RW	0x00

Table 215. SECURED_REG_H

I2C Address	0x4B						
Physical Address	0x07	**Instance**		SECURED_REG			
Description	(Back-up domain)						
Type	RW						

7	6	5	4	3	2	1	0
SECURED_DATA							

Bits	Field Name	Description	Type	Reset
7:0	SECURED_DATA		RW	0x00

Table 216. SECURED_REG_I

I2C Address	0x4B						
Physical Address	0x08	**Instance**		SECURED_REG			
Description	(Back-up domain)						
Type	RW						

7	6	5	4	3	2	1	0
SECURED_DATA							

Bits	Field Name	Description	Type	Reset
7:0	SECURED_DATA		RW	0x00

Table 217. SECURED_REG_J

I2C Address	0x4B						
Physical Address	0x09	**Instance**		SECURED_REG			
Description	(Back-up domain)						
Type	RW						

7	6	5	4	3	2	1	0
SECURED_DATA							

Bits	Field Name	Description	Type	Reset
7:0	SECURED_DATA		RW	0x00

Table 218. SECURED_REG_K

I2C Address	0x4B						
Physical Address	0x0A	**Instance**		SECURED_REG			
Description	(Back-up domain)						
Type	RW						

7	6	5	4	3	2	1	0
SECURED_DATA							

Bits	Field Name	Description	Type	Reset
7:0	SECURED_DATA		RW	0x00

Table 219. SECURED_REG_L

I2C Address	0x4B						
Physical Address	0x0B	Instance		SECURED_REG			
Description	(Back-up domain)						
Type	RW						

7	6	5	4	3	2	1	0
SECURED_DATA							

Bits	Field Name	Description	Type	Reset
7:0	SECURED_DATA		RW	0x00

Table 220. SECURED_REG_M

I2C Address	0x4B						
Physical Address	0x0C	Instance		SECURED_REG			
Description	(Back-up domain)						
Type	RW						

7	6	5	4	3	2	1	0
SECURED_DATA							

Bits	Field Name	Description	Type	Reset
7:0	SECURED_DATA		RW	0x00

Table 221. SECURED_REG_N

I2C Address	0x4B						
Physical Address	0x0D	Instance		SECURED_REG			
Description	(Back-up domain)						
Type	RW						

7	6	5	4	3	2	1	0
SECURED_DATA							

Bits	Field Name	Description	Type	Reset
7:0	SECURED_DATA		RW	0x00

Table 222. SECURED_REG_O

I2C Address	0x4B						
Physical Address	0x0E	Instance		SECURED_REG			
Description	(Back-up domain)						
Type	RW						

7	6	5	4	3	2	1	0
SECURED_DATA							

Bits	Field Name	Description	Type	Reset
7:0	SECURED_DATA		RW	0x00

Table 223. SECURED_REG_P

I2C Address	0x4B			
Physical Address	0x0F	Instance	SECURED_REG	
Description	(Back-up domain)			
Type	RW			

7	6	5	4	3	2	1	0
SECURED_DATA							

Bits	Field Name	Description	Type	Reset
7:0	SECURED_DATA		RW	0x00

Table 224. SECURED_REG_Q

I2C Address	0x4B			
Physical Address	0x10	Instance	SECURED_REG	
Description	(Back-up domain)			
Type	RW			

7	6	5	4	3	2	1	0
SECURED_DATA							

Bits	Field Name	Description	Type	Reset
7:0	SECURED_DATA		RW	0x00

Table 225. SECURED_REG_R

I2C Address	0x4B			
Physical Address	0x11	Instance	SECURED_REG	
Description	(Back-up domain)			
Type	RW			

7	6	5	4	3	2	1	0
SECURED_DATA							

Bits	Field Name	Description	Type	Reset
7:0	SECURED_DATA		RW	0x00

Table 226. SECURED_REG_S

I2C Address	0x4B			
Physical Address	0x12	Instance	SECURED_REG	
Description	(Back-up domain)			
Type	RW			

7	6	5	4	3	2	1	0
SECURED_DATA							

Bits	Field Name	Description	Type	Reset
7:0	SECURED_DATA		RW	0x00

Table 227. SECURED_REG_U

I2C Address	0x4B		
Physical Address	0x13	**Instance**	SECURED_REG
Description	(Back-up domain)		
Type	RW		

7	6	5	4	3	2	1	0
SECURED_DATA							

Bits	Field Name	Description	Type	Reset
7:0	SECURED_DATA		RW	0x00

5.3 BACKUP_REG

This section provides information on the BACKUP_REG module instances within this product. Each of the registers within the different BACKUP_REG module instances is described separately below.

Bank of back-up regsiters (Back-up domain)

5.3.1 BACKUP_REG Registers Mapping Summary

Table 228. BACKUP_REG Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	Address offset	Physical Address
BACKUP_REG_A	RW	8	0x00	0x0	0x14
BACKUP_REG_B	RW	8	0x00	0x1	0x15
BACKUP_REG_C	RW	8	0x00	0x2	0x16
BACKUP_REG_D	RW	8	0x00	0x3	0x17
BACKUP_REG_E	RW	8	0x00	0x4	0x18
BACKUP_REG_F	RW	8	0x00	0x5	0x19
BACKUP_REG_G	RW	8	0x00	0x6	0x1A
BACKUP_REG_H	RW	8	0x00	0x7	0x1B

5.3.2 BACKUP_REG Register Descriptions

Table 229. BACKUP_REG_A

I2C Address	0x4B		
Physical Address	0x14	**Instance**	BACKUP_REG
Description	Back-up register A (Back-up domain)		
Type	RW		

7	6	5	4	3	2	1	0
DATA							

Bits	Field Name	Description	Type	Reset
7:0	DATA		RW	0x00

Table 230. BACKUP_REG_B

I2C Address	0x4B		
Physical Address	0x15	**Instance**	BACKUP_REG
Description	Back-up register B (Back-up domain)		
Type	RW		

7	6	5	4	3	2	1	0
DATA							

Bits	Field Name	Description	Type	Reset
7:0	DATA		RW	0x00

Table 231. BACKUP_REG_C

I2C Address	0x4B		
Physical Address	0x16	**Instance**	BACKUP_REG
Description	Back-up register C (Back-up domain)		
Type	RW		

7	6	5	4	3	2	1	0
DATA							

Bits	Field Name	Description	Type	Reset
7:0	DATA		RW	0x00

Table 232. BACKUP_REG_D

I2C Address	0x4B		
Physical Address	0x17	**Instance**	BACKUP_REG
Description	Back-up regsiter D (Back-up domain)		
Type	RW		

7	6	5	4	3	2	1	0
DATA							

Bits	Field Name	Description	Type	Reset
7:0	DATA		RW	0x00

Table 233. BACKUP_REG_E

I2C Address	0x4B		
Physical Address	0x18	**Instance**	BACKUP_REG
Description	Back-up register E (Back-up domain)		
Type	RW		

7	6	5	4	3	2	1	0
DATA							

Bits	Field Name	Description	Type	Reset
7:0	DATA		RW	0x00

Table 234. BACKUP_REG_F

I2C Address	0x4B		
Physical Address	0x19	**Instance**	BACKUP_REG
Description	Back-up regsiter F (Back-up domain)		
Type	RW		

7	6	5	4	3	2	1	0
DATA							

Bits	Field Name	Description	Type	Reset
7:0	DATA		RW	0x00

Table 235. BACKUP_REG_G

I2C Address	0x4B			
Physical Address	0x1A	Instance	BACKUP_REG	
Description	Back-up register G (Back-up domain)			
Type	RW			

7	6	5	4	3	2	1	0
DATA							

Bits	Field Name	Description	Type	Reset
7:0	DATA		RW	0x00

Table 236. BACKUP_REG_H

I2C Address	0x4B			
Physical Address	0x1B	Instance	BACKUP_REG	
Description	Back-up register H (Back-up domain)			
Type	RW			

7	6	5	4	3	2	1	0
DATA							

Bits	Field Name	Description	Type	Reset
7:0	DATA		RW	0x00

5.4 RTC

This section provides information on the RTC module instances within POWER. Each of the registers within the different RTC module instances is described separately below.

(Back-up domain)

5.4.1 RTC Registers Mapping Summary

Table 237. RTC Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	Address Offset	Physical Address
SECONDS_REG	RW	8	0x00	0x00	0x1C
MINUTES_REG	RW	8	0x00	0x01	0x1D
HOURS_REG	RW	8	0x00	0x02	0x1E
DAYS_REG	RW	8	0x01	0x03	0x1F
MONTHS_REG	RW	8	0x01	0x04	0x20
YEARS_REG	RW	8	0x00	0x05	0x21
WEEKS_REG	RW	8	0x00	0x06	0x22
ALARM_SECONDS_REG	RW	8	0x00	0x07	0x23
ALARM_MINUTES_REG	RW	8	0x00	0x08	0x24
ALARM_HOURS_REG	RW	8	0x00	0x09	0x25
ALARM_DAYS_REG	RW	8	0x01	0x0A	0x26
ALARM_MONTHS_REG	RW	8	0x01	0x0B	0x27
ALARM_YEARS_REG	RW	8	0x00	0x0C	0x28
RTC_CTRL_REG	RW	8	0x00	0x0D	0x29
RTC_STATUS_REG	RW	8	0x80	0x0E	0x2A
RTC_INTERRUPTS_REG	RW	8	0x00	0x0F	0x2B
RTC_COMP_LSB_REG	RW	8	0x00	0x10	0x2C
RTC_COMP_MSB_REG	RW	8	0x00	0x11	0x2D

5.4.2 RTC Register Descriptions

Table 238. SECONDS_REG

I2C Address	0x4B		
Physical Address	0x1C	**Instance**	RTC
Description	(Back-up domain)		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	SEC1			SEC0			

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6:4	SEC1	2nd digit of seconds. Range is 0 to 5	RW	0x0
3:0	SEC0	1st digit of seconds. Range is 0 to 9	RW	0x0

Table 239. MINUTES_REG

I2C Address	0x4B			
Physical Address	0x1D	Instance	RTC	
Description	Register for minutes (Back-up domain)			
Type	RW			

7	6	5	4	3	2	1	0
Reserved	MIN1			MIN0			

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6:4	MIN1	2nd digit of minutes. Range is 0 to 5	RW	0x0
3:0	MIN0	1st digit of minutes. Range is 0 to 9	RW	0x0

Table 240. HOURS_REG

I2C Address	0x4B			
Physical Address	0x1E	Instance	RTC	
Description	Register for hours (Back-up domain)			
Type	RW			

7	6	5	4	3	2	1	0
PM_nAM	Reserved	HOUR1		HOUR0			

Bits	Field Name	Description	Type	Reset
7	PM_NAM	Only used in PM_AM mode (otherwise 0)0 => AM1 => PM	RW	0
6	Reserved		RO	0
5:4	HOUR1	2nd digit of hours. Range is 0 to 2	RW	0x0
3:0	HOUR0	1st digit of hours. Range is 0 to 9	RW	0x0

Table 241. DAYS_REG

I2C Address	0x4B			
Physical Address	0x1F	Instance	RTC	
Description	Register for days (Back-up domain)			
Type	RW			

7	6	5	4	3	2	1	0
Reserved		DAY1		DAY0			

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO	0x0
5:4	DAY1	2nd digit of days. Range from 0 to 3	RW	0x0
3:0	DAY0	1st digit of days. Range from 0 to 9	RW	0x1

Table 242. MONTHS_REG

I2C Address	0x4B		
Physical Address	0x20	**Instance**	RTC
Description	Note: Usual notation is taken for month value: 01 => January 02 => February .... 12 => December(Back-up domain)		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			MONTH1	MONTH0			

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4	MONTH1	2nd digit of months. Range from 0 to 1	RW	0
3:0	MONTH0	1st digit of months. Range from 0 to 9	RW	0x1

Table 243. YEARS_REG

I2C Address	0x4B		
Physical Address	0x21	**Instance**	RTC
Description	(Back-up domain)		
Type	RW		

7	6	5	4	3	2	1	0
YEAR1				YEAR0			

Bits	Field Name	Description	Type	Reset
7:4	YEAR1	2nd digit of Years. Range from 0 to 9	RW	0x0
3:0	YEAR0	1st digit of Years. Range from 0 to 9	RW	0x0

Table 244. WEEKS_REG

I2C Address	0x4B		
Physical Address	0x22	**Instance**	RTC
Description	(Back-up domain)		
Type	RW		

7	6	5	4	3	2	1	0
Reserved					WEEK		

Bits	Field Name	Description	Type	Reset
7:3	Reserved		RW	0x00
2:0	WEEK	1st digit of Days in a week. Range from 0 to 6	RW	0x0

Table 245. ALARM_SECONDS_REG

I2C Address	0x4B		
Physical Address	0x23	**Instance**	RTC
Description	Register for seconds for alarm (Back-up domain)		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	ALARM_SEC1			ALARM_SEC0			

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6:4	ALARM_SEC1	2nd digit of seconds. Range is 0 to 5	RW	0x0
3:0	ALARM_SEC0	1st digit of seconds. Range is 0 to 9	RW	0x0

Table 246. ALARM_MINUTES_REG

I2C Address	0x4B		
Physical Address	0x24	**Instance**	RTC
Description	Register for minutes for alarm (Back-up domain)		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	ALARM_MIN1			ALARM_MIN0			

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6:4	ALARM_MIN1	2nd digit of minutes. Range is 0 to 5	RW	0x0
3:0	ALARM_MIN0	1st digit of minutes. Range is 0 to 9	RW	0x0

Table 247. ALARM_HOURS_REG

I2C Address	0x4B		
Physical Address	0x25	**Instance**	RTC
Description	Register for hours for alarm (Back-up domain)		
Type	RW		

7	6	5	4	3	2	1	0
ALARM_PM_nAM	Reserved	ALARM_HOUR1		ALARM_HOUR0			

Bits	Field Name	Description	Type	Reset
7	ALARM_PM_NAM	Only used in PM_AM mode (otherwise 0) 0 => AM 1 => PM	RW	0
6	Reserved		RO	0
5:4	ALARM_HOUR1	2nd digit of hours. Range from 0 to 2	RW	0x0
3:0	ALARM_HOUR0	1st digit of hours. Range from 0 to 9	RW	0x0

Table 248. ALARM_DAYS_REG

I2C Address	0x4B		
Physical Address	0x26	**Instance**	RTC
Description	Register for days for alarm (Back-up domain)		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		ALARM_DAY1		ALARM_DAY0			

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO	0x0
5:4	ALARM_DAY1	2nd digit for days. Range from 0 to 3	RW	0x0
3:0	ALARM_DAY0	1st digit for days. Range from 0 to 9	RW	0x1

Table 249. ALARM_MONTHS_REG

I2C Address	0x4B		
Physical Address	0x27	**Instance**	RTC
Description	Register for months for alarm (Back-up domain)		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			ALARM_MONTH1	ALARM_MONTH0			

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4	ALARM_MONTH1	2nd digit of months. Range from 0 to 1	RW	0
3:0	ALARM_MONTH0	1st digit of months. Range from 0 to 9	RW	0x1

Table 250. ALARM_YEARS_REG

I2C Address	0x4B		
Physical Address	0x28	**Instance**	RTC
Description	Register for years for alarm (Back-up domain)		
Type	RW		

7	6	5	4	3	2	1	0
ALARM_YEAR1				ALARM_YEAR0			

Bits	Field Name	Description	Type	Reset
7:4	ALARM_YEAR1	2nd digit of Years. Range from 0 to 9	RW	0x0
3:0	ALARM_YEAR0	1st digit of Years. Range from 0 to 9	RW	0x0

Table 251. RTC_CTRL_REG

I2C Address	0x4B		
Physical Address	0x29	**Instance**	RTC
Description	SET_32_counter must only be used when the RTC is frozen.ROUND_30S bit is a toggle bit, the host processor can only write 1, RTC clears it. If the host processor sets the ROUND_30S bit and then reads it, the host processor will read 1 until the rounding to the closest minute is performed the next second.MODE_12_24: it is possible to switch between the two modes at any time without disturbed the RTC, read or write are always performed with the current mode.GET_TIME bit is a toggle bit, the host processor can only write 1, RTC clears it. If the host processor sets the GET_TIME bit and then reads it, the host processor will read 0.(Back-up domain)		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	GET_TIME	SET_32_COUNTER	TEST_MODE	MODE_12_24	AUTO_COMP	ROUND_30S	STOP_RTC

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	GET_TIME	0: No action 1: When a one is written, internal Time and Calendar register values are stored in latches. When ALARM_SECONDS_REG, ALARM_MINUTES_REG, ... register are read these latched velues are read. (See note)	RW	0
5	SET_32_COUNTER	0: No action 1: Set the 32-kHz counter with comp_reg value (See note)	RW	0
4	TEST_MODE	0: Functional mode 1: Test mode (Auto compensation is enable when the 32 KHz counter reaches at its end)	RW	0
3	MODE_12_24	0: 24 hours mode (See note) 1: 12 hours mode (PM-AM mode)	RW	0
2	AUTO_COMP	0: No auto compensation 1: Auto compensation enabled	RW	0
1	ROUND_30S	0: No update 1: When a one is written, the time is rounded to the closest minute (See note)	RW	0
0	STOP_RTC	0: RTC is frozen 1: RTC is running	RW	0

Table 252. RTC_STATUS_REG

I2C Address	0x4B		
Physical Address	0x2A	**Instance**	RTC
Description	The alarm interrupt is at low level until the host processor writes 1 to the ALARM bit of the RTC_STATUS_REG register.POWER_UP is set by a reset, is cleared by writing 1 in this bit.(Back-up domain)		
Type	RW		

7	6	5	4	3	2	1	0
POWER_UP	ALARM	EVENT_1D	EVENT_1H	EVENT_1M	EVENT_1S	RUN	Reserved

Bits	Field Name	Description	Type	Reset
7	POWER_UP	Indicates that a reset occurred	RW	1
6	ALARM	Indicates that an alarm interrupt has been generated	RW	0
5	EVENT_1D	One day has occurred	RO	0
4	EVENT_1H	One hour has occurred	RO	0
3	EVENT_1M	One minute has occurred	RO	0
2	EVENT_1S	One second has occurred	RO	0
1	RUN	0: RTC is frozen 1: RTC is running	RO	0
0	Reserved		RO	0

Table 253. RTC_INTERRUPTS_REG

I2C Address	0x4B		
Physical Address	0x2B	**Instance**	RTC
Description	Interrupts register (Back-up domain)		
Type	RW		

7	6	5	4	3	2	1	0
Reserved				IT_ALARM	IT_TIMER	EVERY	

Bits	Field Name	Description	Type	Reset
7:4	Reserved		RW	0x0
3	IT_ALARM	Enable one interrupt when the alarm value is reached (TC ALARM registers) by the TC registers	RW	0
2	IT_TIMER	Enable periodic interrupt 0: Interrupt disabled 1: Interrupt enabled	RW	0
1:0	EVERY	Interrupt period 0: Every second 1: Every minute 2: Every hour 3: Every day	RW	0x0

Table 254. RTC_COMP_LSB_REG

I2C Address	0x4B		
Physical Address	0x2C	**Instance**	RTC
Description	This register must be written in 2's complement. To add one 32-kHz oscillator period every hour the host processor needs to write FFFF into RTC_COMP_MSB_REG & RTC_COMP_LSB_REG. To remove one 32-kHz oscillator period every hour the host processor needs to write 0001 into RTC_COMP_MSB_REG & RTC_COMP_LSB_REG.The 7FFF value is forbidden.(Back-up domain)		
Type	RW		

7	6	5	4	3	2	1	0
RTC_COMP_LSB							

Bits	Field Name	Description	Type	Reset
7:0	RTC_COMP_LSB	Indicates number of 32-kHz periods to be added into the 32-kHz counter every hour	RW	0x00

Table 255. RTC_COMP_MSB_REG

I2C Address	0x4B		
Physical Address	0x2D	**Instance**	RTC
Description	(Back-up domain)		
Type	RW		

7	6	5	4	3	2	1	0
RTC_COMP_MSB							

Bits	Field Name	Description	Type	Reset
7:0	RTC_COMP_MSB	Indicates number of 32-kHz periods to be added into the 32-kHz counter every hour	RW	0x00

5.5 INT

This section provides information on the INT module instances within POWER. Each of the registers within the different INT module instances is described separately below.

(VRRTC domain)

5.5.1 INT Registers Mapping Summary

Table 256. INT Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	Address Offset	Physical Address
PWR_ISR1	RW	8	0x00	0x0	0x2E
PWR_IMR1	RW	8	0x00	0x1	0x2F
PWR_EDR1	RW	8	0xF3	0x5	0x33
PWR_EDR2	RW	8	0xF3	0x6	0x34
PWR_SIH_CTRL	RW	8	0x01	0x7	0x35

5.5.1.1 INT Register Descriptions

Table 257. PWR_ISR1

I2C Address	0x4B		
Physical Address	0x2E	**Instance**	INT
Description	The INTERRUPT STATUS ISR1 REGISTER is used to determine which input event triggered the interrupt line int1_n request (VRRTC domain).		
Type	RW		

7	6	5	4	3	2	1	0
SC_DETECT	MBCHG	Reserved	HOT_DIE	RTC_IT	USB_PRES	Reserved	PWRON

Bits	Field Name	Description	Type	Reset
7	SC_DETECT	Short circuit detection	RW	0
6	MBCHG	Main battery charged	RW	0
5	Reserved		RW	0
4	HOT_DIE	Hot die condition detection	RW	0
3	RTC_IT	Real-time clock event (alarm or periodic)	RW	0
2	USB_PRES	USB detection	RW	0
1	Reserved		RW	0
0	PWRON	As the PWRON signal is active LOW, this signal is used inverted.	RW	0

Table 258. PWR_IMR1

I2C Address	0x4B		
Physical Address	0x2F	**Instance**	INT
Description	The INTERRUPT MASK IMR1 REGISTER allows the user to mask the expected transition event from generating an interrupt request on _int1_n (VRRTC domain).		
Type	RW		

7	6	5	4	3	2	1	0
SC_DETECT	MBCHG	Reserved	HOT_DIE	RTC_IT	USB_PRES	Reserved	PWRON

Bits	Field Name	Description	Type	Reset
7	SC_DETECT	0: Interrupt is unmasked 1: Interrupt is masked	RW	0
6	MBCHG	0: Interrupt is unmasked 1: Interrupt is masked	RW	0
5	Reserved	0: Interrupt is unmasked 1: Interrupt is masked	RW	0
4	HOT_DIE	0: Interrupt is unmasked 1: Interrupt is masked	RW	0
3	RTC_IT	0: Interrupt is unmasked 1: Interrupt is masked	RW	0
2	USB_PRES	0: Interrupt is unmasked 1: Interrupt is masked	RW	0
1	Reserved	0: Interrupt is unmasked 1: Interrupt is masked	RW	0
0	PWRON	0: Interrupt is unmasked 1: Interrupt is masked	RW	0

Table 259. PWR_EDR1

I2C Address	0x4B		
Physical Address	0x33	**Instance**	INT
Description	Power edge detection register 1 for PWON, charger presence, USB presence and RTC IT (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
RTC_IT_RISING	RTC_IT_FALLING	USB_PRES_RISING	USB_PRES_FALLING	Reserved		PWRON_RISING	PWRON_FALLING

Bits	Field Name	Description	Type	Reset
7	RTC_IT_RISING	0: Rising-edge detection disabled 1: Rising-edge detection enabled	RW	1
6	RTC_IT_FALLING	0: Falling-edge detection disabled 1: Falling-edge detection enabled	RW	1
5	USB_PRES_RISING	0: Rising-edge detection disabled 1: Rising-edge detection enabled	RW	1
4	USB_PRES_FALLING	0: Falling-edge detection disabled 1: Falling-edge detection enabled	RW	1
3:2	Reserved		RW	0x0
1	PWRON_RISING	0: Rising-edge detection disabled 1: Rising-edge detection enabled As the PWRON signal is active LOW, this signal is used inverted. Then this register will in fact enable the falling edge of the external PWRON signal.	RW	1
0	PWRON_FALLING	0: Falling-edge detection disabled 1: Falling-edge detection enabled As the PWRON signal is active LOW, this signal is used inverted. Then this register will in fact enable the rising edge of the external PWRON signal.	RW	1

Table 260. PWR_EDR2

I2C Address	0x4B		
Physical Address	0x34	**Instance**	INT
Description	Power edge detection register 2 short circuit detect, main battery charger, power ok and hot die presences (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
SC_DETECT_RISING	SC_DETECT_FALLING	MBCHG_RISING	MBCHG_FALLING	Reserved		HOT_DIE_RISING	HOT_DIE_FALLING

Bits	Field Name	Description	Type	Reset
7	SC_DETECT_RISING	0: Rising-edge detection disabled 1: Rising-edge detection enabled	RW	1
6	SC_DETECT_FALLING	0: Falling-edge detection disabled 1: Falling-edge detection enabled	RW	1
5	MBCHG_RISING	0: Rising-edge detection disabled 1: Rising-edge detection enabled	RW	1
4	MBCHG_FALLING	0: Falling-edge detection disabled 1: Falling-edge detection enabled	RW	1
3:2	Reserved		RW	0x0
1	HOT_DIE_RISING	0: Rising-edge detection disabled 1: Rising-edge detection enabled	RW	1
0	HOT_DIE_FALLING	0: Falling-edge detection disabled 1: Falling-edge detection enabled	RW	1

Table 261. PWR_SIH_CTRL

I2C Address	0x4B		
Physical Address	0x35	**Instance**	INT
Description	Allows the user to disable a pending event incoming during SW interrupt latency by programming 1 in the PENDDIS field.The ClearOnRead bit field enables the Clear on Read feature. That mean that any read access to the ISR clears this register and releases the associated interrupt line (default). If disabled a read access to a specific address value will clear all ISR within the SIH (VRRTC domain).		
Type	RW		

7	6	5	4	3	2	1	0
Reserved					COR	PENDDIS	Reserved

Bits	Field Name	Description	Type	Reset
7:3	Reserved		RO	0x00
2	COR		RW	0
1	PENDDIS		RW	0
0	Reserved		RW	1

5.6 PM_MASTER

This section provides information on the PM_MASTER module instances within POWER. Each of the registers within the different PM_MASTER module instances is described separately below.

5.6.1 PM_MASTER Registers Mapping Summary

Table 262. PM_MASTER Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	Address Offset	Physical Address
CFG_P1_TRANSITION	RW	8	0x7F	0x00	0x36
CFG_P2_TRANSITION	RW	8	0x7F	0x01	0x37
CFG_P3_TRANSITION	RW	8	0x7F	0x02	0x38
CFG_P123_TRANSITION	RW	8	0x2B	0x03	0x39
STS_BOOT	RW	8	0x00	0x04	0x3A
CFG_BOOT	RW	8	0x08	0x05	0x3B
SHUNDAN	RW	8	0x3F	0x06	0x3C
CFG_PWRANA2	RW	8	0x0E	0x09	0x3F
BACKUP_MISC_CFG	RW	8	0x00	0x0C	0x42
PROTECT_KEY	RW	8	0x00	0x0E	0x44
STS_HW_CONDITIONS	RO	8	0x00	0x0F	0x45
P1_SW_EVENTS	RW	8	0x40	0x10	0x46
P2_SW_EVENTS	RW	8	0x40	0x11	0x47
P3_SW_EVENTS	RW	8	0x40	0x12	0x48
STS_P123_STATE	RO	8	0x00	0x13	0x49
PB_CFG	RW	8	0x00	0x14	0x4A
PB_WORD_MSB	RW	8	0xFF	0x15	0x4B
PB_WORD_LSB	RW	8	0xFF	0x16	0x4C
RESERVED_E	RW	8	0x02	0x1B	0x51
SEQ_ADD_W2P	RW	8	0x00	0x1C	0x52
SEQ_ADD_P2A	RW	8	0x04	0x1D	0x53
SEQ_ADD_A2W	RW	8	0x0D	0x1E	0x54
SEQ_ADD_A2S	RW	8	0x3F	0x1F	0x55
SEQ_ADD_S2A12	RW	8	0x3F	0x20	0x56
SEQ_ADD_S2A3	RW	8	0x3F	0x21	0x57
SEQ_ADD_WARM	RW	8	0x3F	0x22	0x58
MEMORY_ADDRESS	RW	8	0x00	0x23	0x59
MEMORY_DATA	RW	8	0x18	0x24	0x5A

5.6.2 PM_MASTER Register Descriptions

Table 263. CFG_P1_TRANSITION

I2C Address	0x4B		
Physical Address	0x36	**Instance**	PM_MASTER
Description	Configuration register for processor 1 transition(Back-up domain)Write protected with the KEY_CFG		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		STARTON_VBUS	STARTON_VBAT	STARTON_RTC	STARTON_USB	Reserved	STARTON_PWON

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RW	0x1
5	STARTON_VBUS	When 0: Does not affect P1_OFF2ACT transition When 1: Does affect P1_OFF2ACT transition	RW	1
4	STARTON_VBAT	When 0: Does not affect P1_OFF2ACT transition When 1: Does affect P1_OFF2ACT transition	RW	1
3	STARTON_RTC	When 0: Does not affect P1_OFF2ACT transition When 1: Does affect P1_OFF2ACT transition	RW	1
2	STARTON_USB	When 0: Does not affect P1_OFF2ACT transition When 1: Does affect P1_OFF2ACT transition	RW	1
1	Reserved		RW	1
0	STARTON_PWON	When 0: Does not affect P1_OFF2ACT transition When 1: Does affect P1_OFF2ACT transition	RW	1

Table 264. CFG_P2_TRANSITION

I2C Address	0x4B		
Physical Address	0x37	**Instance**	PM_MASTER
Description	Configuration register for processor 2 transition(Back-up domain)Write protected with the KEY_CFG		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		STARTON_VBUS	STARTON_VBAT	STARTON_RTC	STARTON_USB	Reserved	STARTON_PWON

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RW	0x1
5	STARTON_VBUS	When 0: Does not affect P2_OFF2ACT transition When 1: Does affect P2_OFF2ACT transition	RW	1
4	STARTON_VBAT	When 0: Does not affect P2_OFF2ACT transition When 1: Does affect P2_OFF2ACT transition	RW	1
3	STARTON_RTC	When 0: Does not affect P2_OFF2ACT transition When 1: Does affect P2_OFF2ACT transition	RW	1
2	STARTON_USB	When 0: Does not affect P2_OFF2ACT transition When 1: Does affect P2_OFF2ACT transition	RW	1
1	Reserved		RW	1
0	STARTON_PWON	When 0: Does not affect P2_OFF2ACT transition When 1: Does affect P2_OFF2ACT transition	RW	1

Table 265. CFG_P3_TRANSITION

I2C Address	0x4B		
Physical Address	0x38	**Instance**	PM_MASTER
Description	Configuration register for processor 3 transition(Back-up domain)Write protected with the KEY_CFG		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		STARTON_VBUS	STARTON_VBAT	STARTON_RTC	STARTON_USB	Reserved	STARTON_PWON

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RW	0x1
5	STARTON_VBUS	When 0: Does not affect p3_OFF2ACT transition When 1: Does affect P3_OFF2ACT transition	RW	1
4	STARTON_VBAT	When 0: Does not affect p3_OFF2ACT transition When 1: Does affect P3_OFF2ACT transition	RW	1
3	STARTON_RTC	When 0: Does not affect p3_OFF2ACT transition When 1: Does affect P3_OFF2ACT transition	RW	1
2	STARTON_USB	When 0: Does not affect p3_OFF2ACT transition When 1: Does affect P3_OFF2ACT transition	RW	1
1	Reserved		RW	1
0	STARTON_PWON	When 0: Does not affect p3_OFF2ACT transition When 1: Does affect P3_OFF2ACT transition	RW	1

Table 266. CFG_P123_TRANSITION

I2C Address	0x4B		
Physical Address	0x39	**Instance**	PM_MASTER
Description	Configuration regsiter for transition processors 1/2/3 (Back-up domain)Write protected with the KEY_CFG		
Type	RW		

7	6	5	4	3	2	1	0
MSK_THERMAL_SHUTDOWN	MSK_MBLO	SEQ_MSK_BAT_PRESENCE	SEQ_MSK_BAT_LEVEL	SEQ_MSK_THERM_HD	SEQ_FREEZE	SEQ_ONSYNC	SEQ_OFFSYNC

Bits	Field Name	Description	Type	Reset
7	MSK_THERMAL_SHUTDOWN	When 0: PMC is reset when TS = 1 When 1: PMC is not reset when TS = 1	RO	0
6	MSK_MBLO	When 0: PMC is reset when MBLO = 1 When 1: PMC is not reset when MBLO = 1	RW	0
5	SEQ_MSK_BAT_PRESENCE	Vbat presence comparator is not used to check a valid OFF to ACTIV transition, the comparator status is seen as equal to 1This bit is Read only.	RORreturns1s	1
4	SEQ_MSK_BAT_LEVEL	When 0: Vbat voltage comparator is used to check a valid OFF to ACTIV transition When 1: Vbat voltage comparator is not used to check a valid OFF to ACTIV transition, the comparator status is seen as equal to 1	RW	0
3	SEQ_MSK_THERM_HD	When 0: Therm HD is used to check a valid OFF to ACTIV transition When 1: Therm HD not used to check a valid OFF to ACTIV transition	RW	1
2	SEQ_FREEZE	1: Freeze all sequencers in their current state, sequencers finish their current transition if one is on going. 0: Sequencers are able to initiate a new transition	RW	0
1	SEQ_ONSYNC	1: Sequencers wait for each other before any - P[123]_OFF2ACT transition Any switch-on of one sequencer is applied to all sequencers. (Has priority on switch-on mask condition) 0: Sequencers don't wait for each other before any - P[123]_OFF2ACT transition This register can be used to switch on one part of the design by software and not with a HW condition	RW	1
0	SEQ_OFFSYNC	1: Sequencers wait for each other before any - P[123]_ACT2WAITON transition Any write to P[123]_DEVOFF write also the value to P[123]_DEVOFF 0: Sequencers don't wait for each other before any - P[123]_ACT2WAITON transition This register can be used to switch off one part of the design by software and not the whole design.	RW	1

Table 267. STS_BOOT

I2C Address	0x4B		
Physical Address	0x3A	**Instance**	PM_MASTER
Description	(Back-up domain)		
Type	RW		

7	6	5	4	3	2	1	0
BACKUP	TS	WATCHDOG_RESET	ITCHECK_RESET	PWRON_8s	SETUP_DONE_BCK	SETUP_DONE_PMC	SYSEN_RESET

Bits	Field Name	Description	Type	Reset
7	BACKUP	1: TPS65921 entered backup mode since last register clear. 0: TPS65921 did not enter backup mode since last register clear.	RW	0
6	TS	1: A thermal shutdown occurred since last register clear. 0: No thermal shutdown occurred since last register clear.	RW	0
5	WATCHDOG_RESET	1: Reset due to a Warmreset occured since last register clear. 0: No reset due to a Warmreset occured since last register clear.	RW	0
4	ITCHECK_RESET	1: Reset due to an IT_Check occured since last register clear. 0: No reset due to an IT_Check occured since last register clear.	RW	0
3	PWRON_8S	1: Restart due to a PWRON low more than 8s occured since last register clear. 0: No restart due to a PWRON low more than 8s occured since last register clear.	RW	0
2	SETUP_DONE_BCK	This may be used to know that the backup configuration is done (RTC, BACKUP registers, ...). This bit can be set to 1 by the user when the configurationof the backup domain is done. This bit is automatically reset to 0 when the backup configuration is lost.	RW	0
1	SETUP_DONE_PMC	This may be used to know that the PMC configuration is done. This bit can be set to 1 by the user when the configuration of the PMC is done.This bit is atomatically reset to 0 when the PMC configuration is lost.	RW	0
0	SYSEN_RESET	1: SYSEN was driven low by an external device since last register clear. 0: SYSEN was not driven low by an external device since last register clear.	RW	0

Table 268. CFG_BOOT

I2C Address	0x4B			
Physical Address	0x3B	Instance	PM_MASTER	
Description	Boot configuration register (Back-up domain)Write protected with the KEY_CFG			
Type	RW			

7	6	5	4	3	2	1	0
CK32K_LOWPWR_EN	BOOT_CFG			HIGH_PERF_SQ	SLICER_BYPASS	HFCLK_FREQ	

Bits	Field Name	Description	Type	Reset
7	CK32K_LOWPWR_EN	0: The 32-kHz oscilator will never goes in low-power mode 1: The 32-kHz oscilator will goes in low-power mode if the main battery voltage is low.	RW	0
6:4	BOOT_CFG	BOOT_CFG = (TEST.RESET, BOOT1, BOOT0)	RO	0x0
3	HIGH_PERF_SQ	0: Slicer not in high perf mode 1: Slicer in high perf mode	RW	1
2	SLICER_BYPASS	0: Slicer not bypassed 1: Slicer bypassed	RW	0
1:0	HFCLK_FREQ	00: not programmed 01: 19.2 MHz 10: 26 MHz 11: 38.4 MHz The software should program this register during the boot sequence.If this register remains at 00 then: - The internal clock_OK from the Slicer is tied to 1. - The DCDCs will not be able to use the divided HF clock (they will remain on their internal oscilator. - The main clock generator will not be able to provide the clock to the MADC and the USB.	RW	0x2

Table 269. SHUNDAN

I2C Address	0x4B			
Physical Address	0x3C	Instance	PM_MASTER	
Description	(Back-up domain)			
Type	RW			

7	6	5	4	3	2	1	0
Reserved		CNT					

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO	0x0
5:0	CNT	When Vbat is low, count up to 2 seconds using a 32-Hz clock (32.768kHz/1024). The default value of this register is 0x3F after the first main battery insertion. The maximum value is 0x3E. This register can be set back to 0x00 by software.	RW	0x3F

Table 270. CFG_PWRANA2

I2C Address	0x4B		
Physical Address	0x3F	**Instance**	PM_MASTER
Description	Configuration for PWRANA2 voltage regulator (Back-up domain)All bits protected with the KEY_TST except VRRTC_SLEEP.		
Type	RW		

7	6	5	4	3	2	1	0
VRRTC_DISABLE	VRRTC_SLEEP	VRRTC_TRIEN	VRRTC_TRIM		LOJIT1_LOWV	LOJIT0_LOWV	BYP_32KHZ_LOWV

Bits	Field Name	Description	Type	Reset
7	VRRTC_DISABLE	0: Functional mode 1: VRRTC LDO will be in OFF mode when it should be in active mode Protected with the KEY_TST	RW	0
6	VRRTC_SLEEP	0: Functional mode 1: VRRTC LDO will be in sleep mode when it should be in active mode	RW	0
5	VRRTC_TRIEN	0: Functional mode 1: Regulator output is High Impedence. Protected with the KEY_TST	RW	0
4:3	VRRTC_TRIM	2 trim bits. Protected with the KEY_TST	RW	0x1
2	LOJIT1_LOWV	This bit is protected with the KEY_TST. If it is used in functionnal mode, the user has to lock back the KEY_TST just after register write.	RW	1
1	LOJIT0_LOWV	If LOJIT0 and LOJT1 are low then the 32k oscilator is in high jitter mode (Low IDDQ/Low Accuracy). In any other cases, the 32k oscilator is in low jitter mode (high IDDQ/High Accuracy). This bit is protected with the KEY_TST. If it is used in functionnal mode, the user has to lock back the KEY_TST just after register write.	RW	1
0	BYP_32KHZ_LOWV	Protected with the KEY_TST This bit reset value is 1 in Slave and test mode.	RW	0

Table 271. BACKUP_MISC_CFG

I2C Address	0x4B		
Physical Address	0x42	**Instance**	PM_MASTER
Description	(Back-up domain)Write protected with the KEY_CFG		
Type	RW		

7	6	5	4	3	2	1	0
Reserved				Reserved		PWR_CLK_MAN	PWR_CLK_FREQ

Bits	Field Name	Description	Type	Reset
7:4	Reserved		RO	0x0
3:2	Reserved	These bits should be used for Metal Fix only	RW	0x0
1	PWR_CLK_MAN	0: Automatic mode. If the HF frequency is at least set to 26MHz, the power internal clock is set to 3 MHz. If the HF frequency is less than 26MHz, the power internal clock is set to 1.5 MHz. 1: Manual mode. The PWR_CLK_FREQ bit is used to select the power internal clock frequency.	RW	0
0	PWR_CLK_FREQ	If PWR_CLK_MAN is equal to 0: no action If PWR_CLK_MAN is equal to 1: 0: The power internal clock is set to 3 MHz. 1: The power internal clock is set to 1.5 MHz.	RW	0

Table 272. PROTECT_KEY

I2C Address	0x4B		
Physical Address	0x44	**Instance**	PM_MASTER
Description	Write any other values than the "good ones" disable access to Power Configuration and Test Registers.Read 01 when access to Power TEST Registers is enabled.Read 10 when access to Power Configuration Registers is enabled.Read 11 when access to Power Configuration and Test Registers is enabled.Read 00 when access to Power Configuration and Test Registers is disabled.When KEY_CFG = 0No write in all register bits protectedRead is still possibleWhen KEY_CFG = 1Read and Write possible in register bits protectedWhen KEY_TST = 0No write in all register bits protectedNo READ in all register bits protected (RETURN 0)When KEY_TST = 1Read and Write possible in register bits protected(VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
PROTECT_KEY							

Bits	Field Name	Description	Type	Reset
7:0	PROTECT_KEY		RW	0x00

Table 273. STS_HW_CONDITIONS

I2C Address	0x4B		
Physical Address	0x45	**Instance**	PM_MASTER
Description	(VRRTC domain)		
Type	RO		

7	6	5	4	3	2	1	0
STS_VBUS	STS_WAKEUP3	Reserved	STS_WAKEUP1	STS_WARMRESET	STS_USB	Reserved	STS_PWON

Bits	Field Name	Description	Type	Reset
7	STS_VBUS	Level status of VBUS port, 1 means usb is plugged, 0 unplugged	RO	0
6	STS_WAKEUP3	Level status of WAKEUP3 pad (active high) = CLKREQ	RO	0
5	Reserved		RO	0
4	STS_WAKEUP1	Level status of WAKEUP1 pad (active high) = NSLEEP1	RO	0
3	STS_WARMRESET	0: Warmreset is not active, nreswarm pad is high1: warmreset is active, nreswarm pad is low.	RO	0
2	STS_USB	Level status of USB port , 1 means usb is plugged , 0 unplugged	RO	0
1	Reserved		RO	0
0	STS_PWON	Level status of PWON button (active high), after debouncing	RO	0

Table 274. P1_SW_EVENTS

I2C Address	0x4B		
Physical Address	0x46	**Instance**	PM_MASTER
Description	(VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	STOPON_PWRON	STOPON_SYSEN	ENABLE_WARMRESET	LVL_WAKEUP	DEVACT	DEVSLP	DEVOFF

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	STOPON_PWRON	0: The registers except backup domain will not be reset by the PWRON key push longer than 8 seconds 1: The registers except backup domain will be reset by the PWRON key push longer than 8 seconds and TPS65921 will restart This bit is common to all processor and can be updated from registers P1_SW_EVENTS, P2_SW_EVENTS, P3_SW_EVENTS	RW	1
5	STOPON_SYSEN	0: disable triton reset when SYSEN is driven low by an external device. 1: enable triton reset when SYSEN is driven low by an external device.This bit is common to all processor and can be updated from registers P1_SW_EVENTS, P2_SW_EVENTS, P3_SW_EVENTS	RW	0
4	ENABLE_WARMRESET	0: Disable Warmreset feature for all processor 1: Enable Warmreset feature for all processor	RW	0
3	LVL_WAKEUP	0: NSLEEP1 signal can't set P1 subsystem resources in sleep mode. Resources will still wakeup on the NSLEEP1 rising edge. 1: Resources associated to P1 will be in Active mode if NSLEEP1 is high and in sleep mode if NSLEEP1 is low.	RW	0
2	DEVACT	Write 1 will start a OFF2ACT or SLP2ACT transition.This bit is cleared automatically.	WO	0
1	DEVSLP	Write 1 will start a ACT2SLP transition. This bit is cleared automatically.	WO	0
0	DEVOFF	Write 1 will start a ACT2OFF or SLP2OFF transition. This bit is cleared automatically.	WO	0

Table 275. P2_SW_EVENTS

I2C Address	0x4B		
Physical Address	0x47	**Instance**	PM_MASTER
Description	(VRRTC domain)Must not be used as NSLEEP2 removed.		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	STOPON_PWRON	STOPON_SYSEN	ENABLE_WARMRESET	LVL_WAKEUP	DEVACT	DEVSLP	DEVOFF

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	STOPON_PWRON	0: The registers except backup domain will not be reset by the PWRON key push longer than 8 seconds 1: The registers except backup domain will be reset by the PWRON key push longer than 8 seconds and TPS65921 will restart This bit is common to all processor and can be updated from registers P1_SW_EVENTS, P2_SW_EVENTS, P3_SW_EVENTS	RW	1
5	STOPON_SYSEN	0: disable triton reset when SYSEN is driven low by an external device. 1: enable triton reset when SYSEN is driven low by an external device. This bit is common to all processor and can be updated from registers P1_SW_EVENTS, P2_SW_EVENTS, P3_SW_EVENTS	RW	0
4	ENABLE_WARMRESET	0: Disable Warmreset feature for all processor 1: Enable Warmreset feature for all processor	RW	0
3	LVL_WAKEUP	0: NSLEEP2 signal can't set P2 subsystem resources in sleep mode. Resources will still wakeup on the NSLEEP2 rising edge. 1: Resources associated to P2 will be in Active mode if NSLEEP2 is high and in sleep mode if NSLEEP2 is low.	RW	0
2	DEVACT	Write 1 will start a OFF2ACT or SLP2ACT transition.This bit is cleared automatically.	WO	0
1	DEVSLP	Write 1 will start a ACT2SLP transition.This bit is cleared automatically.	WO	0
0	DEVOFF	Write 1 will start a ACT2OFF or SLP2OFF transition.This bit is cleared automatically.	WO	0

Table 276. P3_SW_EVENTS

I2C Address	0x4B		
Physical Address	0x48	**Instance**	PM_MASTER
Description	(VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	STOPON_PWRON	STOPON_SYSEN	ENABLE_WARMRESET	LVL_WAKEUP	DEVACT	DEVSLP	DEVOFF

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	STOPON_PWRON	0: The registers except backup domain will not be reset by the PWRON key push longer than 8 seconds 1: The registers except backup domain will be reset by the PWRON key push longer than 8 seconds and TPS65921 will restart This bit is common to all processor and can be updated from registers P1_SW_EVENTS, P2_SW_EVENTS, P3_SW_EVENTS	RW	1
5	STOPON_SYSEN	0: disable triton reset when SYSEN is driven low by an external device. 1: enable triton reset when SYSEN is driven low by an external device.This bit is common to all processor and can be updated from registers P1_SW_EVENTS, P2_SW_EVENTS, P3_SW_EVENTS	RW	0
4	ENABLE_WARMRESET	0: Disable Warmreset feature for all processor 1: Enable Warmreset feature for all processor	RW	0
3	LVL_WAKEUP	0: CLKREQ signal can't set P3 subsystem resources in sleep mode. Resources will still wakeup on the CLKREQ rising edge. 1: Resources associated to P3 will be in Active mode if CLKREQ is high and in sleep mode if CLKREQ is low.	RW	0
2	DEVACT	Write 1 will start a OFF2ACT or SLP2ACT transition.This bit is cleared automatically.	WO	0
1	DEVSLP	Write 1 will start a ACT2SLP transition. This bit is cleared automatically.	WO	0
0	DEVOFF	Write 1 will start a ACT2OFF or SLP2OFF transition. This bit is cleared automatically.	WO	0

Table 277. STS_P123_STATE

I2C Address	0x4B		
Physical Address	0x49	**Instance**	PM_MASTER
Description	(VRRTC domain)		
Type	RO		

7	6	5	4	3	2	1	0
Reserved	STS_P123_STATE_STABLE	SEQ_P3_STATE		SEQ_P2_STATE		SEQ_P1_STATE	

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	STS_P123_STATE_STABLE	Status of P123 state machine. 0: A transition is on-going on one of the state machines. 1: No transition is on-going on the state machines.	RO	0
5:4	SEQ_P3_STATE	Current state of sequencer P3 00 = WaitOn 01 = Active 10 = Sleep 11 = Others	RO	0x0
3:2	SEQ_P2_STATE	Current state of sequencer P2 00 = WaitOn 01 = Active 10 = Sleep 11 = Others	RO	0x0
1:0	SEQ_P1_STATE	Current state of sequencer P1 00 = WaitOn 01 = Active 10 = Sleep 11 = Others	RO	0x0

Table 278. PB_CFG

I2C Address	0x4B			
Physical Address	0x4A	Instance	PM_MASTER	
Description	(VRRTC domain)			
Type	RW			

7	6	5	4	3	2	1	0
Reserved				PB_P123_BW		PB_I2C_BWEN	PB_I2C_BUSY

Bits	Field Name	Description	Type	Reset
7:4	Reserved		RO	0x0
3:2	PB_P123_BW	00 : P1, P2 , P3 have each band width equity (33% if PB_I2C_BWEN is low or 25% if PB_I2C_BWEN is high) 01 : P1 has 50% Power Bus band width, others shared 50% Band width with equity (25% if PB_I2C_BWEN is low or 16% if PB_I2C_BWEN is high)10 : P2 has 50% Power Bus band width, others shared 50% Band width with equity(25% if PB_I2C_BWEN is low or 16% if PB_I2C_BWEN is high)11 : P3 has 50% Power Bus band width, others shared 50% Band width with equity(25% if PB_I2C_BWEN is low or 16% if PB_I2C_BWEN is high)	RW	0x0
1	PB_I2C_BWEN	When 0 : I2C has no access on Power Bus When 1 : I2C has access to Power Bus (Reduce Band width for P[123] that have not the 50% band width)	RW	0
0	PB_I2C_BUSY	1 : PB Word is queued and has not been send on power bus 0: buffer empty / ready to send a word on power bus	RO	0

Table 279. PB_WORD_MSB

I2C Address	0x4B			
Physical Address	0x4B	Instance	PM_MASTER	
Description	(VRRTC domain)			
Type	RW			

7	6	5	4	3	2	1	0
PB_WORD_MSB							

Bits	Field Name	Description	Type	Reset
7:0	PB_WORD_MSB	PB_Word MSB	RW	0xFF

Table 280. PB_WORD_LSB

I2C Address	0x4B			
Physical Address	0x4C	Instance	PM_MASTER	
Description	(VRRTC domain)			
Type	RW			

7	6	5	4	3	2	1	0
PB_WORD_LSB							

Bits	Field Name	Description	Type	Reset
7:0	PB_WORD_LSB	PB_Word LSB. This register write trigs PB word write.	RW	0xFF

Table 281. RESERVED_E

I2C Address	0x4B						
Physical Address	0x51	**Instance**		PM_MASTER			
Description	Write protected with the KEY_CFG (VRRTC domain)						
Type	RW						

7	6	5	4	3	2	1	0
Reserved					CFG_VBUSDEB		

Bits	Field Name	Description	Type	Reset
7:3	Reserved		RO	0x00
2:0	CFG_VBUSDEB	Programmable debounce on VBUS and ID for Power SC starting event and IT generation. 000: 0 ms 001: 14 ms 010: 28 ms 011: 42 ms 100: 70 ms 101: 93 ms 110: 140 ms 111: 233 ms	RW	0x2

Table 282. SEQ_ADD_W2P

I2C Address	0x4B						
Physical Address	0x52	**Instance**		PM_MASTER			
Description	Memory Address of WaitOn toPresenceCheck sequence base add (VRRTC domain)Write protected with the KEY_CFG						
Type	RW						

7	6	5	4	3	2	1	0
Reserved		SEQ_ADD					

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO	0x0
5:0	SEQ_ADD	Memory Adress for transition start step.	RW	0x00

Table 283. SEQ_ADD_P2A

I2C Address	0x4B						
Physical Address	0x53	**Instance**		PM_MASTER			
Description	Memory Address of PresenceCheck to Active sequence base add (VRRTC domain)Write protected with the KEY_CFG						
Type	RW						

7	6	5	4	3	2	1	0
Reserved		SEQ_ADD					

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO	0x0
5:0	SEQ_ADD	Memory Adress for transition start step.	RW	0x04

Table 284. SEQ_ADD_A2W

I2C Address	0x4B			
Physical Address	0x54	Instance	PM_MASTER	
Description	Memory Address of All to WaitOn sequence base add (VRRTC domain)Write protected with the KEY_CFG			
Type	RW			

7	6	5	4	3	2	1	0
Reserved		SEQ_ADD					

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO	0x0
5:0	SEQ_ADD	Memory Adress for transition start step.	RW	0x0D

Table 285. SEQ_ADD_A2S

I2C Address	0x4B			
Physical Address	0x55	Instance	PM_MASTER	
Description	Memory Address of Active to Sleep sequence base add (VRRTC domain)Write protected with the KEY_CFG			
Type	RW			

7	6	5	4	3	2	1	0
Reserved		SEQ_ADD					

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO	0x0
5:0	SEQ_ADD	Memory Adress for transition start step.	RW	0x3F

Table 286. SEQ_ADD_S2A12

I2C Address	0x4B			
Physical Address	0x56	Instance	PM_MASTER	
Description	Memory Address of Sleep to Active sequence base add (VRRTC domain)Write protected with the KEY_CFG			
Type	RW			

7	6	5	4	3	2	1	0
Reserved		SEQ_ADD					

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO	0x0
5:0	SEQ_ADD	Memory Adress for transition start step.	RW	0x3F

Table 287. SEQ_ADD_S2A3

I2C Address	0x4B		
Physical Address	0x57	**Instance**	PM_MASTER
Description	Memory Address of Sleep to Active sequence base add (VRRTC domain)Write protected with the KEY_CFG		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		SEQ_ADD					

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO	0x0
5:0	SEQ_ADD	Memory Adress for transition start step.	RW	0x3F

Table 288. SEQ_ADD_WARM

I2C Address	0x4B		
Physical Address	0x58	**Instance**	PM_MASTER
Description	Memory Address of Sleep to Active sequence base add (VRRTC domain)Write protected with the KEY_CFG		
Type	RW		

7	6	5	4	3	2	1	0
Reserved		SEQ_ADD					

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO	0x0
5:0	SEQ_ADD	Memory Adress for transition start step.	RW	0x3F

Table 289. MEMORY_ADDRESS

I2C Address	0x4B		
Physical Address	0x59	**Instance**	PM_MASTER
Description	Select the memory location to be upbated (VRRTC domain)Write protected with the KEY_CFG		
Type	RW		

7	6	5	4	3	2	1	0
ADDRESS							

Bits	Field Name	Description	Type	Reset
7:0	ADDRESS	Memory Write Address : address(6 bit) of Sequences memory concatenated with byte number within the world	RW	0x00

Table 290. MEMORY_DATA

I2C Address	0x4B		
Physical Address	0x5A	**Instance**	PM_MASTER
Description	Data to write in the selected Memory address (VRRTC domain)Write protected with the KEY_CFG		
Type	RW		

7	6	5	4	3	2	1	0
MEMORY_DATA							

Bits	Field Name	Description	Type	Reset
7:0	MEMORY_DATA	Memory Datawhen accessing to MEMORY_DATA register, the MEMORY_ADRRESS is automatically incremented.	RW	0x18

5.7 PM_RECEIVER

This section provides information on the PM_RECEIVER module instances POWER. Each of the registers within the different PM_RECEIVER module instances is described separately below.

(VRRTC domain)

5.7.1 PM_RECEIVER Registers Mapping Summary

Table 291. PM_RECEIVER Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	Address Offset	Physical Address
SC_CONFIG	RW	8	0x00	0x00	0x5B
SC_DETECT1	RW	8	0x00	0x01	0x5C
SC_DETECT2	RW	8	0x00	0x02	0x5D
WATCHDOG_CFG	RW	8	0x1F	0x03	0x5E
IT_CHECK_CFG	RW	8	0x00	0x04	0x5F
DCDC_GLOBAL_CFG	RW	8	0x00	0x06	0x61
MISC_CFG	RW	8	0x12	0x0D	0x68
VAUX2_DEV_GRP	RW	8	0x00	0x1B	0x76
VAUX2_TYPE	RW	8	0x00	0x1C	0x77
VAUX2_REMAP	RW	8	0x08	0x1D	0x78
VAUX2_DEDICATED	RW	8	0x09	0x1E	0x79
VMMC1_DEV_GRP	RW	8	0x00	0x27	0x82
VMMC1_TYPE	RW	8	0x00	0x28	0x83
VMMC1_REMAP	RW	8	0x08	0x29	0x84
VMMC1_DEDICATED	RW	8	0x02	0x2A	0x85
VPLL1_DEV_GRP	RW	8	0x20	0x2F	0x8A
VPLL1_TYPE	RW	8	0x03	0x30	0x8B
VPLL1_REMAP	RW	8	0x08	0x31	0x8C
VPLL1_DEDICATED	RW	8	0x03	0x32	0x8D
VDAC_DEV_GRP	RW	8	0x00	0x3B	0x96
VDAC_TYPE	RW	8	0x00	0x3C	0x97
VDAC_REMAP	RW	8	0x08	0x3D	0x98
VDAC_DEDICATED	RW	8	0x02	0x3E	0x99
VINTANA1_DEV_GRP	RW	8	0xE0	0x3F	0x9A
VINTANA1_TYPE	RW	8	0x01	0x40	0x9B
VINTANA1_REMAP	RW	8	0x08	0x41	0x9C
VINTANA1_DEDICATED	RW	8	0x00	0x42	0x9D
VINTANA2_DEV_GRP	RW	8	0xE0	0x43	0x9E
VINTANA2_TYPE	RW	8	0x00	0x44	0x9F
VINTANA2_REMAP	RW	8	0x08	0x45	0xA0
VINTANA2_DEDICATED	RW	8	0x01	0x46	0xA1
VINTDIG_DEV_GRP	RW	8	0xE0	0x47	0xA2
VINTDIG_TYPE	RW	8	0x01	0x48	0xA3
VINTDIG_REMAP	RW	8	0x08	0x49	0xA4
VINTDIG_DEDICATED	RW	8	0x04	0x4A	0xA5
VIO_DEV_GRP	RW	8	0xE0	0x4B	0xA6
VIO_TYPE	RW	8	0x02	0x4C	0xA7
VIO_REMAP	RW	8	0x08	0x4D	0xA8
VIO_CFG	RW	8	0x00	0x4E	0xA9

Table 291. PM_RECEIVER Register Summary (continued)

Register Name	Type	Register Width (Bits)	Register Reset	Address Offset	Physical Address
VIO_MISC_CFG	RW	8	0x00	0x4F	0xAA
VIO_OSC	RW	8	0x00	0x52	0xAD
VIO_VSEL	RW	8	0x00	0x54	0xAF
VDD1_DEV_GRP	RW	8	0x20	0x55	0xB0
VDD1_TYPE	RW	8	0x04	0x56	0xB1
VDD1_REMAP	RW	8	0x08	0x57	0xB2
VDD1_CFG	RW	8	0x00	0x58	0xB3
VDD1_MISC_CFG	RW	8	0x00	0x59	0xB4
VDD1_OSC	RW	8	0x00	0x5C	0xB7
VDD1_VSEL	RW	8	0x30	0x5E	0xB9
VDD1_VMODE_CFG	RW	8	0x00	0x5F	0xBA
VDD1_VFLOOR	RW	8	0x00	0x60	0xBB
VDD1_STEP	RW	8	0x00	0x62	0xBD
VDD2_DEV_GRP	RW	8	0x20	0x63	0xBE
VDD2_TYPE	RW	8	0x03	0x64	0xBF
VDD2_REMAP	RW	8	0x08	0x65	0xC0
VDD2_CFG	RW	8	0x00	0x66	0xC1
VDD2_MISC_CFG	RW	8	0x00	0x67	0xC2
VDD2_OSC	RW	8	0x00	0x6A	0xC5
VDD2_VSEL	RW	8	0x30	0x6C	0xC7
VDD2_VMODE_CFG	RW	8	0x00	0x6D	0xC8
VDD2_VFLOOR	RW	8	0x00	0x6E	0xC9
VDD2_STEP	RW	8	0x00	0x70	0xCB
VUSB1V5_DEV_GRP	RW	8	0x00	0x71	0xCC
VUSB1V5_TYPE	RW	8	0x00	0x72	0xCD
VUSB1V5_REMAP	RW	8	0x08	0x73	0xCE
VUSB1V8_DEV_GRP	RW	8	0x00	0x74	0xCF
VUSB1V8_TYPE	RW	8	0x00	0x75	0xD0
VUSB1V8_REMAP	RW	8	0x08	0x76	0xD1
VUSB3V1_DEV_GRP	RW	8	0xE0	0x77	0xD2
VUSB3V1_TYPE	RW	8	0x00	0x78	0xD3
VUSB3V1_REMAP	RW	8	0x08	0x79	0xD4
VUSB_DEDICATED1	RW	8	0x14	0x7D	0xD8
VUSB_DEDICATED2	RW	8	0x08	0x7E	0xD9
REGEN_DEV_GRP	RW	8	0xE0	0x7F	0xDA
REGEN_TYPE	RW	8	0x02	0x80	0xDB
REGEN_REMAP	RW	8	0x08	0x81	0xDC
NRESPWRON_DEV_GRP	RW	8	0xE0	0x82	0xDD
NRESPWRON_TYPE	RW	8	0x00	0x83	0xDE
NRESPWRON_REMAP	RW	8	0x08	0x84	0xDF
CLKEN_DEV_GRP	RW	8	0xE0	0x85	0xE0
CLKEN_TYPE	RW	8	0x03	0x86	0xE1
CLKEN_REMAP	RW	8	0x08	0x87	0xE2
SYSEN_DEV_GRP	RW	8	0xE0	0x88	0xE3
SYSEN_TYPE	RW	8	0x06	0x89	0xE4
SYSEN_REMAP	RW	8	0x08	0x8A	0xE5

Table 291. PM_RECEIVER Register Summary (continued)

Register Name	Type	Register Width (Bits)	Register Reset	Address Offset	Physical Address
HFCLKOUT_DEV_GRP	RW	8	0xE0	0x8B	0xE6
HFCLKOUT_TYPE	RW	8	0x00	0x8C	0xE7
HFCLKOUT_REMAP	RW	8	0x08	0x8D	0xE8
CLKOUT32K_DEV_GRP	RW	8	0xE0	0x8E	0xE9
CLKOUT32K_TYPE	RW	8	0x00	0x8F	0xEA
CLKOUT32K_REMAP	RW	8	0x08	0x90	0xEB
TRITON_RESET_DEV_GRP	RW	8	0xE0	0x91	0xEC
TRITON_RESET_TYPE	RW	8	0x06	0x92	0xED
TRITON_RESET_REMAP	RW	8	0x08	0x93	0xEE
MAINREF_DEV_GRP	RW	8	0xE0	0x94	0xEF
MAINREF_TYPE	RW	8	0x00	0x95	0xF0
MAINREF_REMAP	RW	8	0x08	0x96	0xF1

5.7.2 PM_RECEIVER Register Descriptions

Table 292. SC_CONFIG

I2C Address	0x4B		
Physical Address	0x5B	**Instance**	PM_RECEIVER
Description	short circuit configuraion regsiter (VRRTC domain)Reset when signal triton_reset_na is low (WAITON state)		
Type	RW		

7	6	5	4	3	2	1	0
ENABLE	MODE	AUTOCUT	TEN_SEL				

Bits	Field Name	Description	Type	Reset
7	ENABLE	0: OFF 1: ACTIVE	RW	0
6	MODE	Mode = 1 then TEN_SEL is updated by a SW write. =0 then sc_sel is updated every 0.083 s (from 1 to 12) 0 = Unused	RW	0
5	AUTOCUT	0: no AUTOCUT 1: LDOs/DCDCs can be put in sleepmode or the system can goes in waiton state.See SC_DETECT1 and SC_DETECT2 registers.	RW	0
4:0	TEN_SEL	00000: Reserved 00001: TEST_AUX2_LOWV 00010: Reserved 00011: Reserved 00100: TEST_MMC1_LOWV 00101: Reserved 00110: TEST_INTDIG_LOWV 00111: TEST_VINTANA2_LOWV 01000: Reserved 01001: TEST_VDD1_LOWV(0) 01010: TEST_VDD2_LOWV(0) 01011: TEST_VIO_LOWV(0) 01100: TEST_VDAC_LOWV 01101: TEST_VUSB1V5_LOWV 01110: TEST_VUSB1V8_LOWV 01111: TEST_VUSB3V1_LOWV ---------- 10000: TEST_VINTANA_LOWV 10001: TEST_PLL1_LOWV 10010: TEST_POR_LOWV 10011: Reserved 10100: TEST_TSHUT_LOWV 10101: TEST_TSHUT_REG_LOWV 10110: TEST_UPR_LOWV 10111: TEST_VRRTC_LOWV 11000: TEST_HFCLK_LOWV 11001: no output driven high ... 11110: no output driven high 11111: Testv_sw_ctrl (drive the TESTV pad to GND)	RW	0x00

Table 293. SC_DETECT1

I2C Address	0x4B			
Physical Address	0x5C	**Instance**	PM_RECEIVER	
Description	short-circuit detect 1 regsiter (VRRTC domain)			
Type	RW			

7	6	5	4	3	2	1	0
SC_VINTANA2	SC_VINTDIG	Reserved	SC_VMMC1	Reserved	Reserved	SC_VAUX2	Reserved

Bits	Field Name	Description	Type	Reset
7	SC_VINTANA2	0: Normal operation 1: Short circuit present, regulator goes in sleep mode if SC AUTOCUT = 1 This bit is stuck to 1 until the user writes it to 0.Real time short circuit detection value can be read from this register when SC_STATUS of IT_CHECK_CFG Register = 1	RW	0
6	SC_VINTDIG	0: Normal operation 1: Short circuit present, TPS65921 goes in Waiton state if SC AUTOCUT = 1 This bit is stuck to 1 until the user writes it to 0 Real time short circuit detection value can be read from this register when SC_STATUS of IT_CHECK_CFG Register = 1	RW	0
5	Reserved		RW	0
4	SC_VMMC1	0: Normal operation 1: Short circuit present, regulator goes in sleep mode if SC AUTOCUT = 1 This bit is stuck to 1 until the user writes it to 0. Real time short circuit detection value can be read from this register when SC_STATUS of IT_CHECK_CFG Register = 1	RW	0
3	Reserved		RW	0
2	Reserved		RW	0
1	SC_VAUX2	0: Normal operation 1: Short circuit present, regulator goes in sleep mode if SC AUTOCUT = 1 This bit is stuck to 1 until the user writes it to 0. Real time short circuit detection value can be read from this register when SC_STATUS of IT_CHECK_CFG Register = 1	RW	0
0	Reserved		RW	0

Table 294. SC_DETECT2

I2C Address	0x4B				
Physical Address	0x5D	**Instance**	PM_RECEIVER		
Description	short-circuit detect 2 (VRRTC domain)				
Type	RW				

7	6	5	4	3	2	1	0
SC_VUSB3V1	SC_VUSB1V8	SC_VUSB1V5	SC_VDAC	SC_VIO	SC_VDD2	SC_VDD1	Reserved

Bits	Field Name	Description	Type	Reset
7	SC_VUSB3V1	0: Normal operation 1: Short circuit present, regulator goes in sleep mode if SC AUTOCUT = 1 This bit is stuck to 1 until the user writes it to 0. Real time short circuit detection value can be read from this register when SC_STATUS of IT_CHECK_CFG Register = 1	RW	0
6	SC_VUSB1V8	0: Normal operation 1: Short circuit present, regulator goes in off mode if SC AUTOCUT = 1 This bit is stuck to 1 until the user writes it to 0. Real time short circuit detection value can be read from this register when SC_STATUS of IT_CHECK_CFG Register = 1	RW	0
5	SC_VUSB1V5	0: Normal operation 1: Short circuit present, regulator goes in off mode if SC AUTOCUT = 1 This bit is stuck to 1 until the user writes it to 0.Real time short circuit detection value can be read from this register when SC_STATUS of IT_CHECK_CFG Register = 1	RW	0
4	SC_VDAC	0: Normal operation 1: Short circuit present, regulator goes in sleep mode if SC AUTOCUT = 1 This bit is stuck to 1 until the user writes it to 0.Real time short circuit detection value can be read from this register when SC_STATUS of IT_CHECK_CFG Register = 1	RW	0
3	SC_VIO	0: Normal operation 1: Short circuit present, TPS65921 goes in Waiton state if SC AUTOCUT = 1 This bit is stuck to 1 until the user writes it to 0.Real time short circuit detection value can be read from this register when SC_STATUS of IT_CHECK_CFG Register = 1	RW	0
2	SC_VDD2	0: Normal operation 1: Short circuit present, TPS65921 goes in Waiton state if SC AUTOCUT = 1 This bit is stuck to 1 until the user writes it to 0.Real time short circuit detection value can be read from this register when SC_STATUS of IT_CHECK_CFG Register = 1	RW	0
1	SC_VDD1	0: Normal operation 1: Short circuit present, TPS65921 goes in Waiton state if SC AUTOCUT = 1 This bit is stuck to 1 until the user writes it to 0.Real time short circuit detection value can be read from this register when SC_STATUS of IT_CHECK_CFG Register = 1	RW	0
0	Reserved		RW	0

Table 295. WATCHDOG_CFG

I2C Address	0x4B		
Physical Address	0x5E	**Instance**	PM_RECEIVER
Description	watch dog configuration register (VRRTC domain)Reset when signal triton_reset_na is low (WAITON state)This watchdog can be used to stop or restart the system when there is a software or hardware issue.The counter is set to a value (1 to 30 seconds) and if the software doesn't write back a value on the counter or disable the counter (writing 0 on the watchdog), the system is reset after the specified delay.		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			WATCHDOG				

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x00
4:0	WATCHDOG	00000: Watchdog disabled 00001: Device goes to WAIT-ON state 00010: Device goes to WAIT-ON state in 1 second. 00011: Device goes to WAIT-ON state in 2 seconds. 00100: Device goes to WAIT-ON state in 3 seconds. ... When 11110: Device goes to WAIT-ON state in 29 seconds. When 11111: Device goes to WAIT-ON state in 30 seconds. This register is updated every second: Watchdog <= Watchdog – 1 every second.	RW	0x00

Table 296. IT_CHECK_CFG

I2C Address	0x4B		
Physical Address	0x5F	**Instance**	PM_RECEIVER
Description	Interrupts check configuration register (VRRTC domain)This PWRON Interupt check can be used to stop or restart the system when there is a software or hardware issue.If the PWRON interrupt is present and not cleared by the software during the IT_CHECK_DELAY (3 to 6 seconds) then if the IT Check is enabled, the system is reset.If the STARTON_SWBUG bit of the CFG_P1_TRANSITION or CFG_P2_TRANSITION or CFG_P3_TRANSITION is set to 1 then the system restart automaticaly.This register is protected by the power KEY_TST. (VRRTC domain).		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	SC_VREFA_SEL_LOWV	SC_VREFB_SEL_LOWV		SC_STATUS	IT_CHECK_DELAY		ITcheck_Enable

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	SC_VREFA_SEL_LOWV	Set short circuit detection thresold for ressources connected on channel A 0: 0.5 Volts 1: 0.75 Volts This fields are protected by power KEY_TST.	RW	0
5:4	SC_VREFB_SEL_LOWV	Set short circuit detection thresold for ressources connected on channel B 00: 0.5 Volts 01: 0.75 Volts 10: 1.5 Volts 11: 2.0 Volts This fields are protected by power KEY_TST.	RW	0x0
3	SC_STATUS	Set SC_DETECT Register behavior (see SC_DETECT1 and SC_DETECT2 Register description) Reset when signal triton_reset_na is low (WAITON state)	RW	0
2:1	IT_CHECK_DELAY	When 00: IT_CHECK DELAY =3s When 01: IT_CHECK DELAY =4s When 10: IT_CHECK DELAY =5s When 11: IT_CHECK DELAY =6s Reset when signal triton_reset_na is low (WAITON state)	RW	0x0
0	ITCHECK_ENABLE	When 0: Powon IT Check disabled When 1: Powon IT Check enabled Reset when signal triton_reset_na is low (WAITON state)	RW	0

Table 297. DCDC_GLOBAL_CFG

I2C Address	0x4B		
Physical Address	0x61	**Instance**	PM_RECEIVER
Description	DCDC voltage egulators configuration registers (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
CARD_DETECT_2_LEVEL	CARD_DETECT_1_LEVEL	REGEN_PU_DISABLE	SYSEN_PU_DISABLE	SMARTREFLEX_ENABLE	CARD_DETECT_CFG	CLK_32K_DEGATE	CLK_HF_DEGATE

Bits	Field Name	Description	Type	Reset
7	CARD_DETECT_2_LEVEL	0: Card presence detected at high level 1: Card presence detected at low level	RW	0
6	CARD_DETECT_1_LEVEL	0: Card presence detected at high level 1: Card presence detected at low level	RW	0
5	REGEN_PU_DISABLE	0: REGEN Pullup enabled when the open drain is not driven 1: REGEN Pullup never enable	RW	0
4	SYSEN_PU_DISABLE	0: SYSEN Pullup enabled when the open drain is not driven 1: SYSEN Pullup never enable	RW	0
3	SMARTREFLEX_ENABLE	0: Smartreflex is disabled. 1: Smartreflex is Enabled	RW	0
2	CARD_DETECT_CFG	0: The Sim Card is plugged on GPIO1/INT1 (CD2) 1: The MMC2 Card is plugged on GPIO1/INT1 (CD2)	RW	0
1	CLK_32K_DEGATE	0: clk32kout gating is controlled by the PMC STM (default) 1: clk32kout gating is disabled Write access to these bits only in SECURITY_REG_READ_WRITE_MODE mode only. (MSECURE pad = 1)These bits are sync reset to 0 when NRESPWRON is driven low (usual PMC_RESET async reset).	RW	0
0	CLK_HF_DEGATE	0: clkhfout gating is controlled by the PMC STM (default) Clken is controlled by the PMC STM 1: clkhfout gating is disabled Clken is tied to 1 Write access to these bits only in SECURITY_REG_READ_WRITE_MODE mode only. (MSECURE pad = 1)These bits are sync reset to 0 when NRESPWRON is driven low (usual PMC_RESET async reset).	RW	0

Table 298. MISC_CFG

I2C Address	0x4B				
Physical Address	0x68	Instance	PM_RECEIVER		
Description	(VRRTC domain)				
Type	RW				

7	6	5	4	3	2	1	0
TEMP_SEL		VINTANA2_SWITCH_AUTO	CLK_HF_DRV	Reserved	Reserved	Reserved	

Bits	Field Name	Description	Type	Reset
7:6	TEMP_SEL	Hot die interrupt temperature selection.	RW	0x0
5	VINTANA2_SWITCH_AUTO	0: Switch from 2V75 to 2V5 if battery voltage is below 3V0 is manual. 1: Automatic switch is enabled.	RW	0
4	CLK_HF_DRV	Drive capability of the pad. 0: 5 pF 1: 40-pFdefault value for PG 1.0 was 0.	RW	1
3	Reserved		RW	0
2	Reserved		RW	0
1:0	Reserved		RW	0x2

Table 299. VAUX2_DEV_GRP

I2C Address	0x4B				
Physical Address	0x76	Instance	PM_RECEIVER		
Description					
Type	RW				

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device Group 000: Associated with no device group 001: Associated with P1 device group 010: Associated with P2 device group 011: Associated with P1 and P2 device group 100: Associated with P3 device group 101: Associated with P1 and P3 device group 110: Associated with P2 and P3 device group 111: Associated with all device groups	RW	0x0
4	WARM_CFG	1: When the resource is in the Warmreset state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in the Warmreset state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	RO	0x0

Table 300. VAUX2_TYPE

I2C Address	0x4B		
Physical Address	0x77	**Instance**	PM_RECEIVER
Description			
Type	RW		

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4:3	RES_TYPE2	Ressource Type 2 (Mainly used for Warmreset)	RW	0x0
2:0	RES_TYPE	Ressource Type	RW	0x0

Table 301. VAUX2_REMAP

I2C Address	0x4B		
Physical Address	0x78	**Instance**	PM_RECEIVER
Description			
Type	RW		

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in OFF mode, the OFF_STATE allows to set the resource in SLEEP or ACTIVE mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in SLEEP mode, the SLEEP_STATE allows to set the resource in OFF or ACTIVE mode.	RW	0x8

Table 302. VAUX2_DEDICATED

I2C Address	0x4B		
Physical Address	0x79	**Instance**	PM_RECEIVER
Description			
Type	RW		

7	6	5	4	3	2	1	0
Reserved	TRIEN	TRIM		VSEL			

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	TRIEN	0: Functionnal mode 1: Regulator output is High Impedence. Protected with the KEY_TST	RW	0
5:4	TRIM	2 trim bits. Protected with the KEY_TST	RW	0x0
3:0	VSEL	Select LDO output voltageVSEL 0000: 1.70, 1000: 2.10 0001: 1.70, 1001: 2.80 0010: 1.90, 1010: 2.20 0011: 1.30, 1011: 2.30 0100: 1.50, 1100: 2.40 0101: 1.80, 1101: 2.40 0110: 2.00, 1110: 2.40 0111: 2.50, 1111: 2.40	RW	0x5

Table 303. VMMC1_DEV_GRP

I2C Address	0x4B		
Physical Address	0x82	**Instance**	PM_RECEIVER
Description	Voltage regulator : VMMC1 device group register (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device Group 000: Associated with no device group 001: Associated with P1 device group 010: Associated with P2 device group 011: Associated with P1 and P2 device group 100: Associated with P3 device group 101: Associated with P1 and P3 device group 110: Associated with P2 and P3 device group 111: Associated with all device groups	RW	0x0
4	WARM_CFG	1: When the resource is in the Warmreset state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in the Warmreset state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	RO	0x0

Table 304. VMMC1_TYPE

I2C Address	0x4B		
Physical Address	0x83	**Instance**	PM_RECEIVER
Description	VMMC1 ressource type setting (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4:3	RES_TYPE2	Ressource Type 2 (Mainly used for Warmreset)	RW	0x0
2:0	RES_TYPE	Ressource Type	RW	0x0

Table 305. VMMC1_REMAP

I2C Address	0x4B		
Physical Address	0x84	**Instance**	PM_RECEIVER
Description	When VMMC1 device is either in SLEEP or OFF mode allows to set the resource in Active or OFF/SLEEP (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in OFF mode, the OFF_STATE allows to set the resource in SLEEP or ACTIVE mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in SLEEP mode, the SLEEP_STATE allows to set the resource in OFF or ACTIVE mode.	RW	0x8

Table 306. VMMC1_DEDICATED

I2C Address	0x4B		
Physical Address	0x85	**Instance**	PM_RECEIVER
Description	Voltage regulator: VMMC1 basic settings (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	TRIEN	TRIM		Reserved		VSEL	

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	TRIEN	0: Functionnal mode 1: Regulator output is High Impedence. Protected with the KEY_TST	RW	0
5:4	TRIM	2 trim bits. Protected with the KEY_TST	RW	0x0
3:2	Reserved		RO	0x0
1:0	VSEL	Select LDO output voltage 00: 1.85 01: 2.85 10: 3.00 11: 3.15	RW	0x2

Table 307. VPLL1_DEV_GRP

I2C Address	0x4B		
Physical Address	0x8A	**Instance**	PM_RECEIVER
Description	Voltage regulator : VPLL1 device group register (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device Group 000: Associated with no device group 001: Associated with P1 device group 010: Associated with P2 device group 011: Associated with P1 and P2 device group 100: Associated with P3 device group 101: Associated with P1 and P3 device group 110: Associated with P2 and P3 device group 111: Associated with all device groups	RW	0x1
4	WARM_CFG	1: When the resource is in the Warmreset state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in the Warmreset state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	RO	0x0

Table 308. VPLL1_TYPE

I2C Address	0x4B			
Physical Address	0x8B	**Instance**	PM_RECEIVER	
Description	VPLL1 ressource type setting (VRRTC domain)			
Type	RW			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4:3	RES_TYPE2	Ressource Type 2 (Mainly used for Warmreset)	RW	0x0
2:0	RES_TYPE	Ressource Type	RW	0x3

Table 309. VPLL1_REMAP

I2C Address	0x4B			
Physical Address	0x8C	**Instance**	PM_RECEIVER	
Description	When VPLL1 device is either in SLEEP or OFF mode allows to set the resource in Active or OFF/SLEEP (VRRTC domain)			
Type	RW			

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in OFF mode, the OFF_STATE allows to set the resource in SLEEP or ACTIVE mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in SLEEP mode, the SLEEP_STATE allows to set the resource in OFF or ACTIVE mode.	RW	0x8

Table 310. VPLL1_DEDICATED

I2C Address	0x4B		
Physical Address	0x8D	**Instance**	PM_RECEIVER
Description	Voltage regulator: VPLL1 basic settings (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	TRIEN	TRIM		Reserved	VSEL		

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	TRIEN	0: Functionnal mode 1: Regulator output is High Impedence. Protected with the KEY_TST	RW	0
5:4	TRIM	2 trim bits. Protected with the KEY_TST	RW	0x0
3	Reserved		RO	0
2:0	VSEL	Select LDO output voltage 000: 1.0 001: 1.2 010: 1.3 011: 1.8 100: 2.8 101: 3.0 110: 3.0 111: 3.0	RW	0x3

Table 311. VDAC_DEV_GRP

I2C Address	0x4B		
Physical Address	0x96	**Instance**	PM_RECEIVER
Description	Voltage regulator : VDAC device group register (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device Group 000: Associated with no device group 001: Associated with P1 device group 010: Associated with P2 device group 011: Associated with P1 and P2 device group 100: Associated with P3 device group 101: Associated with P1 and P3 device group 110: Associated with P2 and P3 device group 111: Associated with all device groups	RW	0x0
4	WARM_CFG	1: When the resource is in the Warmreset state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in the Warmreset state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	RO	0x0

Table 312. VDAC_TYPE

I2C Address	0x4B			
Physical Address	0x97	**Instance**	PM_RECEIVER	
Description	VDAC ressource type setting (VRRTC domain)			
Type	RW			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4:3	RES_TYPE2	Ressource Type 2 (Mainly used for Warmreset)	RW	0x0
2:0	RES_TYPE	Ressource Type	RW	0x0

Table 313. VDAC_REMAP

I2C Address	0x4B			
Physical Address	0x98	**Instance**	PM_RECEIVER	
Description	When VDAC device is either in SLEEP or OFF mode allows to set the resource in Active or OFF/SLEEP (VRRTC domain)			
Type	RW			

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in OFF mode, the OFF_STATE allows to set the resource in SLEEP or ACTIVE mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in SLEEP mode, the SLEEP_STATE allows to set the resource in OFF or ACTIVE mode.	RW	0x8

Table 314. VDAC_DEDICATED

I2C Address	0x4B			
Physical Address	0x99	**Instance**	PM_RECEIVER	
Description	Voltage regulator: VDAC basic settings (VRRTC domain)			
Type	RW			

7	6	5	4	3	2	1	0
Reserved	TRIEN	TRIM		Reserved		VSEL	

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	TRIEN	0: Functionnal mode 1: Regulator output is High Impedence. Protected with the KEY_TST	RW	0
5:4	TRIM	2 trim bits. Protected with the KEY_TST	RW	0x0
3:2	Reserved		RO	0x0
1:0	VSEL	Select LDO output voltage 00: 1.2 01: 1.3 10: 1.8 11: 1.8	RW	0x2

Table 315. VINTANA1_DEV_GRP

I2C Address	0x4B						
Physical Address	0x9A	**Instance**		PM_RECEIVER			
Description	Voltage regulator : VINTANA1 device group register (VRRTC domain)						
Type	RW						

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device Group 000: Associated with no device group 001: Associated with P1 device group 010: Associated with P2 device group 011: Associated with P1 and P2 device group 100: Associated with P3 device group 101: Associated with P1 and P3 device group 110: Associated with P2 and P3 device group 111: Associated with all device groups	RW	0x7
4	WARM_CFG	1: When the resource is in the Warmreset state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in the Warmreset state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	RO	0x0

Table 316. VINTANA1_TYPE

I2C Address	0x4B						
Physical Address	0x9B	**Instance**		PM_RECEIVER			
Description	VINTANA1 ressource type setting (VRRTC domain)						
Type	RW						

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4:3	RES_TYPE2	Ressource Type 2 (Mainly used for Warmreset)	RW	0x0
2:0	RES_TYPE	Ressource Type	RW	0x1

Table 317. VINTANA1_REMAP

I2C Address	0x4B		
Physical Address	0x9C	**Instance**	PM_RECEIVER
Description	When VINTANA1 device is either in SLEEP or OFF mode allows to set the resource in Active or OFF/SLEEP (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in OFF mode, the OFF_STATE allows to set the resource in SLEEP or ACTIVE mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in SLEEP mode, the SLEEP_STATE allows to set the resource in OFF or ACTIVE mode.	RW	0x8

Table 318. VINTANA1_DEDICATED

I2C Address	0x4B		
Physical Address	0x9D	**Instance**	PM_RECEIVER
Description	Voltage regulator: VINTANA1 basic settings (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	TRIEN	TRIM		Reserved			

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	TRIEN	0: Functionnal mode 1: Regulator output is High Impedence. Protected with the KEY_TST	RW	0
5:4	TRIM	2 trim bits. Protected with the KEY_TST	RW	0x0
3:0	Reserved		RO	0x0

Table 319. VINTANA2_DEV_GRP

I2C Address	0x4B						
Physical Address	0x9E	**Instance**		PM_RECEIVER			
Description	Voltage regulator : VINTANA2 device group register (VRRTC domain)						
Type	RW						

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device Group 000: Associated with no device group 001: Associated with P1 device group 010: Associated with P2 device group01 011: Associated with P1 and P2 device group 100: Associated with P3 device group 101: Associated with P1 and P3 device group 110: Associated with P2 and P3 device group 111: Associated with all device groups	RW	0x7
4	WARM_CFG	1: When the resource is in the Warmreset state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in the Warmreset state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	RO	0x0

Table 320. VINTANA2_TYPE

I2C Address	0x4B						
Physical Address	0x9F	**Instance**		PM_RECEIVER			
Description	VINTANA2 ressource type setting (VRRTC domain)						
Type	RW						

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4:3	RES_TYPE2	Ressource Type 2 (Mainly used for Warmreset)	RW	0x0
2:0	RES_TYPE	Ressource Type	RW	0x0

Table 321. VINTANA2_REMAP

I2C Address	0x4B		
Physical Address	0xA0	**Instance**	PM_RECEIVER
Description	When VINTANA2 device is either in SLEEP or OFF mode allows to set the resource in Active or OFF/SLEEP (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in OFF mode, the OFF_STATE allows to set the resource in SLEEP or ACTIVE mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in SLEEP mode, the SLEEP_STATE allows to set the resource in OFF or ACTIVE mode.	RW	0x8

Table 322. VINTANA2_DEDICATED

I2C Address	0x4B		
Physical Address	0xA1	**Instance**	PM_RECEIVER
Description	Voltage regulator: VINTANA2 basic settings (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	TRIEN	TRIM		Reserved			VSEL

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	TRIEN	0: Functionnal mode 1: Regulator output is High Impedence. Protected with the KEY_TST	RW	0
5:4	TRIM	2 trim bits. Protected with the KEY_TST	RW	0x0
3:1	Reserved		RO	0x0
0	VSEL	Select LDO output voltage 0: 2.50 1: 2.75	RW	1

Table 323. VINTDIG_DEV_GRP

I2C Address	0x4B			
Physical Address	0xA2	**Instance**	PM_RECEIVER	
Description	Voltage regulator : VINTDIG device group register (VRRTC domain)			
Type	RW			

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device Group 000: Associated with no device group 001: Associated with P1 device group 010: Associated with P2 device group 011: Associated with P1 and P2 device group 100: Associated with P3 device group 101: Associated with P1 and P3 device group 110: Associated with P2 and P3 device group 111: Associated with all device groups	RW	0x7
4	WARM_CFG	1: When the resource is in the Warmreset state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in the Warmreset state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	RO	0x0

Table 324. VINTDIG_TYPE

I2C Address	0x4B			
Physical Address	0xA3	**Instance**	PM_RECEIVER	
Description	VINTDIG ressource type setting (VRRTC domain)			
Type	RW			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4:3	RES_TYPE2	Ressource Type 2 (Mainly used for Warmreset)	RW	0x0
2:0	RES_TYPE	Ressource Type	RW	0x1

Table 325. VINTDIG_REMAP

I2C Address	0x4B		
Physical Address	0xA4	**Instance**	PM_RECEIVER
Description	When VINTDIG device is either in SLEEP or OFF mode allows to set the resource in Active or OFF/SLEEP (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in OFF mode, the OFF_STATE allows to set the resource in SLEEP or ACTIVE mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in SLEEP mode, the SLEEP_STATE allows to set the resource in OFF or ACTIVE mode.	RW	0x8

Table 326. VINTDIG_DEDICATED

I2C Address	0x4B		
Physical Address	0xA5	**Instance**	PM_RECEIVER
Description	Voltage regulator: VINTDIG basic settings (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	TRIEN	TRIM		VSEL			

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	TRIEN	0: Functionnal mode1: Regulator output is High Impedence. Protected with the KEY_TST	RW	0
5:4	TRIM	2 trim bits. Protected with the KEY_TST	RW	0x0
3:0	VSEL	Select LDO output voltage.This LDO voltage is limited in the range 1.0 to 1.5 volts since it is 0000: 1.00 0001: 1.00 0010: 1.20 0011: 1.30 0100: 1.50... 1111: 1.50	RW	0x4

Table 327. VIO_DEV_GRP

I2C Address	0x4B						
Physical Address	0xA6	**Instance**	PM_RECEIVER				
Description	VIO device group register (VRRTC domain)						
Type	RW						

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device Group 000: Associated with no device group 001: Associated with P1 device group 010: Associated with P2 device group 011: Associated with P1 and P2 device group 100: Associated with P3 device group 101: Associated with P1 and P3 device group 110: Associated with P2 and P3 device group 111: Associated with all device groups	RW	0x7
4	WARM_CFG	1: When the resource is in the Warmreset state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in the Warmreset state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	RO	0x0

Table 328. VIO_TYPE

I2C Address	0x4B						
Physical Address	0xA7	**Instance**	PM_RECEIVER				
Description	Resource type set (VRRTC domain)						
Type	RW						

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4:3	RES_TYPE2	Ressource Type 2 (Mainly used for Warmreset)	RW	0x0
2:0	RES_TYPE	Ressource Type	RW	0x2

Table 329. VIO_REMAP

I2C Address	0x4B		
Physical Address	0xA8	Instance	PM_RECEIVER
Description	When VIO device is either in SLEEP or OFF mode allows to set the resource in Active or OFF/SLEEP (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in OFF mode, the OFF_STATE allows to set the resource in SLEEP or ACTIVE mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in SLEEP mode, the SLEEP_STATE allows to set the resource in OFF or ACTIVE mode.	RW	0x8

Table 330. VIO_CFG

I2C Address	0x4B		
Physical Address	0xA9	Instance	PM_RECEIVER
Description	VIO configuration register (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
Reserved						EN_NDRV_LOWV	BUCK_HIZ_LOWV

Bits	Field Name	Description	Type	Reset
7:2	Reserved		RO	0x00
1	EN_NDRV_LOWV	Forces PWM operation by requiring Synchronous NMOS On every cycle.	RW	0
0	BUCK_HIZ_LOWV	Hi-Z disable mode enable. VDIG level.	RW	0

Table 331. VIO_MISC_CFG

I2C Address	0x4B						
Physical Address	0xAA	**Instance**		PM_RECEIVER			
Description	VIO configuration register (VRRTC domain)						
Type	RW						

7	6	5	4	3	2	1	0
Reserved			BUCK_AMUX		DRIVE_SEL		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4:3	BUCK_AMUX	These bits are the BUCK_VDD1_AMUX bits.	RW	0x0
2:0	DRIVE_SEL	If expected OSC DRIVE is 000 then reg value should be 101 If expected OSC DRIVE is 001 then reg value should be 100 If expected OSC DRIVE is 010 then reg value should be 111 If expected OSC DRIVE is 011 then reg value should be 110 If expected OSC DRIVE is 100 then reg value should be 001 If expected OSC DRIVE is 101 then reg value should be 000 If expected OSC DRIVE is 110 then reg value should be 011 If expected OSC DRIVE is 111 then reg value should be 010	RW	0x0

Table 332. VIO_OSC

I2C Address	0x4B						
Physical Address	0xAD	**Instance**		PM_RECEIVER			
Description	(VRRTC domain)						
Type	RW						

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	OVLAP_SEL			SH_RAMP_SWITCH	

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RW	0
5	Reserved		RO	0
4:2	OVLAP_SEL	If expected OSC OVLAP_SEL is 000 then reg value should be 110 If expected OSC OVLAP_SEL is 001 then reg value should be 111 If expected OSC OVLAP_SEL is 010 then reg value should be 100 If expected OSC OVLAP_SEL is 011 then reg value should be 101 If expected OSC OVLAP_SEL is 100 then reg value should be 010 If expected OSC OVLAP_SEL is 101 then reg value should be 011 If expected OSC OVLAP_SEL is 110 then reg value should be 000 If expected OSC OVLAP_SEL is 111 then reg value should be 001	RW	0x0
1:0	SH_RAMP_SWITCH		RW	0x0

Table 333. VIO_VSEL

I2C Address	0x4B			
Physical Address	0xAF	Instance	PM_RECEIVER	
Description	Controls the output voltage (VRRTC domain)			
Type	RW			

7	6	5	4	3	2	1	0
Reserved							VSEL

Bits	Field Name	Description	Type	Reset
7:1	Reserved		RO	0x00
0	VSEL	0 = 1p8V 1 = 1p85V	RW	0

Table 334. VDD1_DEV_GRP

I2C Address	0x4B			
Physical Address	0xB0	Instance	PM_RECEIVER	
Description	VDD1 device group register (VRRTC domain)			
Type	RW			

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device Group 000: Associated with no device group 001: Associated with P1 device group 010: Associated with P2 device group 011: Associated with P1 and P2 device group 100: Associated with P3 device group 101: Associated with P1 and P3 device group 110: Associated with P2 and P3 device group 111: Associated with all device groups	RW	0x1
4	WARM_CFG	1: When the resource is in the Warmreset state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in the Warmreset state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	RO	0x0

Table 335. VDD1_TYPE

I2C Address	0x4B			
Physical Address	0xB1	Instance	PM_RECEIVER	
Description	Resource type set (VRRTC domain)			
Type	RW			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4:3	RES_TYPE2	Ressource Type 2 (Mainly used for Warmreset)	RW	0x0
2:0	RES_TYPE	Ressource Type	RW	0x4

Table 336. VDD1_REMAP

I2C Address	0x4B		
Physical Address	0xB2	**Instance**	PM_RECEIVER
Description	When VDD1 device is either in SLEEP or OFF mode allows to set the resource in Active or OFF/SLEEP (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in OFF mode, the OFF_STATE allows to set the resource in SLEEP or ACTIVE mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in SLEEP mode, the SLEEP_STATE allows to set the resource in OFF or ACTIVE mode.	RW	0x8

Table 337. VDD1_CFG

I2C Address	0x4B		
Physical Address	0xB3	**Instance**	PM_RECEIVER
Description	VDD1 configuration register (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
Reserved						EN_NDRV_LOWV	BUCK_HIZ_LOWV

Bits	Field Name	Description	Type	Reset
7:2	Reserved		RO	0x00
1	EN_NDRV_LOWV	Forces PWM operation by requiring Synchronous NMOS On every cycle.	RW	0
0	BUCK_HIZ_LOWV	Hi-Z disable mode enable. VDIG level.	RW	0

Table 338. VDD1_MISC_CFG

I2C Address	0x4B		
Physical Address	0xB4	**Instance**	PM_RECEIVER
Description	VDD1 configuration register (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			BUCK_AMUX		DRIVE_SEL		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4:3	BUCK_AMUX	These bits are the BUCK_VDD2_AMUX bits.	RW	0x0
2:0	DRIVE_SEL	If expected OSC DRIVE is 000 then reg value should be 011 If expected OSC DRIVE is 001 then reg value should be 010 If expected OSC DRIVE is 010 then reg value should be 001 If expected OSC DRIVE is 011 then reg value should be 000 If expected OSC DRIVE is 100 then reg value should be 111 If expected OSC DRIVE is 101 then reg value should be 110 If expected OSC DRIVE is 110 then reg value should be 101 If expected OSC DRIVE is 111 then reg value should be 100	RW	0x0

Table 339. VDD1_OSC

I2C Address	0x4B		
Physical Address	0xB7	**Instance**	PM_RECEIVER
Description	(VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	OVLAP_SEL			SH_RAMP_SWITCH	

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RW	0
5	Reserved		RO	0
4:2	OVLAP_SEL	If expected OSC OVLAP_SEL is 000 then reg value should be 11 0If expected OSC OVLAP_SEL is 001 then reg value should be 111 If expected OSC OVLAP_SEL is 010 then reg value should be 100 If expected OSC OVLAP_SEL is 011 then reg value should be 101 If expected OSC OVLAP_SEL is 100 then reg value should be 010 If expected OSC OVLAP_SEL is 101 then reg value should be 011 If expected OSC OVLAP_SEL is 110 then reg value should be 000 If expected OSC OVLAP_SEL is 111 then reg value should be 001	RW	0x0
1:0	SH_RAMP_SWITCH		RW	0x0

Table 340. VDD1_VSEL

I2C Address	0x4B						
Physical Address	0xB9	**Instance**	PM_RECEIVER				
Description	Controls the output voltage (VRRTC domain)						
Type	RW						

7	6	5	4	3	2	1	0
Reserved	VSEL						

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6:0	VSEL	WRITE: Control output voltage when SmartReflex not enabled. READ: if READ_REG = 0: Control output voltage if READ_REG = 1: Value of the register	RW	0x30

Table 341. VDD1_VMODE_CFG

I2C Address	0x4B						
Physical Address	0xBA	**Instance**	PM_RECEIVER				
Description	vmode configuration register (VRRTC domain)						
Type	RW						

7	6	5	4	3	2	1	0
Reserved		STS_BUSY	Reserved	STS_FLOOR	DCDC_SLP	READ_REG	Reserved

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO	0x0
5	STS_BUSY	0: DCDC is not computing a VMODE transition 1: DCDC is computing a VMODE transition	RO	0
4	Reserved		RO	0
3	STS_FLOOR	0: DCDC has not reach VFLOOR voltage output 1: DCDC has reach VFLOOR voltage output	RO	0
2	DCDC_SLP	0: Output voltage in SLEEP mode is the same as in ACTIVE mode 1: Output voltage in SLEEP mode is VFLOOR	RW	0
1	READ_REG	Enable VSEL Register value read	RW	0
0	Reserved		RW	0

Table 342. VDD1_VFLOOR

I2C Address	0x4B						
Physical Address	0xBB	**Instance**	PM_RECEIVER				
Description	Sets the voltage floor of DCDC regulator (VRRTC domain)						
Type	RW						

7	6	5	4	3	2	1	0
Reserved	VFLOOR						

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6:0	VFLOOR	Sets the voltage of the DCDC regulator when the DCDC goes in sleep and DCDC_SLP=1 in VDD1_VMODE_CFG	RW	0x00

Table 343. VDD1_STEP

I2C Address	0x4B			
Physical Address	0xBD	Instance	PM_RECEIVER	
Description	Set the step between 2 voltages changes for VDD1 resource (VRRTC domain)			
Type	RW			

7	6	5	4	3	2	1	0
Reserved			STEP_REG				

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4:0	STEP_REG	Step between 2 voltages changes.STEP = STEP_REG * 10 µs.That is from 10 µs to 310 µs. When STEP_REG = 0 then STEP_PER = 10 µs	RW	0x00

Table 344. VDD2_DEV_GRP

I2C Address	0x4B			
Physical Address	0xBE	Instance	PM_RECEIVER	
Description	VDD2 device group regsiter (VRRTC domain)			
Type	RW			

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device Group 000: Associated with no device group 001: Associated with P1 device group 010: Associated with P2 device group 011: Associated with P1 and P2 device group 100: Associated with P3 device group 101: Associated with P1 and P3 device group 110: Associated with P2 and P3 device group 111: Associated with all device group	RW	0x1
4	WARM_CFG	1: When the resource is in the Warmreset state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in the Warmreset state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	RO	0x0

Table 345. VDD2_TYPE

I2C Address	0x4B			
Physical Address	0xBF	Instance	PM_RECEIVER	
Description	Resource type set (VRRTC domain)			
Type	RW			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4:3	RES_TYPE2	Ressource Type 2 (Mainly used for Warmreset)	RW	0x0
2:0	RES_TYPE	Ressource Type	RW	0x3

Table 346. VDD2_REMAP

I2C Address	0x4B		
Physical Address	0xC0	**Instance**	PM_RECEIVER
Description	When VDD2 device is either in SLEEP or OFF mode allows to set the resource in Active or OFF/SLEEP (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in OFF mode, the OFF_STATE allows to set the resource in SLEEP or ACTIVE mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in SLEEP mode, the SLEEP_STATE allows to set the resource in OFF or ACTIVE mode.	RW	0x8

Table 347. VDD2_CFG

I2C Address	0x4B		
Physical Address	0xC1	**Instance**	PM_RECEIVER
Description	VDD2 configuration register (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
Reserved						EN_NDRV_LOWV	BUCK_HIZ_LOWV

Bits	Field Name	Description	Type	Reset
7:2	Reserved		RO	0x00
1	EN_NDRV_LOWV	Forces PWM operation by requiring Synchronous NMOS On every cycle.	RW	0
0	BUCK_HIZ_LOWV	Hi-Z disable mode enable. VDIG level.	RW	0

Table 348. VDD2_MISC_CFG

I2C Address	0x4B		
Physical Address	0xC2	**Instance**	PM_RECEIVER
Description	VDD2 configuration register (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			BUCK_AMUX		DRIVE_SEL		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4:3	BUCK_AMUX	These bits are the BUCK_VIO_AMUX bits.	RW	0x0
2:0	DRIVE_SEL	If expected OSC DRIVE is 000 then reg value should be 011 If expected OSC DRIVE is 001 then reg value should be 010 If expected OSC DRIVE is 010 then reg value should be 001 If expected OSC DRIVE is 011 then reg value should be 000 If expected OSC DRIVE is 100 then reg value should be 111 If expected OSC DRIVE is 101 then reg value should be 110 If expected OSC DRIVE is 110 then reg value should be 101 If expected OSC DRIVE is 111 then reg value should be 100	RW	0x0

Table 349. VDD2_OSC

I2C Address	0x4B		
Physical Address	0xC5	**Instance**	PM_RECEIVER
Description	(VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	OVLAP_SEL			SH_RAMP_SWITCH	

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6	Reserved		RW	0
5	Reserved		RO	0
4:2	OVLAP_SEL	If expected OSC OVLAP_SEL is 000 then reg value should be 110 If expected OSC OVLAP_SEL is 001 then reg value should be 111 If expected OSC OVLAP_SEL is 010 then reg value should be 100 If expected OSC OVLAP_SEL is 011 then reg value should be 101 If expected OSC OVLAP_SEL is 100 then reg value should be 010 If expected OSC OVLAP_SEL is 101 then reg value should be 011 If expected OSC OVLAP_SEL is 110 then reg value should be 000 If expected OSC OVLAP_SEL is 111 then reg value should be 001	RW	0x0
1:0	SH_RAMP_SWITCH		RW	0x0

Table 350. VDD2_VSEL

I2C Address	0x4B						
Physical Address	0xC7	**Instance**	PM_RECEIVER				
Description	Controls the output voltage (VRRTC domain)						
Type	RW						

7	6	5	4	3	2	1	0
Reserved	VSEL						

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6:0	VSEL	WRITE: Control output voltage when SmartReflex not enabled. READ: if READ_REG = 0: Control output voltage if READ_REG = 1: Value of the register	RW	0x30

Table 351. VDD2_VMODE_CFG

I2C Address	0x4B						
Physical Address	0xC8	**Instance**	PM_RECEIVER				
Description	vmode configuration register (VRRTC domain)						
Type	RW						

7	6	5	4	3	2	1	0
Reserved		STS_BUSY	Reserved	STS_FLOOR	DCDC_SLP	READ_REG	Reserved

Bits	Field Name	Description	Type	Reset
7:6	Reserved		RO	0x0
5	STS_BUSY	0: DCDC is not computing a VMODE transition 1: DCDC is computing a VMODE transition	RO	0
4	Reserved		RO	0
3	STS_FLOOR	0: DCDC has not reach VFLOOR voltage output 1: DCDC has reach VFLOOR voltage output	RO	0
2	DCDC_SLP	0: Output voltage in SLEEP mode is the same as in ACTIVE mode 1: Output voltage in SLEEP mode is VFLOOR	RW	0
1	READ_REG	Enable VSEL Register value read	RW	0
0	Reserved		RW	0

Table 352. VDD2_VFLOOR

I2C Address	0x4B						
Physical Address	0xC9	**Instance**	PM_RECEIVER				
Description	Sets the voltage floor of DCDC regulator (VRRTC domain)						
Type	RW						

7	6	5	4	3	2	1	0
Reserved	VFLOOR						

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6:0	VFLOOR	Sets the voltage of the DCDC regulator when the DCDC goes in sleep and DCDC_SLP=1 in VDD2_VMODE_CFG	RW	0x00

Table 353. VDD2_STEP

I2C Address	0x4B			
Physical Address	0xCB	Instance	PM_RECEIVER	
Description	Set the step between 2 voltages changes for VDD1 resource (VRRTC domain)			
Type	RW			

7	6	5	4	3	2	1	0
Reserved			STEP_REG				

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4:0	STEP_REG	Step between 2 voltages changes.STEP = STEP_REG * 10 µs.That is from 10 µs to 310 µs. When STEP_REG = 0 the DVS is in JUMP mode.	RW	0x00

Table 354. VUSB1V5_DEV_GRP

I2C Address	0x4B			
Physical Address	0xCC	Instance	PM_RECEIVER	
Description	Voltage regulator : VUSB1V5 device group register (VRRTC domain)			
Type	RW			

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device Group 000: Associated with no device group 001: Associated with P1 device group 010: Associated with P2 device group 011: Associated with P1 and P2 device group 100: Associated with P3 device group 101: Associated with P1 and P3 device group 110: Associated with P2 and P3 device group 111: Associated with all device groups	RW	0x0
4	WARM_CFG	1: When the resource is in the Warmreset state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in the Warmreset state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	RO	0x0

Table 355. VUSB1V5_TYPE

I2C Address	0x4B			
Physical Address	0xCD	Instance	PM_RECEIVER	
Description	VUSB1V5 ressource type setting (VRRTC domain)			
Type	RW			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4:3	RES_TYPE2	Ressource Type 2 (Mainly used for Warmreset)	RW	0x0
2:0	RES_TYPE	Ressource Type	RW	0x0

Table 356. VUSB1V5_REMAP

I2C Address	0x4B		
Physical Address	0xCE	**Instance**	PM_RECEIVER
Description	When VUSB1V5 device is either in SLEEP or OFF mode allows to set the resource in Active or OFF/SLEEP (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in OFF mode, the OFF_STATE allows to set the resource in SLEEP or ACTIVE mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in SLEEP mode, the SLEEP_STATE allows to set the resource in OFF or ACTIVE mode.	RW	0x8

Table 357. VUSB1V8_DEV_GRP

I2C Address	0x4B		
Physical Address	0xCF	**Instance**	PM_RECEIVER
Description	Voltage regulator : VUSB1V8 device group register (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device Group 000: Associated with no device group 001: Associated with P1 device group 010: Associated with P2 device group 011: Associated with P1 and P2 device group 100: Associated with P3 device group 101: Associated with P1 and P3 device group 110: Associated with P2 and P3 device group 111: Associated with all device groups	RW	0x0
4	WARM_CFG	1: When the resource is in the Warmreset state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in the Warmreset state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	RO	0x0

Table 358. VUSB1V8_TYPE

I2C Address	0x4B				
Physical Address	0xD0	Instance	PM_RECEIVER		
Description	VUSB1V8 ressource type setting (VRRTC domain)				
Type	RW				

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4:3	RES_TYPE2	Ressource Type 2 (Mainly used for Warmreset)	RW	0x0
2:0	RES_TYPE	Ressource Type	RW	0x0

Table 359. VUSB1V8_REMAP

I2C Address	0x4B				
Physical Address	0xD1	Instance	PM_RECEIVER		
Description	When VUSB1V8 device is either in SLEEP or OFF mode allows to set the resource in Active or OFF/SLEEP (VRRTC domain)				
Type	RW				

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in OFF mode, the OFF_STATE allows to set the resource in SLEEP or ACTIVE mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in SLEEP mode, the SLEEP_STATE allows to set the resource in OFF or ACTIVE mode.	RW	0x8

Table 360. VUSB3V1_DEV_GRP

I2C Address	0x4B			
Physical Address	0xD2	**Instance**	PM_RECEIVER	
Description	Voltage regulator : VUSB3V1 device group register (VRRTC domain)			
Type	RW			

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device Group 000: Associated with no device group 001: Associated with P1 device group 010: Associated with P2 device group 011: Associated with P1 and P2 device group 100: Associated with P3 device group 101: Associated with P1 and P3 device group 110: Associated with P2 and P3 device group 111: Associated with all device group	RW	0x7
4	WARM_CFG	1: When the resource is in the Warmreset state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in the Warmreset state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	RO	0x0

Table 361. VUSB3V1_TYPE

I2C Address	0x4B		
Physical Address	0xD3	**Instance**	PM_RECEIVER
Description	VUSB3V1 ressource type setting (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4:3	RES_TYPE2	Ressource Type 2 (Mainly used for Warmreset)	RW	0x0
2:0	RES_TYPE	Ressource Type	RW	0x0

Table 362. VUSB3V1_REMAP

I2C Address	0x4B		
Physical Address	0xD4	**Instance**	PM_RECEIVER
Description	When VUSB3V1 device is either in SLEEP or OFF mode allows to set the resource in Active or OFF/SLEEP (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in OFF mode, the OFF_STATE allows to set the resource in SLEEP or ACTIVE mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in SLEEP mode, the SLEEP_STATE allows to set the resource in OFF or ACTIVE mode.	RW	0x8

Table 363. VUSB_DEDICATED1

I2C Address	0x4B		
Physical Address	0xD8	**Instance**	PM_RECEIVER
Description	Voltage regulator: VUSB basic settings (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
Reserved	VSEL		WKUPCOMP_EN	USBIN_SW		G1	G0

Bits	Field Name	Description	Type	Reset
7	Reserved		RO	0
6:5	VSEL	VRUSB3P1V level control 000: VRUSB3P1V = 3.10 V 001: VRUSB3P1V = 2.65 V 010: VRUSB3P1V = 2.75 V 011: VRUSB3P1V = 2.85 V 100: VRUSB3P1V = 3.20 V 101: VRUSB3P1V = 3.30 V 110: VRUSB3P1V = 3.40 V 111: VRUSB3P1V = 3.50 V	RW	0x0
4	WKUPCOMP_EN	Enable the VBUS and ID wake-up comparators. For test purpose only, to evaluate VRRTC current consumption. See USB Specification.	RW	1
3:2	USBIN_SW	VRUSB_3V1 VDD switch to VBUS/VBAT 00: No supply 01: Supply is VBAT 10: Supply is VBUS 11: No supply See USB Specification.	RW	0x1
1	G1	Gain loop trimming (for Test mode). See USB Specification.	RW	0
0	G0	Gain loop trimming (for Test mode). See USB Specification.	RW	0

Table 364. VUSB_DEDICATED2

I2C Address	0x4B						
Physical Address	0xD9	**Instance**		PM_RECEIVER			
Description	Voltage regulator: VUSB basic settings (VRRTC domain)						
Type	RW						

7	6	5	4	3	2	1	0
Reserved				VUSB3V1_SLEEP	Reserved		

Bits	Field Name	Description	Type	Reset
7:4	Reserved		RO	0x0
3	VUSB3V1_SLEEP	1: Remap the Active State in Sleep State 0: Active state remapping disabled.This register bit will be set to 1 when LDO is in off state.	RW	1
2:0	Reserved		RO	0x0

Table 365. REGEN_DEV_GRP

I2C Address	0x4B						
Physical Address	0xDA	**Instance**		PM_RECEIVER			
Description	device group register (VRRTC domain)						
Type	RW						

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device Group 000: Associated with no device group 001: Associated with P1 device group 010: Associated with P2 device group 011: Associated with P1 and P2 device group 100: Associated with P3 device group 101: Associated with P1 and P3 device group 110: Associated with P2 and P3 device group 111: Associated with all device groups	RW	0x7
4	WARM_CFG	1: When the resource is in the Warmreset state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in the Warmreset state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	RO	0x0

Table 366. REGEN_TYPE

I2C Address	0x4B			
Physical Address	0xDB	**Instance**	PM_RECEIVER	
Description	ressource type setting (VRRTC domain)			
Type	RW			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4:3	RES_TYPE2	Ressource Type 2 (Mainly used for Warmreset)	RW	0x0
2:0	RES_TYPE	Ressource Type	RW	0x2

Table 367. REGEN_REMAP

I2C Address	0x4B			
Physical Address	0xDC	**Instance**	PM_RECEIVER	
Description	When the device is either in SLEEP or OFF mode allows to set the resource in Active or OFF/SLEEP (VRRTC domain)			
Type	RW			

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in OFF mode, the OFF_STATE allows to set the resource in SLEEP or ACTIVE mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in SLEEP mode, the SLEEP_STATE allows to set the resource in OFF or ACTIVE mode.	RW	0x8

Table 368. NRESPWRON_DEV_GRP

I2C Address	0x4B			
Physical Address	0xDD	**Instance**	PM_RECEIVER	
Description	NRESPWRON device group register (VRRTC domain)			
Type	RW			

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device Group 000: Associated with no device group 001: Associated with P1 device group 010: Associated with P2 device group 011: Associated with P1 and P2 device group 100: Associated with P3 device group 101: Associated with P1 and P3 device group 110: Associated with P2 and P3 device group 111: Associated with all device groups	RW	0x7
4	WARM_CFG	1: When the resource is in the Warmreset state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in the Warmreset state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	RO	0x0

Table 369. NRESPWRON_TYPE

I2C Address	0x4B			
Physical Address	0xDE	**Instance**	PM_RECEIVER	
Description	NRESPWRON ressource type setting (VRRTC domain)			
Type	RW			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4:3	RES_TYPE2	Ressource Type 2 (Mainly used for Warmreset)	RW	0x0
2:0	RES_TYPE	Ressource Type	RW	0x0

Table 370. NRESPWRON_REMAP

I2C Address	0x4B		
Physical Address	0xDF	**Instance**	PM_RECEIVER
Description	When the device is either in SLEEP or OFF mode allows to set the resource in Active or OFF/SLEEP (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in OFF mode, the OFF_STATE allows to set the resource in SLEEP or ACTIVE mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in SLEEP mode, the SLEEP_STATE allows to set the resource in OFF or ACTIVE mode.	RW	0x8

Table 371. CLKEN_DEV_GRP

I2C Address	0x4B		
Physical Address	0xE0	**Instance**	PM_RECEIVER
Description	CLKEN device group register (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device Group 000: Associated with no device group 001: Associated with P1 device group 010: Associated with P2 device group 011: Associated with P1 and P2 device group 100: Associated with P3 device group 101: Associated with P1 and P3 device group 110: Associated with P2 and P3 device group 111: Associated with all device group	RW	0x7
4	WARM_CFG	1: When the resource is in the Warmreset state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in the Warmreset state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	RO	0x0

Table 372. CLKEN_TYPE

I2C Address	0x4B			
Physical Address	0xE1	Instance	PM_RECEIVER	
Description	CLKEN ressource type setting (VRRTC domain)			
Type	RW			

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4:3	RES_TYPE2	Ressource Type 2 (Mainly used for Warmreset)	RW	0x0
2:0	RES_TYPE	Ressource Type	RW	0x3

Table 373. CLKEN_REMAP

I2C Address	0x4B		
Physical Address	0xE2	Instance	PM_RECEIVER
Description	When the device is either in SLEEP or OFF mode allows to set the resource in Active or OFF/SLEEP (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in OFF mode, the OFF_STATE allows to set the resource in SLEEP or ACTIVE mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in SLEEP mode, the SLEEP_STATE allows to set the resource in OFF or ACTIVE mode.	RW	0x8

Table 374. SYSEN_DEV_GRP

I2C Address	0x4B						
Physical Address	0xE3	**Instance**	PM_RECEIVER				
Description	device group register (VRRTC domain)						
Type	RW						

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device Group 000: Associated with no device group 001: Associated with P1 device group 010: Associated with P2 device group 011: Associated with P1 and P2 device group 100: Associated with P3 device group 101: Associated with P1 and P3 device group 110: Associated with P2 and P3 device group 111: Associated with all device groups	RW	0x7
4	WARM_CFG	1: When the resource is in the Warmreset state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in the Warmreset state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	RO	0x0

Table 375. SYSEN_TYPE

I2C Address	0x4B						
Physical Address	0xE4	**Instance**	PM_RECEIVER				
Description	ressource type setting (VRRTC domain)						
Type	RW						

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4:3	RES_TYPE2	Ressource Type 2 (Mainly used for Warmreset)	RW	0x0
2:0	RES_TYPE	Ressource Type	RW	0x6

Table 376. SYSEN_REMAP

I2C Address	0x4B		
Physical Address	0xE5	**Instance**	PM_RECEIVER
Description	When the device is either in SLEEP or OFF mode allows to set the resource in Active or OFF/SLEEP (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in OFF mode, the OFF_STATE allows to set the resource in SLEEP or ACTIVE mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in SLEEP mode, the SLEEP_STATE allows to set the resource in OFF or ACTIVE mode.	RW	0x8

Table 377. HFCLKOUT_DEV_GRP

I2C Address	0x4B		
Physical Address	0xE6	**Instance**	PM_RECEIVER
Description	HFCLKOUT device group register (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device Group 000: Associated with no device group 001: Associated with P1 device group 010: Associated with P2 device group 011: Associated with P1 and P2 device group 100: Associated with P3 device group 101: Associated with P1 and P3 device group 110: Associated with P2 and P3 device group 111: Associated with all device group	RW	0x7
4	WARM_CFG	1: When the resource is in the Warmreset state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in the Warmreset state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	RO	0x0

Table 378. HFCLKOUT_TYPE

I2C Address	0x4B		
Physical Address	0xE7	**Instance**	PM_RECEIVER
Description	HFCLKOUT ressource type setting (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4:3	RES_TYPE2	Ressource Type 2 (Mainly used for Warmreset)	RW	0x0
2:0	RES_TYPE	Ressource Type	RW	0x0

Table 379. HFCLKOUT_REMAP

I2C Address	0x4B		
Physical Address	0xE8	**Instance**	PM_RECEIVER
Description	When the device is either in SLEEP or OFF mode allows to set the resource in Active or OFF/SLEEP (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in OFF mode, the OFF_STATE allows to set the resource in SLEEP or ACTIVE mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in SLEEP mode, the SLEEP_STATE allows to set the resource in OFF or ACTIVE mode.	RW	0x8

Table 380. CLKOUT32K_DEV_GRP

I2C Address	0x4B						
Physical Address	0xE9	**Instance**		PM_RECEIVER			
Description	32KCLKOUT device group register (VRRTC domain)						
Type	RW						

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device Group 000: Associated with no device grou 001: Associated with P1 device group 010: Associated with P2 device group 011: Associated with P1 and P2 device group 100: Associated with P3 device group 101: Associated with P1 and P3 device group 110: Associated with P2 and P3 device group 111: Associated with all device groups	RW	0x7
4	WARM_CFG	1: When the resource is in the Warmreset state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in the Warmreset state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	RO	0x0

Table 381. CLKOUT32K_TYPE

I2C Address	0x4B						
Physical Address	0xEA	**Instance**		PM_RECEIVER			
Description	32KCLKOUT ressource type setting (VRRTC domain)						
Type	RW						

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4:3	RES_TYPE2	Ressource Type 2 (Mainly used for Warmreset)	RW	0x0
2:0	RES_TYPE	Ressource Type	RW	0x0

Table 382. CLKOUT32K_REMAP

I2C Address	0x4B		
Physical Address	0xEB	**Instance**	PM_RECEIVER
Description	When the device is either in SLEEP or OFF mode allows to set the resource in Active or OFF/SLEEP (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in OFF mode, the OFF_STATE allows to set the resource in SLEEP or ACTIVE mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in SLEEP mode, the SLEEP_STATE allows to set the resource in OFF or ACTIVE mode.	RW	0x8

Table 383. TRITON_RESET_DEV_GRP

I2C Address	0x4B		
Physical Address	0xEC	**Instance**	PM_RECEIVER
Description	device group register (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device Group 000: Associated with no device group 001: Associated with P1 device group 010: Associated with P2 device group 011: Associated with P1 and P2 device group 100: Associated with P3 device group 101: Associated with P1 and P3 device group 110: Associated with P2 and P3 device group 111: Associated with all device group	RW	0x7
4	WARM_CFG	1: When the resource is in the Warmreset state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in the Warmreset state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	RO	0x0

Table 384. TRITON_RESET_TYPE

I2C Address	0x4B		
Physical Address	0xED	**Instance**	PM_RECEIVER
Description	ressource type setting (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4:3	RES_TYPE2	Ressource Type 2 (Mainly used for Warmreset)	RW	0x0
2:0	RES_TYPE	Ressource Type	RW	0x6

Table 385. TRITON_RESET_REMAP

I2C Address	0x4B		
Physical Address	0xEE	**Instance**	PM_RECEIVER
Description	When the device is either in SLEEP or OFF mode allows to set the resource in Active or OFF/SLEEP (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in OFF mode, the OFF_STATE allows to set the resource in SLEEP or ACTIVE mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in SLEEP mode, the SLEEP_STATE allows to set the resource in OFF or ACTIVE mode.	RW	0x8

Table 386. MAINREF_DEV_GRP

I2C Address	0x4B		
Physical Address	0xEF	**Instance**	PM_RECEIVER
Description	Voltage regulator : main reference device group register (VRRTC domain)		
Type	RW		

7	6	5	4	3	2	1	0
DEV_GRP			WARM_CFG	STATE			

Bits	Field Name	Description	Type	Reset
7:5	DEV_GRP	Device Group 000: Associated with no device group 001: Associated with P1 device group 010: Associated with P2 device group 011: Associated with P1 and P2 device group 100: Associated with P3 device group 101: Associated with P1 and P3 device group 110: Associated with P2 and P3 device group 111: Associated with all device groups	RW	0x7
4	WARM_CFG	1: When the resource is in the Warmreset state, DEV_GRP is set to 111 and the vsel is set back to the default value. 0: When the resource is in the Warmreset state, DEV_GRP is not changed and the vsel is set back to the default value.	RW	0
3:0	STATE	Current state of the resource	RO	0x0

Table 387. MAINREF_TYPE

I2C Address	0x4B						
Physical Address	0xF0	**Instance**	PM_RECEIVER				
Description	Main reference ressource type setting (VRRTC domain)						
Type	RW						

7	6	5	4	3	2	1	0
Reserved			RES_TYPE2		RES_TYPE		

Bits	Field Name	Description	Type	Reset
7:5	Reserved		RO	0x0
4:3	RES_TYPE2	Ressource Type 2 (Mainly used for Warmreset)	RW	0x0
2:0	RES_TYPE	Ressource Type	RW	0x0

Table 388. MAINREF_REMAP

I2C Address	0x4B						
Physical Address	0xF1	**Instance**	PM_RECEIVER				
Description	When MAIN reference device is either in SLEEP or OFF mode allows to set the resource in Active or OFF/SLEEP (VRRTC domain)						
Type	RW						

7	6	5	4	3	2	1	0
OFF_STATE				SLEEP_STATE			

Bits	Field Name	Description	Type	Reset
7:4	OFF_STATE	When the system requires the resource to be in OFF mode, the OFF_STATE allows to set the resource in SLEEP or ACTIVE mode.	RW	0x0
3:0	SLEEP_STATE	When the system requires the resource to be in SLEEP mode, the SLEEP_STATE allows to set the resource in OFF or ACTIVE mode.	RW	0x8

6 POWER_SR

This section provides information on the POWER_SR module instances within this product. Each of the registers within the different POWER_SR module instances is described separately below.

6.1 POWER_ SR Sub-Chip Instance Summary

The table below shows the base address and address space for the POWER_SR module instances.

Table 389. POWER_SR Instance Summary

Module Name	Base Address
SMARTREFLEX_REG	0x00

6.2 SMARTREFLEX_REG Registers Mapping Summary

Table 390. SMARTREFLEX_REG Register Summary

Register Name	Type	Register Width (Bits)	Register Reset	Address Offset	Physical Address
VDD1_SR_CONTROL	RW	8	0x30	0x00	0x00
VDD2_SR_CONTROL	RW	8	0x30	0x01	0x01

6.3 SMARTREFLEX_REG Register Descriptions

Table 391. VDD1_SR_CONTROL

I2C Address	0x12		
Physical Address	0x00	**Instance**	SMARTREFLEX_REG
Description	Vbat DomainIf the user write X1111111 in this register, only the MODE bit is updated (the VSEL field is not updated).		
Type	RW		

7	6	5	4	3	2	1	0
MODE	VSEL						

Bits	Field Name	Description	Type	Reset
7	MODE	0: VDD1 is in ACTIVE mode 1: VDD1 is in SLEEP mode	RW	0
6:0	VSEL	DCDC Voltage: VSEL*12.5mv + 0.6v.	RW	0x30

Table 392. VDD2_SR_CONTROL

I2C Address	0x12		
Physical Address	0x01	**Instance**	SMARTREFLEX_REG
Description	Vbat DomainIf the user write X1111111 in this register, only the MODE bit is updated (the VSEL field is not updated).		
Type	RW		

7	6	5	4	3	2	1	0
MODE	VSEL						

Bits	Field Name	Description	Type	Reset
7	MODE	0: VDD2 is in ACTIVE mode (and associated ressources VPLL and VIO will also be in active mode) 1: VDD2 is in SLEEP mode (VPLL will be in sleep mode and VIO will be in sleep mode if no other processor needs it)	RW	0
6:0	VSEL	DCDC Voltage: VSEL*12.5mv + 0.6v	RW	0x30

7 Revision History

Table 393. REVISION HISTORY

Version	Literature Number	Date	Notes
C	SWCU067	March 2012	See (1)

(1) *TPSTPS65921*, SWCU067C -
- WATCHDOG_CFG: Update register description and bits [4:0] description
- USB_SW_CHRG_CTRL: Update bits [5:0] description
- CFG_P123_TRANSITION: Update bit [7]

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