TPS659106 User's Guide For i.MX53 Processors

Version A

User's Guide

Literature Number: SWCU090A
July 2011–Revised November 2012

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This document can be used as a reference for connectivity between the TPS659106 power-management unit (PMU) and the Freescale i.MX53 processor.

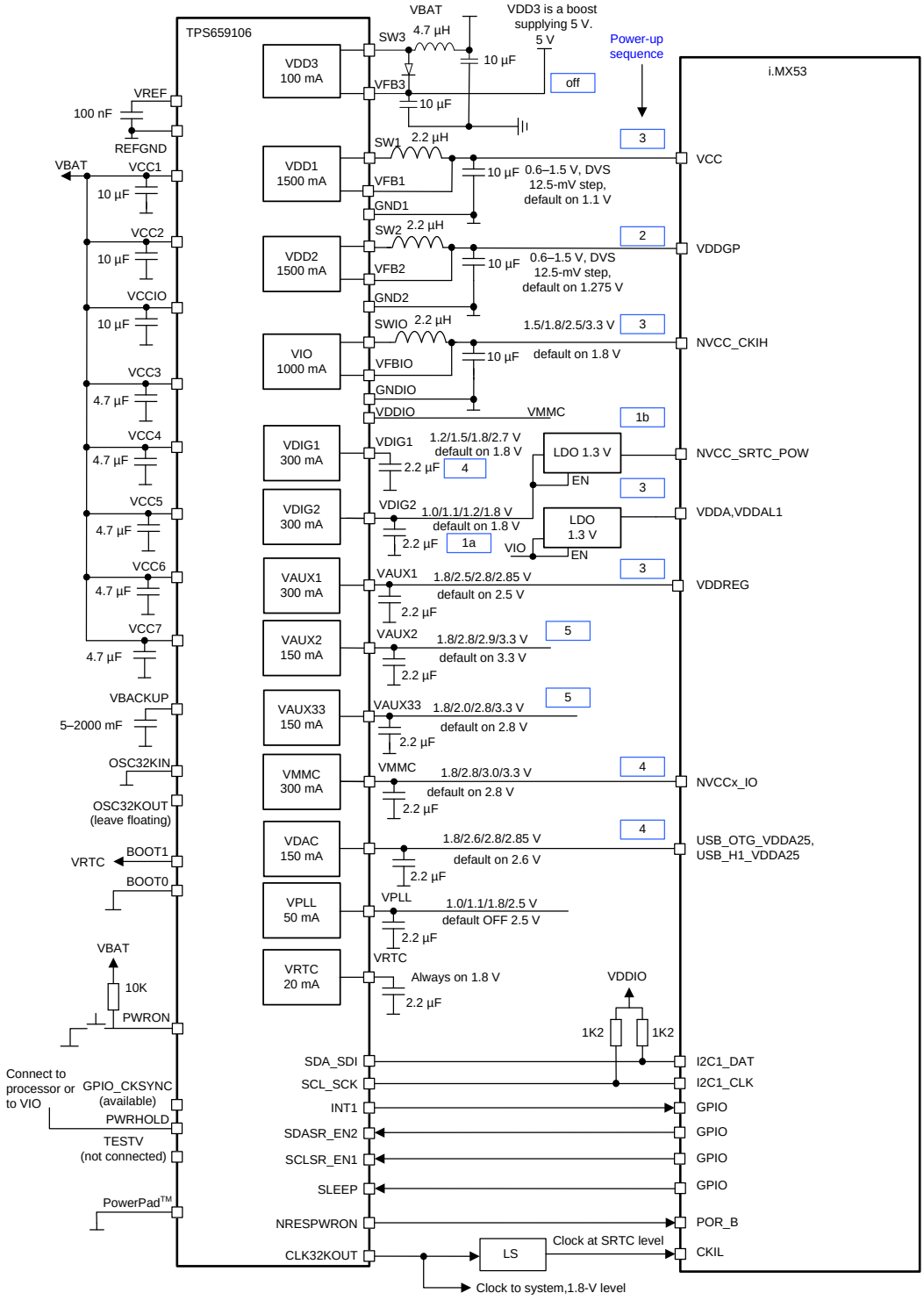
1 Introduction

This document can be used as a reference for connectivity between the TPS659106 PMU and Freescale i.MX53 processor. This document does not provide details about the power resources or the functionality of the PMU device. Refer to the TPS65910x data sheet (TI Literature Number SWCS046) for such information. For information about i.MX53 processors, refer to official information from Freescale.

2 Connection Diagram and TPS659106 EEPROM Configuration For i.MX53

Figure 1 shows connection diagram between the i.MX53 processor and the TPS659106.

Table 1 shows the TPS659106 EEPROM configuration for the i.MX53.



Notes for connection diagram:

- To support the i.MX53 power-up sequence, connect BOOT0 to ground and BOOT1 to VRTC to select the EEPROM boot mode.
- The TPS659106 powers up when a supply is inserted for the first time (defined by the EEPROM bit).
- The level shifter for the 32-kHz clock can be replaced by a resistive divider.
- NVCC_EMI_DRAM of the processor is assumed to be from a discrete buck converter. VDIG1 can be used as an enable signal for the buck.
- The TPS659106 digital control signal level is defined by the VDDIO connection.

Figure 1. Connection Diagram, TPS659106 For i.MX53

Table 1. TPS659106 EEPROM Configuration

Register	Bit	Description	TPS659106 EEPROM
VDD1_OP_REG	SEL	VDD1 voltage level selection for boot	1.1 V
VDD1_REG	VGAIN_SEL	VDD1 gain selection, x1 or x2	x1
EEPROM		VDD1 time slot selection	3
DCDCCTRL_REG	VDD1_PSKIP	VDD1 pulse skip mode enable	Skip enabled
VDD2_OP_REG / VDD2_SR_REG	SEL	VDD2 voltage level selection for boot	1.275 V
VDD2_REG	VGAIN_SEL	VDD2 gain selection, x1 or x3	x1
EEPROM		VDD2 time slot selection	2
DCDCCTRL_REG	VDD2_PSKIP	VDD2 pulse skip mode enable	Skip enabled
VIO_REG	SEL	VIO voltage selection	1.8 V
EEPROM		VIO time slot selection	3
DCDCCTRL_REG	VIO_PSKIP	VIO pulse skip mode enable	Skip enabled
EEPROM		VDD3 time slot	OFF
VDIG1_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	4
VDIG2_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	1
VDAC_REG	SEL	LDO voltage selection	2.6 V
EEPROM		LDO time slot	4
VPLL_REG	SEL	LDO voltage selection	2.5 V
EEPROM		LDO time slot	OFF
VAUX1_REG	SEL	LDO voltage selection	2.5 V
EEPROM		LDO time slot	3
VMMC_REG	SEL	LDO voltage selection	2.8 V
EEPROM		LDO time slot	4
VAUX33_REG	SEL	LDO voltage selection	2.8 V
EEPROM		LDO time slot	5
VAUX2_REG	SEL	LDO voltage selection	3.3 V
EEPROM		LDO time slot	5
CLK32KOUT		CLK32KOUT time slot	7
NRESPWRON		NRESPWRON time slot	7 + 1
VRTC_REG	VRTC_OFFMASK	0 = VRTC LDO will be in low-power mode during the OFF state. 1 = VRC LDO will be in full-power mode during the OFF state.	Low-power mode
DEVCTRL_REG	RTC_PWDN	0 = RTC in normal power mode 1 = Clock gating of RTC register and logic, low-power mode	1
DEVCTRL_REG	CK32K_CTRL	0 = Clock source is crystal/external clock. 1 = Clock source is internal RC oscillator.	RC
DEVCTRL2_REG	TSLOT_LENGTH	Boot sequence time slot duration: 0 = 0.5 ms 1 = 2 ms	2 ms
DEVCTRL2_REG	IT_POL	0 = INT1 signal will be active low. 1 = INT1 signal will be active high.	Active high
INT_MSK_REG	VMBHI_IT_MSK	0 = Device automatically switches on at NO SUPPLY-to-OFF or BACKUP-to-OFF transition. 1 = Start-up is reason required before switch-on.	0
VMBCH_REG	VMBCH_SEL[1:0]	Select threshold for main battery comparator threshold VMBCH.	Bypass

2.1 First Initialization

2.1.1 I/O Polarity/Muxing Configuration

Program the SLEEPSIG_POL bit in the DEVCTRL2_REG register according to the GPIO level setting on the i.MX53 processor. This can be set to active low or active high for SLEEP transitions. Software configuration allows specific power resources to enter a low consumption state.

Set the DEV_SLP bit in the DEVCTRL_REG register to 1 to allow SLEEP transitions when requested.

Update the GPIO0 configuration (GPIO0_REG) based on your needs.

2.1.2 Define Wake-Up/Interrupt Event (Sleep Or Off)

Select the appropriate bits in the INT_MSK_REG and INT_MSK2_REG registers to activate an interrupt to the processor on the INT1 line.

2.1.3 Backup Battery Configuration

If a backup battery is used, then enable backup battery charging by setting the BBCHEN bit in the BBCH_REG register to 1. The maximum voltage can be set based on backup battery specifications by using the BBSEL bits in the BBCH_REG register.

2.1.4 DCDC and Voltage Scaling Resource Configuration

If the SmartReflex™ interface is not used for voltage scaling (power saving) then these pins can be used to control the power resources.

Configure two operating voltages for DCDC1 and DCDC2:

- SEL bit in the VDDx_OP_REG register = Roof voltage (Enx ball high)
- SEL bit in the VDDx_SR_REG register = Floor voltage (Enx ball low)

Assign control for DCDC1 to SCLSR_EN1 and DCDC2 to SCLSR_EN2:

- Set the VDD1_EN1 bit in the EN1_SMPS_ASS_REG register to 1
- Set the VDD2_EN2 bit in the EN2_SMPS_ASS_REG register to 1
- Set the VDD2_KEEPON bit in the SLEEP_KEEP_RES_ON_REG register to 1 (allow low-power mode)
- Set the VDD1_KEEPON bit in the SLEEP_KEEP_RES_ON_REG register to 1 (allow low-power mode)

2.1.5 Sleep Platform Configuration

Configure the state of the LDOs when the SLEEP signal is used. (By default, in the SLEEP state the LDO voltage is maintained but the transient and load capability is reduced.)

Resources that must provide full load capability must be set in the SLEEP_KEEP_LDO_ON_REG register.

Resources that can be set to off in the SLEEP state to optimize power consumption must be set in the SLEEP_SET_LDO_OFF_REG register.

2.2 Event Management Through Interrupts

2.2.1 INT_STS_REG.VMBHI_IT

The VMBHI_IT interrupt bit indicates that a supply (VBAT) is connected. Leaving the BACKUP or NO SUPPLY state, initialization of the system is needed (see Section 2.1, *First Initialization*).

2.2.2 INT_STS_REG.PWRON_IT

The PWRON_IT interrupt bit is triggered by a PWRON button press. If the device is in the OFF or SLEEP state, this acts as a wake-up event and resources are reinitialized.

2.2.3 INT_STS_REG.PWRON_LP_IT

The PWRON_LP_IT interrupt bit is the PWRON long press interrupt. This interrupt is generated when the PWRON switch is pressed for 6 seconds. The application processor can decide to acknowledge the interrupt. If this interrupt is not acknowledged in the next 2 seconds, the device interprets this as a power-down event.

2.2.4 INT_STS_REG.HOTDIE_IT

The HOTDIE_IT interrupt bit indicates that the temperature of the die is reaching the maximum limit. Software must take action to decrease power consumption before automatic shutdown.

2.2.5 INT_STS_REG.VMBDCH_IT

The VMBDCH_IT interrupt bit indicates that the input supply is low and the processor must prepare a shutdown to prevent from losing data.

This interrupt is linked to VBAT but does not apply in a system where the PMIC is not connected directly to VBAT, but to 5-V rails.

2.2.6 INT_STS2_REG.GPIO_R/F_IT

The GPIO interrupt event can be used to awaken the device from the SLEEP state. This can be an interrupt coming from any peripheral device or alike. This wake-up event is not valid for transitions from the OFF state.

2.2.7 INT_STS_REG.RTC_ALARM_IT

The RTC_ALARM_IT interrupt bit is triggered when the set RTC alarm time is reached.

3 Revision History

The following table summarizes the TPS659106 User's Guide For i.MX53 Processors versions.

Note: Numbering may vary from previous versions.

Version	Literature Number	Date	Notes
*	SWCU090	July 2011	See (1)
A	SWCU090A	November 2012	See (2)

(1) TPS659106 User's Guide For i.MX53 Processors, (SWCU090) - Initial release

(2) TPS659106 User's Guide For i.MX53 Processors, (SWCU090A) -

- Figure 1 - Update:
  - VCC power-up sequence: Replcae 2 by 3
  - VDD1 default on: Replace 1.35 V by 1.1 V
  - VDDGP power-up sequence: Replace 3 by 2
  - VDD2 default on: Replace 1.1 V by 1.275 V

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