CC2651P3 SimpleLink™ Single-Protocol 2.4 GHz Wireless MCU With Integrated Power Amplifier

1 Features

Wireless microcontroller

- Powerful 48-MHz Arm® Cortex®-M4 processor
- 352KB flash program memory
- 32KB of ultra-low leakage SRAM
- 8KB of Cache SRAM (Alternatively available as general-purpose RAM)
- Programmable radio includes support for 2-(G)FSK, 4-(G)FSK, MSK, *Bluetooth*® 5.2 Low Energy, IEEE 802.15.4 PHY and MAC
- Supports over-the-air upgrade (OTA)

Low power consumption

- MCU consumption:
  - 2.91 mA active mode, CoreMark®
  - 61 µA/MHz running CoreMark
  - 0.8 µA standby mode, RTC, 32KB RAM
  - 0.1 µA shutdown mode, wake-up on pin
- Radio Consumption:
  - 6.4 mA RX
  - 7.1 mA TX at 0 dBm
  - 9.5 mA TX at +5 dBm
  - 22 mA TX at +10 dBm
  - 101 mA TX at +20 dBm (7x7 package)

Wireless protocol support

- Zigbee®
- *Bluetooth*® 5.2 Low Energy
- SimpleLink™ TI 15.4-stack
- Proprietary systems

High performance radio

- -104 dBm for *Bluetooth*® Low Energy 125-kbps
- Output power up to +20 dBm with temperature compensation

Regulatory compliance

- Suitable for systems targeting compliance with these standards:
  - ETSI EN 300 328, EN 300 440 Cat. 2 and 3
  - FCC CFR47 Part 15
  - ARIB STD-T66

MCU peripherals

- Digital peripherals can be routed to any GPIO
- Four 32-bit or eight 16-bit general-purpose timers
- 12-bit ADC, 200 kSamples/s, 8 channels
- 8-bit DAC
- Analog Comparator
- UART, SSI, I^2C, I^2S
- Real-time clock (RTC)
- Integrated temperature and battery monitor

Security enablers

- AES 128-bit cryptographic accelerator
- True random number generator (TRNG)
- Additional cryptography drivers available in Software Development Kit (SDK)

Development tools and software

- LP-CC2651P3 Development Kit
- SimpleLink™ CC13xx and CC26xx Software Development Kit (SDK)
- SmartRF™ Studio for simple radio configuration
- SysConfig system configuration tool

Operating range

- On-chip buck DC/DC converter
- 1.8-V to 3.8-V single supply voltage
- -40 to +105°C

Package

- 7-mm × 7-mm RGZ VQFN48 (26 GPIOs)
- 5-mm × 5-mm RKP VQFN40 (18 GPIOs)
- RoHS-compliant package

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

2 Applications

- 2400 to 2500 MHz ISM and SRD systems [1] with down to 4 kHz of receive bandwidth
- Building automation
  - Building security systems – motion detector, electronic smart lock, door and window sensor, garage door system, gateway
  - HVAC – thermostat, wireless environmental sensor, HVAC system controller, gateway
  - Fire safety system – smoke and heat detector, fire alarm control panel (FACP)
  - Video surveillance – IP network camera
  - Elevators and escalators – elevator main control panel for elevators and escalators
- Industrial transport – asset tracking
- Factory automation and control
- Medical
- Electronic point of sale (EPOS) – Electronic Shelf Label (ESL)
- Communication equipment
  - Wired networking – wireless LAN or Wi-Fi access points, edge router , small business router
- Personal electronics
  - Home theater & entertainment – smart speakers, smart display, set-top box
  - Wearables (non-medical) – smart trackers, smart clothing

3 Description

The SimpleLink™ CC2651P3 device is a single-protocol 2.4-GHz wireless microcontroller (MCU) supporting Zigbee®, *Bluetooth*®5.2 Low Energy, IEEE 802.15.4g, TI 15.4-Stack (2.4 GHz). The CC2651P3 is based on an Arm® Cortex® M4 main processor and optimized for low-power wireless communication and advanced sensing in grid infrastructure, building automation, retail automation, personal electronics and medical applications.

The CC2651P3 has a software defined radio powered by an Arm® Cortex® M0, which allows support for multiple physical layers and RF standards. The device supports operation in the 2360 to 2500-MHz frequency band. The CC2651P3 has an efficient built-in PA that supports +10 dBm TX at 21 mA and +20 dBm TX at 101 mA (7x7 package). CC2651P3 has a receive sensitivity of -104 dBm for 125-kbps Bluetooth® Low Energy Coded PHY.

The CC2651P3 has a low sleep current of 0.8 µA with RTC and 32KB RAM retention.

Consistent with many customers' 10 to 15 years or longer life cycle requirements, TI has a product life cycle policy with a commitment to product longevity and continuity of supply.

The CC2651P3 device is part of the SimpleLink™ MCU platform, which consists of Wi-Fi®, *Bluetooth*® Low Energy, Thread, Zigbee, Wi-SUN®, Amazon Sidewalk, mioty, Sub-1 GHz MCUs, and host MCUs. CC2651P3 is part of a scalable portfolio with flash sizes from 32KB to 704KB with pin-to-pin compatible package options. The common SimpleLink™CC13xx and CC26xx Software Development Kit (SDK) and SysConfig system configuration tool supports migration between devices in the portfolio. A comprehensive number of software stacks, application examples and SimpleLink™ Academy training sessions are included in the SDK. For more information, visit wireless connectivity.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
CC2651P31T0RGZR	VQFN (48)	7.00 mm × 7.00 mm
CC2651P31T0RKPR	VQFN (40)	5.00 mm × 5.00 mm

(1) For the most current part, package, and ordering information for all available devices, see the Package Option Addendum in Section 12, or see the TI website.

[1] See *RF Core* for additional details on supported protocol standards, modulation formats, and data rates.

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4 Functional Block Diagram

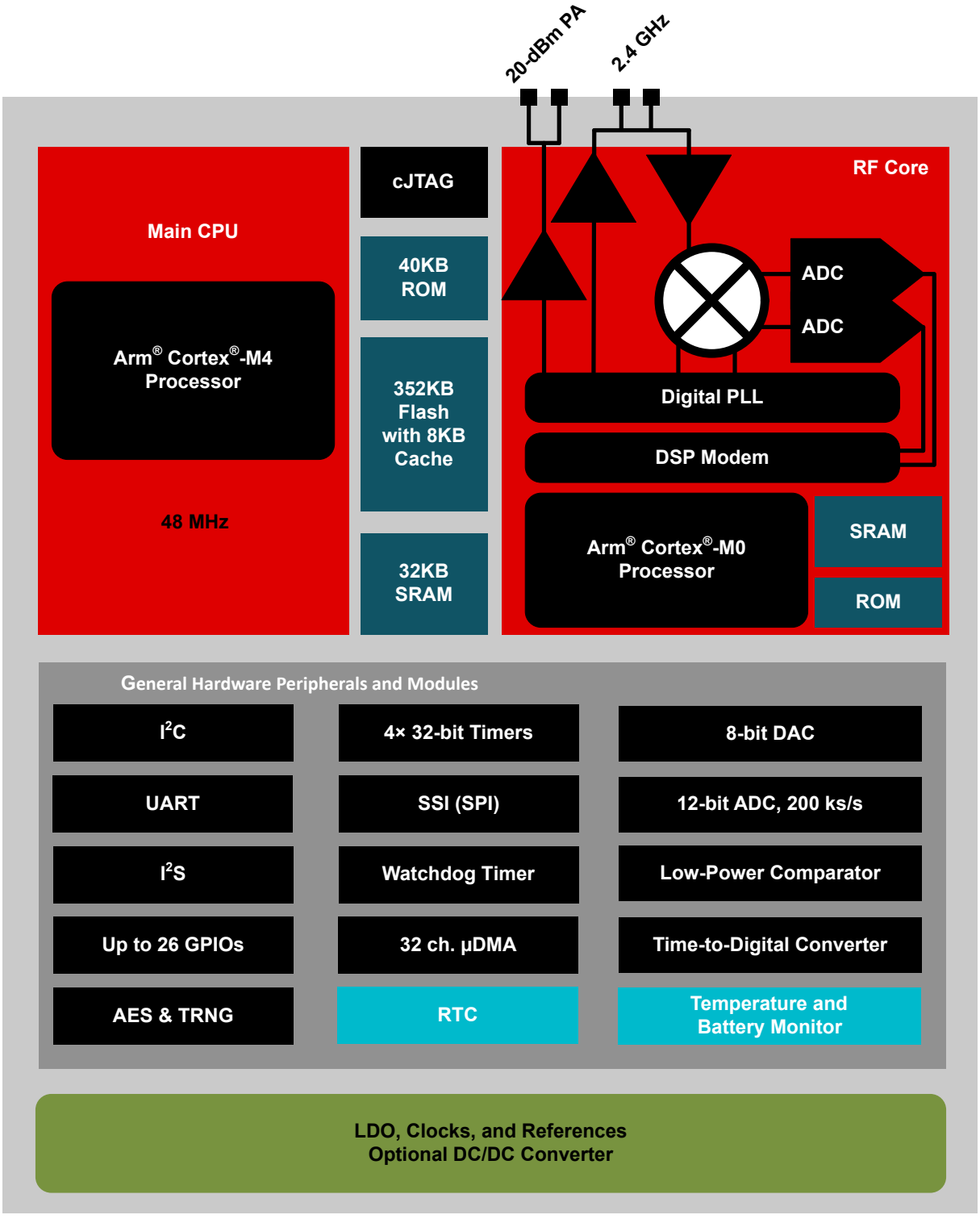

Figure 4-1. CC2651P3 Functional Block Diagram

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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2022	*	Initial Release

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6 Device Comparison

Device	RADIO SUPPORT											FLASH (KB)	RAM + Cache (KB)	GPIO	PACKAGE SIZE			
	Sub-1 GHz Prop.	2.4GHz Prop.	Wireless M-Bus	mioty	Wi-SUN®	Sidewalk	*Bluetooth*® 5.2 LE	ZigBee	Thread	Multiprotocol	+20 dBm PA				4 X 4 mm VQFN (32)	5 X 5 mm VQFN (32)	5 X 5 mm VQFN (40)	7 X 7 mm VQFN (48)
CC1310	X		X	X								32-128	16-20 + 8	10-30	X	X		X
CC1311R3	X		X	X								352	32 + 8	22-30			X	X
CC1311P3	X		X	X							X	352	32 + 8	26				X
CC1312R	X		X	X	X							352	80 + 8	30				X
CC1312R7	X		X	X	X	X				X		704	144 + 8	30				X
CC1352R	X	X	X	X	X		X	X	X	X		352	80 + 8	28				X
CC1352P	X	X	X	X	X		X	X	X	X	X	352	80 + 8	26				X
CC1352P7	X	X	X	X	X	X	X	X	X	X	X	704	144 + 8	26				X
CC2640R2F							X					128	20 + 8	10-31	X	X		X
CC2642R							X					352	80 + 8	31				X
CC2642R-Q1							X					352	80 + 8	31				X
CC2651R3		X					X	X				352	32 + 8	23-31			X	X
CC2651P3		X					X	X			X	352	32 + 8	22-26			X	X
CC2652R		X					X	X	X	X		352	80 + 8	31				X
CC2652RB		X					X	X	X	X		352	80 + 8	31				X
CC2652R7		X					X	X	X	X		704	144 + 8	31				X
CC2652P		X					X	X	X	X	X	352	80 + 8	26				X
CC2652P7		X					X	X	X	X	X	704	144 + 8	26				X

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7 Pin Configuration and Functions

7.1 Pin Diagram – RGZ Package (Top View)

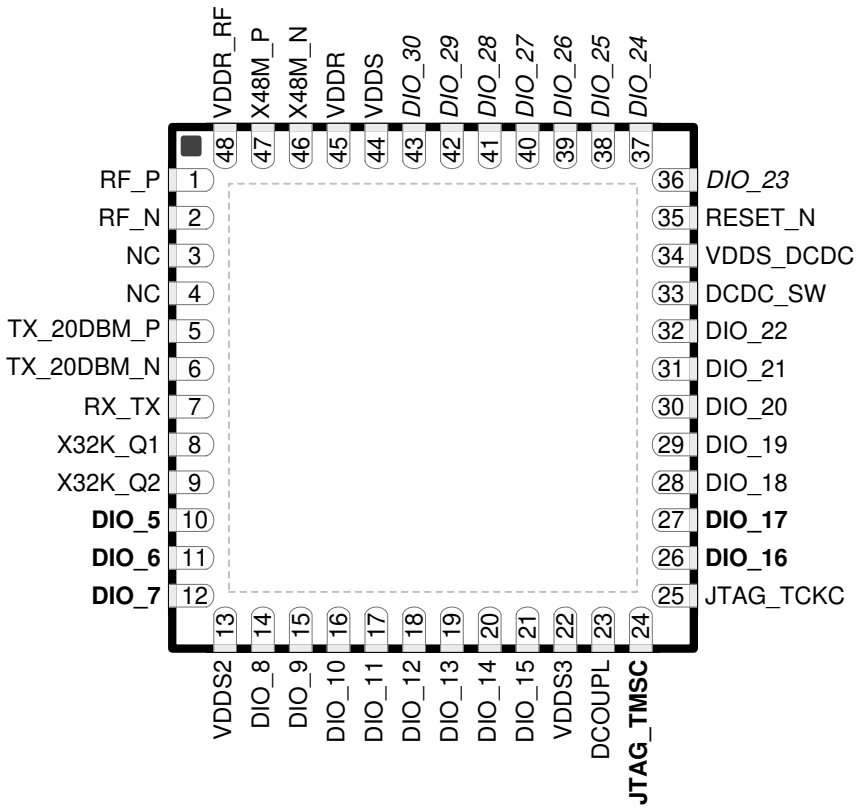

Figure 7-1. RGZ (7-mm × 7-mm) Pinout, 0.5-mm Pitch (Top View)

The following I/O pins marked in Figure 7-1 in **bold** have high-drive capabilities:

- Pin 10, DIO_5
- Pin 11, DIO_6
- Pin 12, DIO_7
- Pin 24, JTAG_TMSC
- Pin 26, DIO_16
- Pin 27, DIO_17

The following I/O pins marked in Figure 7-1 in *italics* have analog capabilities:

- Pin 36, DIO_23
- Pin 37, DIO_24
- Pin 38, DIO_25
- Pin 39, DIO_26
- Pin 40, DIO_27
- Pin 41, DIO_28
- Pin 42, DIO_29
- Pin 43, DIO_30

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7.2 Signal Descriptions – RGZ Package

Table 7-1. Signal Descriptions – RGZ Package

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
DCDC_SW	33	—	Power	Output from internal DC/DC converter(1)
DCOUPL	23	—	Power	For decoupling of internal 1.27 V regulated digital-supply (2)
DIO_5	10	I/O	Digital	GPIO, high-drive capability
DIO_6	11	I/O	Digital	GPIO, high-drive capability
DIO_7	12	I/O	Digital	GPIO, high-drive capability
DIO_8	14	I/O	Digital	GPIO
DIO_9	15	I/O	Digital	GPIO
DIO_10	16	I/O	Digital	GPIO
DIO_11	17	I/O	Digital	GPIO
DIO_12	18	I/O	Digital	GPIO
DIO_13	19	I/O	Digital	GPIO
DIO_14	20	I/O	Digital	GPIO
DIO_15	21	I/O	Digital	GPIO
DIO_16	26	I/O	Digital	GPIO, JTAG_TDO, high-drive capability
DIO_17	27	I/O	Digital	GPIO, JTAG_TDI, high-drive capability
DIO_18	28	I/O	Digital	GPIO
DIO_19	29	I/O	Digital	GPIO
DIO_20	30	I/O	Digital	GPIO
DIO_21	31	I/O	Digital	GPIO
DIO_22	32	I/O	Digital	GPIO
DIO_23	36	I/O	Digital or Analog	GPIO, analog capability
DIO_24	37	I/O	Digital or Analog	GPIO, analog capability
DIO_25	38	I/O	Digital or Analog	GPIO, analog capability
DIO_26	39	I/O	Digital or Analog	GPIO, analog capability
DIO_27	40	I/O	Digital or Analog	GPIO, analog capability
DIO_28	41	I/O	Digital or Analog	GPIO, analog capability
DIO_29	42	I/O	Digital or Analog	GPIO, analog capability
DIO_30	43	I/O	Digital or Analog	GPIO, analog capability
EGP	—	—	GND	Ground – exposed ground pad(3)
JTAG_TMSC	24	I/O	Digital	JTAG TMSC, high-drive capability
JTAG_TCKC	25	I	Digital	JTAG TCKC
RESET_N	35	I	Digital	Reset, active low. No internal pullup resistor
RF_P	1	—	RF	Positive RF input signal to LNA during RX Positive RF output signal from PA during TX
RF_N	2	—	RF	Negative RF input signal to LNA during RX Negative RF output signal from PA during TX
RX_TX	7	—	RF	Optional bias pin for the RF LNA
TX_20DBM_P	5	—	RF	Positive high-power TX signal
TX_20DBM_N	6	—	RF	Negative high-power TX signal
VDDR	45	—	Power	Internal supply, must be powered from the internal DC/DC converter or the internal LDO(2) (4) (6)
VDDR_RF	48	—	Power	Internal supply, must be powered from the internal DC/DC converter or the internal LDO(2) (5) (6)
VDDS	44	—	Power	1.8-V to 3.8-V main chip supply(1)

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Table 7-1. Signal Descriptions – RGZ Package (continued)

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
VDDS2	13	—	Power	1.8-V to 3.8-V DIO supply(1)
VDDS3	22	—	Power	1.8-V to 3.8-V DIO supply(1)
VDDS_DCDC	34	—	Power	1.8-V to 3.8-V DC/DC converter supply
X48M_N	46	—	Analog	48-MHz crystal oscillator pin 1
X48M_P	47	—	Analog	48-MHz crystal oscillator pin 2
X32K_Q1	8	—	Analog	32-kHz crystal oscillator pin 1
X32K_Q2	9	—	Analog	32-kHz crystal oscillator pin 2

(1) For more details, see the device technical reference manual listed in Section 11.3.
(2) Do not supply external circuitry from this pin.
(3) EGP is the only ground connection for the device. Good electrical connection to device ground on printed circuit board (PCB) is imperative for proper device operation.
(4) If internal DC/DC converter is not used, this pin is supplied internally from the main LDO.
(5) If internal DC/DC converter is not used, this pin must be connected to VDDR for supply from the main LDO.
(6) Output from internal DC/DC and LDO is trimmed to 1.68 V.

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7.3 Pin Diagram – RKP Package (Top View)

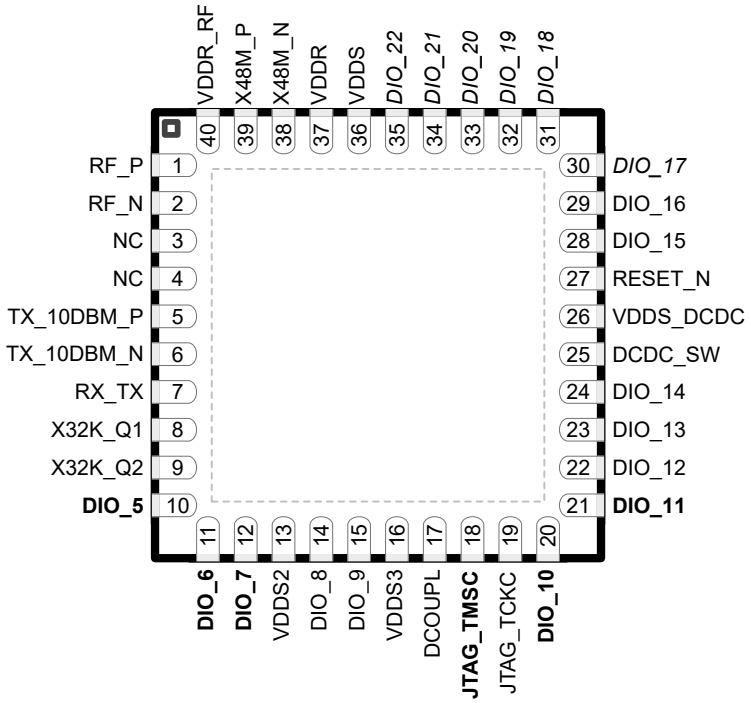

Figure 7-2. RKP (5-mm × 5-mm) Pinout, 0.4-mm Pitch (Top View)

The following I/O pins marked in Figure 7-2 in **bold** have high-drive capabilities:

- Pin 10, DIO_5
- Pin 11, DIO_6
- Pin 12, DIO_7
- Pin 18, JTAG_TMSC
- Pin 20, DIO_10
- Pin 21, DIO_11

The following I/O pins marked in Figure 7-2 in *italics* have analog capabilities:

- Pin 28, DIO_15
- Pin 29, DIO_16
- Pin 30, DIO_17
- Pin 31, DIO_18
- Pin 32, DIO_19
- Pin 33, DIO_20
- Pin 34, DIO_21
- Pin 35, DIO_22

7.4 Signal Descriptions – RKP Package

Table 7-2. Signal Descriptions – RKP Package

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
DCDC_SW	25	—	Power	Output from internal DC/DC converter(1)
DCOUPL	17	—	Power	For decoupling of internal 1.27 V regulated digital-supply (2)
DIO_5	10	I/O	Digital	GPIO, high-drive capability
DIO_6	11	I/O	Digital	GPIO, high-drive capability
DIO_7	12	I/O	Digital	GPIO, high-drive capability

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Table 7-2. Signal Descriptions – RKP Package (continued)

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
DIO_8	14	I/O	Digital	GPIO
DIO_9	15	I/O	Digital	GPIO
DIO_10	20	I/O	Digital	GPIO, JTAG_TDO, high-drive capability
DIO_11	21	I/O	Digital	GPIO, JTAG_TDI, high-drive capability
DIO_12	22	I/O	Digital	GPIO
DIO_13	23	I/O	Digital	GPIO
DIO_14	24	I/O	Digital	GPIO
DIO_15	28	I/O	Digital	GPIO, analog capability
DIO_16	29	I/O	Digital	GPIO, analog capability
DIO_17	30	I/O	Digital	GPIO, analog capability
DIO_18	31	I/O	Digital	GPIO, analog capability
DIO_19	32	I/O	Digital	GPIO, analog capability
DIO_20	33	I/O	Digital	GPIO, analog capability
DIO_21	34	I/O	Digital	GPIO, analog capability
DIO_22	35	I/O	Digital	GPIO, analog capability
EGP	—	—	GND	Ground – exposed ground pad(3)
JTAG_TSMC	18	I/O	Digital	JTAG TMSC, high-drive capability
JTAG_TCKC	19	I	Digital	JTAG TCKC
RESET_N	27	I	Digital	Reset, active low. No internal pullup resistor
RF_P	1	—	RF	Positive RF input signal to LNA during RX Positive RF output signal from PA during TX
RF_N	2	—	RF	Negative RF input signal to LNA during RX Negative RF output signal from PA during TX
RX_TX	7	—	RF	Optional bias pin for the RF LNA
TX_20DBM_P	5	—	RF	Positive high-power TX signal
TX_20DBM_N	6	—	RF	Negative high-power TX signal
VDDR	37	—	Power	Internal supply, must be powered from the internal DC/DC converter or the internal LDO(2) (4) (6)
VDDR_RF	40	—	Power	Internal supply, must be powered from the internal DC/DC converter or the internal LDO(2) (5) (6)
VDDS	36	—	Power	1.8-V to 3.8-V main chip supply(1)
VDDS2	13	—	Power	1.8-V to 3.8-V DIO supply(1)
VDDS3	16	—	Power	1.8-V to 3.8-V DIO supply(1)
VDDS_DCDC	26	—	Power	1.8-V to 3.8-V DC/DC converter supply
X48M_N	38	—	Analog	48-MHz crystal oscillator pin 1
X48M_P	39	—	Analog	48-MHz crystal oscillator pin 2
X32K_Q1	8	—	Analog	32-kHz crystal oscillator pin 1
X32K_Q2	9	—	Analog	32-kHz crystal oscillator pin 2

(1) For more details, see the device technical reference manual listed in Section 11.3.
(2) Do not supply external circuitry from this pin.
(3) EGP is the only ground connection for the device. Good electrical connection to device ground on printed circuit board (PCB) is imperative for proper device operation.
(4) If internal DC/DC converter is not used, this pin is supplied internally from the main LDO.
(5) If internal DC/DC converter is not used, this pin must be connected to VDDR for supply from the main LDO.
(6) Output from internal DC/DC and LDO is trimmed to 1.68 V.

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7.5 Connections for Unused Pins and Modules

Table 7-3. Connections for Unused Pins – RGZ Package

FUNCTION	SIGNAL NAME	PIN NUMBER	ACCEPTABLE PRACTICE(1)	PREFERRED PRACTICE(1)
GPIO	DIO_n	10–12 14–21 26–32 36–43	NC or GND	NC
32.768-kHz crystal	X32K_Q1	8	NC or GND	NC
	X32K_Q2	9		
No Connects	NC	3–4	NC	NC
DC/DC converter(2)	DCDC_SW	33	NC	NC
	VDDS_DCDC	34	VDDS	VDDS

(1) NC = No connect
(2) When the DC/DC converter is not used, the inductor between DCDC_SW and VDDR can be removed. VDDR and VDDR_RF must still be connected and the 22 uF DCDC capacitor must be kept on the VDDR net.

Table 7-4. Connection for Unused Pins and Modules – RKP Package

FUNCTION	SIGNAL NAME	PIN NUMBER	ACCEPTABLE PRACTICE	PREFERRED PRACTICE
GPIO	DIO_n	10-12 14-15 20-24 28-35	NC or GND	NC
32.768-kHz crystal	X32K_Q1	3	NC or GND	NC
	X32K_Q2	4		
No Connects	NC	3–4	NC	NC
DC/DC converter	DCDC_SW	25	NC	NC
	VDDS_DCDC	26	VDDS	VDDS

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8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
VDDS(3) (6)	Supply voltage		–0.3	4.1	V
	Voltage on any digital pin(4) (5)		–0.3	VDDS + 0.3, max 4.1	V
	Voltage on crystal oscillator pins, X32K_Q1, X32K_Q2, X48M_N and X48M_P		–0.3	VDDR + 0.3, max 2.25	V
V_{in}	Voltage on ADC input	Voltage scaling enabled	–0.3	VDDS	V
		Voltage scaling disabled, internal reference	–0.3	1.49	
		Voltage scaling disabled, VDDS as reference	–0.3	VDDS / 2.9	
	Input level, RF pins (RF_P and RF_N)			5	dBm
T_{stg}	Storage temperature		–40	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime
(2) All voltage values are with respect to ground, unless otherwise noted.
(3) VDDS_DCDC, VDDS2 and VDDS3 must be at the same potential as VDDS.
(4) Including analog capable DIOs.
(5) Injection current is not supported on any GPIO pin
(6) Connect VDDR to the external PA bias voltage for +10dBm and VDDS to the external PA bias voltage for +14dBm to +20dBm

8.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS001(1)	All pins	±2000	V
		Charged device model (CDM), per JESD22-C101(2)	All pins	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Operating ambient temperature(1) (2)	–40	105	°C
Operating junction temperature(1) (2)	–40	115	°C
Operating supply voltage (VDDS)	1.8	3.8	V
Rising supply voltage slew rate	0	100	mV/µs
Falling supply voltage slew rate(3)	0	20	mV/µs

(1) Operation at or near maximum operating temperature for extended durations will result in lifetime reduction.
(2) For thermal resistance characteristics refer to Section 8.8.
(3) For small coin-cell batteries, with high worst-case end-of-life equivalent source resistance, a 22-µF VDDS input capacitor must be used to ensure compliance with this slew rate.

8.4 Power Supply and Modules

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
VDDS Power-on-Reset (POR) threshold			1.1 - 1.55		V
VDDS Brown-out Detector (BOD)	Rising threshold		1.77		V
VDDS Brown-out Detector (BOD), before initial boot (1)	Rising threshold		1.70		V
VDDS Brown-out Detector (BOD)	Falling threshold		1.75		V

(1) Brown-out Detector is trimmed at initial boot, value is kept until device is reset by a POR reset or the RESET_N pin

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8.5 Power Consumption - Power Modes

When measured on the CC26x1-P3EM-XD24-PA24 reference design with T_c = 25 °C, V_{DDS} = 3.0 V with DC/DC enabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Core Current Consumption						
I_{core}	Reset and Shutdown	Reset. RESET_N pin asserted or VDDS below power-on-reset threshold		150		nA
		Shutdown. No clocks running, no retention		100		
	Standby without cache retention	RTC running, CPU, 32KB RAM and (partial) register retention. RCOSC_LF		0.8		µA
		RTC running, CPU, 32KB RAM and (partial) register retention XOSC_LF		0.9		µA
	Standby with cache retention	RTC running, CPU, 32KB RAM and (partial) register retention. RCOSC_LF		2.4		µA
		RTC running, CPU, 32KB RAM and (partial) register retention. XOSC_LF		2.6		µA
	Idle	Supply Systems and RAM powered RCOSC_HF		650		µA
	Active	MCU running CoreMark at 48 MHz RCOSC_HF		2.91		mA
Peripheral Current Consumption						
I_{peri}	Peripheral power domain	Delta current with domain enabled		56.0		µA
	Serial power domain	Delta current with domain enabled		5.0		
	RF Core	Delta current with power domain enabled, clock enabled, RF core idle		144		
	µDMA	Delta current with clock enabled, module is idle		68.6		
	Timers	Delta current with clock enabled, module is idle(1)		102		
	I2C	Delta current with clock enabled, module is idle		12.1		
	I2S	Delta current with clock enabled, module is idle		30.8		
	SSI	Delta current with clock enabled, module is idle		71.7		
	UART	Delta current with clock enabled, module is idle		147		
	CRYPTO (AES)	Delta current with clock enabled, module is idle		28.1		
	TRNG	Delta current with clock enabled, module is idle		27.1		

(1) Only one GPTimer running

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8.6 Power Consumption - Radio Modes

When measured on the CC26x1-P3EM-XD24-PA24 reference design with T_c = 25 °C, V_{DDS} = 3.0 V with DC/DC enabled unless otherwise noted.
High-power PA connected to V_{DDS} unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Radio receive current	2440 MHz		6.4		mA
Radio transmit current 2.4 GHz PA (Bluetooth Low Energy)	0 dBm output power setting 2440 MHz		7.1		mA
	+5 dBm output power setting 2440 MHz		9.5		mA
Radio transmit current High-power PA	+20 dBm output power setting(1) 2440 MHz. VDDS = 3.3 V		101		mA
Radio transmit current High-power PA, 10 dBm configuration(2)	+10 dBm output power setting 2440 MHz VDDR = 1.67 V		22		mA

(1) +20 dBm is only available on the RGZ (7x7) package
(2) Measured on evaluation board as described in https://www.ti.com/lit/pdf/swra636.

8.7 Nonvolatile (Flash) Memory Characteristics

Over operating free-air temperature range and V_{DDS} = 3.0 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Flash sector size			8		KB
Supported flash erase cycles before failure, full bank(1) (5)		30			k Cycles
Supported flash erase cycles before failure, single sector(2)		60			k Cycles
Maximum number of write operations per row before sector erase(3)				83	Write Operations
Flash retention	105 °C	11.4			Years
Flash sector erase current	Average delta current		9.7		mA
Flash sector erase time(4)	Zero cycles		10		ms
	30k cycles			4000	ms
Flash write current	Average delta current, 4 bytes at a time		5.3		mA
Flash write time(4)	4 bytes at a time		21.6		µs

(1) A full bank erase is counted as a single erase cycle on each sector.
(2) Up to 4 customer-designated sectors can be individually erased an additional 30k times beyond the baseline bank limitation of 30k cycles
(3) Each wordline is 2048 bits (or 256 bytes) wide. This limitation corresponds to sequential memory writes of 4 (3.1) bytes minimum per write over a whole wordline. If additional writes to the same wordline are required, a sector erase is required once the maximum number of write operations per row is reached.
(4) This number is dependent on Flash aging and increases over time and erase cycles
(5) Aborting flash during erase or program modes is not a safe operation.

8.8 Thermal Resistance Characteristics

THERMAL METRIC(1)		PACKAGE		UNIT
		RGZ (VQFN)	RKP (VQFN)	
		48 PINS	40 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.0	30.9	°C/W(2)
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	14.5	20.2	°C/W(2)
$R_{\theta JB}$	Junction-to-board thermal resistance	8.7	10.3	°C/W(2)
ψ_{JT}	Junction-to-top characterization parameter	0.2	0.2	°C/W(2)
ψ_{JB}	Junction-to-board characterization parameter	8.6	10.3	°C/W(2)
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.1	2.1	°C/W(2)

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) °C/W = degrees Celsius per watt.

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8.9 RF Frequency Bands

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	MIN	TYP	MAX	UNIT
Frequency bands	2360		2500	MHz

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8.10 Bluetooth Low Energy - Receive (RX)

Measured on the CC26x1-P3EM-7XD24-PA24 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF}= 2440 MHz with DC/DC enabled and high power PA connected to V_{DDS} unless otherwise noted.
All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
125 kbps (LE Coded)					
Receiver sensitivity	Differential mode. BER = 10^{-3}		–104		dBm
Receiver sensitivity	Single ended mode. Measured on CC26x1-P3EM-5XS24, at the SMA connector, BER = 10^{-3}		–104		dBm
Receiver saturation	Differential mode. BER = 10^{-3}		>5		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> (–300 / 300)		kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)		> (–320 / 240)		ppm
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (255-byte packets)		> (–125 / 125)		ppm
Co-channel rejection(1)	Wanted signal at –79 dBm, modulated interferer in channel, BER = 10^{-3}		–1.5		dB
Selectivity, ±1 MHz(1)	Wanted signal at –79 dBm, modulated interferer at ±1 MHz, BER = 10^{-3}		8 / 4.5(2)		dB
Selectivity, ±2 MHz(1)	Wanted signal at –79 dBm, modulated interferer at ±2 MHz, BER = 10^{-3}		44 / 39(2)		dB
Selectivity, ±3 MHz(1)	Wanted signal at –79 dBm, modulated interferer at ±3 MHz, BER = 10^{-3}		46 / 44(2)		dB
Selectivity, ±4 MHz(1)	Wanted signal at –79 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}		44 / 46(2)		dB
Selectivity, ±6 MHz(1)	Wanted signal at –79 dBm, modulated interferer at ≥ ±6 MHz, BER = 10^{-3}		48 / 44(2)		dB
Selectivity, ±7 MHz	Wanted signal at –79 dBm, modulated interferer at ≥ ±7 MHz, BER = 10^{-3}		51 / 45(2)		dB
Selectivity, Image frequency(1)	Wanted signal at –79 dBm, modulated interferer at image frequency, BER = 10^{-3}		39		dB
Selectivity, Image frequency ±1 MHz(1)	Note that Image frequency + 1 MHz is the Co- channel –1 MHz. Wanted signal at –79 dBm, modulated interferer at ±1 MHz from image frequency, BER = 10^{-3}		4.5 / 44 (2)		dB
500 kbps (LE Coded)					
Receiver sensitivity	Differential mode. BER = 10^{-3}		–100		dBm
Receiver sensitivity	Single ended mode. Measured on CC26x1-P3EM-5XS24, at the SMA connector, BER = 10^{-3}		–100		dBm
Receiver saturation	Differential mode. BER = 10^{-3}		> 5		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> (–300 / 300)		kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)		> (–450 / 450)		ppm
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (255-byte packets)		> (–175 / 175)		ppm
Co-channel rejection(1)	Wanted signal at –72 dBm, modulated interferer in channel, BER = 10^{-3}		–3.5		dB
Selectivity, ±1 MHz(1)	Wanted signal at –72 dBm, modulated interferer at ±1 MHz, BER = 10^{-3}		8 / 4(2)		dB
Selectivity, ±2 MHz(1)	Wanted signal at –72 dBm, modulated interferer at ±2 MHz, BER = 10^{-3}		44 / 37(2)		dB
Selectivity, ±3 MHz(1)	Wanted signal at –72 dBm, modulated interferer at ±3 MHz, BER = 10^{-3}		46 / 46(2)		dB
Selectivity, ±4 MHz(1)	Wanted signal at –72 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}		45 / 47(2)		dB
Selectivity, ±6 MHz(1)	Wanted signal at –72 dBm, modulated interferer at ≥ ±6 MHz, BER = 10^{-3}		46 / 45(2)		dB

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8.10 Bluetooth Low Energy - Receive (RX) (continued)

Measured on the CC26x1-P3EM-7XD24-PA24 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF}= 2440 MHz with DC/DC enabled and high power PA connected to V_{DDS} unless otherwise noted.
All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Selectivity, ±7 MHz	Wanted signal at –72 dBm, modulated interferer at ≥ ±7 MHz, BER = 10^{-3}		49 / 45[2]		dB
Selectivity, Image frequency[1]	Wanted signal at –72 dBm, modulated interferer at image frequency, BER = 10^{-3}		37		dB
Selectivity, Image frequency ±1 MHz[1]	Note that Image frequency + 1 MHz is the Co- channel –1 MHz. Wanted signal at –72 dBm, modulated interferer at ±1 MHz from image frequency, BER = 10^{-3}		4 / 46[2]		dB
1 Mbps (LE 1M)					
Receiver sensitivity	Differential mode. BER = 10^{-3}		–97		dBm
Receiver sensitivity	Single ended mode. Measured on CC26x1-P3EM-5XS24, at the SMA connector, BER = 10^{-3}		–97		dBm
Receiver saturation	Differential mode. BER = 10^{-3}		> 5		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> (–350 / 350)		kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)		> (–750 / 750)		ppm
Co-channel rejection[1]	Wanted signal at –67 dBm, modulated interferer in channel, BER = 10^{-3}		–6		dB
Selectivity, ±1 MHz[1]	Wanted signal at –67 dBm, modulated interferer at ±1 MHz, BER = 10^{-3}		7 / 4[2]		dB
Selectivity, ±2 MHz[1]	Wanted signal at –67 dBm, modulated interferer at ±2 MHz,BER = 10^{-3}		40 / 33[2]		dB
Selectivity, ±3 MHz[1]	Wanted signal at –67 dBm, modulated interferer at ±3 MHz, BER = 10^{-3}		36 / 41[2]		dB
Selectivity, ±4 MHz[1]	Wanted signal at –67 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}		37 / 45[2]		dB
Selectivity, ±5 MHz or more[1]	Wanted signal at –67 dBm, modulated interferer at ≥ ±5 MHz, BER = 10^{-3}		40		dB
Selectivity, image frequency[1]	Wanted signal at –67 dBm, modulated interferer at image frequency, BER = 10^{-3}		33		dB
Selectivity, image frequency ±1 MHz[1]	Note that Image frequency + 1 MHz is the Co- channel –1 MHz. Wanted signal at –67 dBm, modulated interferer at ±1 MHz from image frequency, BER = 10^{-3}		4 / 41[2]		dB
Out-of-band blocking[3]	30 MHz to 2000 MHz		–10		dBm
Out-of-band blocking	2003 MHz to 2399 MHz		–18		dBm
Out-of-band blocking	2484 MHz to 2997 MHz		–12		dBm
Out-of-band blocking	3000 MHz to 12.75 GHz		–2		dBm
Intermodulation	Wanted signal at 2402 MHz, –64 dBm. Two interferers at 2405 and 2408 MHz respectively, at the given power level		–42		dBm
Spurious emissions, 30 to 1000 MHz	Measurement in a 50-Ω single-ended load.		< –59		dBm
Spurious emissions, 1 to 12.75 GHz	Measurement in a 50-Ω single-ended load.		< –47		dBm
RSSI dynamic range			70		dB
RSSI accuracy			±4		dB
2 Mbps (LE 2M)					
Receiver sensitivity	Differential mode. Measured at SMA connector, BER = 10^{-3}		–92		dBm
Receiver sensitivity	Single ended mode. Measured on CC26x1-P3EM-5XS24, at the SMA connector, BER = 10^{-3}		–92		dBm
Receiver saturation	Differential mode. Measured at SMA connector, BER = 10^{-3}		> 5		dBm

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8.10 Bluetooth Low Energy - Receive (RX) (continued)

Measured on the CC26x1-P3EM-7XD24-PA24 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF}= 2440 MHz with DC/DC enabled and high power PA connected to V_{DDS} unless otherwise noted.
All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> (–500 / 500)		kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)		> (–700 / 750)		ppm
Co-channel rejection(1)	Wanted signal at –67 dBm, modulated interferer in channel,BER = 10^{-3}		–7		dB
Selectivity, ±2 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±2 MHz, Image frequency is at –2 MHz, BER = 10^{-3}		8 / 4(2)		dB
Selectivity, ±4 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}		36 / 31(2)		dB
Selectivity, ±6 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±6 MHz, BER = 10^{-3}		37 / 36(2)		dB
Selectivity, image frequency(1)	Wanted signal at –67 dBm, modulated interferer at image frequency, BER = 10^{-3}		4		dB
Selectivity, image frequency ±2 MHz(1)	Note that Image frequency + 2 MHz is the Co-channel. Wanted signal at –67 dBm, modulated interferer at ±2 MHz from image frequency, BER = 10^{-3}		–7 / 36(2)		dB
Out-of-band blocking(3)	30 MHz to 2000 MHz		–16		dBm
Out-of-band blocking	2003 MHz to 2399 MHz		–21		dBm
Out-of-band blocking	2484 MHz to 2997 MHz		–15		dBm
Out-of-band blocking	3000 MHz to 12.75 GHz		–12		dBm
Intermodulation	Wanted signal at 2402 MHz, –64 dBm. Two interferers at 2408 and 2414 MHz respectively, at the given power level		–38		dBm

(1) Numbers given as I/C dB
(2) X / Y, where X is +N MHz and Y is –N MHz
(3) Excluding one exception at F_{wanted} / 2, per Bluetooth Specification

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8.11 Bluetooth Low Energy - Transmit (TX)

Measured on the CC26x1-P3EM-7XD24-PA24 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF}= 2440 MHz with DC/DC enabled and high power PA connected to V_{DDS} unless otherwise noted.
All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
General Parameters						
Max output power, high power PA	Differential mode, delivered to a single-ended 50 Ω load through a balun			20		dBm
Output power programmable range high power PA	Differential mode, delivered to a single-ended 50 Ω load through a balun			6		dB
Max output power, high power PA, 10 dBm configuration(3)	Differential mode, delivered to a single-ended 50 Ω load through a balun			10.5		dBm
Max output power, high power PA, 10 dBm configuration(3)	Single-ended mode. Measured on CC26x1-P3EM-5XS24, delivered to a single-ended 50 Ω load through a balun			9		dBm
Output power programmable range high power PA, 10 dBm configuration(3)	Differential mode, delivered to a single-ended 50 Ω load through a balun			5		dB
Max output power, regular PA	Differential mode, delivered to a single-ended 50 Ω load through a balun			5		dBm
Max output power, regular PA	Single-ended mode. Measured on CC26x1-P3EM-5XS24, delivered to a single-ended 50 Ω load through a balun			3		dBm
Output power programmable range, regular PA	Differential mode, delivered to a single-ended 50 Ω load through a balun			26		dB
Spurious emissions and harmonics						
Spurious emissions, high-power PA(1)	f < 1 GHz, outside restricted bands	+20 dBm setting		< -36		dBm
	f < 1 GHz, restricted bands FCC			< -55		dBm
	f > 1 GHz, including harmonics			-37		dBm
Harmonics, high-power PA(2)	Second harmonic			-35		dBm
	Third harmonic			-42		dBm
Spurious emissions, high-power PA, 10 dBm configuration(1) (3)	f < 1 GHz, outside restricted bands	+10 dBm setting(3)		< -36		dBm
	f < 1 GHz, restricted bands ETSI			< -54		dBm
	f < 1 GHz, restricted bands FCC			< -55		dBm
	f > 1 GHz, including harmonics			-41		dBm
Harmonics, high-power PA, 10 dBm configuration(3)	Second harmonic			< -42		dBm
	Third harmonic			< -42		dBm
Spurious emissions, regular PA	f < 1 GHz, outside restricted bands	+5 dBm setting		< –36		dBm
	f < 1 GHz, restricted bands ETSI			< –54		dBm
	f < 1 GHz, restricted bands FCC			< –55		dBm
	f > 1 GHz, including harmonics			< –42		dBm
Harmonics, regular PA	Second harmonic			< –42		dBm
	Third harmonic			< –42		dBm

(1) To ensure margins for passing FCC band edge requirements at 2483.5 MHz, a lower than maximum output-power setting or less than 100% duty cycle may be used when operating at the upper Bluetooth Low Energy channel(s).
(2) To ensure margins for passing FCC requirements for harmonic emission, duty cycling may be required. The CC2651P3 LaunchPad reference design should also be reviewed as the filter provides higher attenuation of harmonics compared to the CC26x1-P3EM-XD24-PA24 reference design.
(3) Measured on evaluation board as described in www.ti.com/lit/pdf/swra636.

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8.12 Zigbee - IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps) - RX

Measured on the CC26x1-P3EM-7XD24-PA24 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF}= 2440 MHz with DC/DC enabled and high power PA connected to V_{DDS} unless otherwise noted.
All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General Parameters					
Receiver sensitivity	Differential mode PER = 1%		–100		dBm
Receiver sensitivity	Single-Ended mode. Measured on CC26x1-P3EM-5XS24 at the SMA connector. PER = 1%		-99		dBm
Receiver saturation	PER = 1%		> 5		dBm
Adjacent channel rejection	Wanted signal at –82 dBm, modulated interferer at ±5 MHz, PER = 1%		36		dB
Alternate channel rejection	Wanted signal at –82 dBm, modulated interferer at ±10 MHz, PER = 1%		57		dB
Channel rejection, ±15 MHz or more	Wanted signal at –82 dBm, undesired signal is IEEE 802.15.4 modulated channel, stepped through all channels 2405 to 2480 MHz, PER = 1%		59		dB
Blocking and desensitization, 5 MHz from upper band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		57		dB
Blocking and desensitization, 10 MHz from upper band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		63		dB
Blocking and desensitization, 20 MHz from upper band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		63		dB
Blocking and desensitization, 50 MHz from upper band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		66		dB
Blocking and desensitization, –5 MHz from lower band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		60		dB
Blocking and desensitization, –10 MHz from lower band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		60		dB
Blocking and desensitization, –20 MHz from lower band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		63		dB
Blocking and desensitization, –50 MHz from lower band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		65		dB
Spurious emissions, 30 MHz to 1000 MHz	Measurement in a 50-Ω single-ended load(1)		–66		dBm
Spurious emissions, 1 GHz to 12.75 GHz	Measurement in a 50-Ω single-ended load(1)		–53		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> 350		ppm
Symbol rate error tolerance	Difference between incoming symbol rate and the internally generated symbol rate		> 1000		ppm
RSSI dynamic range			95		dB
RSSI accuracy			±4		dB

(1) Suitable for systems targeting compliance with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66

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8.13 Zigbee - IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps) - TX

Measured on the CC26x1-P3EM-7XD24-PA24 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF}= 2440 MHz with DC/DC enabled and high power PA connected to V_{DDS} unless otherwise noted.
All measurements are performed at the antenna input with a combined RX and TX path, except for high power PA which is measured at a dedicated antenna connection. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
General Parameters						
Max output power, high power PA	Differential mode, delivered to a single-ended 50-Ω load through a balun			20		dBm
Output power programmable range, high power PA	Differential mode, delivered to a single-ended 50-Ω load through a balun			6		dB
Max output power, high power PA, 10 dBm configuration(4)	Differential mode, delivered to a single-ended 50-Ω load through a balun			10.5		dBm
Max output power, high power PA, 10 dBm configuration(4)	Single-ended mode. Measured on CC26x1-P3EM-5XS24, delivered to a single-ended 50-Ω load through a balun			9		dBm
Output power programmable range, high power PA, 10 dBm configuration(4)	Differential mode, delivered to a single-ended 50-Ω load through a balun			5		dB
Max output power, regular PA	Differential mode, delivered to a single-ended 50-Ω load through a balun			5		dBm
Output power programmable range, regular PA	Differential mode, delivered to a single-ended 50-Ω load through a balun			26		dB
Spurious emissions and harmonics						
Spurious emissions, high-power PA(2)	f < 1 GHz, outside restricted bands	+20 dBm setting			< -39	dBm
	f < 1 GHz, restricted bands FCC				< -49	dBm
	f > 1 GHz, including harmonics				-40	dBm
Harmonics, high-power PA(3)	Second harmonic				-35	dBm
	Third harmonic				-42	dBm
Spurious emissions, high-power PA, 10 dBm configuration(2) (4)	f < 1 GHz, outside restricted bands	+10 dBm setting(4)			< -36	dBm
	f < 1 GHz, restricted bands ETSI				< -47	dBm
	f < 1 GHz, restricted bands FCC				< -55	dBm
	f > 1 GHz, including harmonics				-42	dBm
Harmonics, high-power PA, 10 dBm configuration(4)	Second harmonic				< -42	dBm
	Third harmonic				< -42	dBm
Spurious emissions, regular PA (1)	f < 1 GHz, outside restricted bands	+5 dBm setting			< -36	dBm
	f < 1 GHz, restricted bands ETSI				< -47	dBm
	f < 1 GHz, restricted bands FCC				< -55	dBm
	f > 1 GHz, including harmonics				< –42	dBm
Harmonics, regular PA	Second harmonic				< -42	dBm
	Third harmonic				< -42	dBm
IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps)						
Error vector magnitude, high power PA	+20 dBm setting			2		%
Error vector magnitude, high power PA, 10 dBm configuration(4)	+10 dBm setting			2		%
Error vector magnitude Regular PA	+5 dBm setting			2		%

(1) To ensure margins for passing FCC band edge requirements at 2483.5 MHz, a lower than maximum output-power setting or less than 100% duty cycle may be used when operating at 2480 MHz.

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(2) To ensure margins for passing FCC band edge requirements at 2483.5 MHz, a lower than maximum output-power setting or less than 100% duty cycle may be used when operating at the upper 802.15.4 channel(s).
(3) To ensure margins for passing FCC requirements for harmonic emission, duty cycling may be required. The CC2651P3 LaunchPad reference design should also be reviewed as the filter provides higher attenuation of harmonics compared to the CC26x1-P3EM-7XD24-PA24 reference design.
(4) Measured on evaluation board as described in https://www.ti.com/lit/pdf/swra636.

8.14 Timing and Switching Characteristics

8.14.1 Reset Timing

PARAMETER	MIN	TYP	MAX	UNIT
RESET_N low duration	1			µs

8.14.2 Wakeup Timing

Measured over operating free-air temperature with V_{DDS} = 3.0 V (unless otherwise noted). The times listed here do not include software overhead.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
MCU, Reset to Active(1)			850 - 4000		µs
MCU, Shutdown to Active(1)			850 - 4000		µs
MCU, Standby to Active			160		µs
MCU, Active to Standby			36		µs
MCU, Idle to Active			14		µs

(1) The wakeup time is dependent on remaining charge on VDDR capacitor when starting the device, and thus how long the device has been in Reset or Shutdown before starting up again. The wake up time increases with a higher capacitor value.

8.14.3 Clock Specifications

8.14.3.1 48 MHz Crystal Oscillator (XOSC_HF)

Measured on a Texas Instruments reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.(1)

	PARAMETER	MIN	TYP	MAX	UNIT
	Crystal frequency		48		MHz
ESR	Equivalent series resistance 6 pF < C_L ≤ 9 pF		20	60	Ω
ESR	Equivalent series resistance 5 pF < C_L ≤ 6 pF			80	Ω
L_M	Motional inductance, relates to the load capacitance that is used for the crystal (C_L in Farads)(5)		< 3 × 10^{-25} / C_L ^{2}		H
C_L	Crystal load capacitance(4)	5	7(3)	9	pF
	Start-up time(2)		200		µs

(1) Probing or otherwise stopping the crystal while the DC/DC converter is enabled may cause permanent damage to the device.
(2) Start-up time using the TI-provided power driver. Start-up time may increase if driver is not used.
(3) On-chip default connected capacitance including reference design parasitic capacitance. Connected internal capacitance is changed through software in the Customer Configuration section (CCFG).
(4) Adjustable load capacitance is integrated into the device. External load capacitors are required for systems targeting compliance with certain regulations. See the device errata for further details.
(5) The crystal manufacturer's specification must satisfy this requirement for proper operation.

8.14.3.2 48 MHz RC Oscillator (RCOSC_HF)

Measured on a Texas Instruments reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

	MIN	TYP	MAX	UNIT
Frequency		48		MHz
Uncalibrated frequency accuracy		±1		%
Calibrated frequency accuracy(1)		±0.25		%
Start-up time		5		µs

(1) Accuracy relative to the calibration source (XOSC_HF)

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8.14.3.3 32.768 kHz Crystal Oscillator (XOSC_LF)

Measured on a Texas Instruments reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

		MIN	TYP	MAX	UNIT
	Crystal frequency		32.768		kHz
ESR	Equivalent series resistance		30	100	kΩ
C_L	Crystal load capacitance	6	7(1)	12	pF

(1) Default load capacitance using TI reference designs including parasitic capacitance. Crystals with different load capacitance may be used.

8.14.3.4 32 kHz RC Oscillator (RCOSC_LF)

Measured on a Texas Instruments reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

		MIN	TYP	MAX	UNIT
Calibrated frequency			32.8		kHz
Calibrated RTC variation(1)	Calibrated periodically against XOSC_HF(2)		±600(3)		ppm
Temperature coefficient.			50		ppm/°C

(1) When using RCOSC_LF as source for the low frequency system clock (SCLK_LF), the accuracy of the SCLK_LF-derived Real Time Clock (RTC) can be improved by measuring RCOSC_LF relative to XOSC_HF and compensating for the RTC tick speed. This functionality is available through the TI-provided Power driver.
(2) TI driver software calibrates the RTC every time XOSC_HF is enabled.
(3) Some device's variation can exceed 1000 ppm. Further calibration will not improve variation.

8.14.4 Synchronous Serial Interface (SSI) Characteristics

8.14.4.1 Synchronous Serial Interface (SSI) Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER NO.	PARAMETER		MIN	TYP	MAX	UNIT
S1	t_{clk_per}	SSIClk cycle time	12		65024	System Clocks (2)
S2(1)	t_{clk_high}	SSIClk high time		0.5		t_{clk_per}
S3(1)	t_{clk_low}	SSIClk low time		0.5		t_{clk_per}

(1) Refer to SSI timing diagrams Figure 8-1, Figure 8-2, and Figure 8-3.
(2) When using the TI-provided Power driver, the SSI system clock is always 48 MHz.

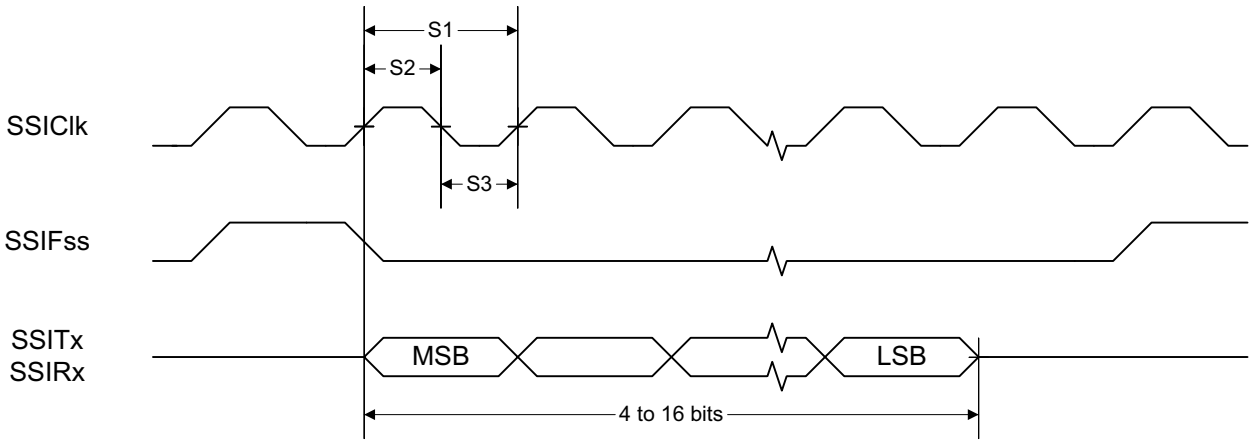

Figure 8-1. SSI Timing for TI Frame Format (FRF = 01), Single Transfer Timing Measurement

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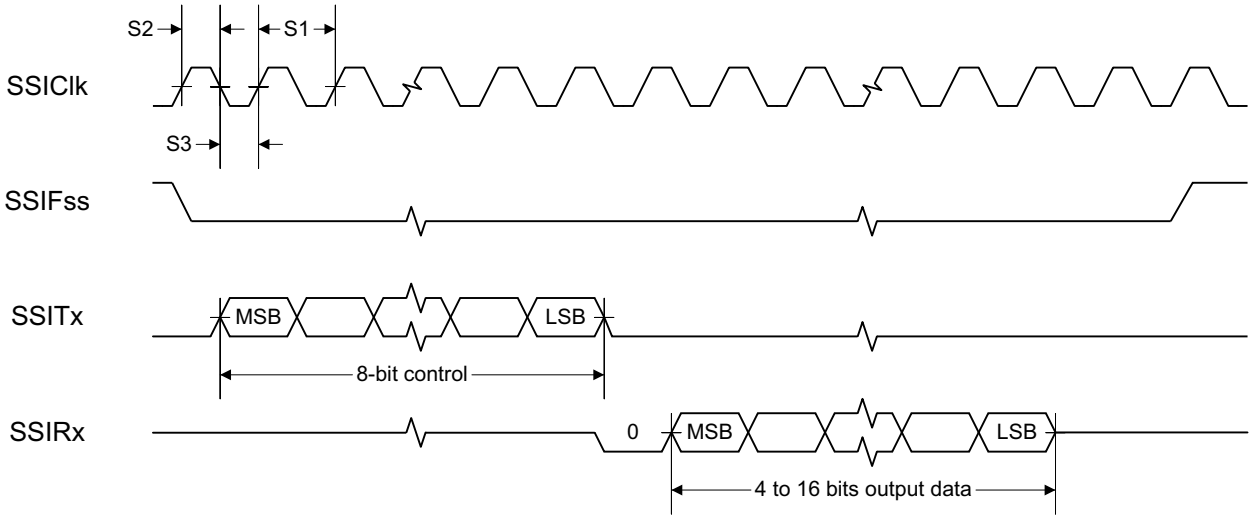

Figure 8-2. SSI Timing for MICROWIRE Frame Format (FRF = 10), Single Transfer

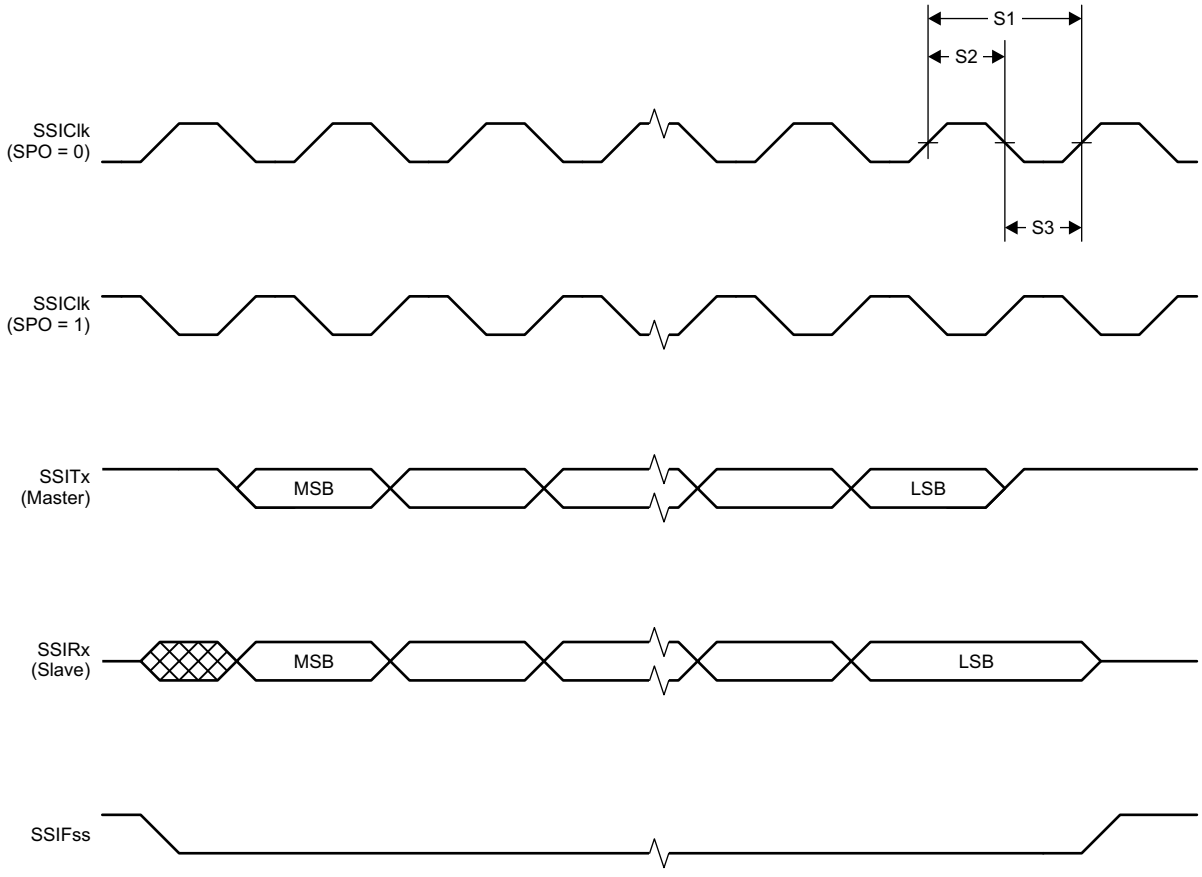

Figure 8-3. SSI Timing for SPI Frame Format (FRF = 00), With SPH = 1

8.14.5 UART

8.14.5.1 UART Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT
UART rate			3	MBaud

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8.15 Peripheral Characteristics

8.15.1 ADC

8.15.1.1 Analog-to-Digital Converter (ADC) Characteristics

T_c = 25 °C, V_{DDS} = 3.0 V and voltage scaling enabled, unless otherwise noted.(1)
Performance numbers require use of offset and gain adjustements in software by TI-provided ADC drivers.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input voltage range		0		VDDS	V
	Resolution			12		Bits
	Sample Rate				200	ksps
	Offset	Internal 4.3 V equivalent reference(2)		–0.24		LSB
	Gain error	Internal 4.3 V equivalent reference(2)		7.14		LSB
DNL(4)	Differential nonlinearity			>–1		LSB
INL	Integral nonlinearity			±4		LSB
ENOB	Effective number of bits	Internal 4.3 V equivalent reference(2), 200 kSamples/s, 9.6 kHz input tone		9.8		Bits
		Internal 4.3 V equivalent reference(2), 200 kSamples/s, 9.6 kHz input tone, DC/DC enabled		9.8		
		VDDS as reference, 200 kSamples/s, 9.6 kHz input tone		10.1		
		Internal reference, voltage scaling disabled, 32 samples average (software), 200 kSamples/s, 300 Hz input tone		11.1		
		Internal reference, voltage scaling disabled, 14-bit mode, 200 kSamples/s, 300 Hz input tone (5)		11.3		
		Internal reference, voltage scaling disabled, 15-bit mode, 200 kSamples/s, 300 Hz input tone (5)		11.6		
THD	Total harmonic distortion	Internal 4.3 V equivalent reference(2), 200 kSamples/s, 9.6 kHz input tone		–65		dB
		VDDS as reference, 200 kSamples/s, 9.6 kHz input tone		–70		
		Internal reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300 Hz input tone		–72		
SINAD, SNDR	Signal-to-noise and distortion ratio	Internal 4.3 V equivalent reference(2), 200 kSamples/s, 9.6 kHz input tone		60		dB
		VDDS as reference, 200 kSamples/s, 9.6 kHz input tone		63		
		Internal reference, voltage scaling disabled, 32 samples average (software), 200 kSamples/s, 300 Hz input tone		68		
SFDR	Spurious-free dynamic range	Internal 4.3 V equivalent reference(2), 200 kSamples/s, 9.6 kHz input tone		70		dB
		VDDS as reference, 200 kSamples/s, 9.6 kHz input tone		73		
		Internal reference, voltage scaling disabled, 32 samples average (software), 200 kSamples/s, 300 Hz input tone		75		
	Conversion time	Serial conversion, time-to-output, 24 MHz clock		50		Clock Cycles
	Current consumption	Internal 4.3 V equivalent reference(2)		0.39		mA
	Current consumption	VDDS as reference		0.56		mA
	Reference voltage	Equivalent fixed internal reference (input voltage scaling enabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS API in order to include the gain/offset compensation factors stored in FCFG1		4.3(2) (3)		V
	Reference voltage	Fixed internal reference (input voltage scaling disabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS API in order to include the gain/offset compensation factors stored in FCFG1. This value is derived from the scaled value (4.3 V) as follows: V_{ref} = 4.3 V × 1408 / 4095		1.48		V
	Reference voltage	VDDS as reference, input voltage scaling enabled		VDDS		V
	Reference voltage	VDDS as reference, input voltage scaling disabled		VDDS / 2.82(3)		V

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8.15.1.1 Analog-to-Digital Converter (ADC) Characteristics (continued)

T_c = 25 °C, V_{DDS} = 3.0 V and voltage scaling enabled, unless otherwise noted.(1)
Performance numbers require use of offset and gain adjustements in software by TI-provided ADC drivers.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input impedance	200 kSamples/s, voltage scaling enabled. Capacitive input, Input impedance depends on sampling frequency and sampling time		>1		MΩ

(1) Using IEEE Std 1241-2010 for terminology and test methods
(2) Input signal scaled down internally before conversion, as if voltage range was 0 to 4.3 V
(3) Applied voltage must be within Absolute Maximum Ratings at all times
(4) No missing codes
(5) ADC_output = Σ(4^n samples) >> n, n = desired extra bits

8.15.2 DAC

8.15.2.1 Digital-to-Analog Converter (DAC) Characteristics

T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
General Parameters						
	Resolution			8		Bits
V_{DDS}	Supply voltage	Any load, any V_{REF}, pre-charge OFF, DAC charge-pump ON	1.8		3.8	V
		External Load(4), any V_{REF}, pre-charge OFF, DAC charge-pump OFF	2.0		3.8	
		Any load, V_{REF} = DCOUPL, pre-charge ON	2.6		3.8	
F_{DAC}	Clock frequency	Buffer ON (recommended for external load)	16		250	kHz
		Buffer OFF (internal load)	16		1000	
	Voltage output settling time	V_{REF} = VDDS, buffer OFF, internal load		13		1 / F_{DAC}
		V_{REF} = VDDS, buffer ON, external capacitive load = 20 pF(3)		13.8		
	External capacitive load			20	200	pF
	External resistive load		10			MΩ
	Short circuit current				400	µA
Z_{MAX}	Max output impedance Vref = VDDS, buffer ON, CLK 250 kHz	VDDS = 3.8 V, DAC charge-pump OFF		50.8		kΩ
		VDDS = 3.0 V, DAC charge-pump ON		51.7		
		VDDS = 3.0 V, DAC charge-pump OFF		53.2		
		VDDS = 2.0 V, DAC charge-pump ON		48.7		
		VDDS = 2.0 V, DAC charge-pump OFF		70.2		
		VDDS = 1.8 V, DAC charge-pump ON		46.3		
		VDDS = 1.8 V, DAC charge-pump OFF		88.9		
Internal Load - Continuous Time Comparator / Low Power Clocked Comparator						
DNL	Differential nonlinearity	V_{REF} = VDDS, load = Continuous Time Comparator or Low Power Clocked Comparator F_{DAC} = 250 kHz		±1		LSB(1)
	Differential nonlinearity	V_{REF} = VDDS, load = Continuous Time Comparator or Low Power Clocked Comparator F_{DAC} = 16 kHz		±1.2		
	Offset error(2) Load = Continuous Time Comparator	V_{REF} = VDDS = 3.8 V		±0.64		LSB(1)
		V_{REF} = VDDS= 3.0 V		±0.81		
		V_{REF} = VDDS = 1.8 V		±1.27		
		V_{REF} = DCOUPL, pre-charge ON		±3.43		
		V_{REF} = DCOUPL, pre-charge OFF		±2.88		
		V_{REF} = ADCREF		±2.37		

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8.15.2.1 Digital-to-Analog Converter (DAC) Characteristics (continued)

T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Offset error[2] Load = Low Power Clocked Comparator	V_{REF} = VDDS= 3.8 V		±0.78		LSB[1]
		V_{REF} = VDDS = 3.0 V		±0.77		
		V_{REF} = VDDS= 1.8 V		±3.46		
		V_{REF} = DCOUPL, pre-charge ON		±3.44		
		V_{REF} = DCOUPL, pre-charge OFF		±4.70		
		V_{REF} = ADCREF		±4.11		
	Max code output voltage variation[2] Load = Continuous Time Comparator	V_{REF} = VDDS = 3.8 V		±1.53		LSB[1]
		V_{REF} = VDDS = 3.0 V		±1.71		
		V_{REF} = VDDS= 1.8 V		±2.10		
		V_{REF} = DCOUPL, pre-charge ON		±6.00		
		V_{REF} = DCOUPL, pre-charge OFF		±3.85		
		V_{REF} = ADCREF		±5.84		
	Max code output voltage variation[2] Load = Low Power Clocked Comparator	V_{REF} = VDDS= 3.8 V		±2.92		LSB[1]
		V_{REF} =VDDS= 3.0 V		±3.06		
		V_{REF} = VDDS= 1.8 V		±3.91		
		V_{REF} = DCOUPL, pre-charge ON		±7.84		
		V_{REF} = DCOUPL, pre-charge OFF		±4.06		
		V_{REF} = ADCREF		±6.94		
	Output voltage range[2] Load = Continuous Time Comparator	V_{REF} = VDDS = 3.8 V, code 1		0.03		V
		V_{REF} = VDDS = 3.8 V, code 255		3.62		
		V_{REF} = VDDS= 3.0 V, code 1		0.02		
		V_{REF} = VDDS= 3.0 V, code 255		2.86		
		V_{REF} = VDDS= 1.8 V, code 1		0.01		
		V_{REF} = VDDS = 1.8 V, code 255		1.71		
		V_{REF} = DCOUPL, pre-charge OFF, code 1		0.01		
		V_{REF} = DCOUPL, pre-charge OFF, code 255		1.21		
		V_{REF} = DCOUPL, pre-charge ON, code 1		1.27		
		V_{REF} = DCOUPL, pre-charge ON, code 255		2.46		
		V_{REF} = ADCREF, code 1		0.01		
		V_{REF} = ADCREF, code 255		1.41		
	Output voltage range[2] Load = Low Power Clocked Comparator	V_{REF} = VDDS = 3.8 V, code 1		0.03		V
		V_{REF} = VDDS= 3.8 V, code 255		3.61		
		V_{REF} = VDDS= 3.0 V, code 1		0.02		
		V_{REF} = VDDS= 3.0 V, code 255		2.85		
		V_{REF} = VDDS = 1.8 V, code 1		0.01		
		V_{REF} = VDDS = 1.8 V, code 255		1.71		
		V_{REF} = DCOUPL, pre-charge OFF, code 1		0.01		
		V_{REF} = DCOUPL, pre-charge OFF, code 255		1.21		
		V_{REF} = DCOUPL, pre-charge ON, code 1		1.27		
		V_{REF} = DCOUPL, pre-charge ON, code 255		2.46		
		V_{REF} = ADCREF, code 1		0.01		
		V_{REF} = ADCREF, code 255		1.41		
External Load (Keysight 34401A Multimeter)						
INL	Integral nonlinearity	V_{REF} = VDDS, F_{DAC} = 250 kHz		±1		LSB[1]
		V_{REF} = DCOUPL, F_{DAC} = 250 kHz		±1		
		V_{REF} = ADCREF, F_{DAC} = 250 kHz		±1		
DNL	Differential nonlinearity	V_{REF} = VDDS, F_{DAC} = 250 kHz		±1		LSB[1]

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8.15.2.1 Digital-to-Analog Converter (DAC) Characteristics (continued)

T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Offset error	V_{REF} = VDDS= 3.8 V		±0.20		LSB(1)
		V_{REF} = VDDS= 3.0 V		±0.25		
		V_{REF} = VDDS = 1.8 V		±0.45		
		V_{REF} = DCOUPL, pre-charge ON		±1.55		
		V_{REF} = DCOUPL, pre-charge OFF		±1.30		
		V_{REF} = ADCREF		±1.10		
	Max code output voltage variation	V_{REF} = VDDS= 3.8 V		±0.60		LSB(1)
		V_{REF} = VDDS= 3.0 V		±0.55		
		V_{REF} = VDDS= 1.8 V		±0.60		
		V_{REF} = DCOUPL, pre-charge ON		±3.45		
		V_{REF} = DCOUPL, pre-charge OFF		±2.10		
		V_{REF} = ADCREF		±1.90		
	Output voltage range Load = Low Power Clocked Comparator	V_{REF} = VDDS = 3.8 V, code 1		0.03		V
		V_{REF} = VDDS = 3.8 V, code 255		3.61		
		V_{REF} = VDDS = 3.0 V, code 1		0.02		
		V_{REF} = VDDS= 3.0 V, code 255		2.85		
		V_{REF} = VDDS= 1.8 V, code 1		0.02		
		V_{REF} = VDDS = 1.8 V, code 255		1.71		
		V_{REF} = DCOUPL, pre-charge OFF, code 1		0.02		
		V_{REF} = DCOUPL, pre-charge OFF, code 255		1.20		
		V_{REF} = DCOUPL, pre-charge ON, code 1		1.27		
		V_{REF} = DCOUPL, pre-charge ON, code 255		2.46		
		V_{REF} = ADCREF, code 1		0.02		
		V_{REF} = ADCREF, code 255		1.42		

(1) 1 LSB (V_{REF} 3.8 V/3.0 V/1.8 V/DCOUPL/ADCREF) = 14.10 mV/11.13 mV/6.68 mV/4.67 mV/5.48 mV
(2) Includes comparator offset
(3) A load > 20 pF will increases the settling time
(4) Keysight 34401A Multimeter

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8.15.3 Temperature and Battery Monitor

8.15.3.1 Temperature Sensor

Measured on a Texas Instruments reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			2		°C
Accuracy	-40 °C to 0 °C		±4.0		°C
Accuracy	0 °C to 105 °C		±2.5		°C
Supply voltage coefficient(1)			3.9		°C/V

(1) The temperature sensor is automatically compensated for VDDS variation when using the TI-provided driver.

8.15.3.2 Battery Monitor

Measured on a Texas Instruments reference design with T_c = 25 °C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			25		mV
Range		1.8		3.8	V
Integral nonlinearity (max)			23		mV
Accuracy	VDDS = 3.0 V		22.5		mV
Offset error			-32		mV
Gain error			-1		%

8.15.4 Comparator

8.15.4.1 Continuous Time Comparator

T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range(1)		0		V_{DDS}	V
Offset	Measured at V_{DDS} / 2		±5		mV
Decision time	Step from –10 mV to 10 mV		0.78		µs
Current consumption	Internal reference		9.2		µA

(1) The input voltages can be generated externally and connected throughout I/Os or an internal reference voltage can be generated using the DAC

8.15.5 GPIO

8.15.5.1 GPIO DC Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_A = 25 °C, V_{DDS} = 1.8 V					
GPIO VOH at 8 mA load	IOCURR = 2, high-drive GPIOs only		1.56		V
GPIO VOL at 8 mA load	IOCURR = 2, high-drive GPIOs only		0.24		V
GPIO VOH at 4 mA load	IOCURR = 1		1.59		V
GPIO VOL at 4 mA load	IOCURR = 1		0.21		V
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V		73		µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDDS		19		µA
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1		1.08		V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0		0.73		V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points		0.35		V
T_A = 25 °C, V_{DDS} = 3.0 V					
GPIO VOH at 8 mA load	IOCURR = 2, high-drive GPIOs only		2.59		V
GPIO VOL at 8 mA load	IOCURR = 2, high-drive GPIOs only		0.42		V
GPIO VOH at 4 mA load	IOCURR = 1		2.63		V
GPIO VOL at 4 mA load	IOCURR = 1		0.40		V

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8.15.5.1 GPIO DC Characteristics (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_A = 25 °C, V_{DDS} = 3.8 V					
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V		282		µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDDS		110		µA
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1		1.97		V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0		1.55		V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points		0.42		V
T_A = 25 °C					
VIH	Lowest GPIO input voltage reliably interpreted as a *High*	0.8*V_{DDS}			V
VIL	Highest GPIO input voltage reliably interpreted as a *Low*			0.2*V_{DDS}	V

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8.16 Typical Characteristics

All measurements in this section are done with T_c = 25 °C and V_{DDS} = 3.0 V, unless otherwise noted. See *Recommended Operating Conditions*, Section 8.3, for device limits. Values exceeding these limits are for reference only.

8.16.1 MCU Current

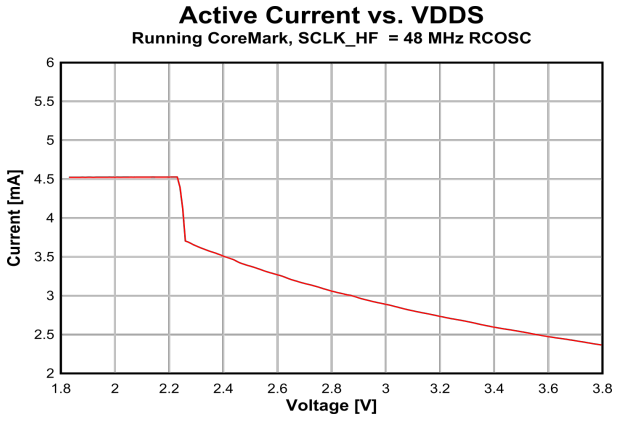

Figure 8-4. Active Mode (MCU) Current vs. Supply Voltage (VDDS)

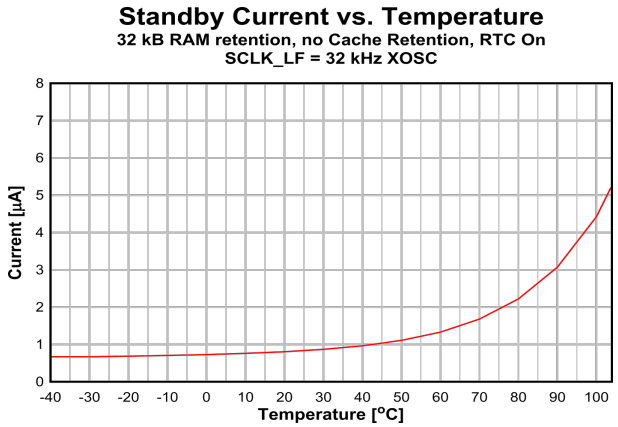

Figure 8-5. Standby Mode (MCU) Current vs. Temperature

8.16.2 RX Current

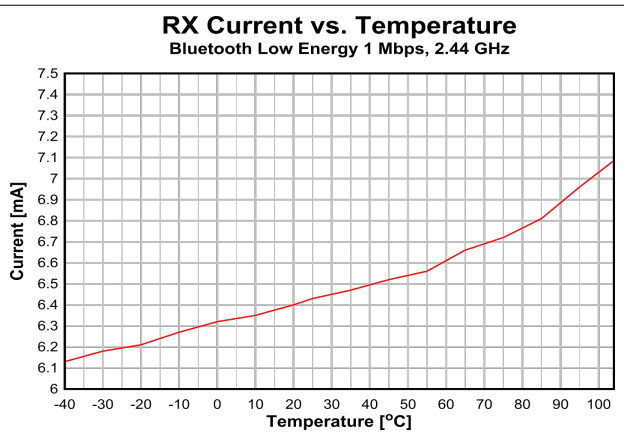

Figure 8-6. RX Current vs. Temperature (BLE 1 Mbps, 2.44 GHz)

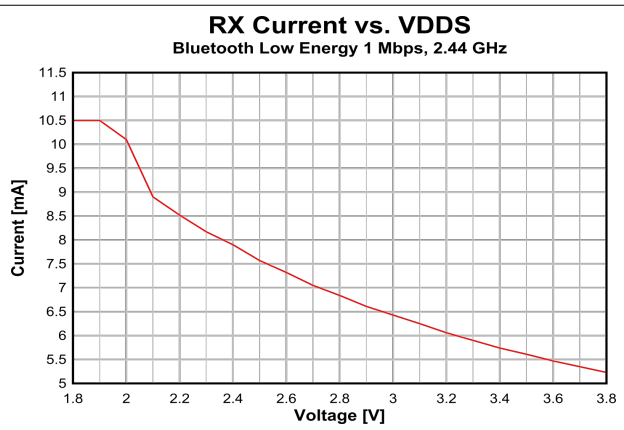

Figure 8-7. RX Current vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz)

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8.16.3 TX Current

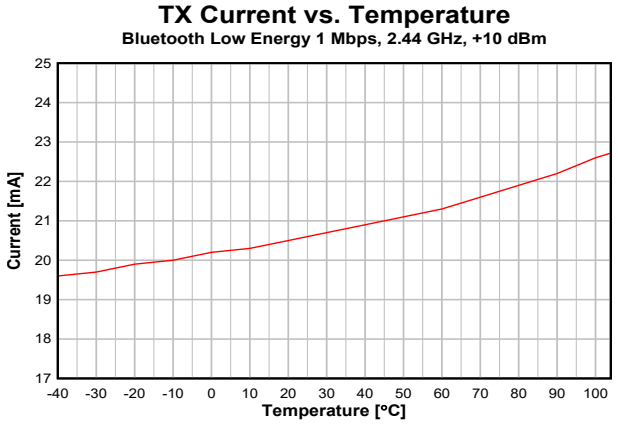

Figure 8-8. TX Current vs. Temperature (BLE 1 Mbps, 2.44 GHz)

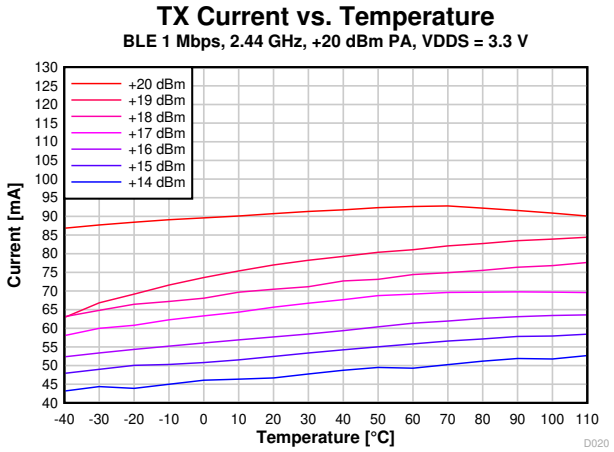

Figure 8-9. TX Current vs. Temperature (BLE 1 Mbps, 2.44 GHz, VDDS = 3.3 V)

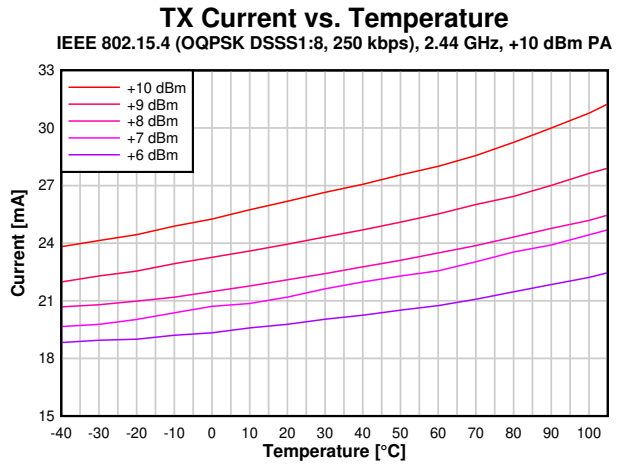

Figure 8-10. TX Current vs. Temperature (250 kbps, 2.44 GHz, +10 dBm PA)

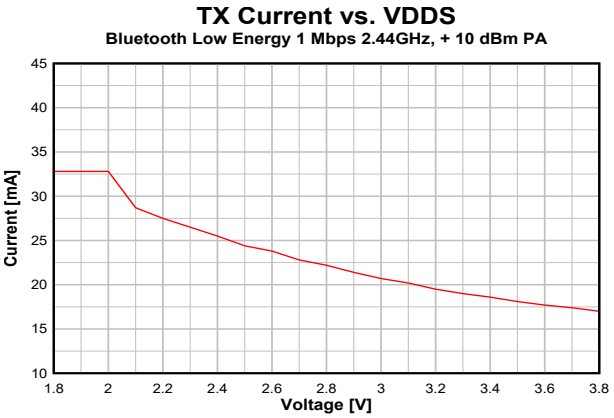

Figure 8-11. TX Current vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz)

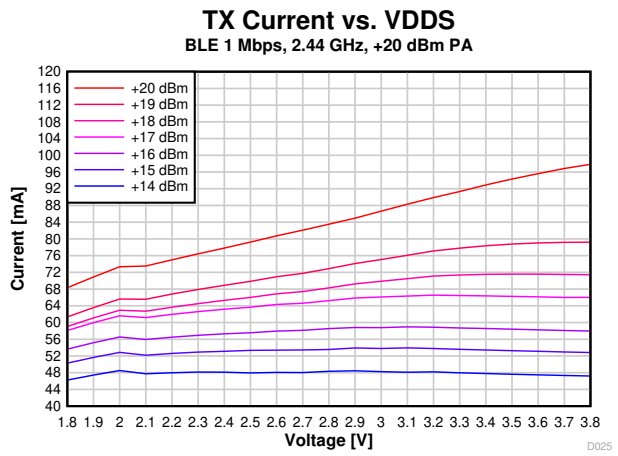

Figure 8-12. TX Current vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz, +20 dBm PA)

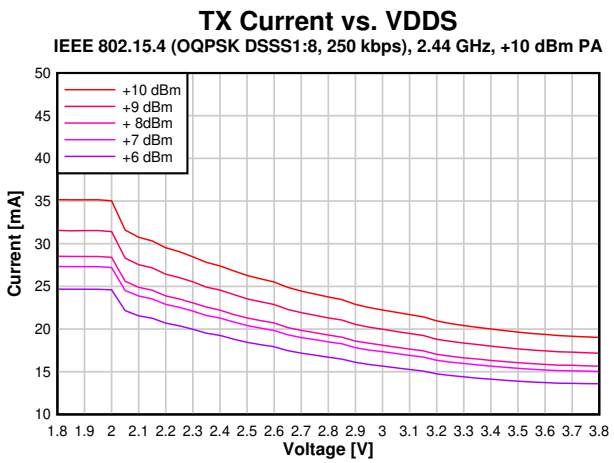

Figure 8-13. TX Current vs. Supply Voltage (VDDS) (250 kbps, 2.44 GHz, +10 dBm PA)

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Table 8-1. Typical TX Current and Output Power, regular PA

CC2651P3 at 2.4 GHz, VDDS = 3.0 V (Measured on CC2651-P3EM-7XD24-PA24)			
txPower	**TX Power Setting (SmartRF Studio)**	**Typical Output Power [dBm]**	**Typical Current Consumption [mA]**
0x701F	5	5.5	12.5
0x3A17	4	4.5	11.9
0x3A64	3	3.1	11.2
0x325F	2	2.0	10.8
0x2C5C	1	1.3	10.5
0x2659	0	0.4	10.2
0x1697	-3	-2.8	9.4
0x1693	-5	-4.8	8.9
0x1292	-6	-5.4	8.8
0xCD3	-9	-9.0	8.4
0xAD1	-10	-10.4	8.2
0xACF	-12	-12.0	8.1
0x6CD	-15	-13.7	7.9
0x6CA	-18	-16.8	7.7
0x4C8	-20	-19.3	7.6

Table 8-2. Typical TX Current and Output Power, high power PA, 10 dBm mode

CC2651P3 at 2.4 GHz, VDDS = 3.0 V (Measured on CC261-P3EM-5XS24-PA24_10dBm)			
txPower	**TX Power Setting (SmartRF Studio)**	**Typical Output Power [dBm]**	**Typical Current Consumption [mA]**
0x14395A	10	10.1	23.6
0x142F55	9	9.0	22.1
0x62F35	8	7.8	21.1
0x63930	7	6.9	20.1
0x6292B	6	5.9	19.1

Table 8-3. Typical TX Current and Output Power, high power PA, 20 dBm mode

CC2651P3 at 2.4 GHz, VDDS = 3.3 V (Measured on CC2651-P3EM-7XD24-PA24)			
txPower	**TX Power Setting (SmartRF Studio)**	**Typical Output Power [dBm]**	**Typical Current Consumption [mA]**
0x3F75F5	20	20.0	100.1
0x3F61E2	19	19.4	91.1
0x3047E0	18	19.0	86.4
0x1B4FE5	17	18.1	78.3
0x1B39DE	16	17.3	71.8
0x1B2FDA	15	16.7	67.1
0x1B27D6	14	15.9	61.8

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8.16.4 RX Performance

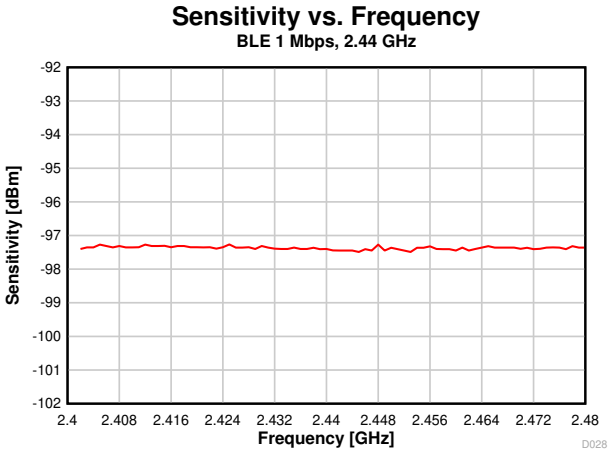

Figure 8-14. Sensitivity vs. Frequency (BLE 1 Mbps, 2.44 GHz)

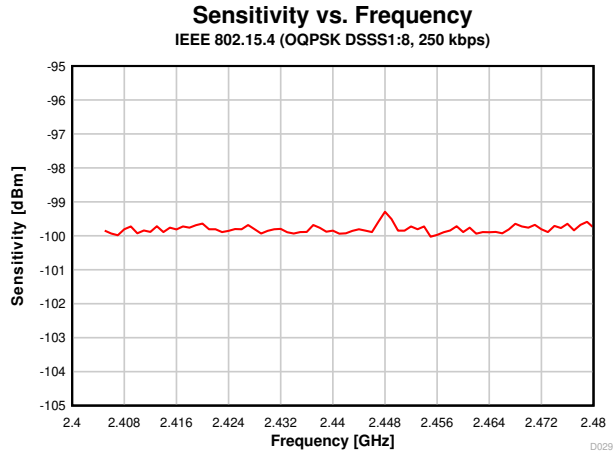

Figure 8-15. Sensitivity vs. Frequency (250 kbps, 2.44 GHz)

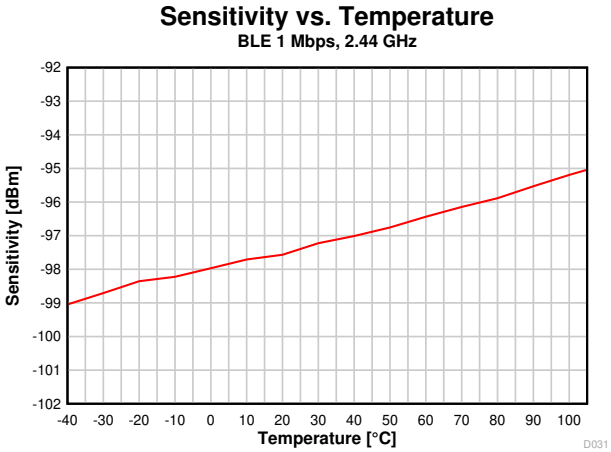

Figure 8-16. Sensitivity vs. Temperature (BLE 1 Mbps, 2.44 GHz)

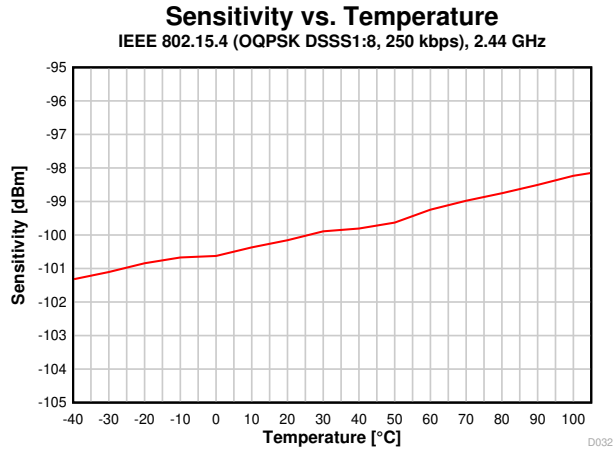

Figure 8-17. Sensitivity vs. Temperature (250 kbps, 2.44 GHz)

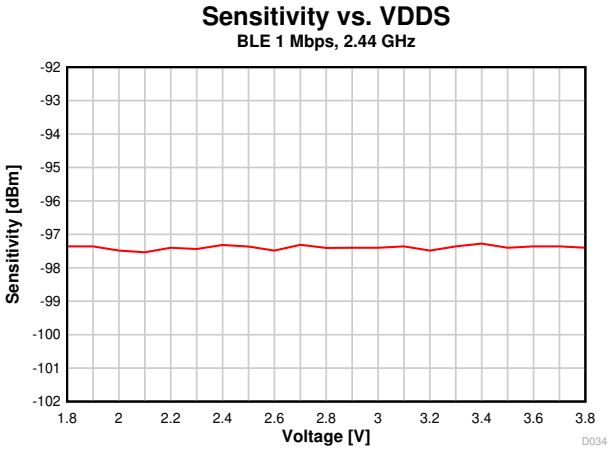

Figure 8-18. Sensitivity vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz)

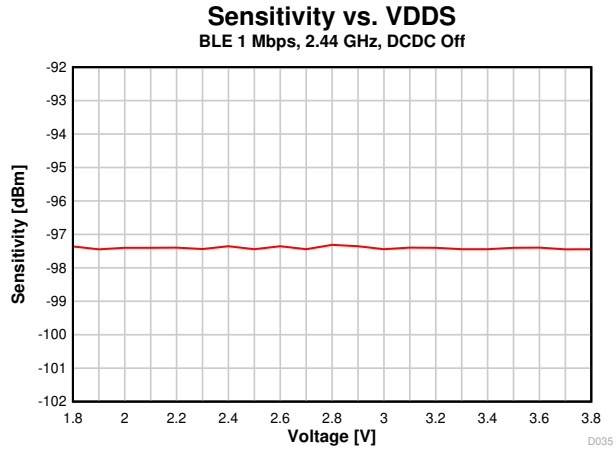

Figure 8-19. Sensitivity vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz, DCDC Off)

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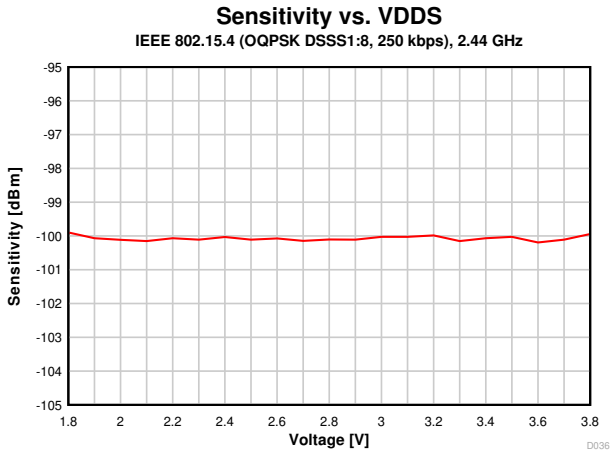

Figure 8-20. Sensitivity vs. Supply Voltage (VDDS) (250 kbps, 2.44 GHz)

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8.16.5 TX Performance

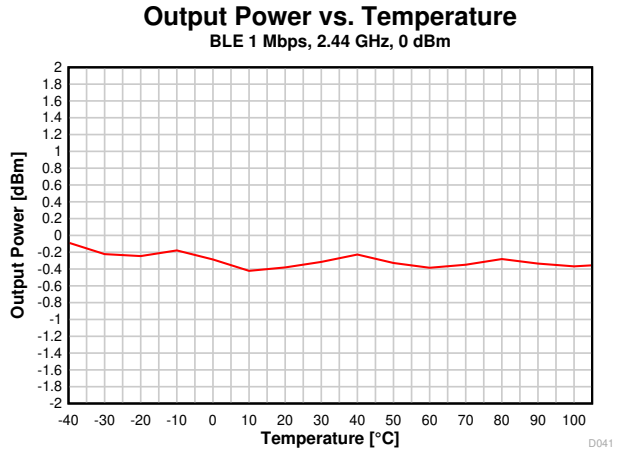

Figure 8-21. Output Power vs. Temperature (BLE 1 Mbps, 2.44 GHz)

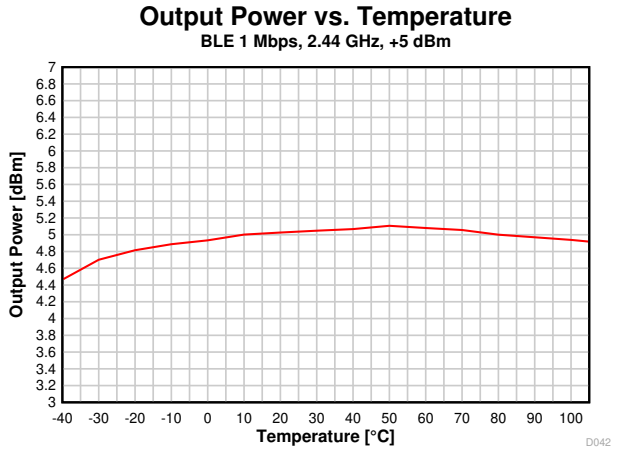

Figure 8-22. Output Power vs. Temperature (BLE 1 Mbps, 2.44 GHz, +5 dBm)

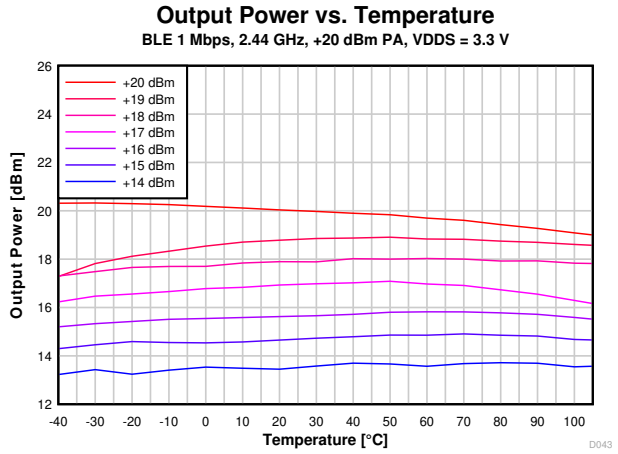

Figure 8-23. Output Power vs. Temperature (BLE 1 Mbps, 2.44 GHz, +20 dBm PA)

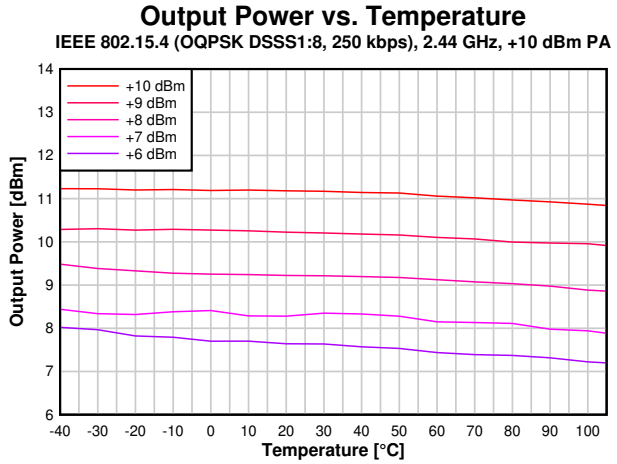

Figure 8-24. Output Power vs. Temperature (2.44 GHz, +10 dBm PA)

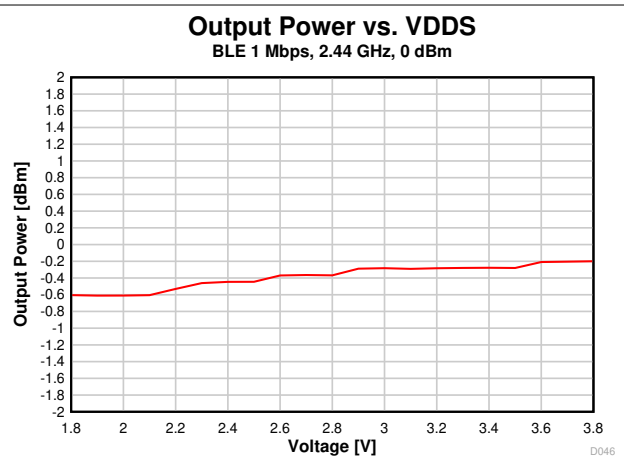

Figure 8-25. Output Power vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz)

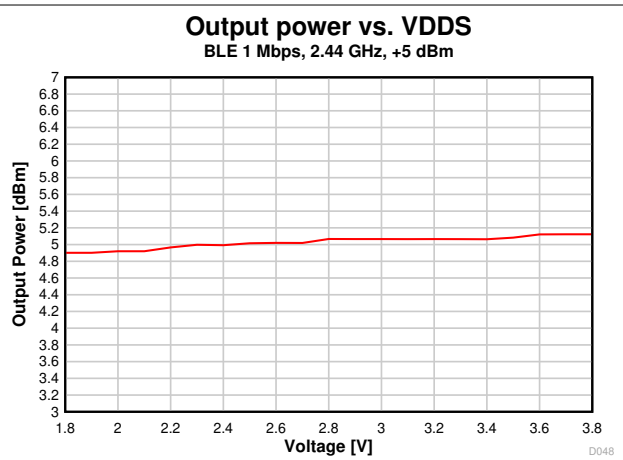

Figure 8-26. Output Power vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz, +5 dBm)

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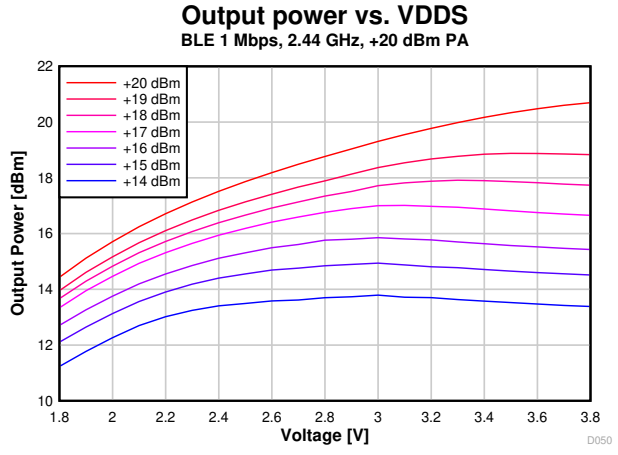

Figure 8-27. Output Power vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz, +20 dBm PA)

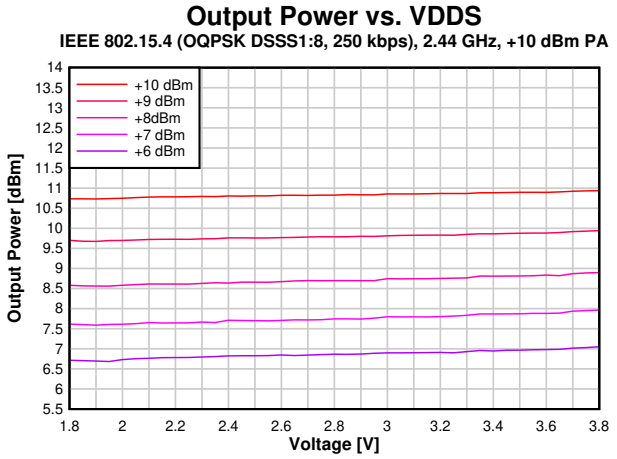

Figure 8-28. Output Power vs. Supply Voltage (VDDS) (2.44 GHz, +10 dBm PA)

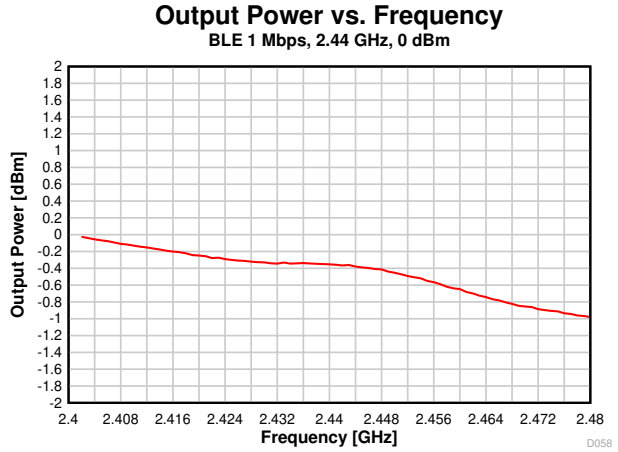

Figure 8-29. Output Power vs. Frequency (BLE 1 Mbps, 2.44 GHz)

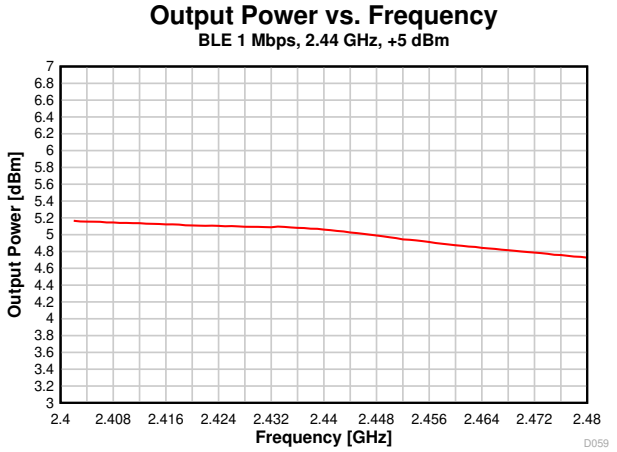

Figure 8-30. Output Power vs. Frequency (BLE 1 Mbps, 2.44 GHz, +5 dBm)

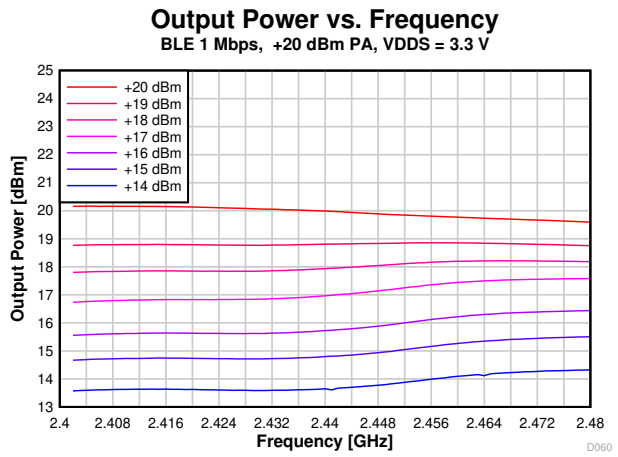

Figure 8-31. Output Power vs. Frequency (BLE 1 Mbps, 2.44 GHz, +20 dBm PA)

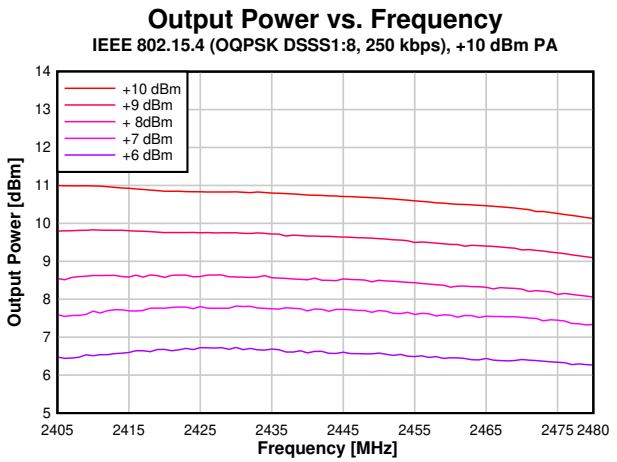

Figure 8-32. Output Power vs. Frequency (250 kbps, +10 dBm PA)

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8.16.6 ADC Performance

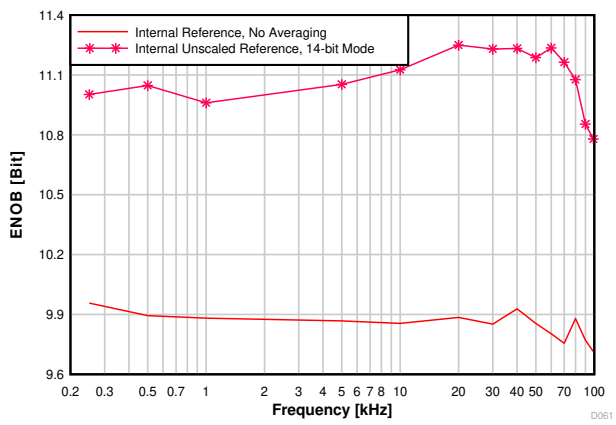

Figure 8-33. ENOB vs. Input Frequency

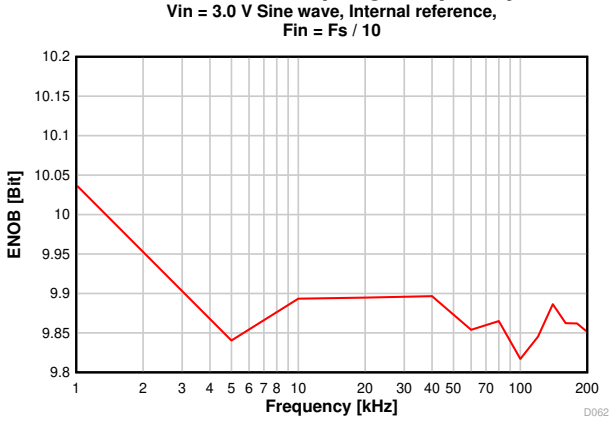

Figure 8-34. ENOB vs. Sampling Frequency

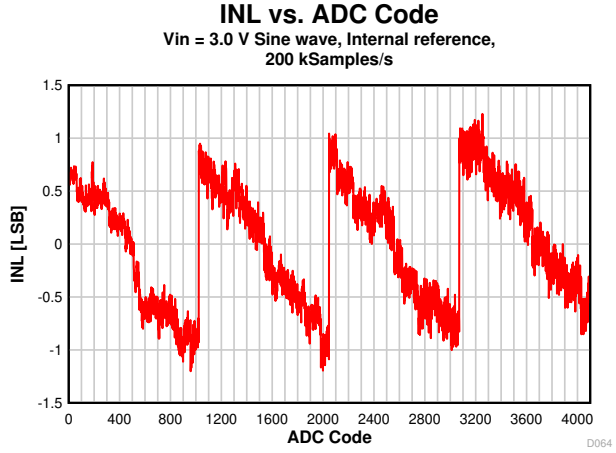

Figure 8-35. INL vs. ADC Code

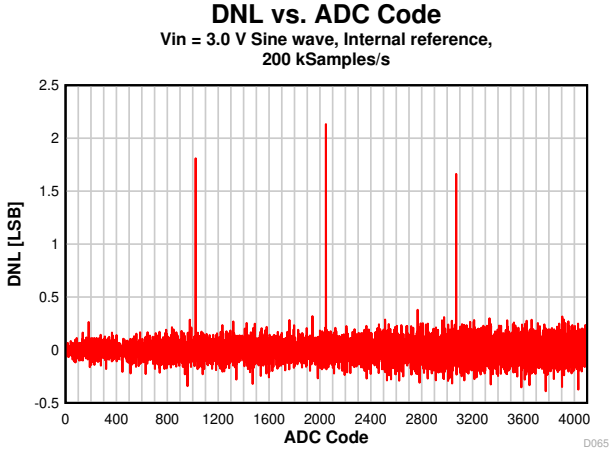

Figure 8-36. DNL vs. ADC Code

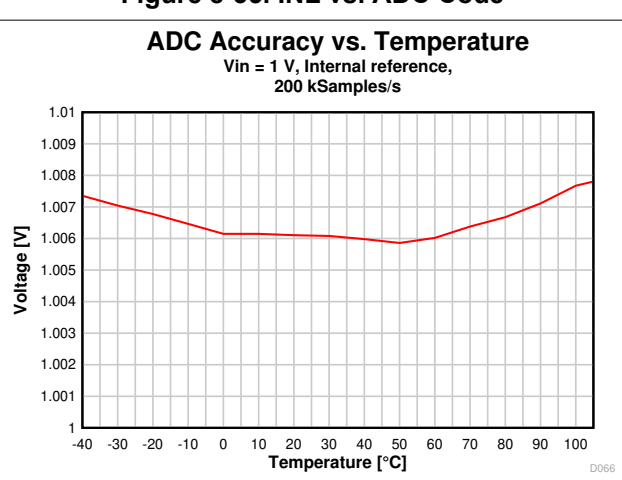

Figure 8-37. ADC Accuracy vs. Temperature

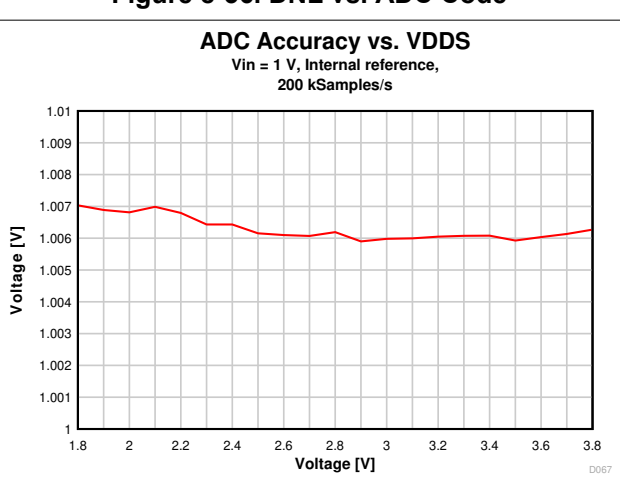

Figure 8-38. ADC Accuracy vs. Supply Voltage (VDDS)

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9 Detailed Description

9.1 Overview

Section 4 shows the core modules of the CC2651P3 device.

9.2 System CPU

The CC2651P3 SimpleLink™ Wireless MCU contains an Arm® Cortex®-M4 system CPU, which runs the application and the higher layers of radio protocol stacks.

The system CPU is the foundation of a high-performance, low-cost platform that meets the system requirements of minimal memory implementation, and low-power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

Its features include the following:

- ARMv7-M architecture optimized for small-footprint embedded applications
- Arm Thumb®-2 mixed 16- and 32-bit instruction set delivers the high performance expected of a 32-bit Arm core in a compact memory size
- Fast code execution permits increased sleep mode time
- Deterministic, high-performance interrupt handling for time-critical applications
- Single-cycle multiply instruction and hardware divide
- Hardware division and fast digital-signal-processing oriented multiply accumulate
- Saturating arithmetic for signal processing
- Full debug with data matching for watchpoint generation
  - Data Watchpoint and Trace Unit (DWT)
  - JTAG Debug Access Port (DAP)
  - Flash Patch and Breakpoint Unit (FPB)
- Trace support reduces the number of pins required for debugging and tracing
  - Instrumentation Trace Macrocell Unit (ITM)
  - Trace Port Interface Unit (TPIU) with asynchronous serial wire output (SWO)
- Optimized for single-cycle flash memory access
- Tightly connected to 8-KB 4-way random replacement cache for minimal active power consumption and wait states
- Ultra-low-power consumption with integrated sleep modes
- 48 MHz operation
- 1.25 DMIPS per MHz

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9.3 Radio (RF Core)

The RF Core is a highly flexible and future proof radio module which contains an Arm Cortex-M0 processor that interfaces the analog RF and base-band circuitry, handles data to and from the system CPU side, and assembles the information bits in a given packet structure. The RF core offers a high level, command-based API to the main CPU that configurations and data are passed through. The Arm Cortex-M0 processor is not programmable by customers and is interfaced through the TI-provided RF driver that is included with the SimpleLink Software Development Kit (SDK).

The RF core can autonomously handle the time-critical aspects of the radio protocols, thus offloading the main CPU, which reduces power and leaves more resources for the user application. Several signals are also available to control external circuitry such as RF switches or range extenders autonomously.

The various physical layer radio formats are partly built as a software defined radio where the radio behavior is either defined by radio ROM contents or by non-ROM radio formats delivered in form of firmware patches with the SimpleLink SDKs. This allows the radio platform to be updated for support of future versions of standards even with over-the-air (OTA) updates while still using the same silicon.

9.3.1 Bluetooth 5.2 Low Energy

The RF Core offers full support for Bluetooth 5.2 Low Energy, including the high-sped 2-Mbps physical layer and the 500-kbps and 125-kbps long range PHYs (Coded PHY) through the TI provided Bluetooth 5.2 stack or through a high-level Bluetooth API.

The new high-speed mode allows data transfers up to 2 Mbps, twice the speed of Bluetooth 4.2 and five times the speed of Bluetooth 4.0, without increasing power consumption. In addition to faster speeds, this mode offers significant improvements for energy efficiency and wireless coexistence with reduced radio communication time.

Bluetooth 5.2 also enables unparalleled flexibility for adjustment of speed and range based on application needs, which capitalizes on the high-speed or long-range modes respectively. Data transfers are now possible at 2 Mbps, enabling development of applications using voice, audio, imaging, and data logging that were not previously an option using Bluetooth low energy. With high-speed mode, existing applications deliver faster responses, richer engagement, and longer battery life. Bluetooth 5.2 enables fast, reliable firmware updates.

9.3.2 802.15.4 (Zigbee and 6LoWPAN)

Through a dedicated IEEE radio API, the RF Core supports the 2.4-GHz IEEE 802.15.4-2011 physical layer (2 Mchips per second Offset-QPSK with DSSS 1:8), used in Zigbee and 6LoWPAN protocols. TI provides royalty-free protocol stacks for Zigbee as part of the SimpleLink SDK, enabling a robust end-to-end solution.

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9.4 Memory

The up to 352-KB nonvolatile (Flash) memory provides storage for code and data. The flash memory is in-system programmable and erasable. The last flash memory sector must contain a Customer Configuration section (CCFG) that is used by boot ROM and TI provided drivers to configure the device. This configuration is done through the ccfg.c source file that is included in all TI provided examples.

The ultra-low leakage system static RAM (SRAM) is a single 32-KB block and can be used for both storage of data and execution of code. Retention of SRAM contents in Standby power mode is enabled by default and included in Standby mode power consumption numbers.

To improve code execution speed and lower power when executing code from nonvolatile memory, a 4-way nonassociative 8-KB cache is enabled by default to cache and prefetch instructions read by the system CPU. The cache can be used as a general-purpose RAM by enabling this feature in the Customer Configuration Area (CCFG).

The ROM contains a serial (SPI and UART) bootloader that can be used for initial programming of the device.

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9.5 Cryptography

The CC2651P3 device comes with a wide set of cryptography-related hardware accelerators, reducing code footprint and execution time for cryptographic operations. It also has the benefit of being lower power and improves availability and responsiveness of the system because the cryptography operations run in a background hardware thread.
The hardware accelerator modules are:

- **True Random Number Generator (TRNG)** module provides a true, nondeterministic noise source for the purpose of generating keys, initialization vectors (IVs), and other random number requirements. The TRNG is built on 24 ring oscillators that create unpredictable output to feed a complex nonlinear-combinatorial circuit.
- **Advanced Encryption Standard (AES)** with 128 bit key lengths

Together with the hardware accelerator module, a large selection of open-source cryptography libraries provided with the Software Development Kit (SDK), this allows for secure and future proof IoT applications to be easily built on top of the platform. The TI provided cryptography drivers are:

- **Key Agreement Schemes**
  - Elliptic curve Diffie–Hellman with static or ephemeral keys (ECDH and ECDHE)
- **Signature Generation**
  - Elliptic curve Diffie-Hellman Digital Signature Algorithm (ECDSA)
- **Curve Support**
  - Short Weierstrass form (full hardware support), such as:
    - NIST-P256
  - Montgomery form (hardware support for multiplication), such as:
    - Curve25519
- **Hash**
  - SHA256
- **MACs**
  - HMAC with SHA256
  - AES CBC-MAC
- **Block ciphers**
  - AESECB
  - AESCBC
  - AESCTR
- **Authenticated Encryption**
  - AESCCM
- **Random number generation**
  - True Random Number Generator
  - AES CTR DRBG

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9.6 Timers

A large selection of timers are available as part of the CC2651P3 device. These timers are:

- **Real-Time Clock (RTC)**

  A 70-bit 3-channel timer running on the 32 kHz low frequency system clock (SCLK_LF)
  This timer is available in all power modes except Shutdown. The timer can be calibrated to compensate for frequency drift when using the LF RCOSC as the low frequency system clock. If an external LF clock with frequency different from 32.768 kHz is used, the RTC tick speed can be adjusted to compensate for this. When using TI-RTOS, the RTC is used as the base timer in the operating system and should thus only be accessed through the kernel APIs such as the Clock module. By default, the RTC halts when a debugger halts the device.
- **General Purpose Timers (GPTIMER)**

  The four flexible GPTIMERs can be used as either 4× 32 bit timers or 8× 16 bit timers, all running on up to 48 MHz. Each of the 16- or 32-bit timers support a wide range of features such as one-shot or periodic counting, pulse width modulation (PWM), time counting between edges and edge counting. The inputs and outputs of the timer are connected to the device event fabric, which allows the timers to interact with signals such as GPIO inputs, other timers, DMA and ADC. The GPTIMERs are available in Active and Idle power modes.
- **Radio Timer**

  A multichannel 32-bit timer running at 4 MHz is available as part of the device radio. The radio timer is typically used as the timing base in wireless network communication using the 32-bit timing word as the network time. The radio timer is synchronized with the RTC by using a dedicated radio API when the device radio is turned on or off. This ensures that for a network stack, the radio timer seems to always be running when the radio is enabled. The radio timer is in most cases used indirectly through the trigger time fields in the radio APIs and should only be used when running the accurate 48 MHz high frequency crystal is the source of SCLK_HF.
- **Watchdog timer**

  The watchdog timer is used to regain control if the system operates incorrectly due to software errors. It is typically used to generate an interrupt to and reset of the device for the case where periodic monitoring of the system components and tasks fails to verify proper functionality. The watchdog timer runs on a 1.5 MHz clock rate and cannot be stopped once enabled. The watchdog timer pauses to run in Standby power mode and when a debugger halts the device.

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9.7 Serial Peripherals and I/O

The SSI is a synchronous serial interface that is compatible with SPI, MICROWIRE, and TI's synchronous serial interfaces. The SSI support both SPI master and slave up to 4 MHz. The SSI module support configurable phase and polarity.

The UART implement universal asynchronous receiver and transmitter functions. It support flexible baud-rate generation up to a maximum of 3 Mbps.

The I^2S interface is used to handle digital audio and can also be used to interface pulse-density modulation microphones (PDM).

The I^2C interface is also used to communicate with devices compatible with the I^2C standard. The I^2C interface can handle 100 kHz and 400 kHz operation, and can serve as both master and slave.

The I/O controller (IOC) controls the digital I/O pins and contains multiplexer circuitry to allow a set of peripherals to be assigned to I/O pins in a flexible manner. All digital I/Os are interrupt and wake-up capable, have a programmable pullup and pulldown function, and can generate an interrupt on a negative or positive edge (configurable). When configured as an output, pins can function as either push-pull or open-drain. Five GPIOs have high-drive capabilities, which are marked in **bold** in Section 7. All digital peripherals can be connected to any digital pin on the device.

For more information, see the CC13x1x3, CC26x1x3 SimpleLink™ Wireless MCU Technical Reference Manual.

9.8 Battery and Temperature Monitor

A combined temperature and battery voltage monitor is available in the CC2651P3 device. The battery and temperature monitor allows an application to continuously monitor on-chip temperature and supply voltage and respond to changes in environmental conditions as needed. The module contains window comparators to interrupt the system CPU when temperature or supply voltage go outside defined windows. These events can also be used to wake up the device from Standby mode through the Always-On (AON) event fabric.

9.9 µDMA

The device includes a direct memory access (µDMA) controller. The µDMA controller provides a way to offload data-transfer tasks from the system CPU, thus allowing for more efficient use of the processor and the available bus bandwidth. The µDMA controller can perform a transfer between memory and peripherals. The µDMA controller has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory when the peripheral is ready to transfer more data.

Some features of the µDMA controller include the following (this is not an exhaustive list):

- Highly flexible and configurable channel operation of up to 32 channels
- Transfer modes: memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral
- Data sizes of 8, 16, and 32 bits
- Ping-pong mode for continuous streaming of data

9.10 Debug

The on-chip debug support is done through a dedicated cJTAG (IEEE 1149.7) or JTAG (IEEE 1149.1) interface. The device boots by default into cJTAG mode and must be reconfigured to use 4-pin JTAG.

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9.11 Power Management

To minimize power consumption, the CC2651P3 supports a number of power modes and power management features (see Table 9-1).

Table 9-1. Power Modes

MODE	SOFTWARE CONFIGURABLE POWER MODES				RESET PIN HELD
	ACTIVE	IDLE	STANDBY	SHUTDOWN	
CPU	Active	Off	Off	Off	Off
Flash	On	Available	Off	Off	Off
SRAM	On	On	Retention	Off	Off
Supply System	On	On	Duty Cycled	Off	Off
Register and CPU retention	Full	Full	Partial	No	No
SRAM retention	Full	Full	Full	No	No
48 MHz high-speed clock (SCLK_HF)	XOSC_HF or RCOSC_HF	XOSC_HF or RCOSC_HF	Off	Off	Off
32 kHz low-speed clock (SCLK_LF)	XOSC_LF or RCOSC_LF	XOSC_LF or RCOSC_LF	XOSC_LF or RCOSC_LF	Off	Off
Peripherals	Available	Available	Off	Off	Off
Wake-up on RTC	Available	Available	Available	Off	Off
Wake-up on pin edge	Available	Available	Available	Available	Off
Wake-up on reset pin	On	On	On	On	On
Brownout detector (BOD)	On	On	Duty Cycled	Off	Off
Power-on reset (POR)	On	On	On	Off	Off
Watchdog timer (WDT)	Available	Available	Paused	Off	Off

In **Active** mode, the application system CPU is actively executing code. Active mode provides normal operation of the processor and all of the peripherals that are currently enabled. The system clock can be any available clock source (see Table 9-1).

In **Idle** mode, all active peripherals can be clocked, but the Application CPU core and memory are not clocked and no code is executed. Any interrupt event brings the processor back into active mode.

In **Standby** mode, only the always-on (AON) domain is active. An external wake-up event or RTC event is required to bring the device back to active mode. MCU peripherals with retention do not need to be reconfigured when waking up again, and the CPU continues execution from where it went into standby mode. All GPIOs are latched in standby mode.

In **Shutdown** mode, the device is entirely turned off (including the AON domain), and the I/Os are latched with the value they had before entering shutdown mode. A change of state on any I/O pin defined as a *wake from shutdown pin* wakes up the device and functions as a reset trigger. The CPU can differentiate between reset in this way and reset-by-reset pin or power-on reset by reading the reset status register. The only state retained in this mode is the latched I/O state and the flash memory contents.

Note

The power, RF and clock management for the CC2651P3 device require specific configuration and handling by software for optimized performance. This configuration and handling is implemented in the TI-provided drivers that are part of the CC2651P3 software development kit (SDK). Therefore, TI highly recommends using this software framework for all application development on the device. The complete SDK with TI-RTOS (optional), device drivers, and examples are offered free of charge in source code.

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9.12 Clock Systems

The CC2651P3 device has several internal system clocks.

The 48 MHz SCLK_HF is used as the main system (MCU and peripherals) clock. This can be driven by the internal 48 MHz RC Oscillator (RCOSC_HF) or an external 48 MHz crystal (XOSC_HF). Radio operation requires an external 48 MHz crystal.

SCLK_LF is the 32.768 kHz internal low-frequency system clock. It can be used for the RTC and to synchronize the radio timer before or after Standby power mode. SCLK_LF can be driven by the internal 32.8 kHz RC Oscillator (RCOSC_LF), a 32.768 kHz watch-type crystal, or a clock input on any digital IO.

When using a crystal or the internal RC oscillator, the device can output the 32 kHz SCLK_LF signal to other devices, thereby reducing the overall system cost.

9.13 Network Processor

Depending on the product configuration, the CC2651P3 device can function as a wireless network processor (WNP - a device running the wireless protocol stack with the application running on a separate host MCU), or as a system-on-chip (SoC) with the application and protocol stack running on the system CPU inside the device.

In the first case, the external host MCU communicates with the device using SPI or UART. In the second case, the application must be written according to the application framework supplied with the wireless protocol stack.

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10 Application, Implementation, and Layout

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

For general design guidelines and hardware configuration guidelines, refer to CC13xx/CC26xx Hardware Configuration and PCB Design Considerations Application Report.

For optimum RF performance, especially when using the high-power PA, it is important to accurately follow the reference design with respect to component values and layout. Failure to do so may lead to reduced RF performance due to balun mismatch. The amplitude- and phase balance through the balun must be <1 dB and <6 degrees, respectively.

PCB stack-up is also critical for proper operation. The CC2651P3 EVMs and characterization boards use a finished thickness between the top layer (RF signals) and layer 2 (ground plane) of 175 µm. It is very important to use the same substrate thickness, or slightly thicker, in an end product implementing the CC2651P3 device.

10.1 Reference Designs

The following reference designs should be followed closely when implementing designs using the CC2651P3 device.

Special attention must be paid to RF component placement, decoupling capacitors and DCDC regulator components, as well as ground connections for all of these.

CC26x1-P3EM-5XS24-PA24_10dBm Design Files	The CC26x1PEM-5XS24-PA24_10dBm reference design provides schematic, layout and production files for the characterization board used for deriving the performance number found in this document. This design is optimized for operating the high power PA at 10 dBm output power and is using a single-ended front-end configuration with external LNA bias for RX.
CC26x1-P3EM-7XD24-PA24 Design Files	The CC26x1-P3EM-7XD24-PA24 reference design provides schematic, layout and production files for the characterization board used for deriving the performance number found in this document. This design is configured for 20 dBm operation on the high output power PA.
LP-CC2651P3 Design Files	The CC2651P3 LaunchPad Design Files contain detailed schematics and layouts to build application specific boards using the CC2651P3 device.
Sub-1 GHz and 2.4 GHz Antenna Kit for LaunchPad™ Development Kit and SensorTag	The antenna kit allows real-life testing to identify the optimal antenna for your application. The antenna kit includes 16 antennas for frequencies from 169 MHz to 2.4 GHz, including: • PCB antennas • Helical antennas • Chip antennas • Dual-band antennas for 868 MHz and 915 MHz combined with 2.4 GHz The antenna kit includes a JSC cable to connect to the Wireless MCU LaunchPad Development Kits and SensorTags.

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11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed as follows.

11.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to all part numbers and/or date-code. Each device has one of three prefixes/identifications: X, P, or null (no prefix) (for example, XCC2651P3 is in preview; therefore, an X prefix/identification is assigned).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, *RGZ*).

For orderable part numbers of *CC2651P3* devices in the RGZ (7-mm x 7-mm) package type, see the *Package Option Addendum* of this document, the Device Information in Section 3, the TI website (www.ti.com), or contact your TI sales representative.

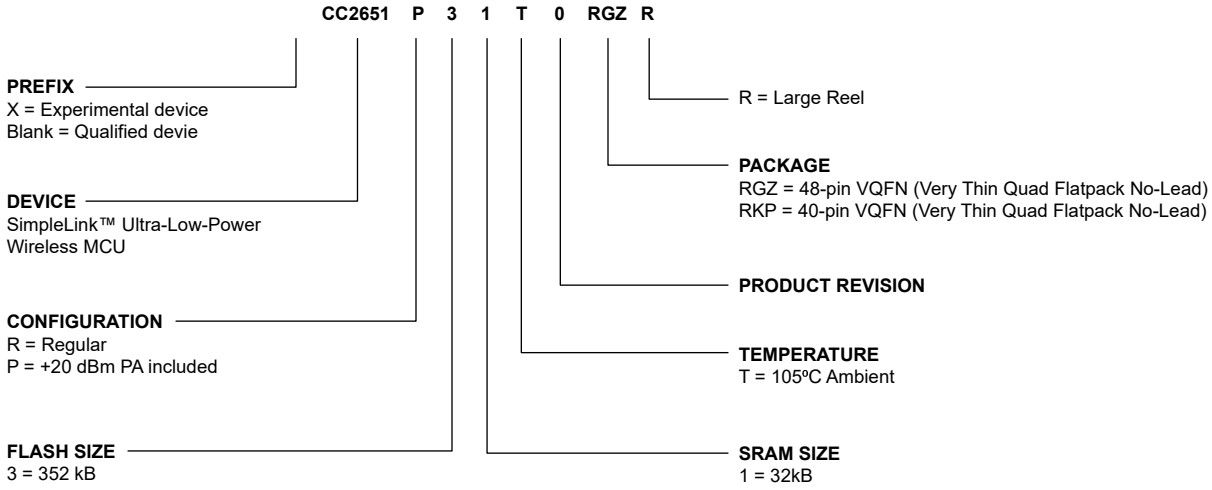

Figure 11-1. Device Nomenclature

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11.2 Tools and Software

The CC2651P3 device is supported by a variety of software and hardware development tools.

Development Kit

CC2651P3 LaunchPad™ Development Kit	The CC2651P3 LaunchPad™ Development Kit enables development of high-performance wireless applications that benefit from low-power operation. The kit features the CC2651P3 SimpleLink Wireless MCU, which allows you to quickly evaluate and prototype 2.4-GHz wireless applications such as Bluetooth 5 Low Energy, Zigbee and Thread, plus combinations of these. The kit works with the LaunchPad ecosystem, easily enabling additional functionality like sensors, display and more.

Software

SimpleLink™ CC13XX-CC26XX SDK

The SimpleLink CC13xx and CC26xx Software Development Kit (SDK) provides a complete package for the development of wireless applications on the CC13XX / CC26XX family of devices. The SDK includes a comprehensive software package for the CC2651P3 device, including the following protocol stacks:

- Bluetooth Low Energy 4 and 5.2
- Thread (based on OpenThread)
- Zigbee 3.0
- Wi-SUN®
- TI 15.4-Stack - an IEEE 802.15.4-based star networking solution for Sub-1 GHz and 2.4 GHz
- Proprietary RF - a large set of building blocks for building proprietary RF software
- Multiprotocol support - concurrent operation between stacks using the Dynamic Multiprotocol Manager (DMM)

The SimpleLink CC13XX-CC26XX SDK is part of TI's SimpleLink MCU platform, offering a single development environment that delivers flexible hardware, software and tool options for customers developing wired and wireless applications. For more information about the SimpleLink MCU Platform, visit http://www.ti.com/simplelink.

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Development Tools

Code Composer Studio™ Integrated Development Environment (IDE)

Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse® software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

CCS has support for all SimpleLink Wireless MCUs and includes support for EnergyTrace™ software (application energy usage profiling). A real-time object viewer plugin is available for TI-RTOS, part of the SimpleLink SDK.

Code Composer Studio is provided free of charge when used in conjunction with the XDS debuggers included on a LaunchPad Development Kit.

Code Composer Studio™ Cloud IDE

Code Composer Studio (CCS) Cloud is a web-based IDE that allows you to create, edit and build CCS and Energia™ projects. After you have successfully built your project, you can download and run on your connected LaunchPad. Basic debugging, including features like setting breakpoints and viewing variable values is now supported with CCS Cloud.

IAR Embedded Workbench® for Arm®

IAR Embedded Workbench® is a set of development tools for building and debugging embedded system applications using assembler, C and C++. It provides a completely integrated development environment that includes a project manager, editor, and build tools. IAR has support for all SimpleLink Wireless MCUs. It offers broad debugger support, including XDS110, IAR I-jet™ and Segger J-Link™. A real-time object viewer plugin is available for TI-RTOS, part of the SimpleLink SDK. IAR is also supported out-of-the-box on most software examples provided as part of the SimpleLink SDK.

A 30-day evaluation or a 32 KB size-limited version is available through iar.com.

SmartRF™ Studio

SmartRF™ Studio is a Windows® application that can be used to evaluate and configure SimpleLink Wireless MCUs from Texas Instruments. The application will help designers of RF systems to easily evaluate the radio at an early stage in the design process. It is especially useful for generation of configuration register values and for practical testing and debugging of the RF system. SmartRF Studio can be used either as a standalone application or together with applicable evaluation boards or debug probes for the RF device. Features of the SmartRF Studio include:

- Link tests - send and receive packets between nodes
- Antenna and radiation tests - set the radio in continuous wave TX and RX states
- Export radio configuration code for use with the TI SimpleLink SDK RF driver
- Custom GPIO configuration for signaling and control of external switches

CCS UniFlash

CCS UniFlash is a standalone tool used to program on-chip flash memory on TI MCUs. UniFlash has a GUI, command line, and scripting interface. CCS UniFlash is available free of charge.

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11.2.1 SimpleLink™ Microcontroller Platform

The SimpleLink microcontroller platform sets a new standard for developers with the broadest portfolio of wired and wireless Arm® MCUs (System-on-Chip) in a single software development environment. Delivering flexible hardware, software and tool options for your IoT applications. Invest once in the SimpleLink software development kit and use throughout your entire portfolio. Learn more on ti.com/simplelink.

11.3 Documentation Support

To receive notification of documentation updates on data sheets, errata, application notes and similar, navigate to the device product folder on ti.com/product/CC2651P3. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the MCU, related peripherals, and other technical collateral is listed as follows.

TI Resource Explorer

TI Resource Explorer	Software examples, libraries, executables, and documentation are available for your device and development board.

Errata

CC2651P3 Silicon Errata	The silicon errata describes the known exceptions to the functional specifications for each silicon revision of the device and description on how to recognize a device revision.

Application Reports

All application reports for the CC2651P3 device are found on the device product folder at: ti.com/product/CC2651P3/#tech-docs.

Technical Reference Manual (TRM)

CC13x1x, CC26x1x SimpleLink™ Wireless MCU TRM	The TRM provides a detailed description of all modules and peripherals available in the device family.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 Trademarks

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC2651P31T0RGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	CC2651 P31	Samples
CC2651P31T0RKPR	ACTIVE	VQFN	RKP	40	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	CC2651 P31	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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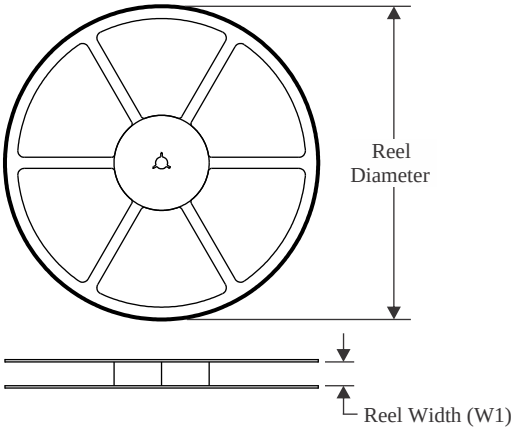
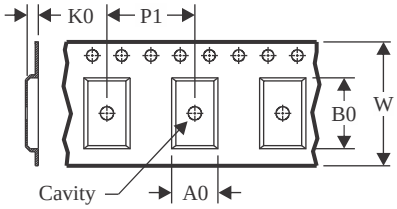
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

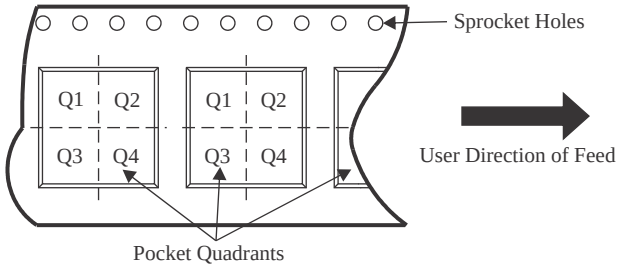


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

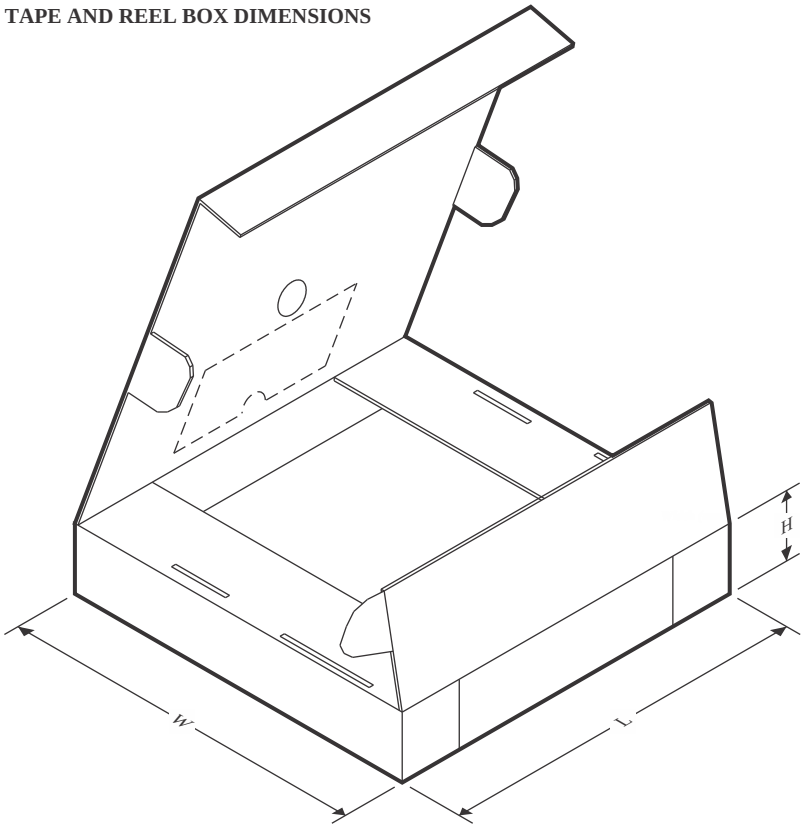
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC2651P31T0RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
CC2651P31T0RKPR	VQFN	RKP	40	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC2651P31T0RGZR	VQFN	RGZ	48	2500	367.0	367.0	35.0
CC2651P31T0RKPR	VQFN	RKP	40	3000	367.0	367.0	35.0

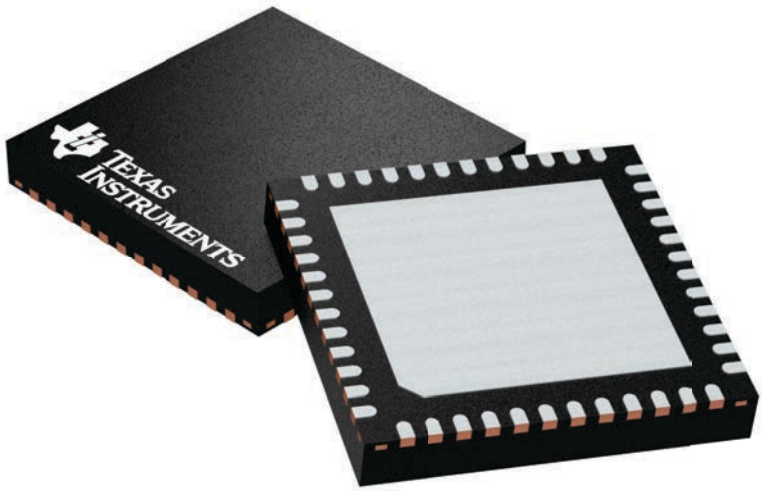
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

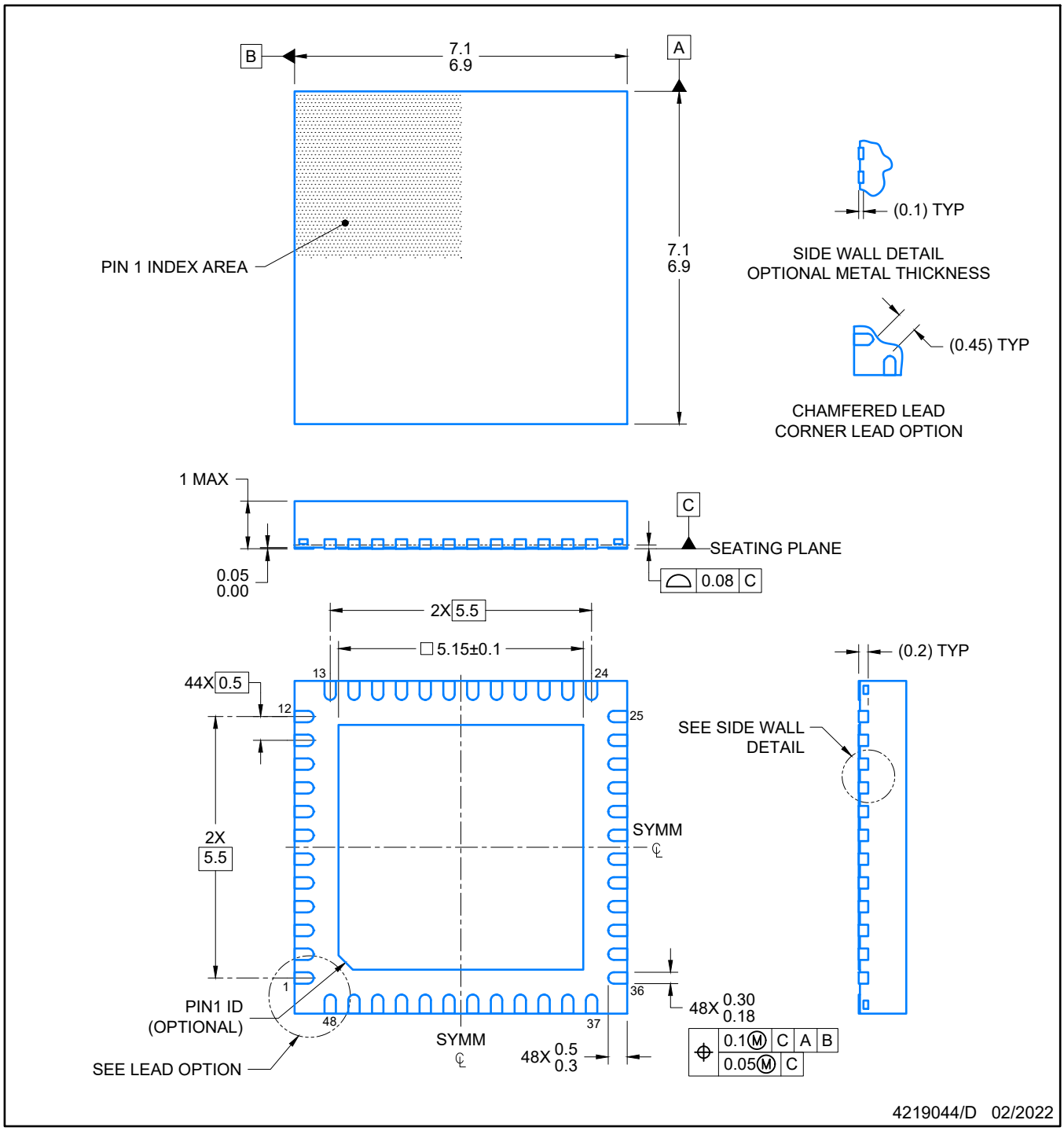
7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



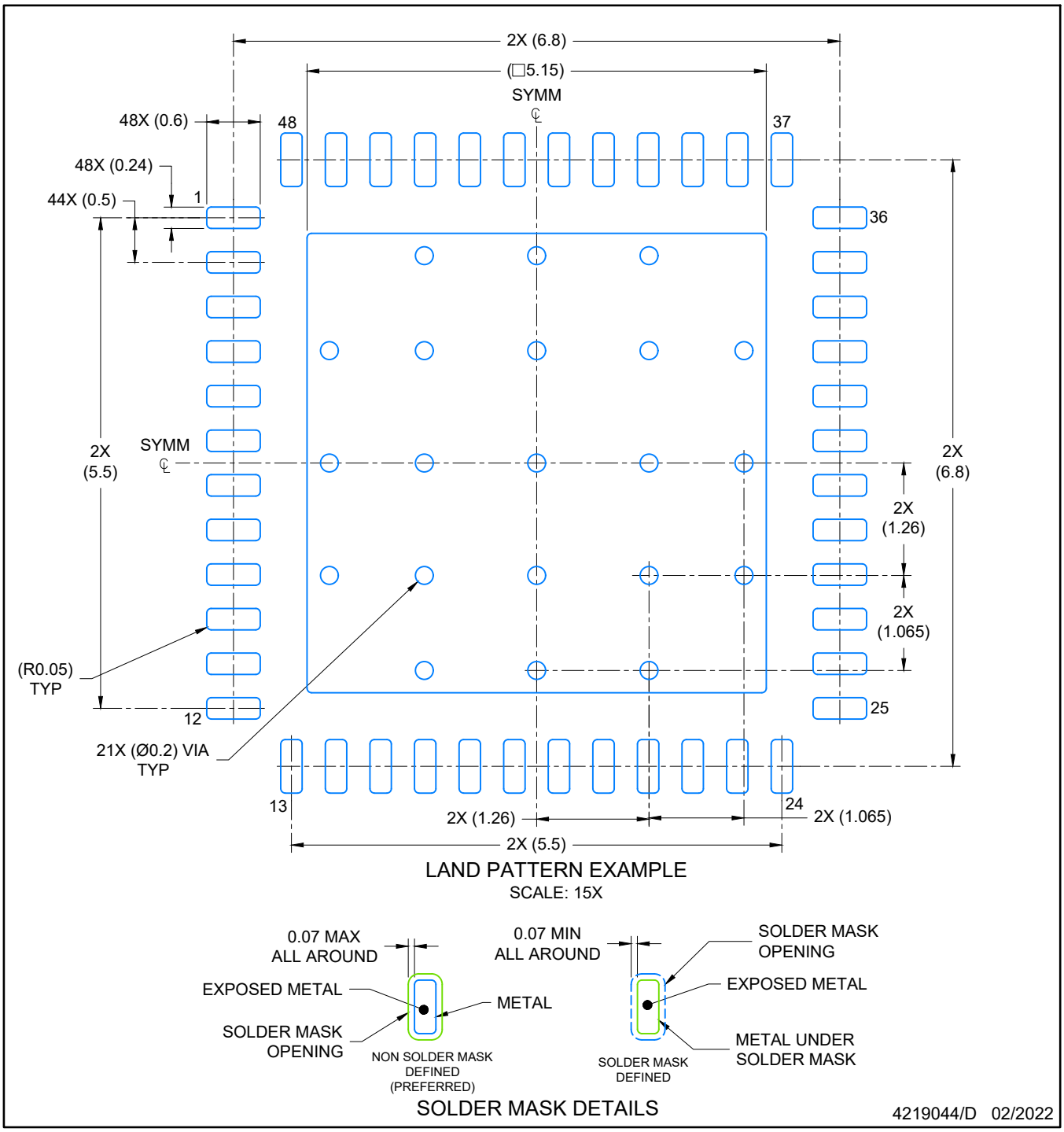
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224671/A



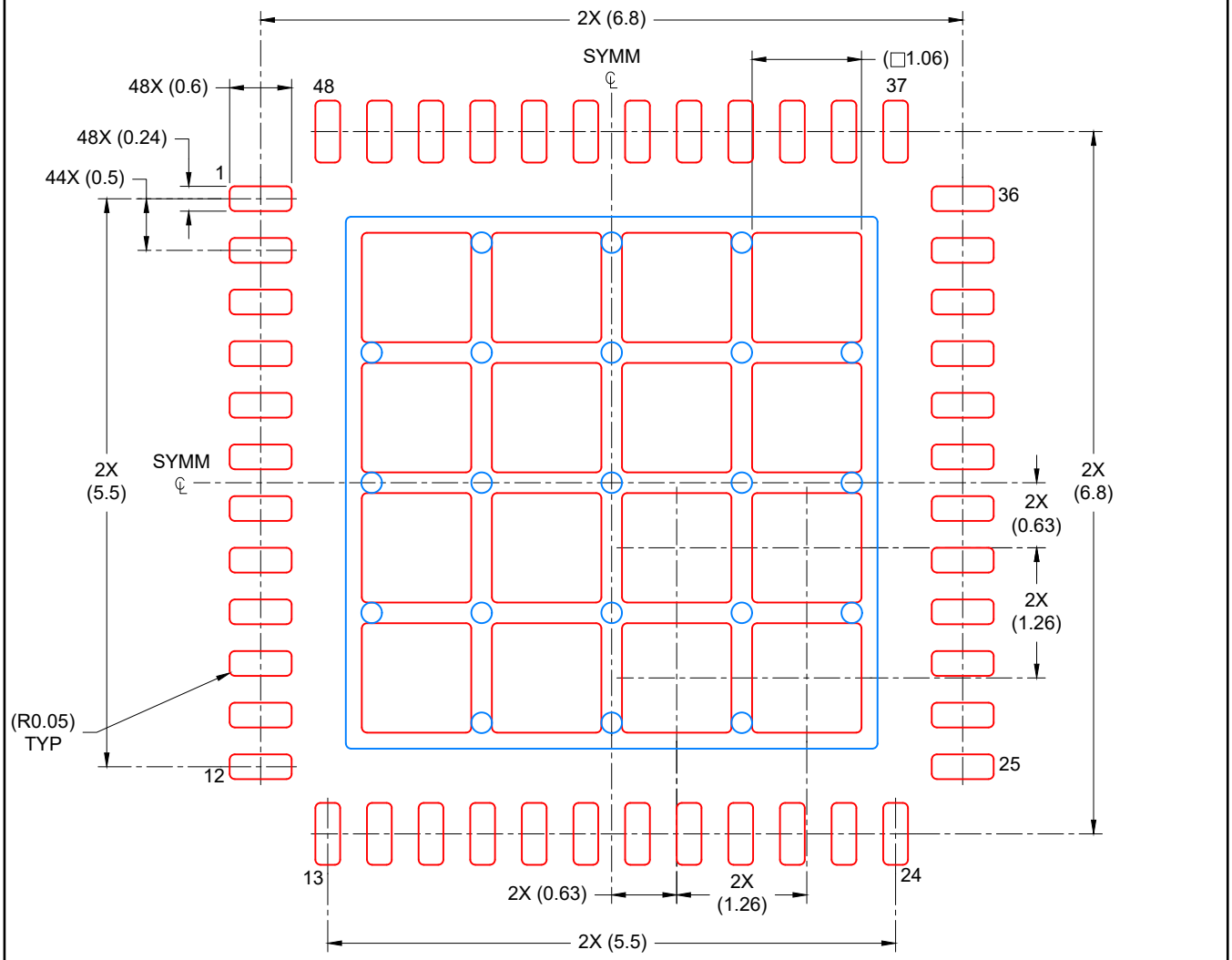
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
67% PRINTED COVERAGE BY AREA
SCALE: 15X

4219044/D 02/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

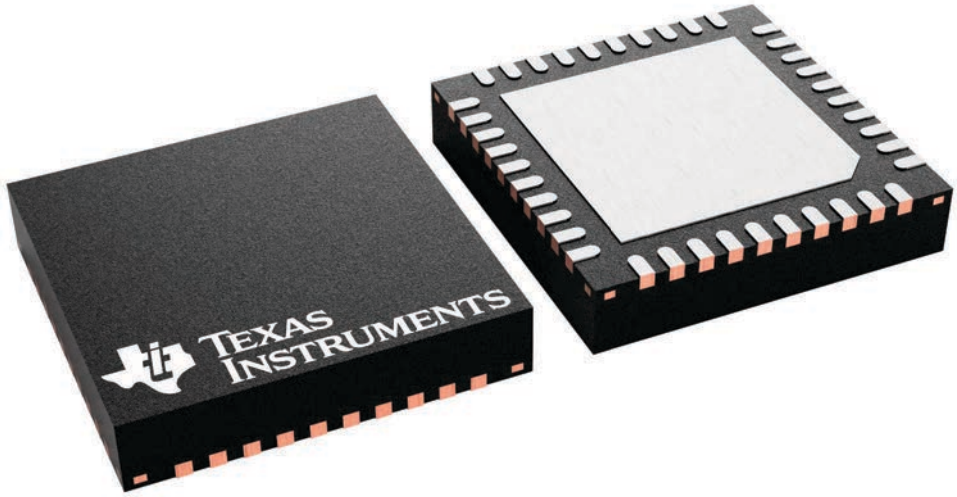
RKP 40

VQFN - 1 mm max height

5 x 5, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



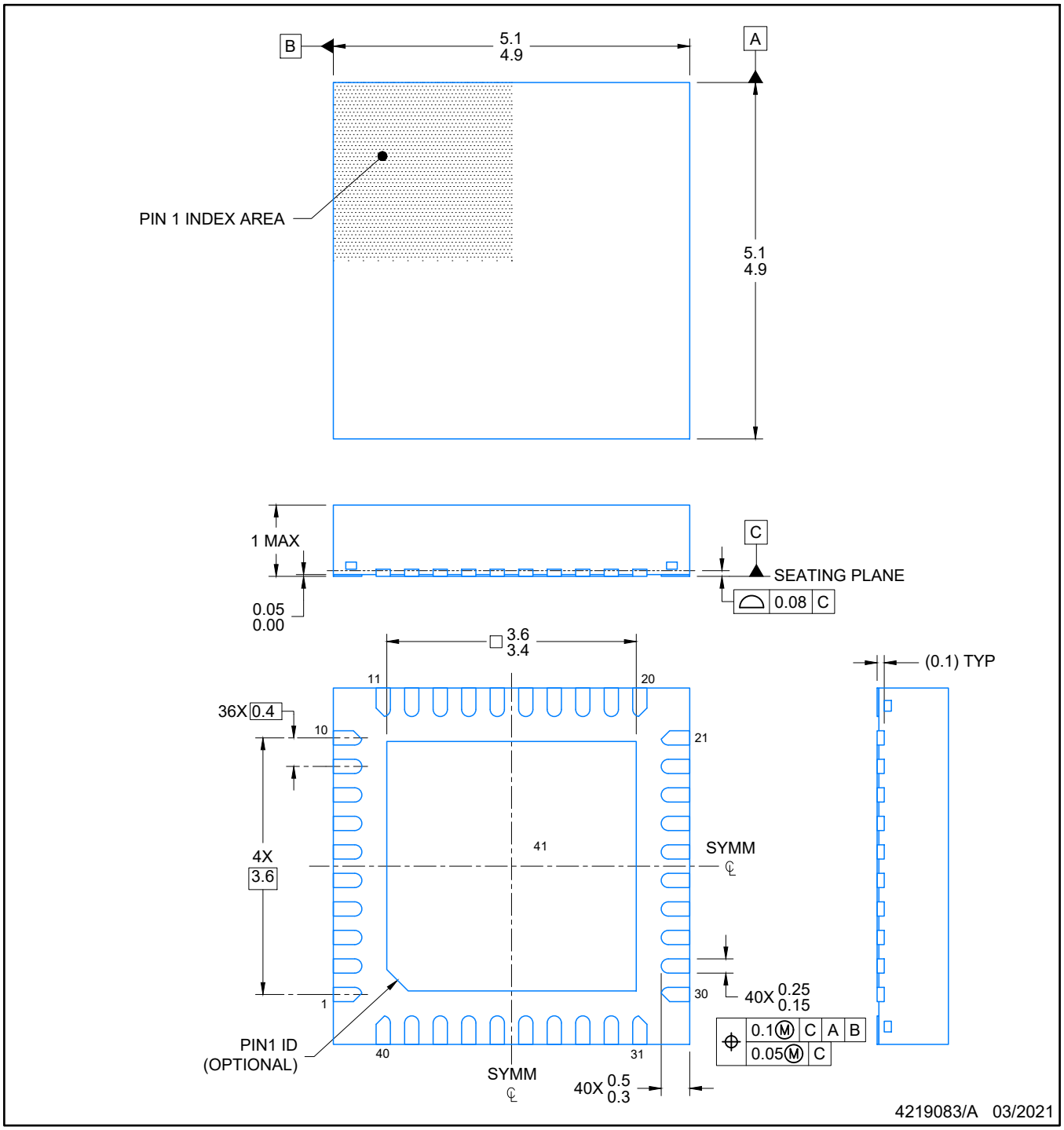
4229305/A

PACKAGE OUTLINE

RKP0040B

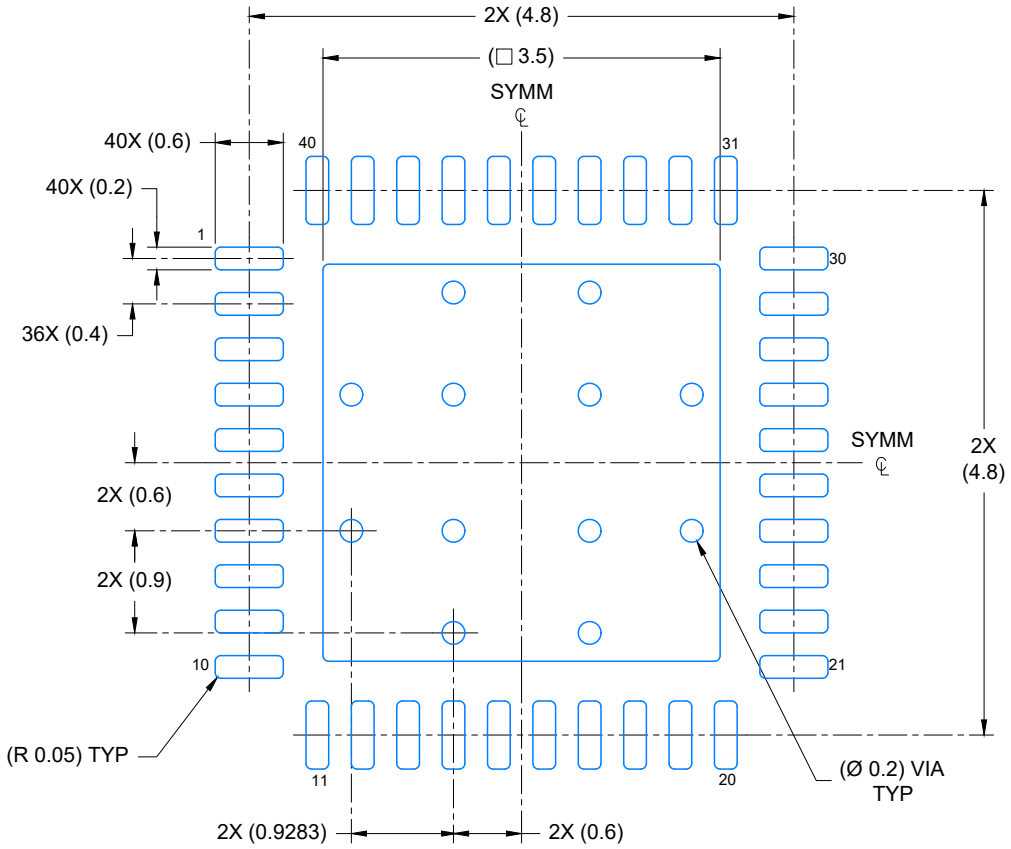
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD

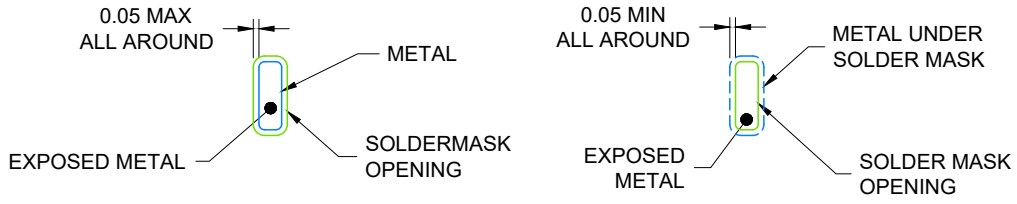


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON- SOLDER MASK DEFINED (PREFERRED)

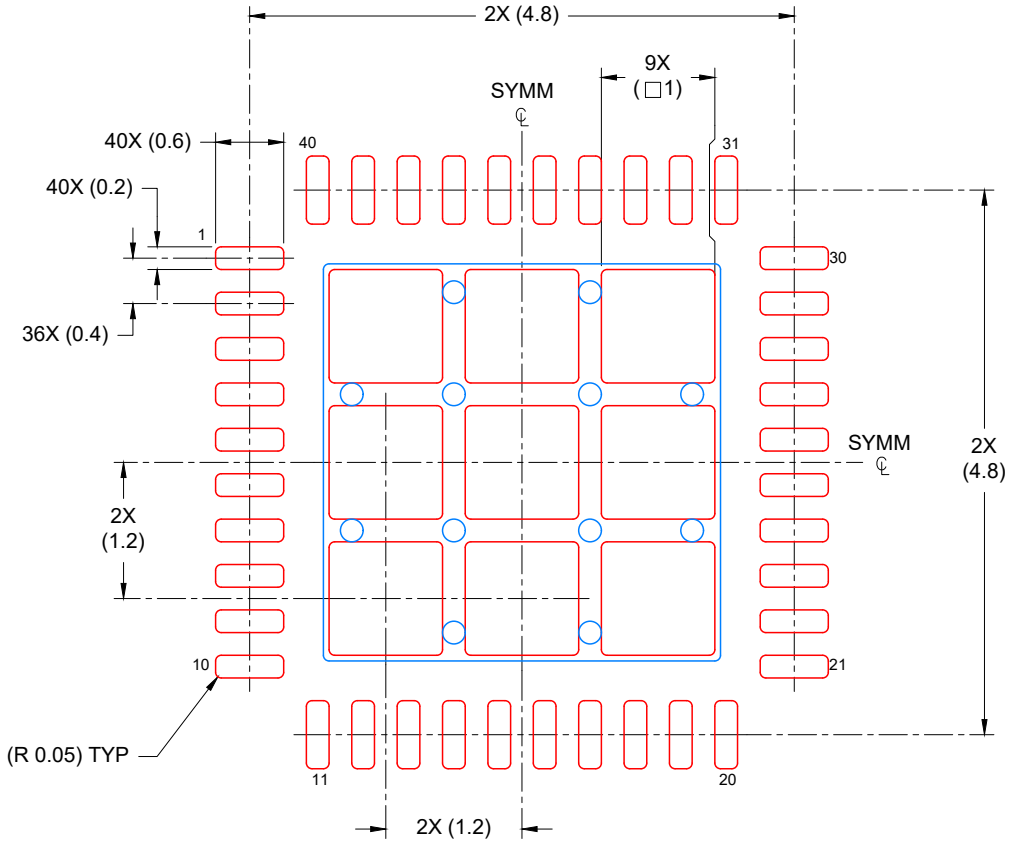
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4219083/A 03/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
74% PRINTED COVERAGE BY AREA
SCALE: 15X

4219083/A 03/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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