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## CC1000 Errata Note 001, rev. 1.0

**Switching between certain combinations of frequency words (FREQ) in CC1000 may cause the PLL never to be able to lock. This is most likely to occur in frequency hopping systems. A software fix solves the problem.**

### **Description and reason for the problem**

When a new frequency is selected by updating the FREQ registers or changing the MAIN.F\_REG bit, a non-valid value can be latched due to internal clock skew. This non-valid value may put the PLL in a deadlock situation and prevent the PLL from locking.

The deadlock situation can happen if the 3 most significant bits of the FREQ words are different for the two frequencies. If the 3 most significant bits are equal, the deadlock will not occur. To ensure that the most significant bits are equal, use the same reference frequency divider value (REFDIV) for all channels.

### **Suggested workarounds**

#### Alternative 1:

As the problem only rise when the MSBs of the FREQ words are different, the first solution is to select the same reference frequency divider value (REFDIV) for all channels. Using a crystal frequency of 14.7456 MHz or above make it possible to generate 50 channels with the same REFDIV value, see AN011.

#### Alternative 2:

If the three MSBs of the FREQ words cannot be made the same for all channels, a software workaround must be used.

#### Alternative 2a:

The general software workaround is to write a “safe” frequency value to the FREQ register before the new frequency is written. The “safe” frequency word is FREQ\_2A (or FREQ\_2B) = E0h. This workaround involves only one additional write operation:

This is the suggestion for a software workaround:

1. Write FREQ\_2A (register 01h) = E0h. (Presuming that frequency A is used.)
2. Write new frequency word to FREQ\_A, or set MAIN.F\_REG = 1 in order to swap the frequency word and use FREQ\_B.

#### Alternative 2b:

An alternative software workaround is to reset the frequency synthesiser. After the new frequency word is programmed, the FS\_RESET\_N bit must be toggled by writing to the FSCTRL register, first setting the bit low, then high. This means two write operations to the register.

This is the suggestion for a software workaround:

1. Write new frequency word to FREQ\_A or FREQ\_B
2. First write FSCTRL (register 13h) = 00h
3. Then write FSCTRL (register 13h) = 01h

**Fix**

This problem is solved by a software workaround.

**Batches affected**

This errata note applies to all chip batches and revisions of the chip.

**CHIPCON,**

Tel. +47-22958544, Fax +47-22958546

[www.chipcon.com](http://www.chipcon.com)

[wireless@chipcon.com](mailto:wireless@chipcon.com)

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Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265

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