FIFO Solutions for Increasing Clock Rates and Data Widths

First-In, First-Out Technology

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SZZA001A

TEXAS INSTRUMENTS

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Introduction

Steady increases in microprocessor operating frequencies and bus widths over recent years have challenged system designers to find FIFO memories that meet their needs. To assist the designer, new FIFOs from Texas Instruments (TI) are available with features that complement these microprocessor trends.

Higher data-transfer rates have dictated the need for FIFOs to evolve into *clocked* architecture wherein data is moved in and out of the device with synchronous controls. Each synchronous control of the clocked FIFO uses enable signals that synchronize the data exchange to a *free-running* (continuous) clock.

Since the continuous clocks on each port of a clocked FIFO can operate asynchronously to each other, internal status signals indicating when the FIFO is empty or full can change with respect to either clock. To use a status signal for port control, it is synchronized to the port's clock on a clocked FIFO. Synchronization of these signals with flip-flops introduces metastability failures that increase with clock frequency. TI uses two-stage flag synchronization to greatly improve reliability.

Higher clock frequencies augment raw speed, but greater bandwidth is also achieved by increasing the data width. Wider datapaths can have the associated cost of large board area due to increased package sizes. New compact packages for TI's FIFOs reduce this cost.

Clocked FIFOs

Clocked FIFOs have become popular for relieving bottlenecks in high-speed data traffic. Data transfers for many systems are synchronized to a central clock with read and write enables. These free-running clocks can be input directly to a clocked FIFO with the same enables controlling its data transfer on the low-to-high transition of the clock.

Reducing the number of clocks keeps the interface simple and easy to manage. Extra logic is needed to produce a gated pulse when using a FIFO that accepts a clock only for a data transfer request. The generated clock signal is a derivative of the master clock with a margin of timing uncertainty. At high clock frequencies, this timing uncertainty is not tolerable and costly adjustments are needed.

Additional logic also is conserved by implementing flag synchronization on the clocked FIFO. Tracking is done to generate flags that indicate when the memory is empty or full. In many applications, the input and output to the FIFO are asynchronous and the flag signals must be synchronized for use as control. A read is not completed on the FIFO if no data is ready, so the $\overline{\text{EMPTY}}$ signal is synchronized to the read clock. This synchronous output-ready (OR) flag is useful for controlling read operations. Likewise, the $\overline{\text{FULL}}$ signal is synchronized to the write clock, producing the input-ready (IR) flag.

Flag Synchronization

As previously explained, one of the advantages of the clocked FIFO is the on-board synchronization of the $\overline{\text{EMPTY}}$ and $\overline{\text{FULL}}$ status flags when the input and output are asynchronous. In one method of synchronization, a single flip-flop captures the asynchronous flag's value (see Figure 1). With this method, the rising transition of data can violate the flip-flop's setup time and produce a metastable event (metastability is a malfunction of a flip-flop wherein the latch hangs between high and low states for an indefinite period of time).

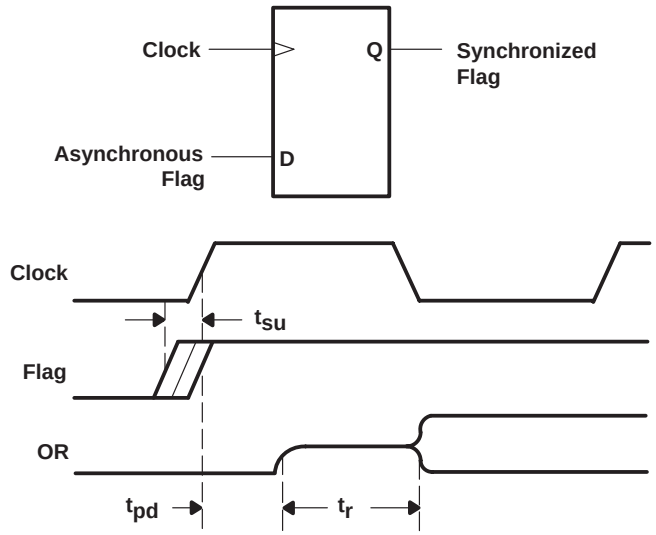


Figure 1. Triggering a Metastable Event With a One-Stage Synchronizer

Once a metastable event is triggered, the probability of the output recovering to a high or low level increases exponentially with increased resolve time (t_r). The expected time until the output of a single flip-flop with asynchronous data has a metastable event that lasts t_r or longer is characterized by the following mean time between failures (MTBF) equation:

$$MTBF_1 = \frac{\exp\left(\frac{t_r}{\tau}\right)}{t_o\ f_c\ f_d}$$

Where:

t_o = flip-flop constant representing the time window during which changing data invokes a failure
t_r = resolve time allowed in excess of the normal propagation delay
t = flip-flop constant related to the settling time of a metastable event
f_c = clock frequency
f_d = asynchronous data frequency. For OR-flag analysis, it is the frequency at which data is written to empty memory. For IR-flag analysis, it is the frequency at which data is read from full memory.

The MTBF decreases as clock and data frequency increase and as the time allowed for a metastable event to settle (t_r) decreases.

Metastability failures are a formidable issue for short-clock cycle times. Increasing the clock frequency linearly increases the number of metastable events triggered, but the shortened available resolve time exponentially increases the failure rate. It is impossible to eliminate the possibility of a metastable event under these conditions, but solutions exist to reliably increase the expected time between failures.

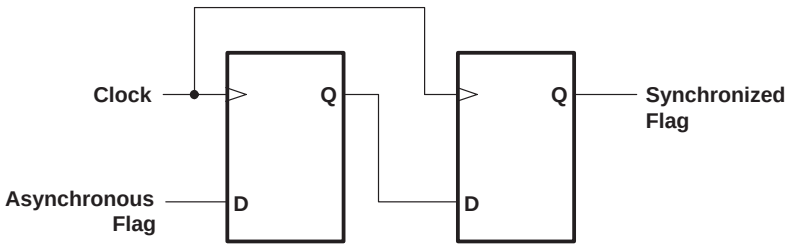


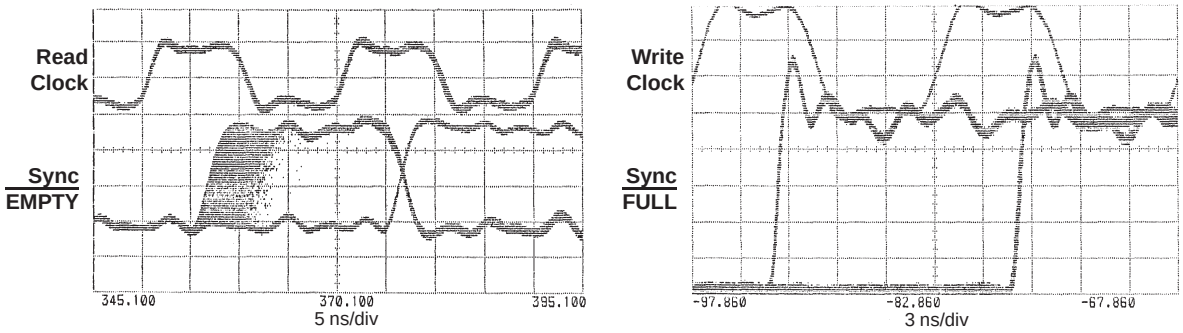
Figure 2. Two-Stage Synchronizer

TI increases the metastable MTBF by several orders of magnitude for IR and OR flags by employing two-stage synchronization (see Figure 2). For the output of the second stage to be metastable, the first stage must have a metastable event that lingers until it encroaches upon the setup time of the second stage. Adding another stage to a single flip-flop synchronizer is statistically equivalent to increasing its resolve time by the clock period minus its propagation delay. The mean time between failures for a two-stage synchronizer is given by:

$$MTBF_2 = \frac{\exp\left(\frac{t_r + \frac{1}{f_c} - t_p}{\tau}\right)}{t_o \; f_c \; f_d}$$

Where:

t_p = propagation delay of the first flip-flop



f_c = 50 MHz, f_d = 5 MHZ, V_{CC} = 5 V

(a) ONE-STAGE SYNCHRONIZATION

f_c = 66.7 MHz, f_d = 6.7 MHz, V_{CC} = 5 V

(b) TWO-STAGE SYNCHRONIZATION

Figure 3. Storage Oscilloscope Plots Taken Over a 15-Hour Duration

Figure 3 compares the two synchronization methods previously discussed. Both plots were taken at room temperature and nominal V_{CC} while each data transition violated setup time. Figure 3(a) shows the performance of an $\overline{\text{EMPTY}}$ flag synchronizer using only one flip-flop, while Figure 3(b) is the IR flag of an SN74ACT7807 with the write clock operating at maximum frequency.

Compact Packaging

Microprocessor bus widths have continuously doubled every few years to maximize their performance. Bus widths of 32 and 64 bits are commonplace today, whereas they were almost unheard of a few years ago. The downside to the increased bit count is that each subordinate device in the system must match this width with corresponding increases in board size.

New shrink packages for TI's clocked FIFOs provide a solution to this problem. Multiple-byte datapaths can be buffered while covering only a fraction of the area of conventional packages. These new FIFO packages are presently available in 56-, 64-, and 80-pin configurations. Dubbed shrink quad flat package (SQFP), the 64-pin package is used for 9-bit-wide FIFOs, and the 80-pin package is used for 18-bit-wide FIFOs. Both SQFP packages have a lead pitch of 0.5 mm. The 56-pin shrink small-outline package has a 0.025-inch lead pitch and also houses 18-bit-wide FIFOs. A variety of TI's FIFOs are offered in these new packages (see Table 1).

Table 1. FIFOs Available in Space-Efficient Packages

DEVICE	CLOCKED	ORGANIZATION	CLOCK CYCLE TIME (ns)	PACKAGES
SN74ACT2235	No	1K × 9 × 2	20, 30 40, 50	64 TQFP 44 PLCC
SN74ACT7802	No	1K × 18	25, 40, 60	80 TQFP 68 PLCC
SN74ACT7811	Yes	1K × 18	15, 18, 20, 25	80 TQFP 68 PLCC
SN74ACT7803 SN74ACT7805 SN74ACT7813	Yes	512 × 18 256 × 18 64 × 18	15, 20, 25, 40	56 SSOP
SN74ACT7804 SN74ACT7806 SN74ACT7814	No	512 × 18 256 × 18 64 × 18	20, 25, 40	56 SSOP
SN74ACT7807	Yes	2K × 9	15, 20, 25, 40	64 TQFP 44 PLCC
SN74ACT7808	No	2K × 9	20, 25, 30, 40	64 TQFP 44 PLCC

Figure 4 compares the space savings of the new compact packages compared to competitive surface-mount solutions. A 4-byte path constructed with four clocked FIFOs in 32-pin PLCC packages occupies 1.16 in^2, while two 56-pin SSOP packages occupy only 0.59 in^2.

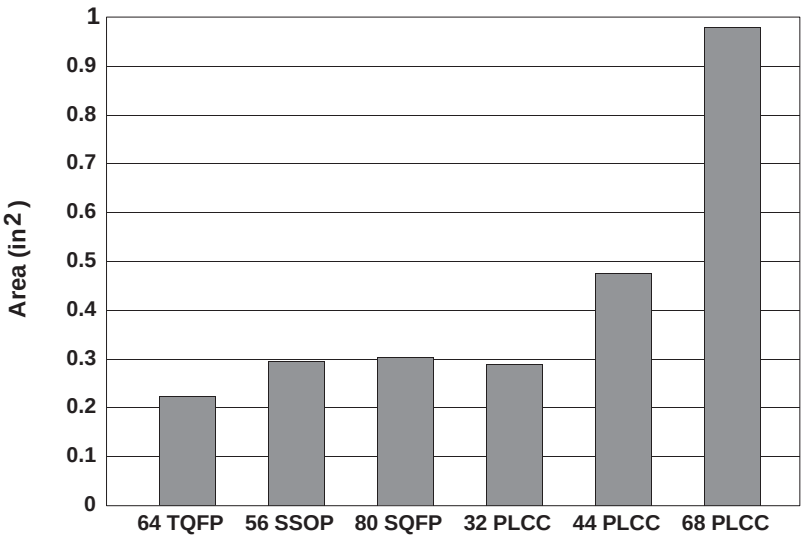


Figure 4. Surface-Mount Package Area Comparison

New Clocked FIFOs

Four new CMOS clocked FIFOs from TI offer a variety of memory depths. All four can match applications that require maximum clock frequencies of 67 MHz and access times of 12 ns. Suited for buffering long packets, the 2K × 9 SN74ACT7807 is the deepest of the four and is available in the 44-pin PLCC or 64-pin TQFP. The SN74ACT7803, SN74ACT7805, and SN74ACT7813 are organized as 512 × 18, 256 × 18, and 64 × 18, respectively, and have the same pin arrangement in the 56-pin SSOP. Every TI clocked FIFO is easily expanded in word width, and the SN74ACT7803/05/13 can also be arranged to form a bidirectional FIFO. With the two FIFOs connected as in Figure 5, no extra logic is needed for bidirectional operation.

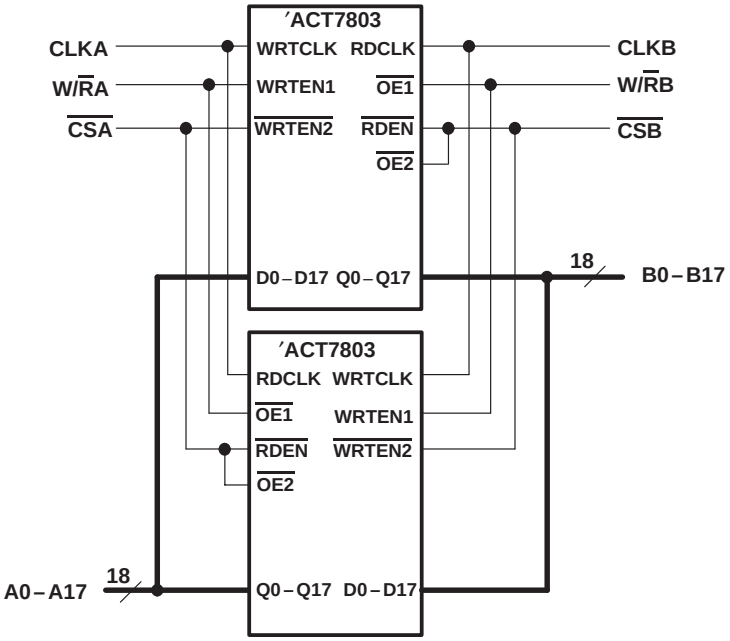


Figure 5. Bidirectional Configuration for the SN74ACT7803

Silicon is currently available for a bidirectional clocked FIFO fabricated in TI's Advanced BiCMOS (ABT) process. The SN74ABT7819 is organized as 512 × 18 × 2 with two internal independent FIFOs. Each port has a continuous free-running clock, a chip select ($\overline{CS}$), a read/write select ($\overline{R}$/W), and two separate read and write enables for control. It supports clock frequencies in excess of 80 MHz and a maximum access time below 10 ns. This device is packaged in the 80-pin QFP and 80-pin SQFP.

Conclusion

Several semiconductor manufacturers, including TI, have responded to customer needs by providing clocked FIFOs whose synchronous interfaces conform to the requirements of many high-performance systems. Capitalizing on the available continuous system clocks, this architecture limits the amount of necessary glue logic and the number of timing constraints.

Flag synchronization is important for clocked FIFOs buffering between asynchronous systems. Flip-flop synchronizers used for this task have a metastable failure rate that grows exponentially with clock frequency. TI employs two stages of synchronization that improve the flags' reliability significantly.

Finally, providing a FIFO buffer for wide buses has historically consumed large amounts of board area. Designers seeking relief from this problem can find it in the packaging options offered for TI's FIFOs. Used to house 9- and 18-bit devices, these packages require only about 50% of the space required for conventional surface-mount packages.