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Input and Output Characteristics of Digital Integrated Circuits at 3.3-V Supply Voltage

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Abstract

This application report contains a comprehensive collection of the input- and output-characteristic curves of integrated circuits from various 3.3-V logic families. These curves go beyond the information given in data sheets by providing additional details regarding the characteristics of the components. This knowledge is particularly useful when, for example, a decision must be made as to which circuit should be used in a bus system, or when the waveforms that can be expected in a transmission system must be predicted using a Bergeron chart. These oscillograms are of great assistance when generating models for simulation programs that analyze the dynamic behavior of the integrated circuits in a particular environment.

1 Introduction

The parameters given in the data sheets of integrated circuits can give only a very limited indication of their behavior in a system. Generally, data sheets give only information regarding the behavior over the input and output (I/O) voltage range of 0 to 3.3 V. Even the output currents specified over this range provide an incomplete picture of in-system performance.

Behavior of integrated circuits outside the usually accepted operating conditions often is of interest. This is, for example, the situation when the characteristic curves need to be used to predict the signal waveforms resulting from line reflections.

Along with the I/O characteristics, use of the Bergeron method, and knowledge of the load resistor, the amplitude of the line reflections can be determined.

Many modern logic families are specified at different voltage nodes, for example the AHC logic, and can be used at 5-V, 3.3-V, or even at 2.5-V supply voltage.

Since three main voltage nodes currently are used, it is necessary to provide I/O-characteristics at these different voltage levels. This report deals exclusively with devices operated at 3.3-V supply voltage.

Two other application reports regarding this topic are available:

- *Input and Output Characteristics of Digital Integrated Circuits at 5-V Supply Voltage*, literature number SZZA008
- *Input and Output Characteristics of Digital Integrated Circuits at 2.5-V Supply Voltage*, literature number SZZA012

In view of the wide range of integrated circuits that are available, it has been necessary to limit this information to typical characteristics only. In the second and third sections of this application report, the input and output characteristics of the following circuits have been shown as being representative of other components that behave similarly in circuit:

’00	The characteristic curves of this NAND gate are given as representative of all logic circuits having normal drive capability, such as gates, flip-flops, counters, multiplexers, etc.
’240/’244	The output characteristics of these bus-interface circuits are of particular importance when a decision must be made as to which circuit family should be used for a specific system requirement. The available output current has a decisive influence on the distortion of signals on bus lines.
’16240/’16244	The output characteristics of these bus-interface devices correspond with the ’240/’244 functions regarding the electrical behavior. However, these devices support 16 drivers within one package. This meets the market requirements, because modern designs are based on wider buses, using 16 bits, 32 bits, or more bits on the backplanes. Further, the noise behavior of the Widebus™ shows a significant improvement versus the standard octal packages.

Representatives of the different logic families (see Table 1) give an overview of the input and output characteristics, which are presented in sections 2 and 3.

Table 1. Representatives of the Different Logic Families

FAMILY	TYPE		
	’00	’240/’244	’16244
SN74AHC	√	√	
SN74AC	√	√	
SN74LV	√	√	
SN74LVC	√	√	
SN74ALVC			√
SN74ALB			√
SN74ALVT			√
SN74LVT		√	

Because the input characteristics depend exclusively on the technology used, not on the logical function of the device, only one representative per logic family is shown (gate function ’00 or driver function ’240) in the input-characteristics section.

Section 4 of this application report presents the calculation of line reflections using the Bergeron method. The calculation is done with the SN74ALVTH16244.

Measurement results demonstrating different switching behaviors of the various logic families are given in Section 5. For these measurements, the devices under test were loaded with a 1.3-m-long coaxial cable having a characteristic impedance of 50 Ω; the end of the line was not connected, i.e., open circuit. These waveforms provide good insight into the dynamic behavior of the devices.

2 Input Characteristics

The high impedance of the input stage of the logic circuit determines the input characteristics of logic circuits in the positive range.

In contrast to the 5-V logic families, all of the 3.3-V families have CMOS input stages. The technologies used are based on the CMOS or the BiCMOS manufacturing process. In both cases, CMOS input stages are used. CMOS input stages are controlled exclusively by the applied voltage, so there is no current flowing into the input stage. Therefore, the input impedance of CMOS and BiCMOS devices is in the megaohm range. Negative voltage peaks are limited by a protection diode.

The input stages of some CMOS and BiCMOS logic families (SN74AC, SN74ALB) also have an input protection diode connected to V_{CC}. This diode limits the positive input voltage to maximum V_{CC} + 0.7 V, but prohibits their use in mixed-voltage systems.

The bus-hold circuit represents a special input circuit that is implemented in the input stages of the LVT and ALVT logic families and is optionally available for the LVC and ALVC family devices.

Inputs of components that have the bus-hold circuit hold the last valid logic state. This feature is suitable in the case where an input stays undefined, e.g., during a high-impedance state on the bus. Using the bus-hold circuit eliminates the need for pullup or pulldown resistors.

Devices with the bus-hold circuit are designated by the ‘H’ in their part numbers, for example, SN74LVTH245.

A more detailed application report, *Bus-Hold Circuits*, literature number SDZAE15, is available from Texas Instruments (TI™).

A list of application reports and other literature is given in Section 7.

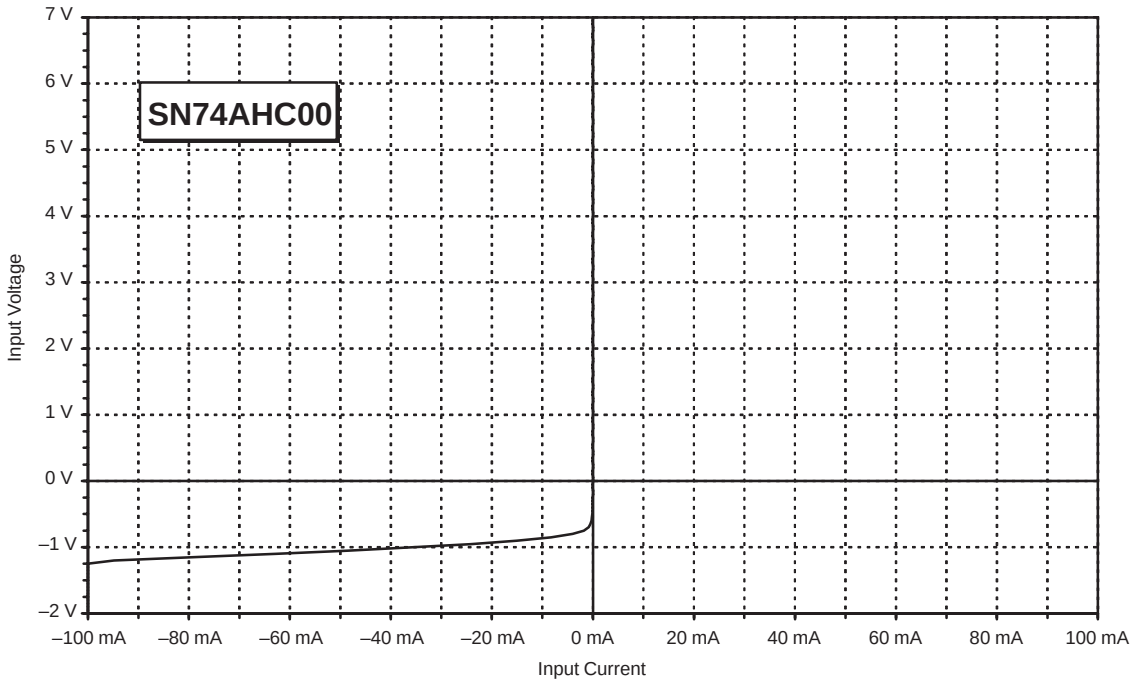

Figure 1. Input Characteristic of the SN74AHCxxx Series

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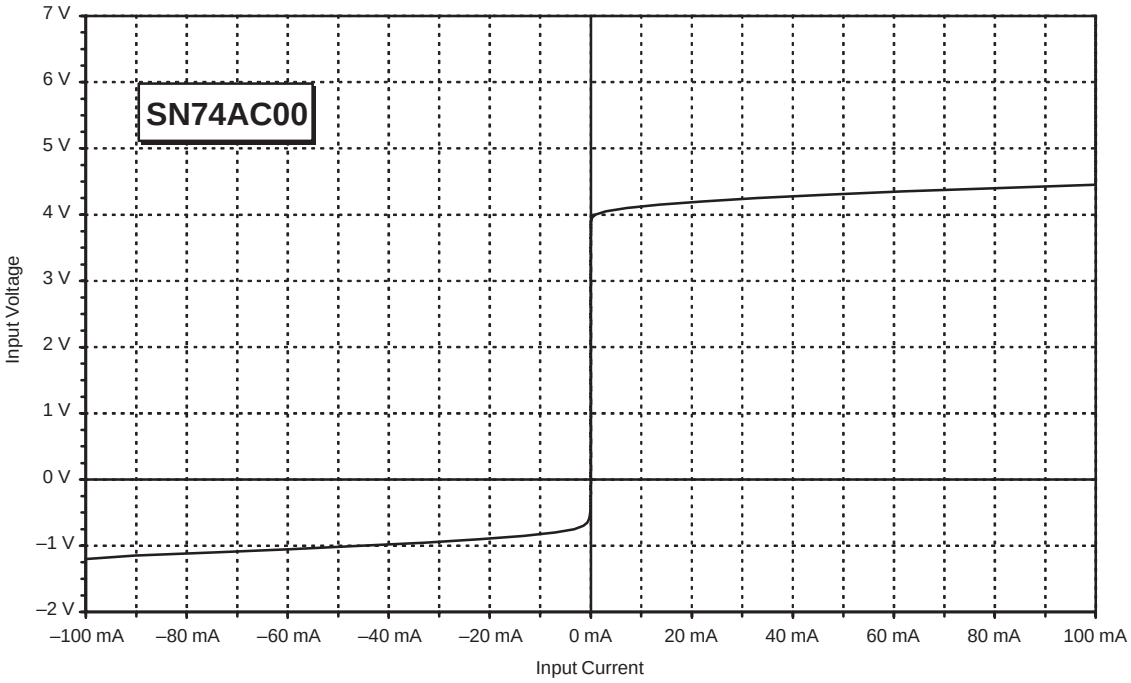


Figure 2. Input Characteristic of the SN74ACxxx Series

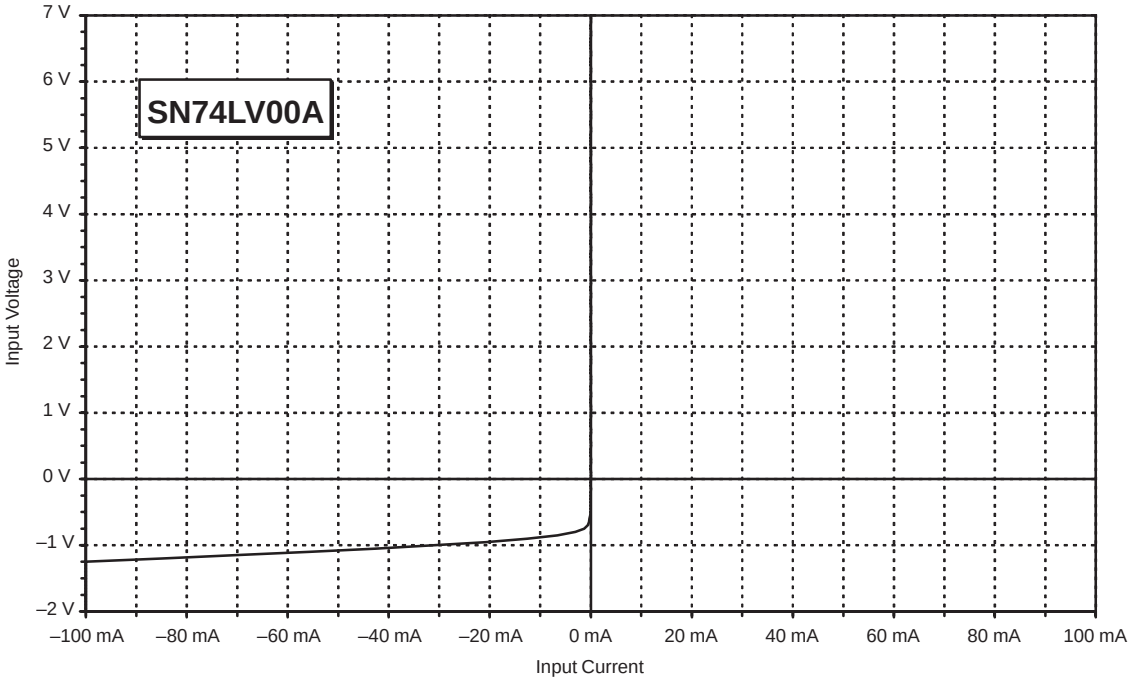


Figure 3. Input Characteristic of the SN74LVxxx Series

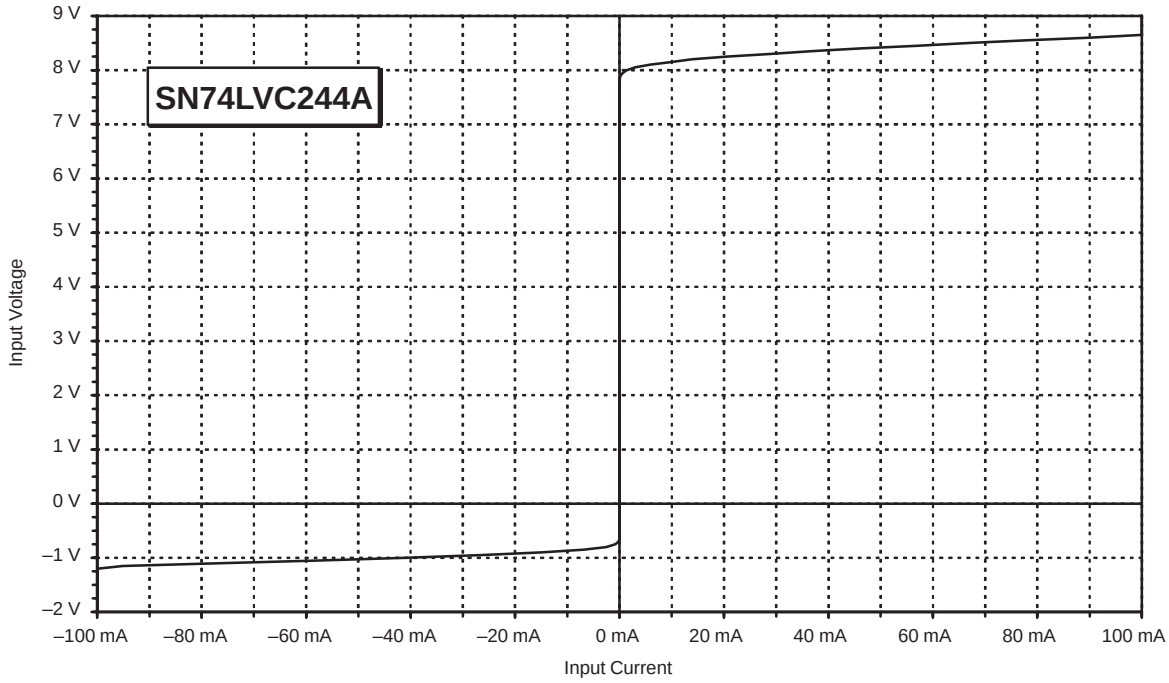


Figure 4. Input Characteristic of the SN74LVCxxx Series

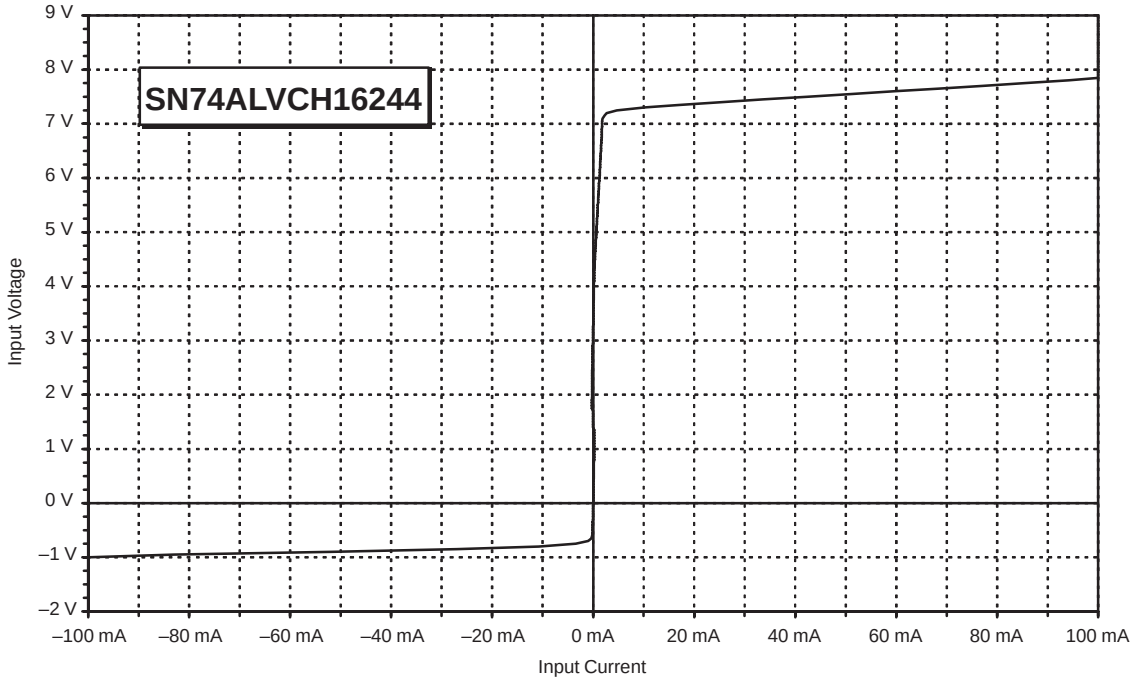


Figure 5. Input Characteristic of the SN74ALVCxxx Series

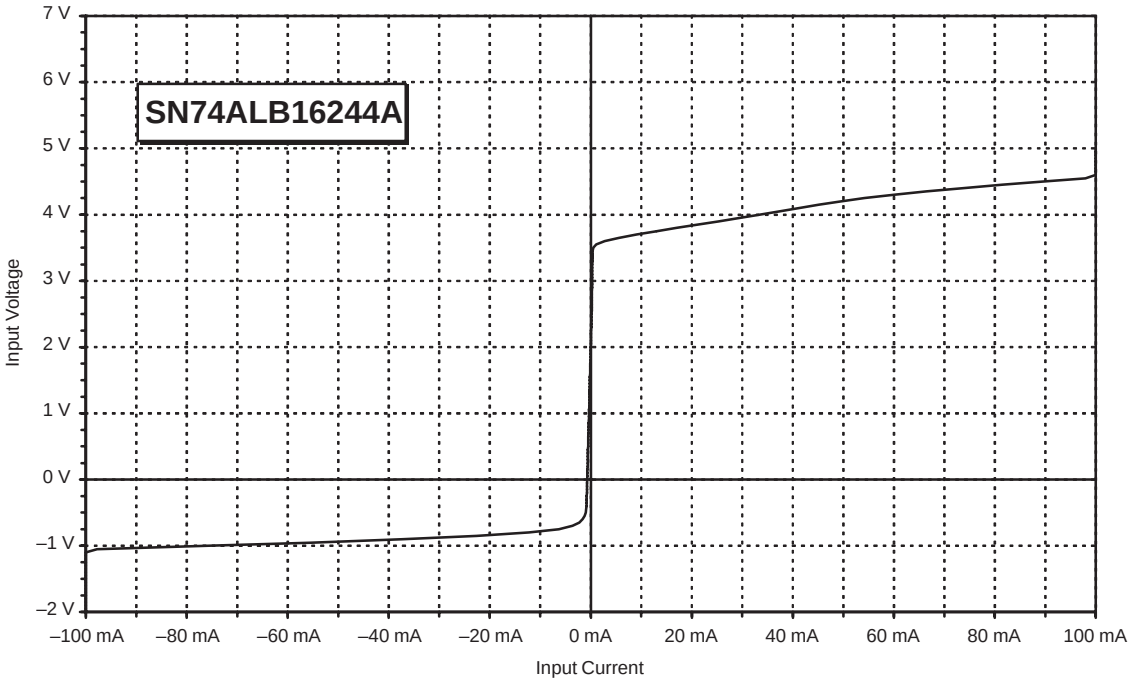


Figure 6. Input Characteristic of the SN74ALBxxx Series

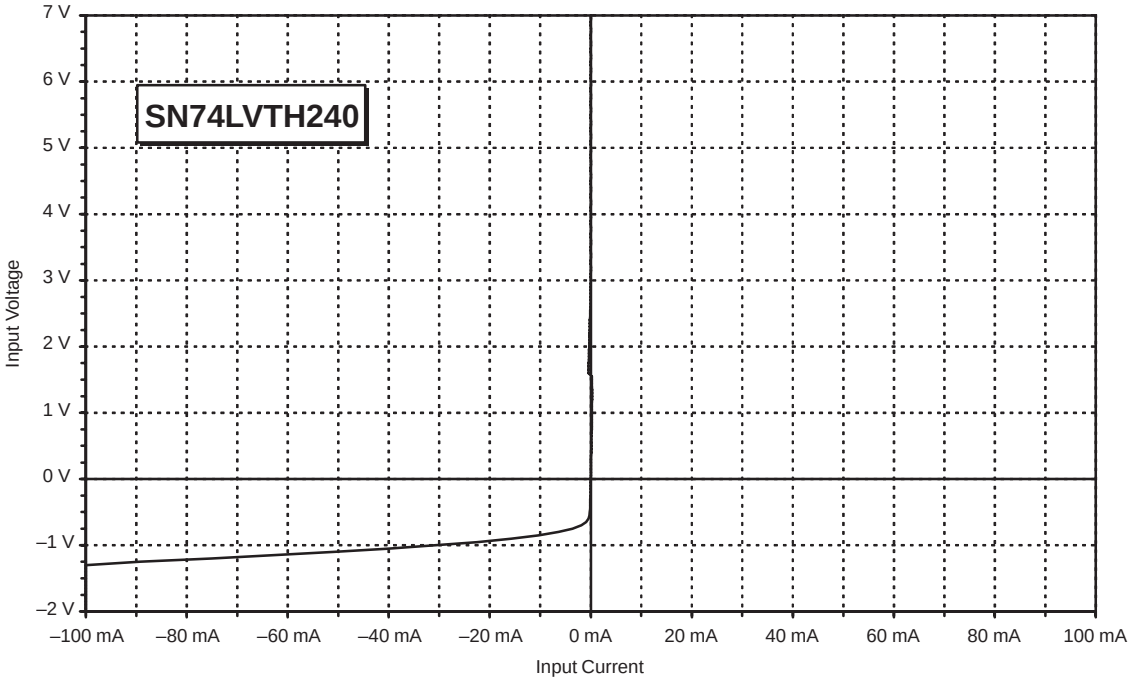


Figure 7. Input Characteristic of the SN74LVTHxxx Series

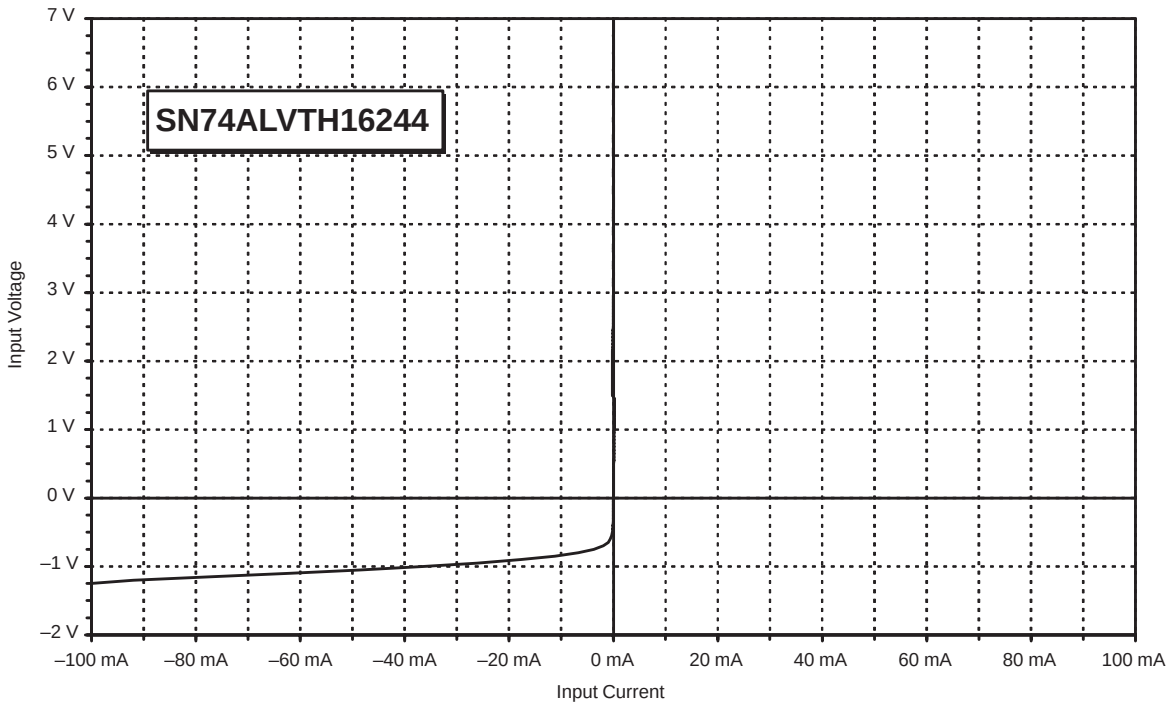


Figure 8. Input Characteristic of the SN74ALVTHxxx Series

3 Output Characteristics

The output stage of a logic circuit in the high-impedance state behaves like a voltage source with an open-circuit voltage of V_{CC} for CMOS logic and low voltage for BiCMOS logic. The internal resistance for the high-impedance state is inversely proportional to the drive capability of the device. The value of the internal resistance for the standard logic families is in the range of 30 Ω to 40 Ω.

In the low state for positive voltages, the output resistance is based on the internal resistance of the conducting transistor, i.e., collector-emitter for BiCMOS technologies and drain-source resistance for CMOS technologies. Negative voltage peaks are limited by a protection diode. The output stages of some CMOS logic families (SN74AHC, SN74AC) also have an output protection diode, which is connected to V_{CC}. This diode limits the positive output voltage to maximum V_{CC} + 0.7 V.

3.1 Series Damping Resistors (SN74XXX2xxx, SN74XXXR2xxx)

In the LVC, ALVC, LVT and ALVT families, TI offers driver options with integrated series resistors of about 25 Ω.

Using the damping resistors at the output stage, the effective output impedance of the driver is about 50 Ω. If the value of the line impedance also is about 50 Ω, no line reflections are observed at the output of the device. In this case, the beginning of the line is terminated perfectly. This option is especially beneficial for memory applications in which overshoots and undershoots might cause a malfunction. In point-to-point applications, nearly ideal signal shapes can be achieved. The “2” in the device part number indicates the presence of a series damping resistor. The “R” in combination with the “2” indicates series damping resistors on both ports of bidirectional devices, for example, the SN74LVC2245A and LVTH162374.

Further information about series damping resistors is given in the TI application report, *Bus-Interface Devices With Output Damping Resistors or Reduced-Drive Outputs*, literature number SCBA012.

A list of available application reports and other literature is in Section 7.

3.2 Automatic High-Impedance State (Auto3-state) Output of the ALVT Family

The auto3-state function, which is implemented in the output stages of the ALVT family, represents a specialty. The principle is shown in Figure 9.

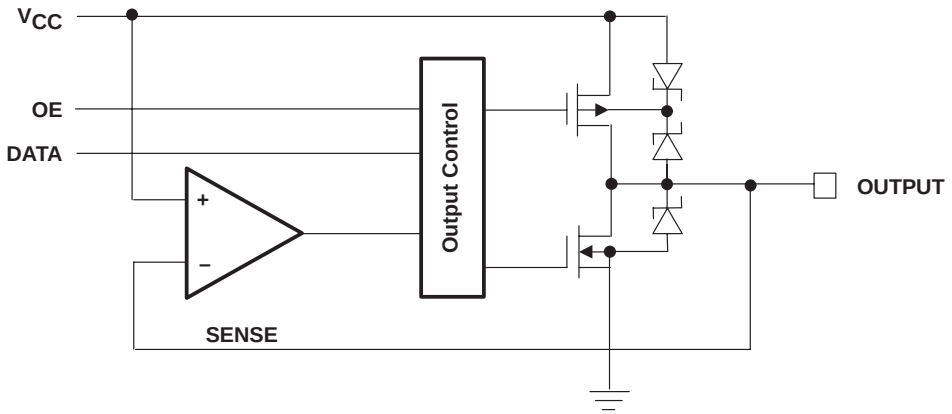


Figure 9. Simplified Output Stage of ALVT Devices

Assume that the output is in the active-high state and a comparator monitors the voltage at the output and compares it with the supply voltage. If the voltage that is applied externally to the output exceeds the supply voltage, the output stage is switched to the high-impedance-state. In this case, the logic levels applied to the data and control input pins of the device are irrelevant.

A current of about 30 mA is needed to trigger the auto3-state circuit, such that bus contentions are prevented, but switching noise does not trigger the protective circuit. However, this also implies that the auto3-state cannot be implemented by using a simple pullup resistor.

Current can flow into the output only in the case of an active high. If the output is set to high impedance by the OE control pin, no current flows.

The series opposed Schottky diodes always connect the back gate of the pullup transistor of the output stage to the higher voltage that is either V_{CC} or the voltage that can be applied externally to the output. In this way, current flow from the output to V_{CC} is suppressed.

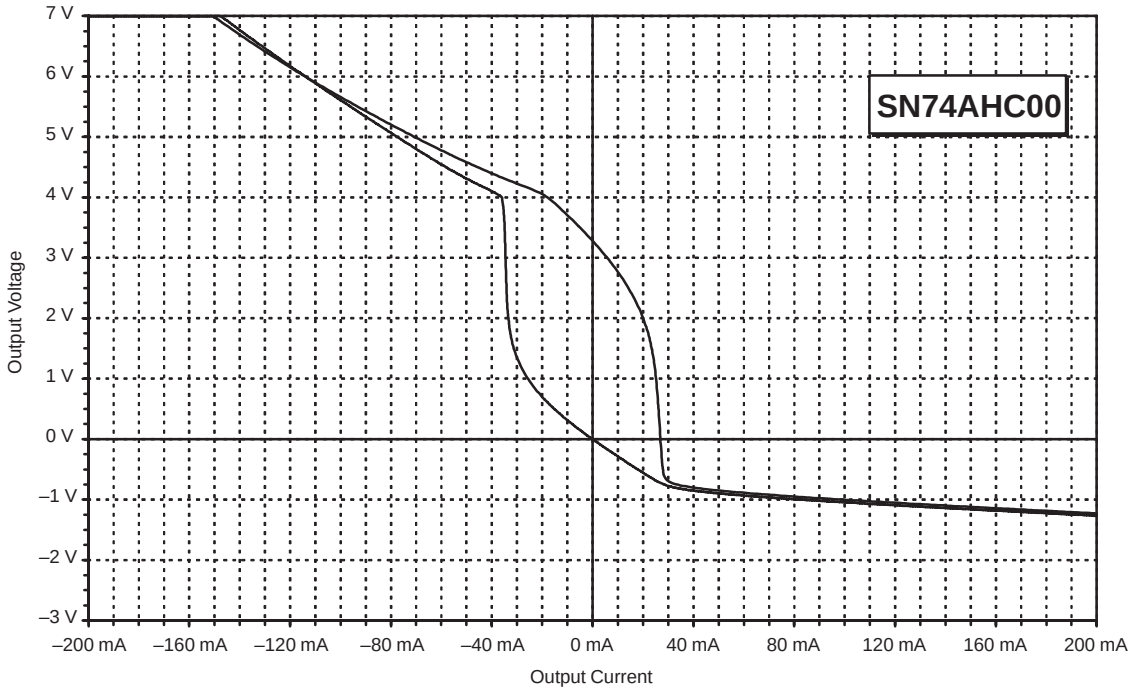


Figure 10. Output Characteristics of the SN74AHC00

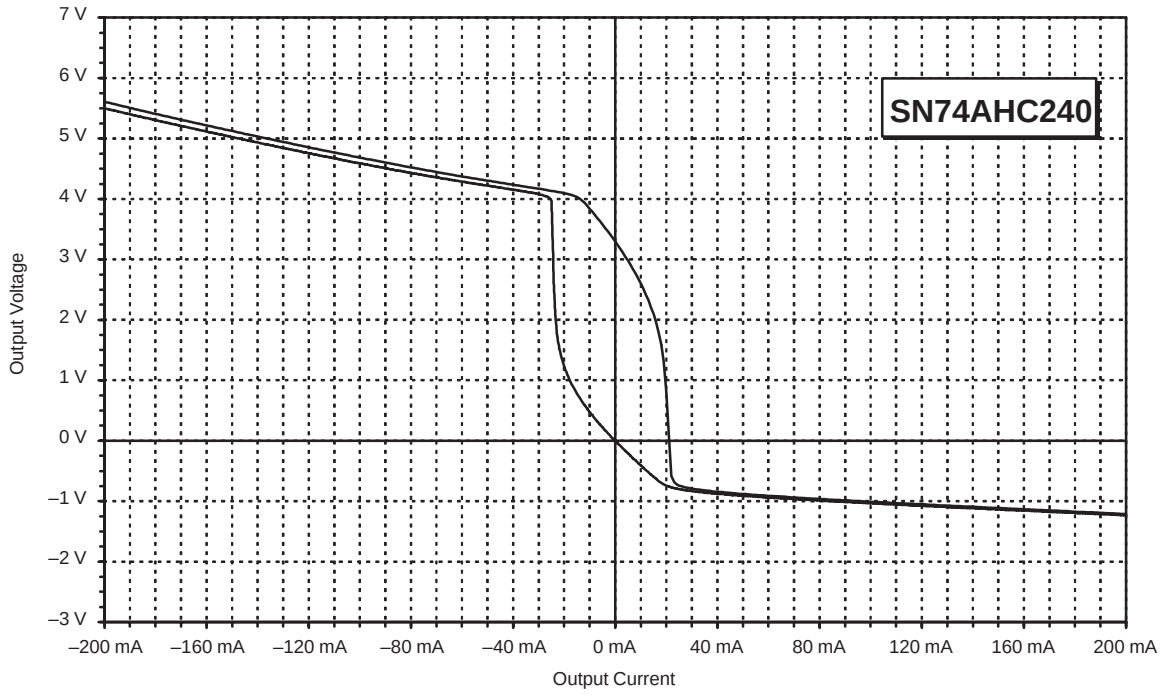


Figure 11. Output Characteristics of the SN74AHC240

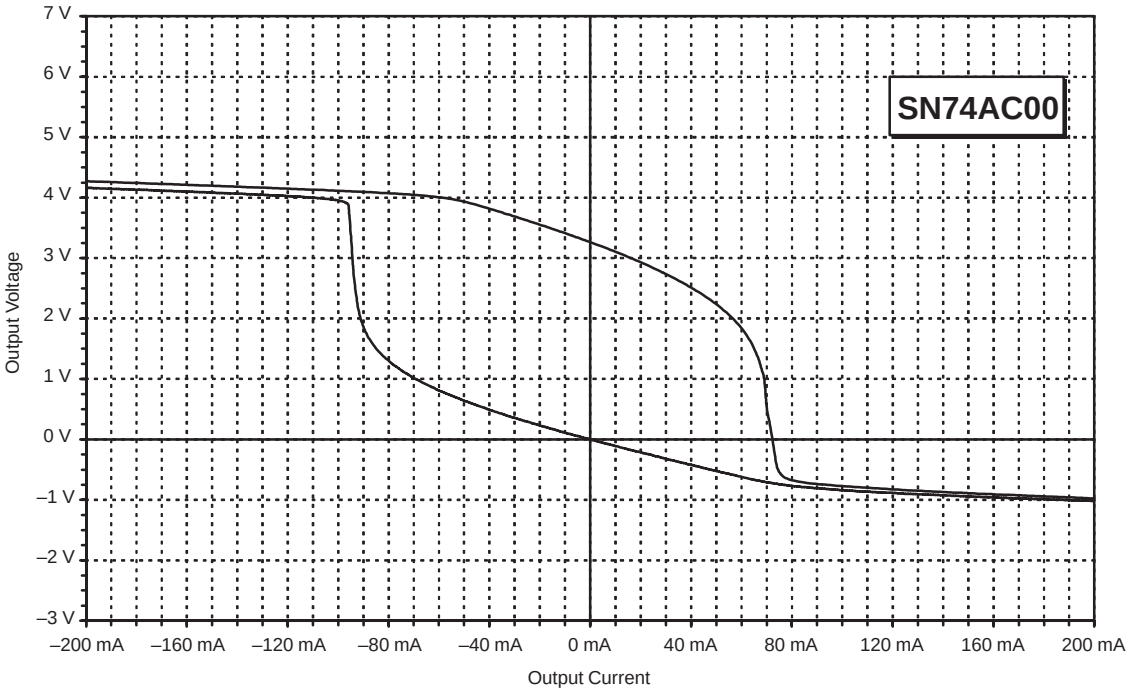


Figure 12. Output Characteristics of the SN74AC00

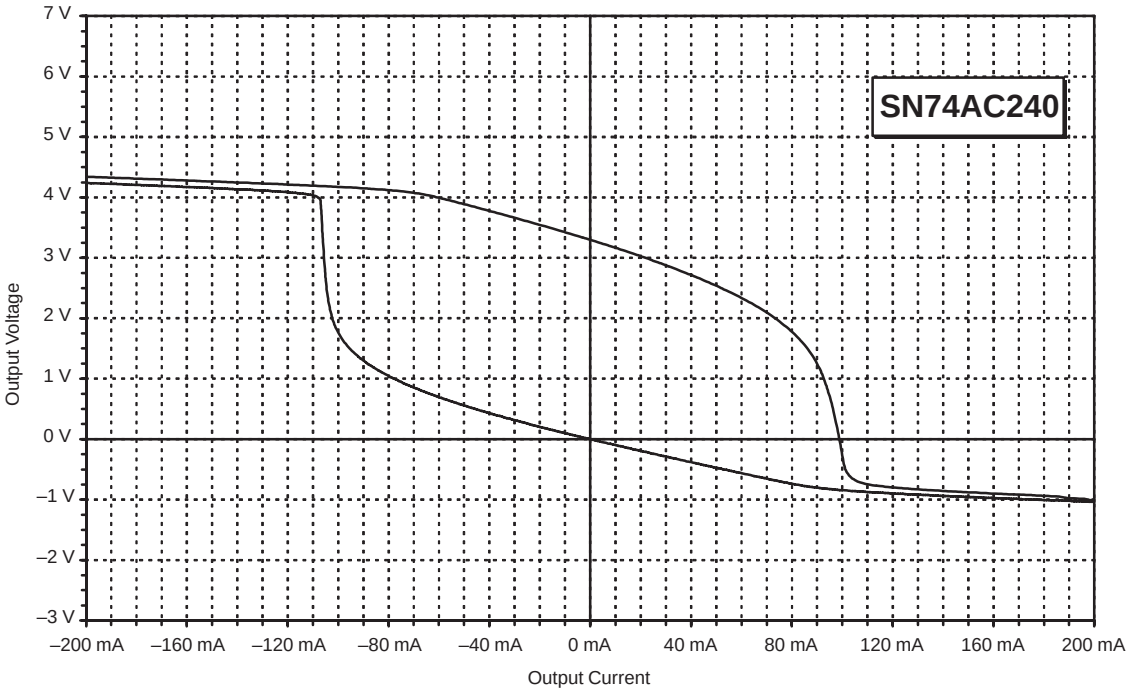


Figure 13. Output Characteristics of the SN74AC240

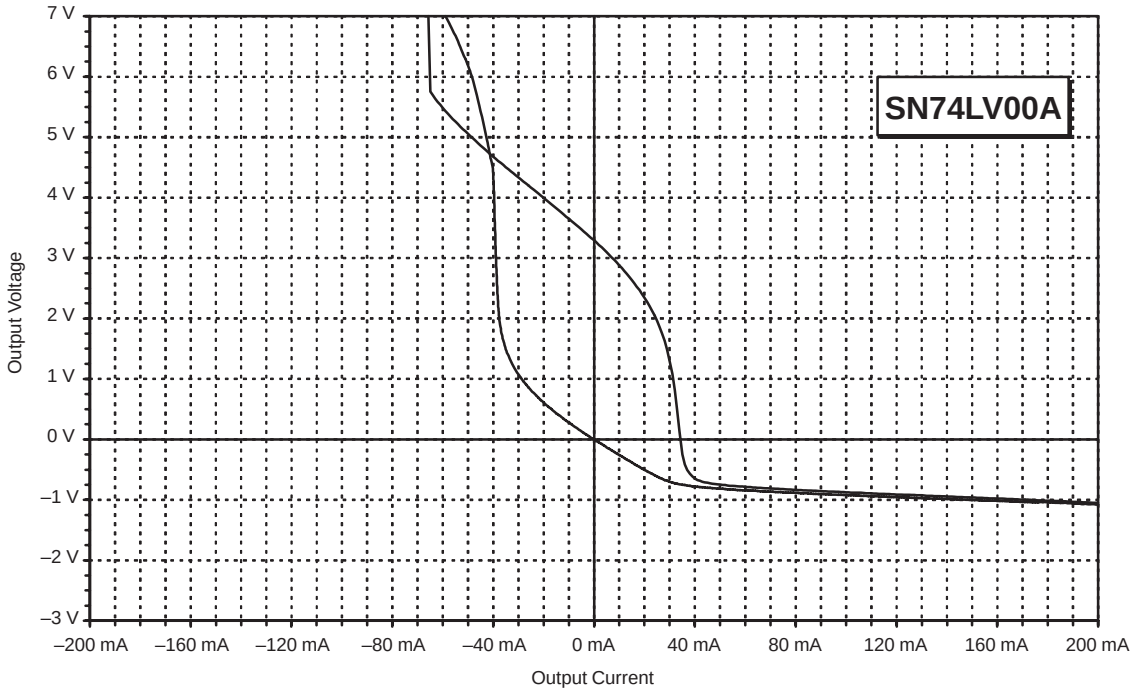


Figure 14. Output Characteristics of the SN74LV00A

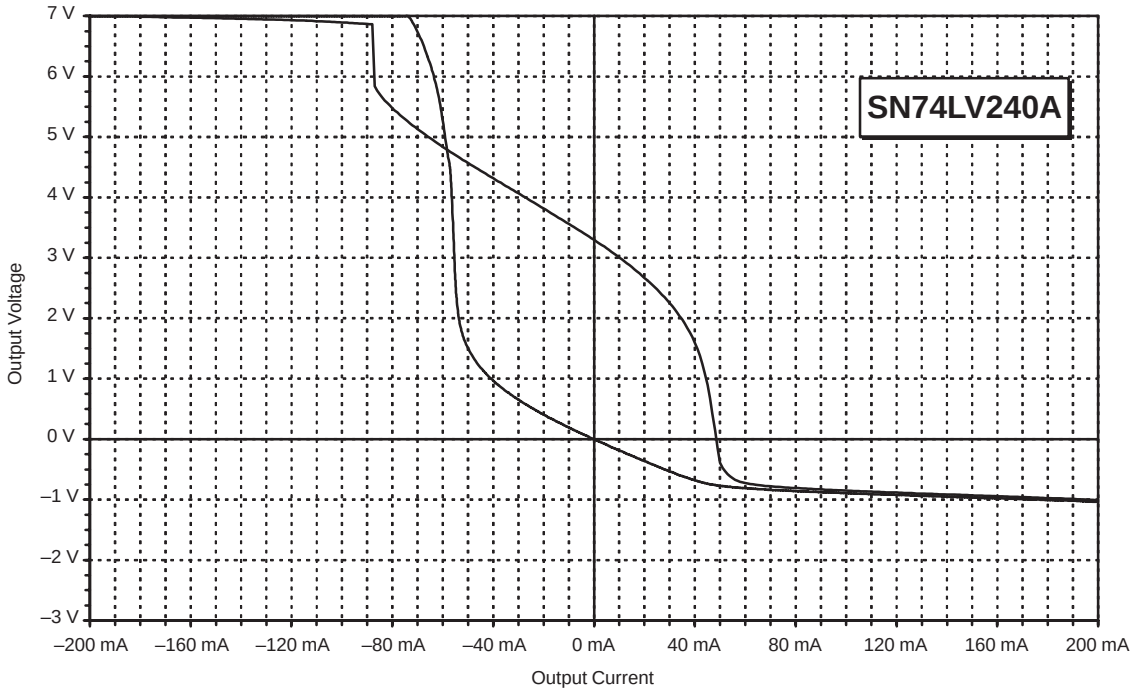


Figure 15. Output Characteristics of the SN74LV240A

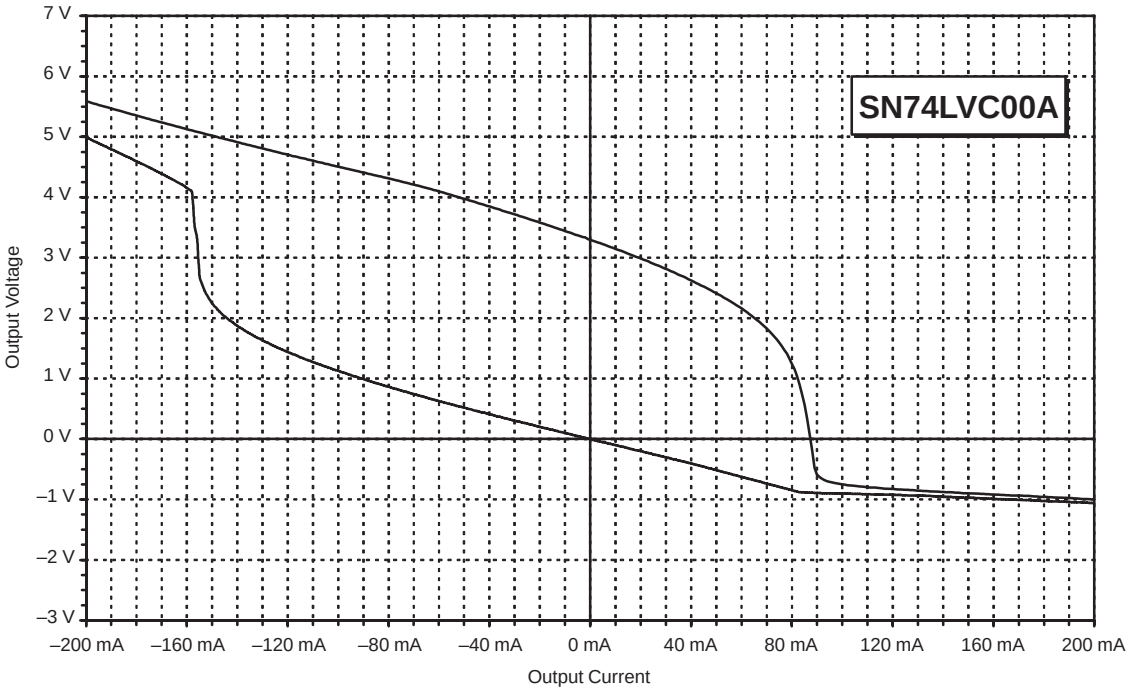


Figure 16. Output Characteristics of the SN74LVC00A

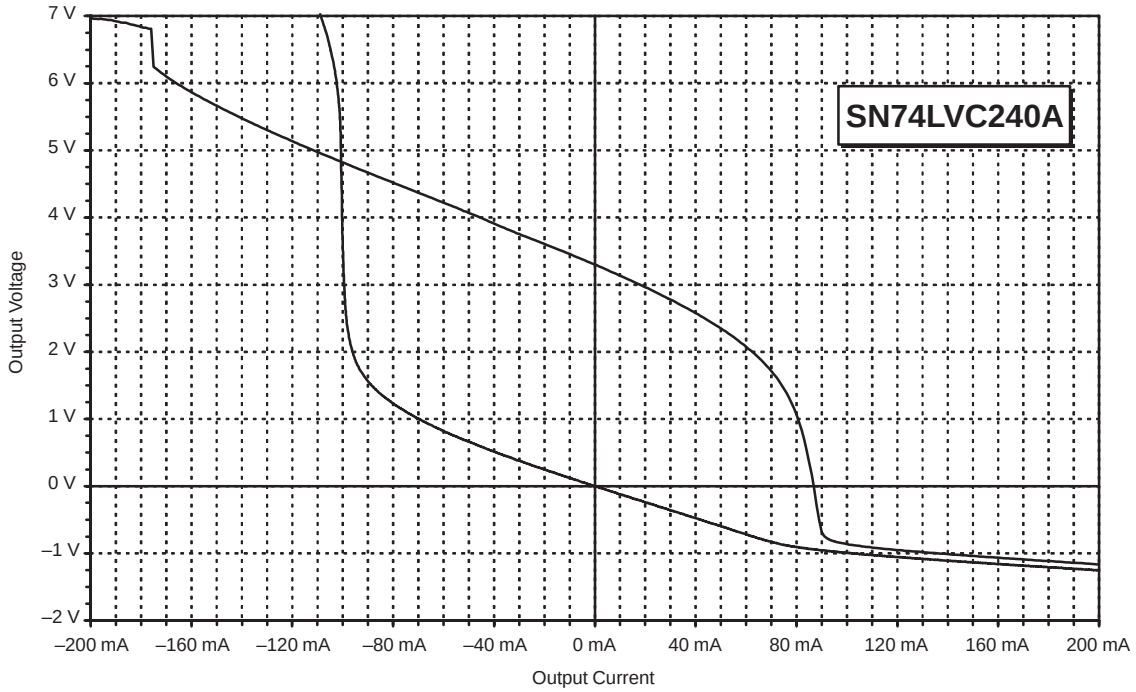


Figure 17. Output Characteristics of the SN74LVC240A

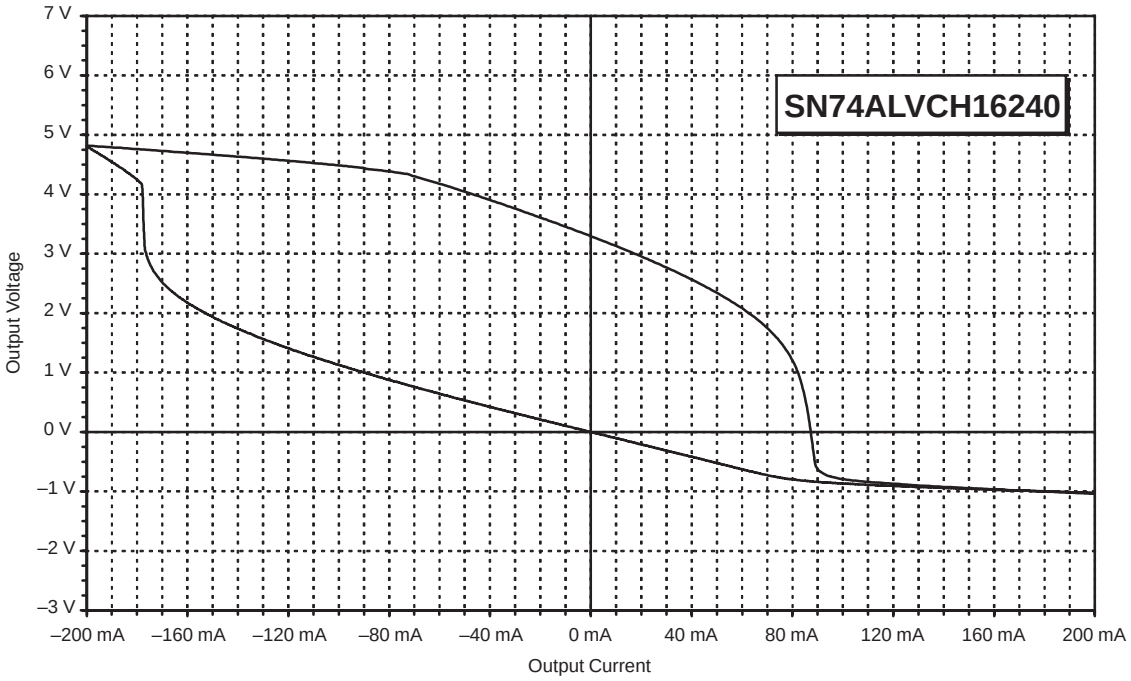


Figure 18. Output Characteristics of the SN74ALVCH16240

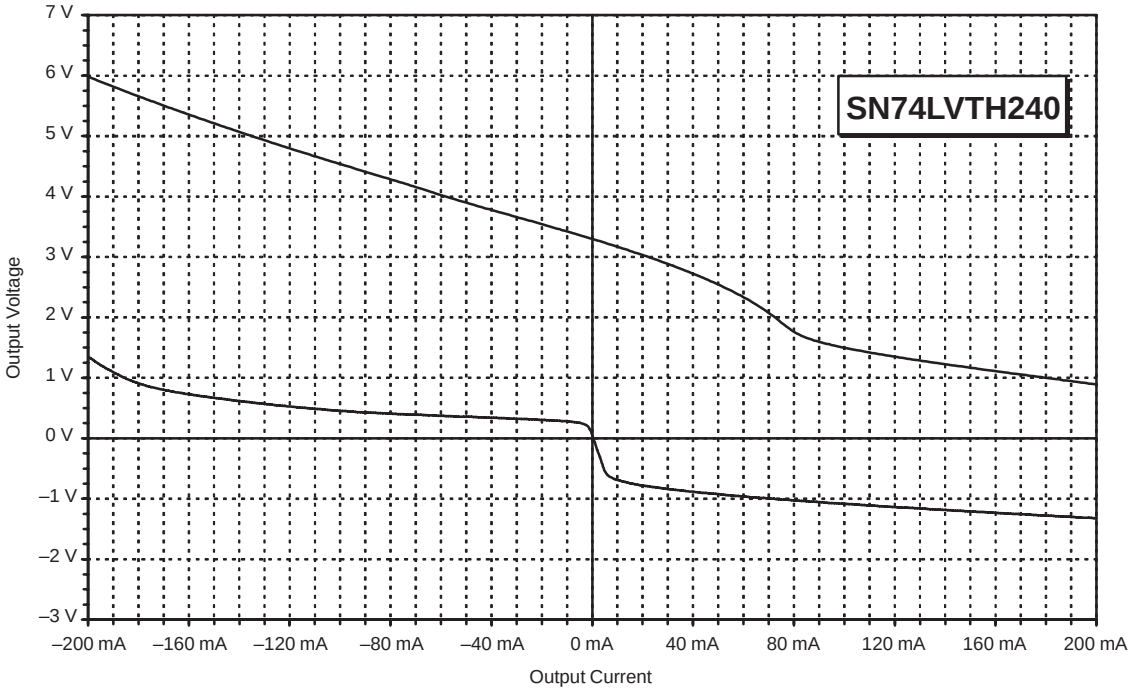


Figure 19. Output Characteristics of the SN74LVTH240

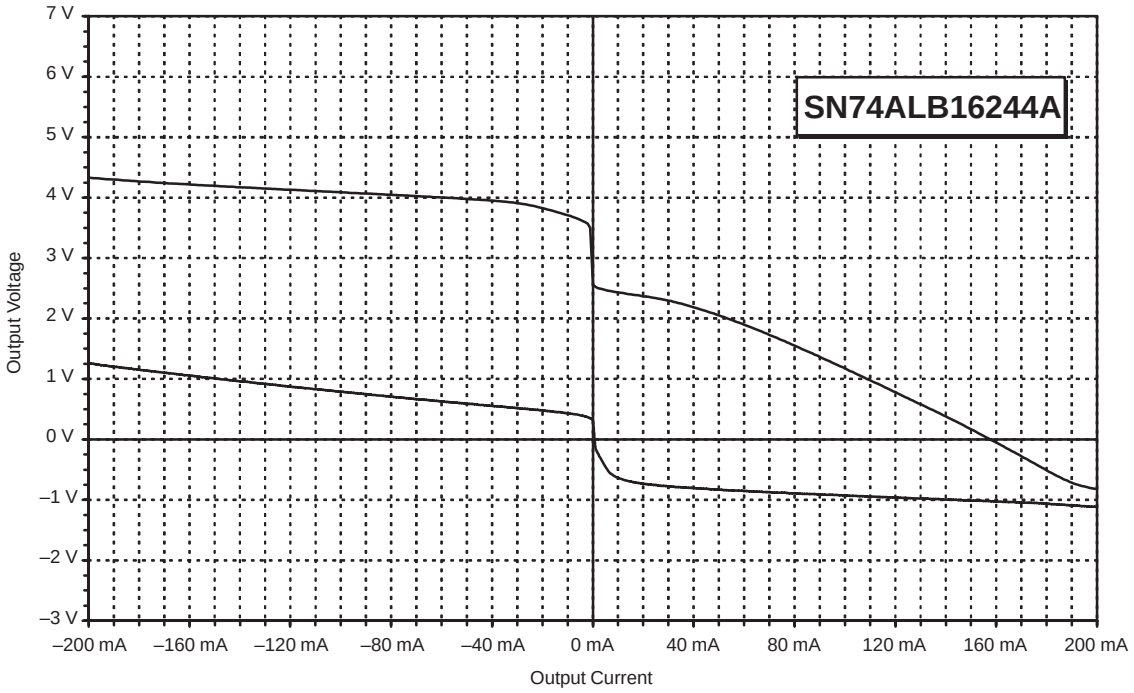


Figure 20. Output Characteristics of the SN74ALB16244A

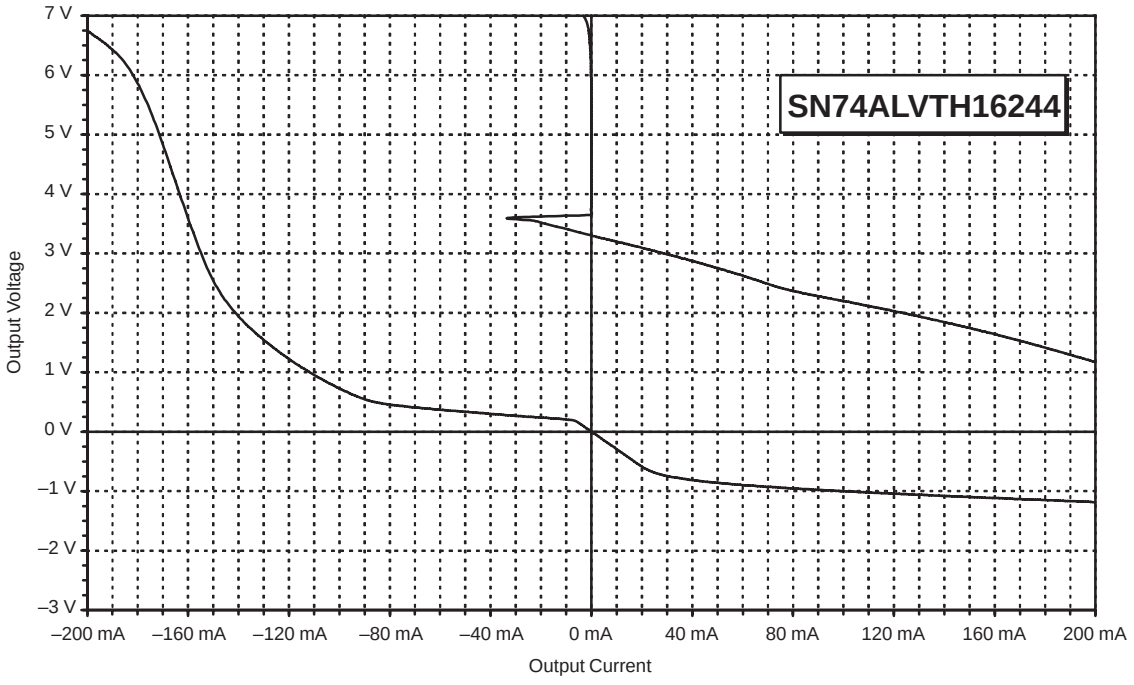


Figure 21. Output Characteristics of the SN74ALVTH16244

4 Bergeron Method Applied to the SN74ALVTH16244

The input and output characteristics, shown in Sections 2 and 3, can be used to determine the signal reflections within a certain application by using a graphical procedure known as the Bergeron method.

The prerequisite for the use of the Bergeron method is that the lines exceed a certain length:

> *If the rise time or the fall time of a signal is shorter than twice the propagation delay on the line, the line theory must be applied.*

Practically, for a line with a signal propagation of 5 ns/m and a signal with a rising or falling edge of 2 ns, starting with a line length that exceeds 20 cm [2 ns / (5 ns/m × 2)], the line theory must be applied.

For a bus line, the signal propagation delay increases to 25 ns/m, so that, in this case, the line theory has to be applied for a line length that exceeds 4 cm [2 ns / (25 ns/m × 2)].

The SN74ALVTH16244 device was tested, using the measurement setup shown in Figure 22. The Bergeron method was used to determine the signal shape in advance.

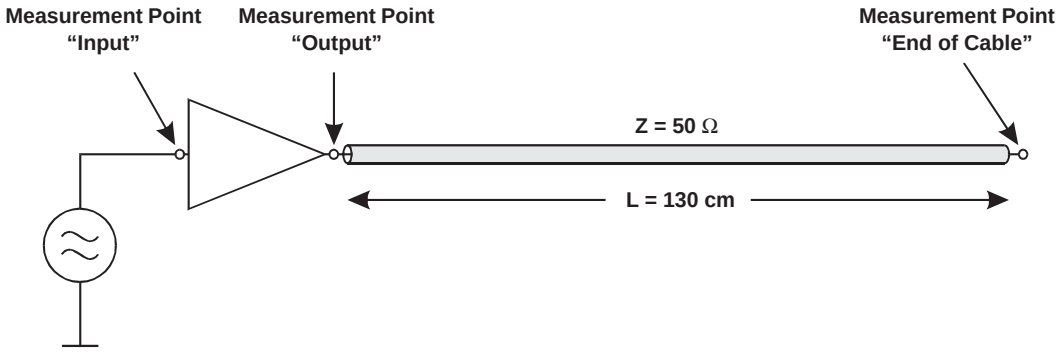


Figure 22. Measurement Setup for the Bergeron Method

The first step in the graphical solution using the Bergeron method is to draw the following characteristics in a voltage-versus-current diagram:

- Output characteristics of the SN74ALVTH16244 device
- Load characteristic at the end of the line

The output characteristics are taken directly from Figure 21. The load characteristic equals the Y-axis for the investigated case because no resistor is connected to the end of the line ($R_L = \infty$).

The intersection between the load characteristic and the output characteristic represents the steady states, the current and voltage values at the line start, and the end of the line at the time $t < 0$, respectively.

4.1 Voltage Value at the Output of the Driver

For the low-to-high transition, draw a straight line, starting at the intersection of the output-low characteristic and the load characteristic. For the high-to-low transition, start the straight line at the cross point of *output-high* characteristic and the load characteristic.

The line impedance, Z_O, determines the steepness of this line. In the example, the line impedance is 50 Ω.

The intersection of this straight line and the output characteristics equals the voltage and current values at the beginning of the line at the time $\tau = 0$.

4.2 Voltage Value at End of the Line

Now, a straight line with the steepness $-Z_O$ is drawn through this point. The intersection between this line and the load characteristics results in the voltage values at the end of the line after one propagation delay time of the line, that is after $\tau = 1$.

Afterward, the procedure is repeated, applying straight lines to the output characteristics and the load characteristics.

The steepness of the straight line is:

- $-Z_O$ from the output characteristics to the load characteristics
- Z_O from the load characteristic to the output characteristics

In this way, current and voltage values are obtained:

- at the end of the line, at the times $\tau = 1, 3, 5 \ldots$
- at the line start, at the times $\tau = 2, 4, 6 \ldots$

The Bergeron diagram is shown in Figure 23. The related diagram (see Figure 24) shows the line reflections.

The precalculated values using the Bergeron procedure match very well with the measured signal shapes. Another TI application report, *The Bergeron Method: A Graphic Method for Determining Line Reflections in Transient Phenomena*, literature number SDYA014, describes the graphic procedure in more detail

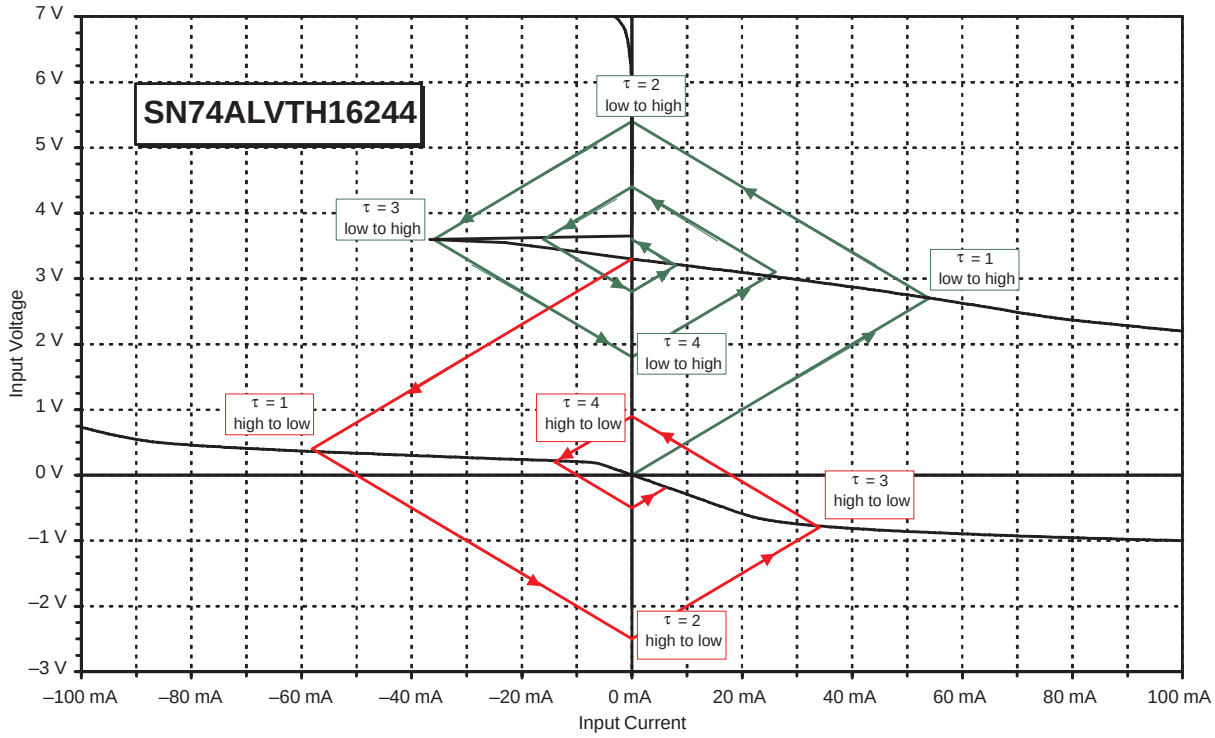
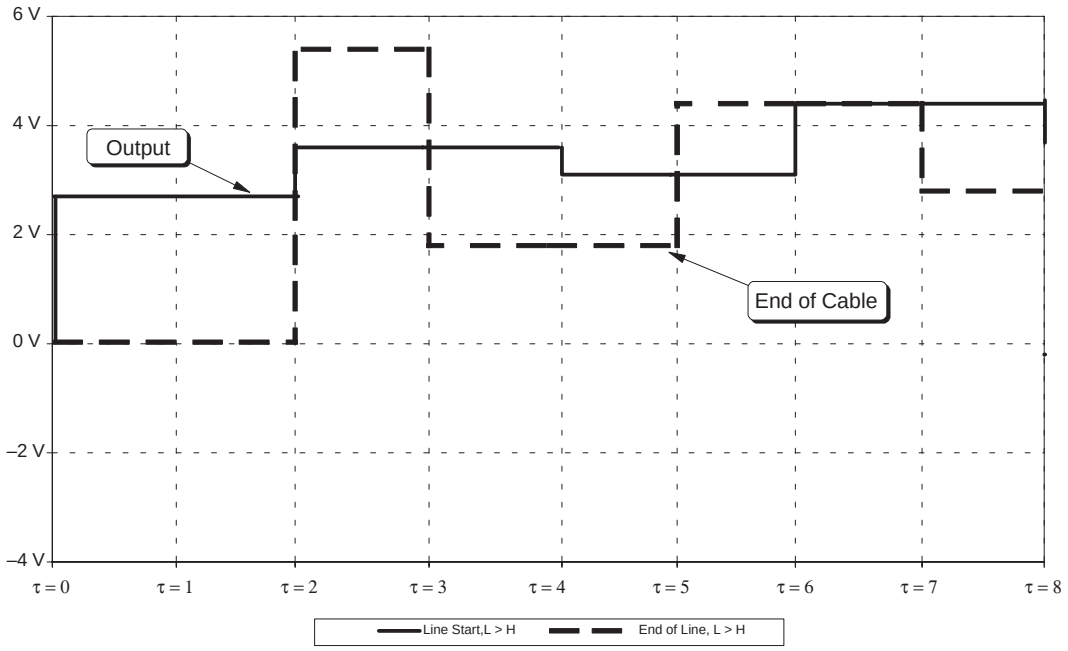


Figure 23. Bergeron Diagram for the SN74ALVTH16244



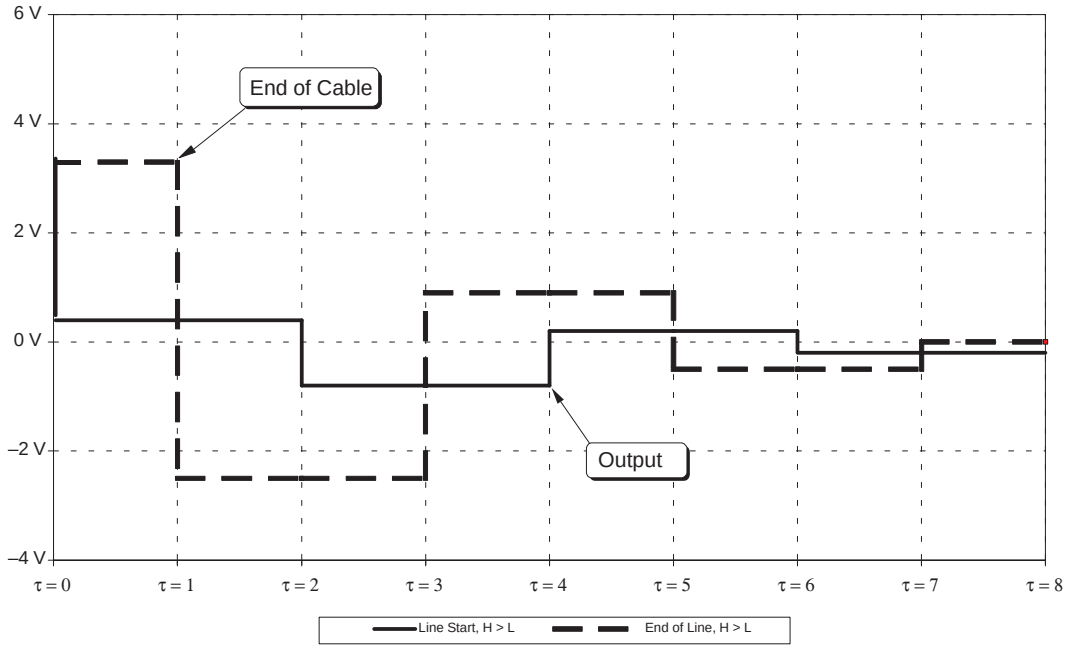


Figure 24. Diagram of Line Reflections for the SN74ALVTH16244

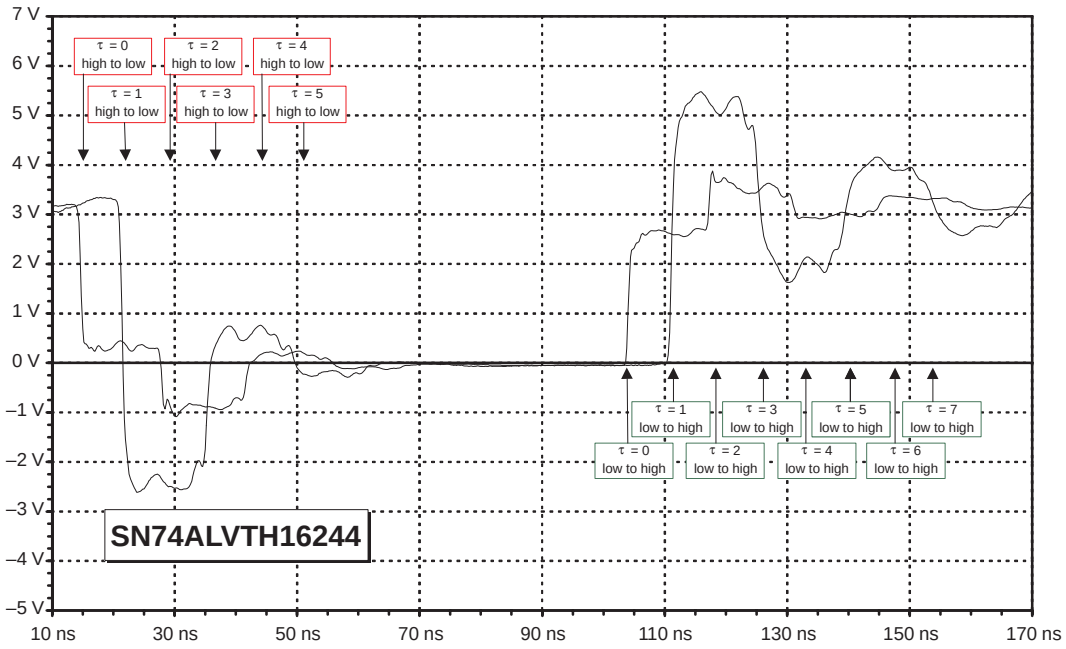


Figure 25. Signal Shape of the SN74ALVTH16244

5 Output Waveforms

The following measurements demonstrate the voltage waveforms of typical output stages. The measurement setup is shown in Figure 22.

For these measurements, the devices under test were loaded with a 1.3-m coaxial cable having a characteristic impedance of 50 Ω; the end of the line was not connected, i.e., open circuit.

These waveforms provide good insight into the dynamic behavior of the devices. In particular, the oscillograms provide information regarding drive capability with a low-resistance load, together with an indication of the line reflections that can be expected.

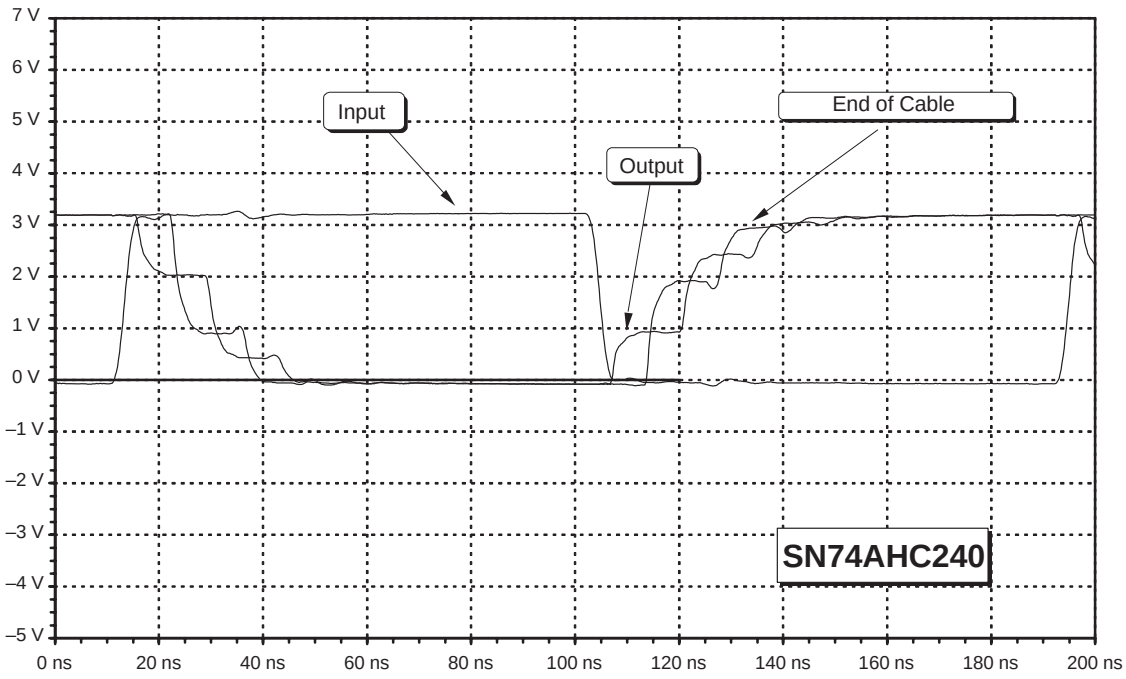


Figure 26. Output Waveforms of the SN74AHC240

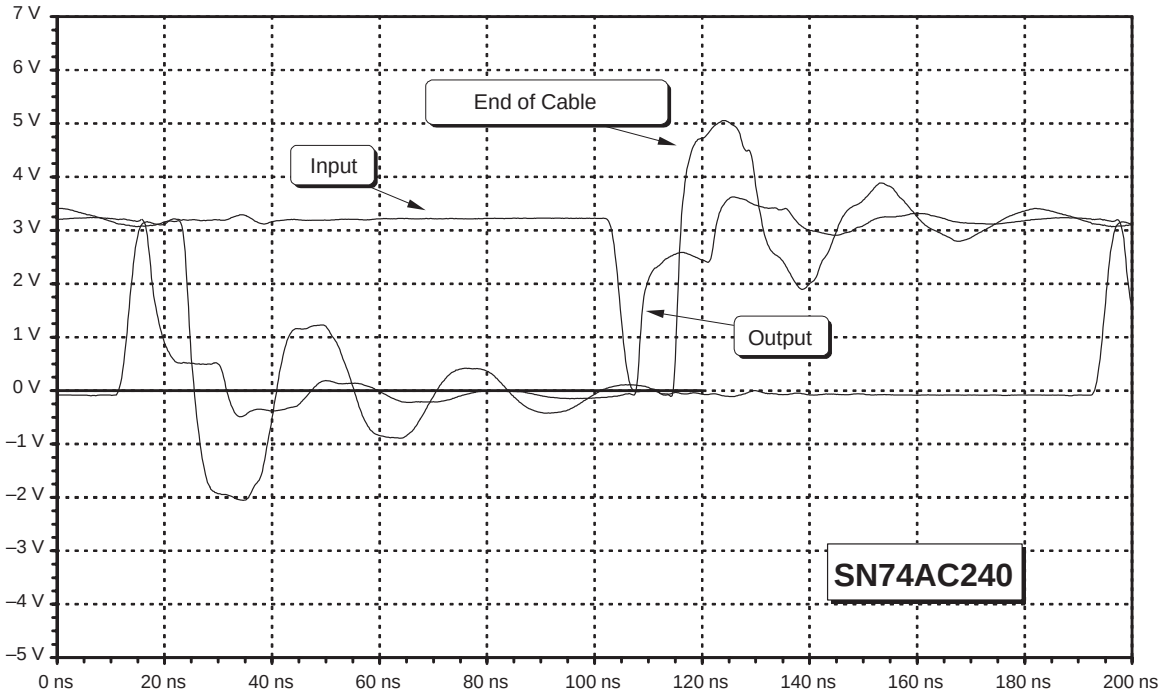


Figure 27. Output Waveforms of the SN74AC240

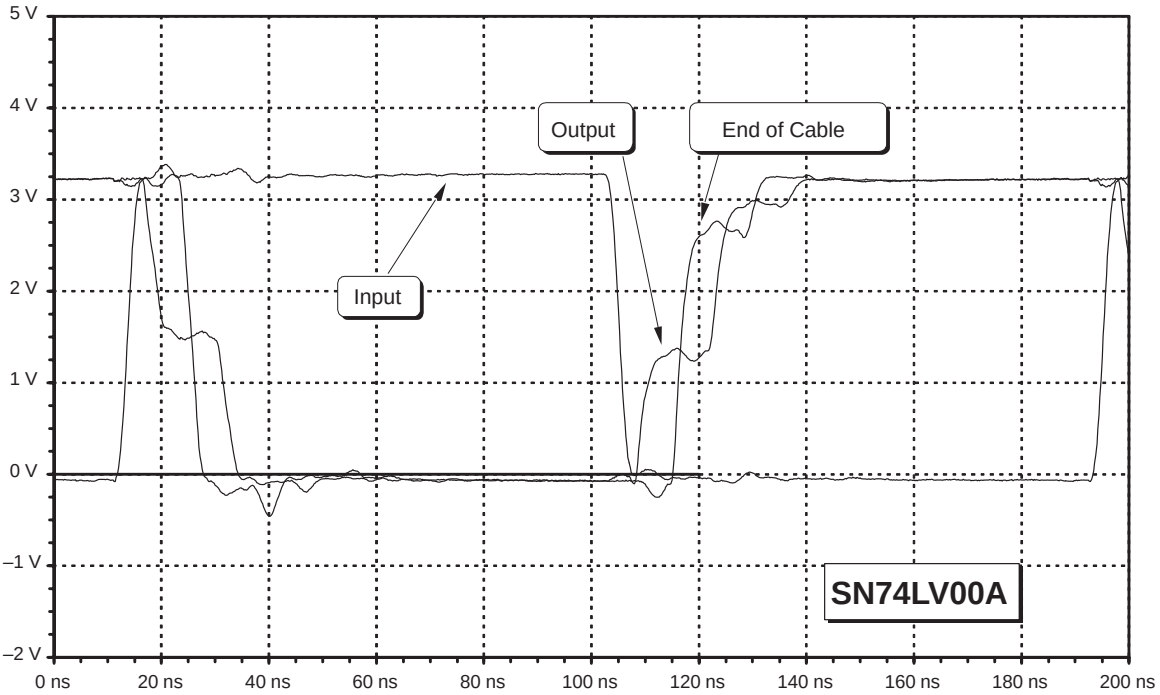


Figure 28. Output Waveforms of the SN74LV00A

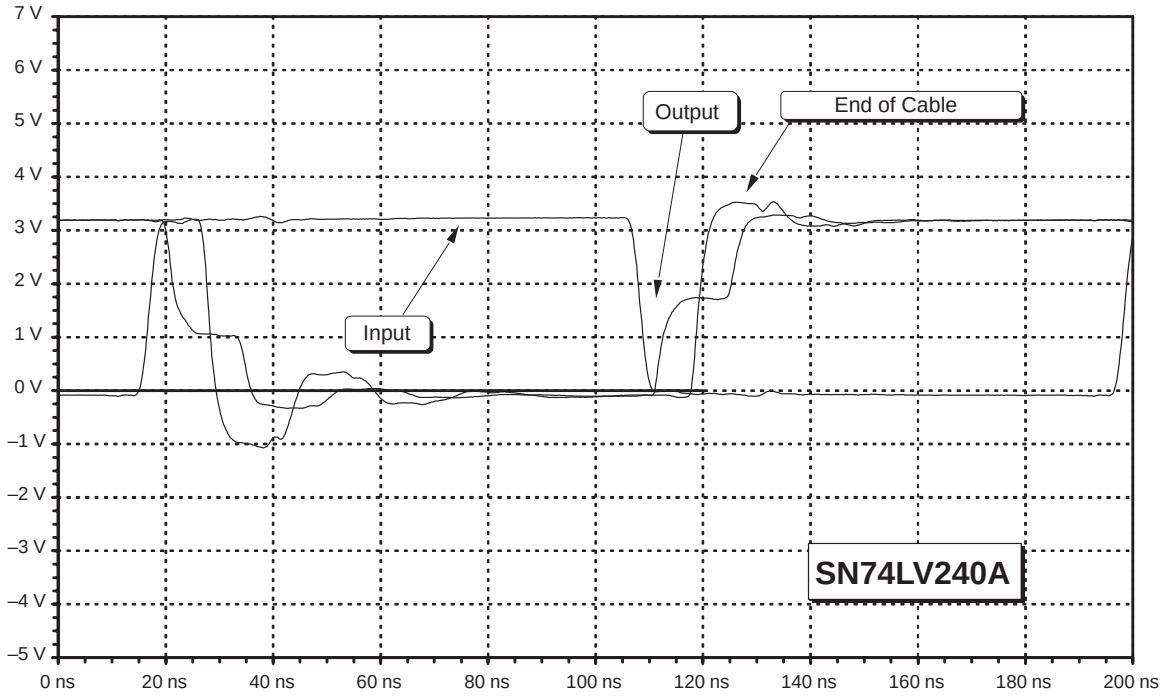


Figure 29. Output Waveforms of the SN74LV240A

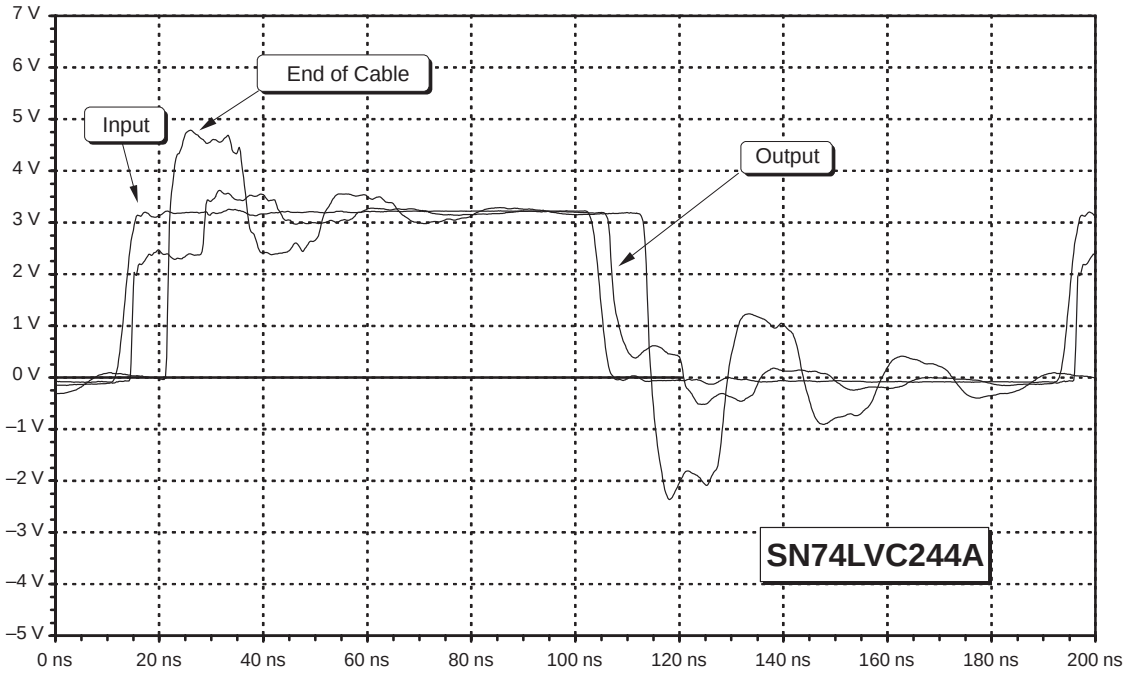


Figure 30. Output Waveforms of the SN74LVC244A

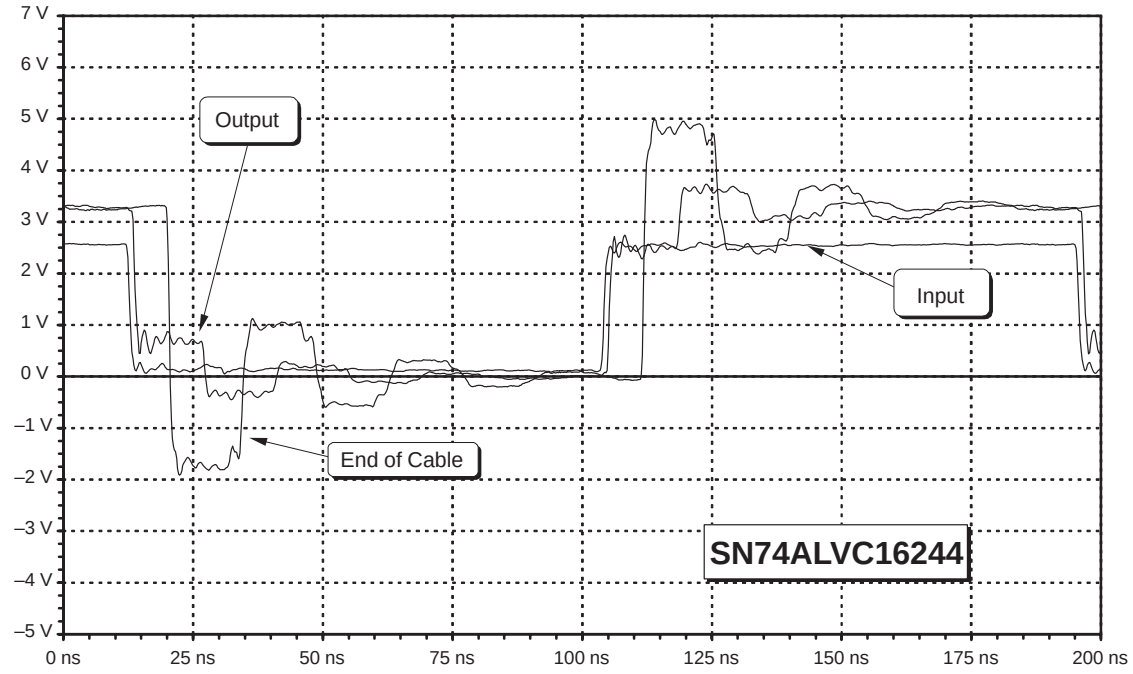


Figure 31. Output Waveforms of the SN74ALVC16244

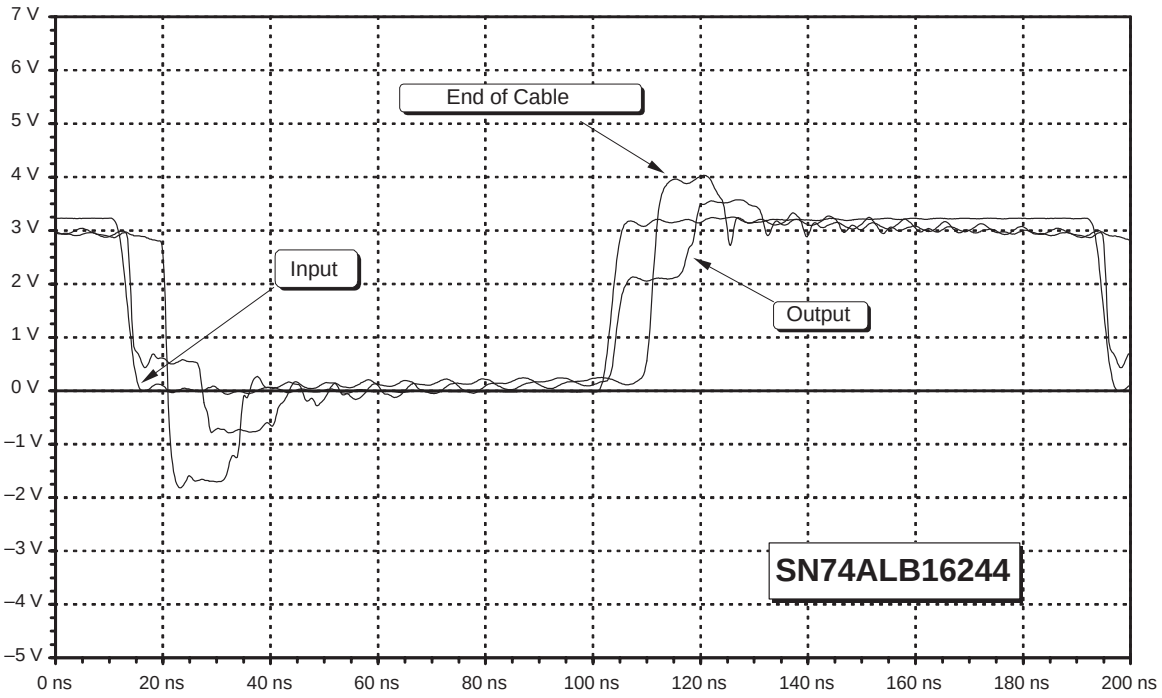


Figure 32. Output Waveforms of the SN74ALB16244

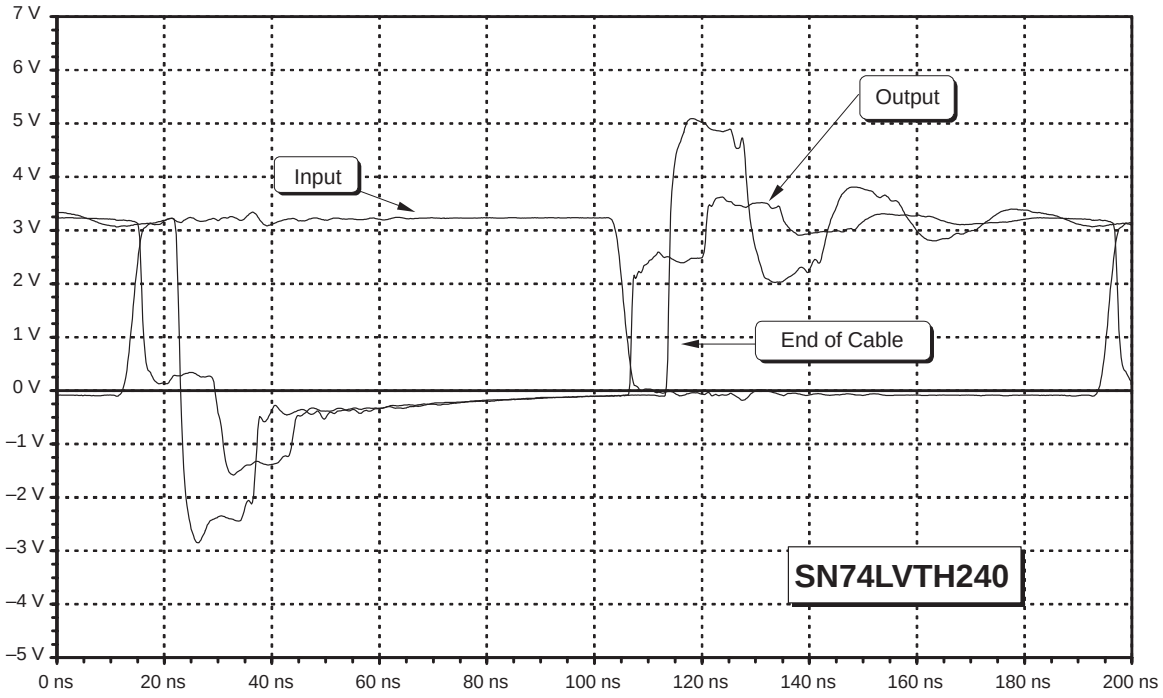


Figure 33. Output Waveforms of the SN74LVTH240

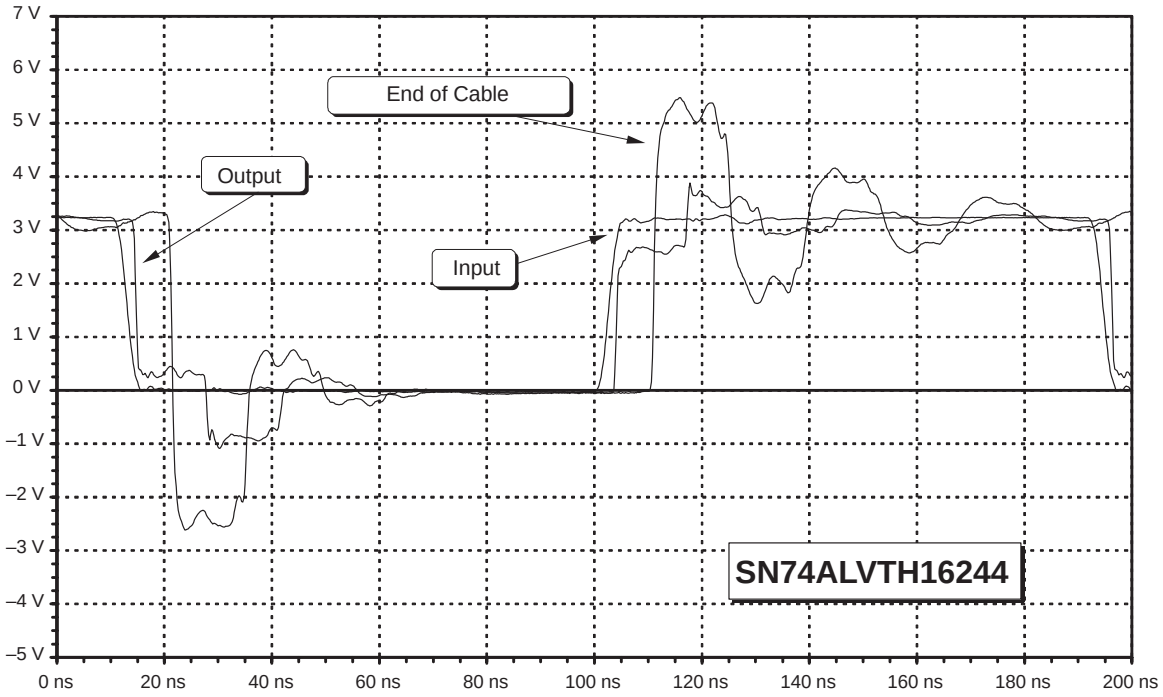


Figure 34. Output Waveforms of the SN74ALVTH16244

6 Abbreviations and Glossary

5-V tolerance	Logic devices with 5-V tolerance allow 5-V CMOS logic levels at their inputs and outputs in the high-impedance state.

A

Auto3-state	Devices tolerate a higher voltage level at the outputs during active high state at the output. Also called overvoltage protection.
SN74ALVC	Advanced Low-Voltage CMOS devices
SN74ALVT	Advanced Low-Voltage Technology devices
SN74AC	Advanced CMOS devices
SN74AHC	Advanced High-speed CMOS devices

B

BiCMOS	Combination of bipolar and CMOS processes (CMOS input structure, bipolar output structure)

G

GND	Ground

I

I/O	Input/Output

L

SN74LV	Low-Voltage CMOS devices, originally designed for V_{CC} = 3.3 V; also specified at 5 V
SN74LVC	Low-Voltage CMOS devices
SN74LVT	Low-Voltage Technology devices with overvoltage protection (see auto3-state)

R

R_L	Load resistor

S

SN74S	Schottky devices
SPICE	Simulation Program with Integrated Circuit Emphasis

T

TTL level	Transistor-Transistor Logic level

V

V_{CC}	Supply voltage

7 References

7.1 Documents Published by TI

ABT Logic Advanced BiCMOS Technology, Data Book, 1998, literature number SCBD002C.

Advanced CMOS Logic, Data Book, 1996, literature number SCADE02.

Logic Selection Guide and Data Book, CD-ROM, April 1998, literature number SCBC001B.

AHC/AHCT Logic Advanced High-Speed CMOS, Data Book, 1997, literature number SCLD003A.

Design Considerations for Logic Products, Application Book, 1997, literature number SDYA002.

Digital Design Seminar, Reference Manual, 1998, literature number SDYDE01B.

Designing With Logic, March 1997, literature number SDYA009.

The Bergeron Method: A Graphic Method for Determining Line Reflections in Transient Phenomena, October 1996, literature number SDYA014.

Bus-Interface Devices With Output Damping Resistors or Reduced Drive Outputs, August 1997, literature number SCBA012A.

Live Insertion, October 1996, literature number SDYA012.

Thin Very Small-Outline Package (TVSOP), March 1997, literature number SCBA009C.

Low-Voltage Logic Families, April 1997, literature number SCVAE01A.

Bus-Hold Circuit, July 1992, literature number SDZAE15.

Electromagnetic Emission from Logic Circuits, November 1998, literature number SZZA007.

PCB Design Guidelines for Reduced EMI, November 1998, literature number SZZA009.

Input and Output Characteristics of Digital Integrated Circuits at 2.5-V Supply Voltage, literature number SZZA012.

Input and Output Characteristics of Digital Integrated Circuits at 5-V Supply Voltage, literature number SZZA008.

7.2 Internet Information Sources

TI Semiconductor Home Page

http://www.ti.com/sc

TI Distributors

http://www.ti.com/sc/docs/distmenu.htm

TI Logic Home Page

http://www.ti.com/sc/docs/asl/home.htm

TI Logic Literature

http://www.ti.com/sc/docs/asl/lit/lit.htm

TI Product Information and Document Search

http://www.ti.com/sc/docs/msp/download.htm

8 Acknowledgment

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