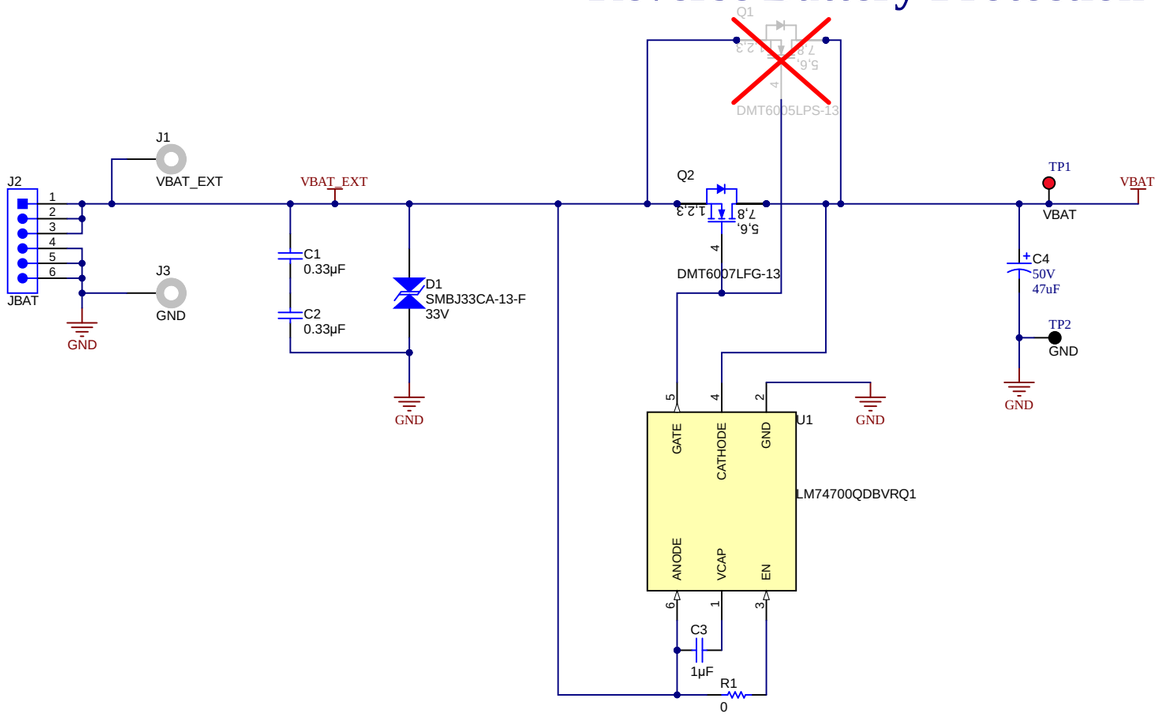
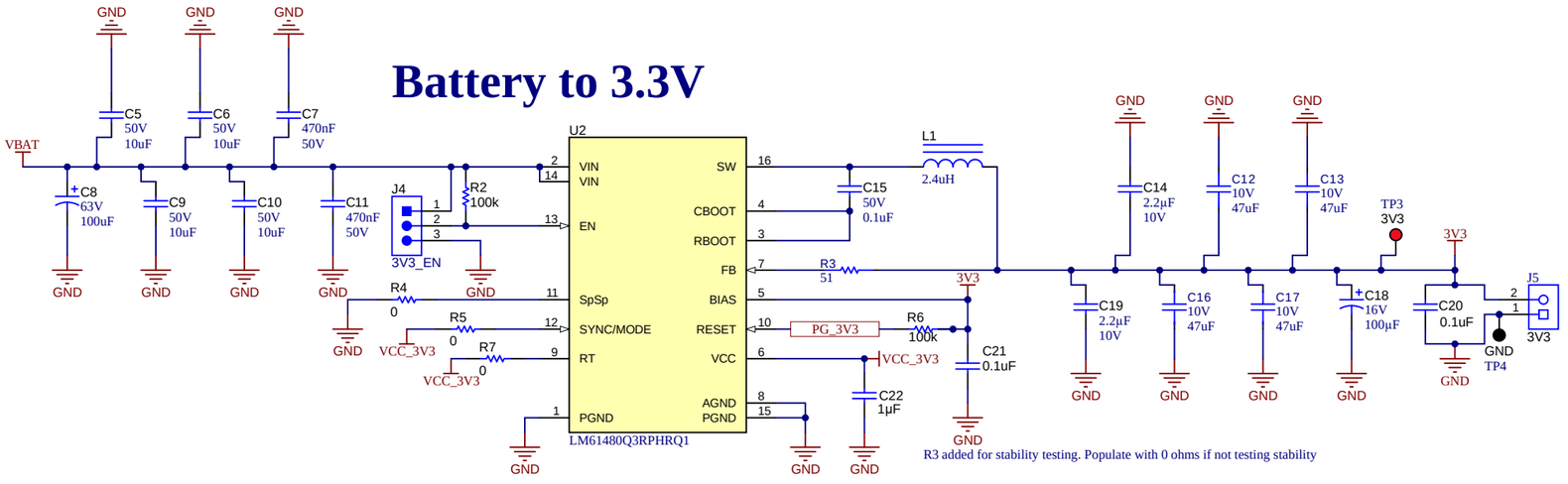
Reverse Battery Protection



Battery to 3.3V



Orderable: ChangeMe in variant	Designed for: Custom	Mod. Date: 11/14/2023
TID #: N/A	Project Title: PMP23242	
Number: PMP23242 Rev: B	Sheet Title:	
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 2 of 7
Drawn By: Cameron Hagg	File: 3V3_OffBattery.SchDoc	Size: B
Engineer: Josh Mandelcorn	Contact: http://www.ti.com/support	

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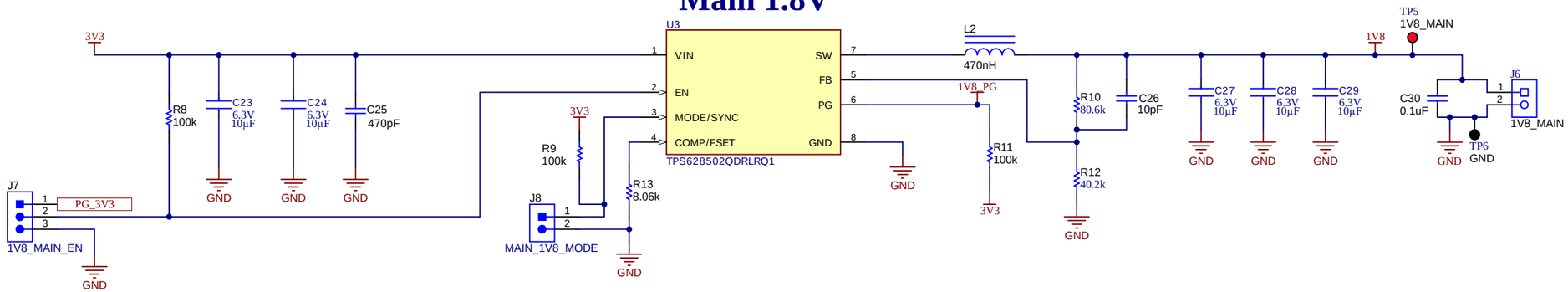
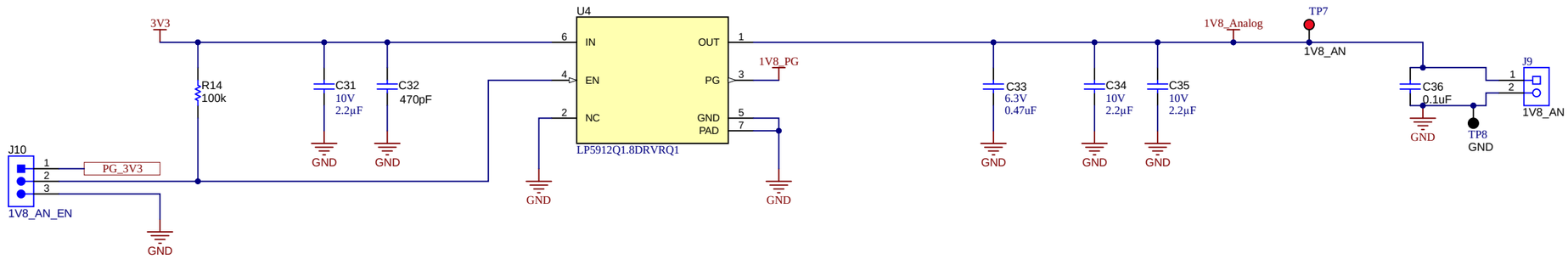
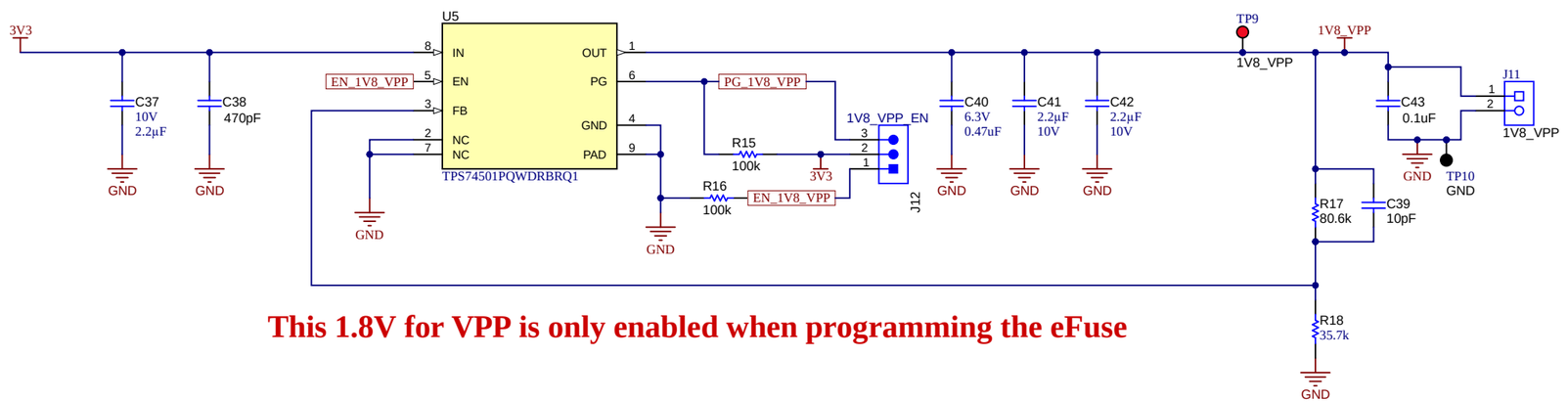
Main 1.8V



1V8_Analog



1V8_VPP



This 1.8V for VPP is only enabled when programming the eFuse

Orderable: ChangeMe in variant	Designed for: Custom	Mod. Date: 11/14/2023
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SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 3 of 7
Drawn By: Cameron Hagg	File: 1V8_outputs.SchDoc	Size: B
Engineer: Josh Mandelcorn	Contact: http://www.ti.com/support	

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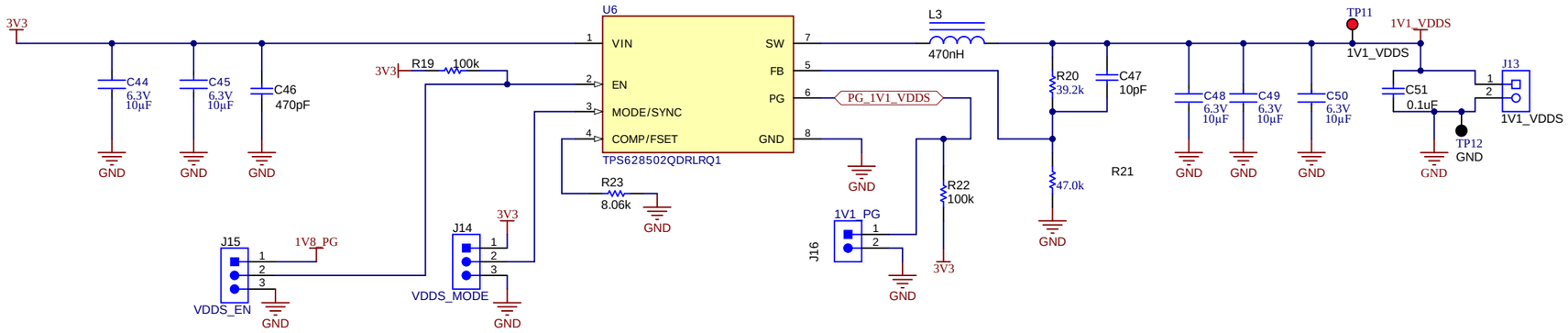
1V1_VDDS

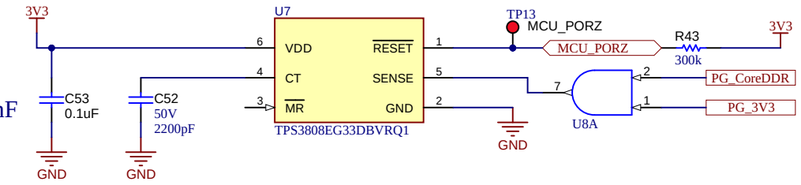


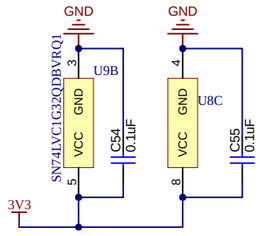
Sequencing Logic for VDD & VDDR Cores and MCU_PORZ signal

MCU_PORZ signal for ramp-up sequencing of main MCU after power supplies to it are up

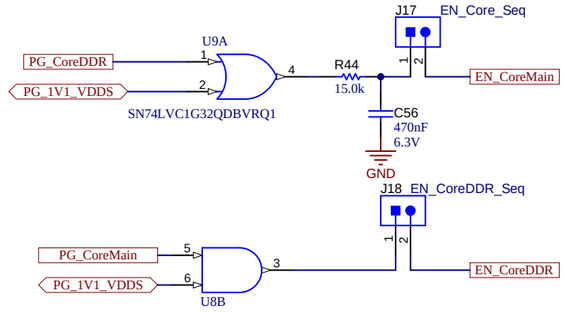
Programmable delay of ~13ms. Minimum 9.5ms

CT = [Td - 0.5E-3]*175
CT = [10- 0.5E-3]*175 > 1.66 nF





If either VDDS_1V1 rail OR VDDR_CORE rail are ON, then VDD_CORE must get enabled



Both VDDS_1V1 AND VDD_CORE to be powered up BEFORE VDDR_CORE is enabled

Orderable: ChangeMe in variant	Designed for: Custom	Mod. Date: 11/14/2023
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SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 4 of 7
Drawn By: Cameron Hagg	File: 1v1_&CoreSeq.SchDoc	Size: B
Engineer: Josh Mandelcorn	Contact: http://www.ti.com/support	

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Main Core 750mV

U11
TPS62871QWRXSRQ1
VIN
VIN
EN
MODE/SYNC
SYNC_OUT
FSEL
SCL
SDA
SW
VOSNS
GOSNS
PG
COMP
VSEL
Thermal_Pad
GND
GND
L4
0.11uH
C58 10uF
C59 2.2µF 10V
C60 470pF
C61 10uF
C62 2.2µF 10V
C63 470pF
R25 100k
EN_CoreMain
MODE/SYNC_U1
R27 0
R28 6.19k
FSEL short to VIN - 3MHz
FSEL 47kOhm to VIN - 2.5MHz
FSEL 6.2kOhm to GND - 2.25MHz
FSEL short to GND - 1.5MHz
C68 6.3V 0.47uF
C69 22uF
C70 22uF
C71 100µF
C72 100µF
C73 100µF
C74 6.3V 0.47uF
C75 22uF
C76 22uF
C77 100µF
C78 100µF
C79 100µF
C80 0.1uF
C81 6800pF
C82 10pF
R26 1.30k
R29 0
VSEL Short to GND - 0.75V
Set VSET[7:0] to 0x5a for 0.850mV
VOSNS
NT1 Net-Tie
0v75_Main
GOSNS
NT2 Net-Tie
VDD_CORE
J19
J20
J22
PG_CoreMain
J21
CORE_EN&PG
R30 100k
BY_A
BY_B
J23
J24
BY_A connected: 0.85V TPS628501-Q1 enabled
BY_B connected: 0.85V TPS628501-Q1 bypassed (TPS62871-Q1 supplies both rails).
Do NOT connect both jumpers
TP14
0v85_DDR
DDR_CORE
J25
CORE_MODE
U12
TPS628501QDRLRQ1
VIN
EN
MODE/SYNC
COMP/FSET
SW
FB
PG
GND
L5
680nH
PG_CoreDDR
R34 8.06k
R32 40.2k
R33 97.6k
C86 10pF
C83 6.3V 10µF
C84 6.3V 10µF
C85 470pF
R31 100k
C87 0.1uF
C88 6.3V 10µF
C89 6.3V 10µF
C90 6.3V 10µF
C91 0.1uF
TP15
J26
J27
DDR_EN
EN_CoreDDR
PG_CoreDDR
R35 100k
J29
DDR_MODE
DDR Core 850mV
J28
USB1
R36 2.00k
R37 2.00k
SCL
SDA
Dynamic Load Tester
Signal generator input
J30
Sig-Gen
R-SG1 1.00
R-SG2 10.0k
Q3
Q-DL
R-GB1 0.1
C-GB1 0.1uF
J-Isns
R-Isns1 49.9
J31
J-Vsns
J32
RVsns1 49.9
Pulse mode
50Hz setting
duty at 5%
Leading ~1usec
trailing ~1usec
Pulse height 1.2-2V typically

Orderable: ChangeMe in variant		Designed for: Custom	Mod. Date: 11/14/2023
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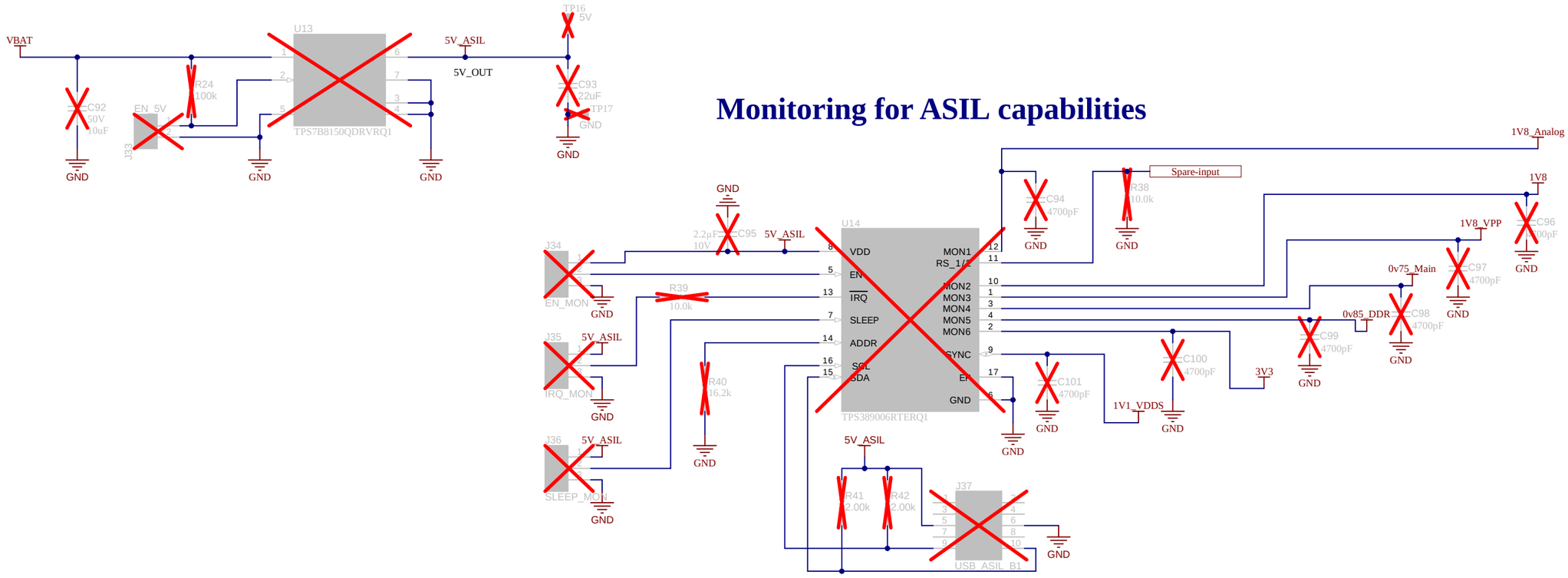
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 5 of 7
Drawn By: Cameron Hagg		File: Core_Main&DDR.SchDoc	Size: B
Engineer: Josh Mandelcorn		Contact: http://www.ti.com/support	

Monitoring for ASIL capabilities



Orderable: ChangeMe in variant		Designed for: Custom	Mod. Date: 11/14/2023
TID #: N/A		Project Title: PMP23242	
Number: PMP23242	Rev: B	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 6 of 7
Drawn By: Cameron Hagg		File: ASIL.SchDoc	Size: B
Engineer: Josh Mandelcorn		Contact: http://www.ti.com/support	

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HARDWARE

MP1 2563

MP2 2563

MP3 2563

MP4 2563

FID1 FID2 FID3

PCB Number: PMP23242
PCB Rev: B

PCB LOGO
Texas Instruments

PCB LOGO
FCC disclaimer

PCB LOGO
WEEE logo

Orderable: ChangeMe in variant		Designed for: Custom	Mod. Date: 5/1/2023
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Number: PMP23242	Rev: B	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 7 of 7
Drawn By: Cameron Hagg		File: Hardware.SchDoc	Size: B
Engineer: Josh Mandelcorn		Contact: http://www.ti.com/support	

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