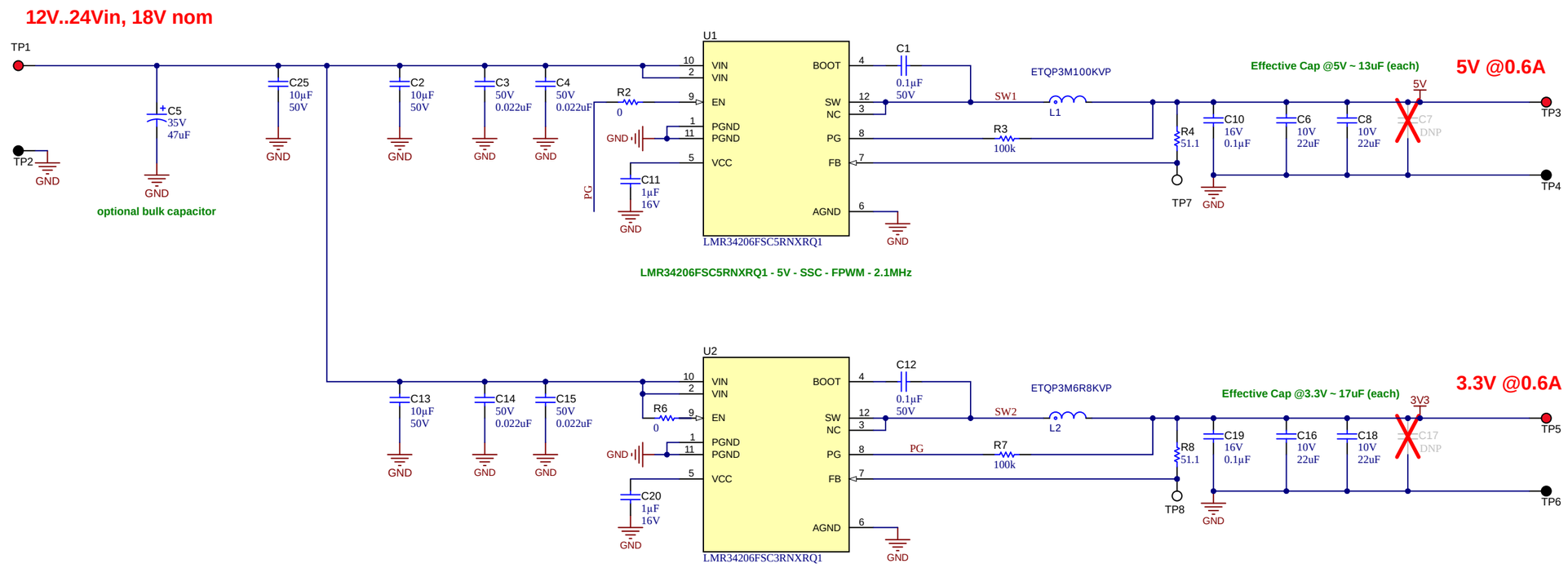
Design Notes:

- Inductor and output capacitors should be optimized according to stability and load transient requirements in the lab

- DNP: Do Not Place

- R4, R8 are only placed for measurement purpose



Orderable: ChangeMe in variant	Designed for: Public Release	Mod. Date: 10/16/2023
TID #: N/A	Project Title: Dual Buck for C2000	
Number: PMP31273 Rev: A	Sheet Title: Power	
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 1 of 2
Drawn By: S. Panaro	File: PMP31273 RevA_Power.SchDoc	Size: B
Engineer: S.Panaro; S.Dotan	Contact: http://www.ti.com/support	

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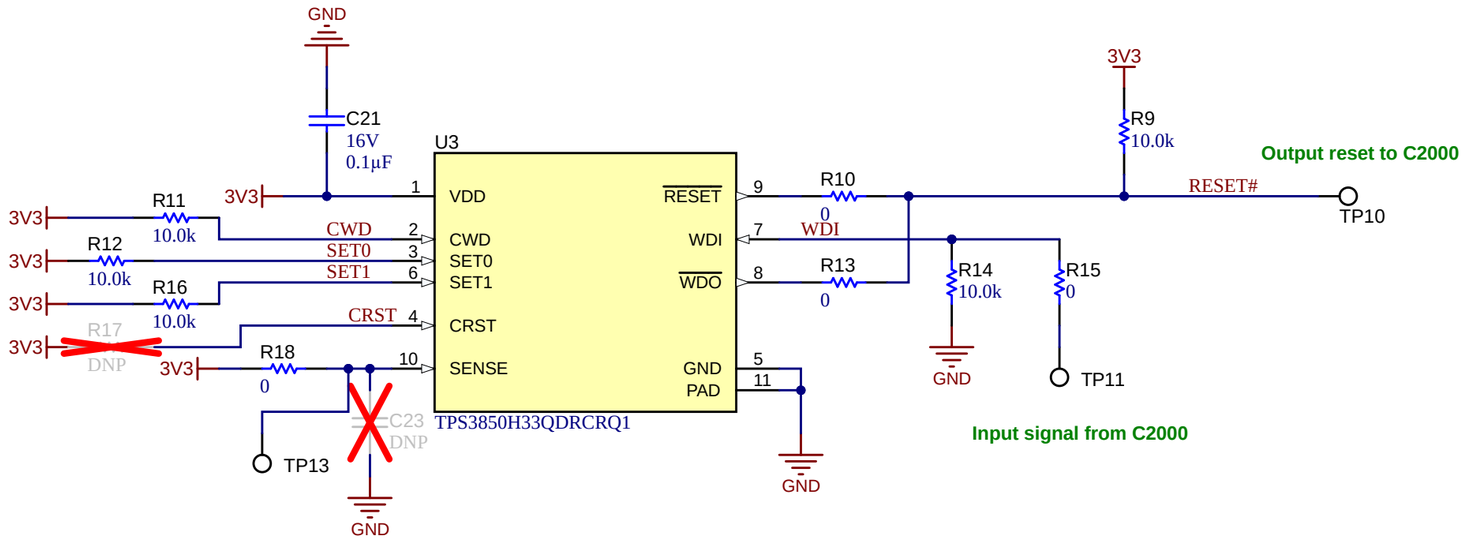
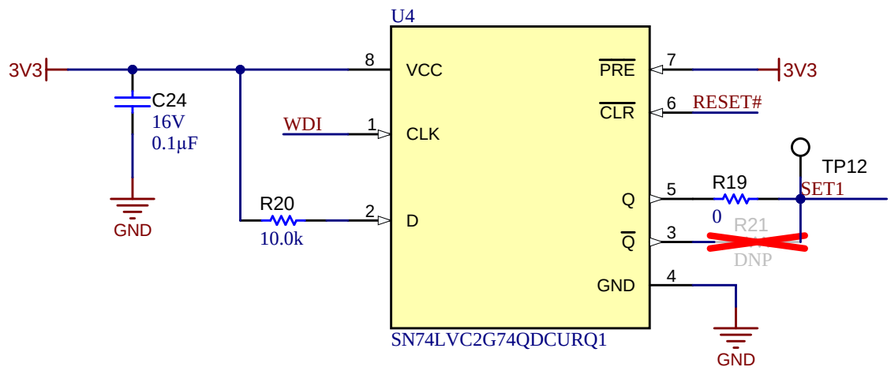
Design Notes:

- CRST, CWD, SET0 and SET1 setting should be selected according to the application requirements

- DNP: Do Not Place



SET1 = 0 until first WDI pulse from C2000



Orderable: ChangeMe in variant		Designed for: Public Release	Mod. Date: 10/16/2023
TID #: N/A		Project Title: Dual Buck for C2000	
Number: PMP31273	Rev: A	Sheet Title: Voltage Supervisor	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 2 of 2
Drawn By: S. Panaro		File: PMP31273 RevA_VoltageSupervisor.SchDoc	Size: A4
Engineer: S.Panaro; S.Dotan		Contact: http://www.ti.com/support	

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