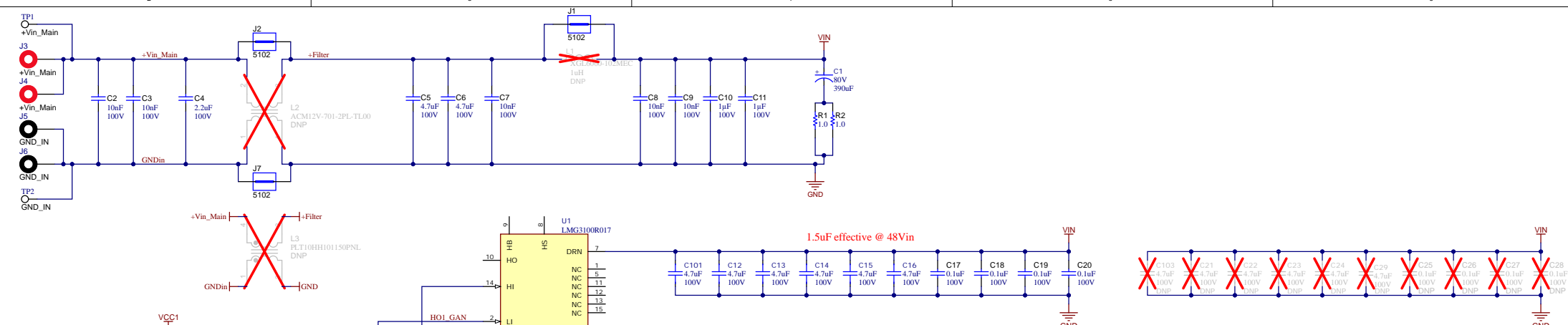
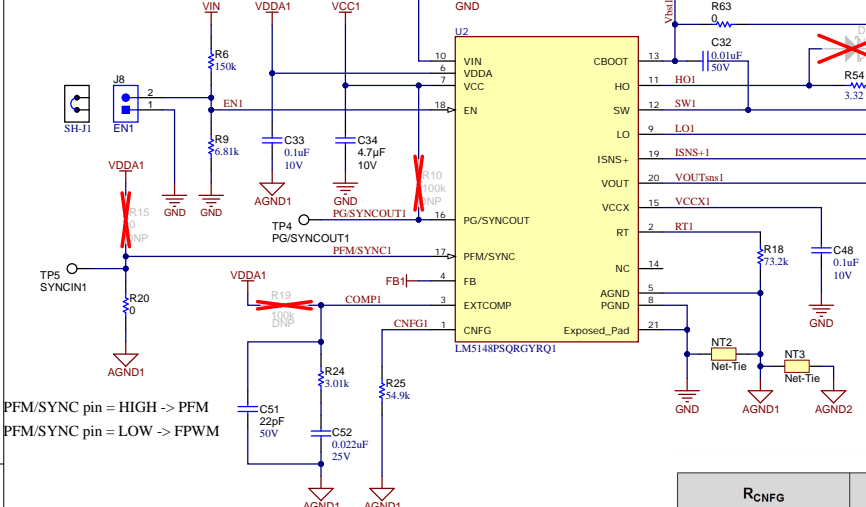


Input Voltage = 48Vin Nominal
(24Vin Min.; 60Vin Max.)



UVLO Rising/Enable = 23.0Vin
UVLO Falling/Disable = 20.0Vin



PFM/SYNC pin = HIGH -> PFM
PFM/SYNC pin = LOW -> FPWM

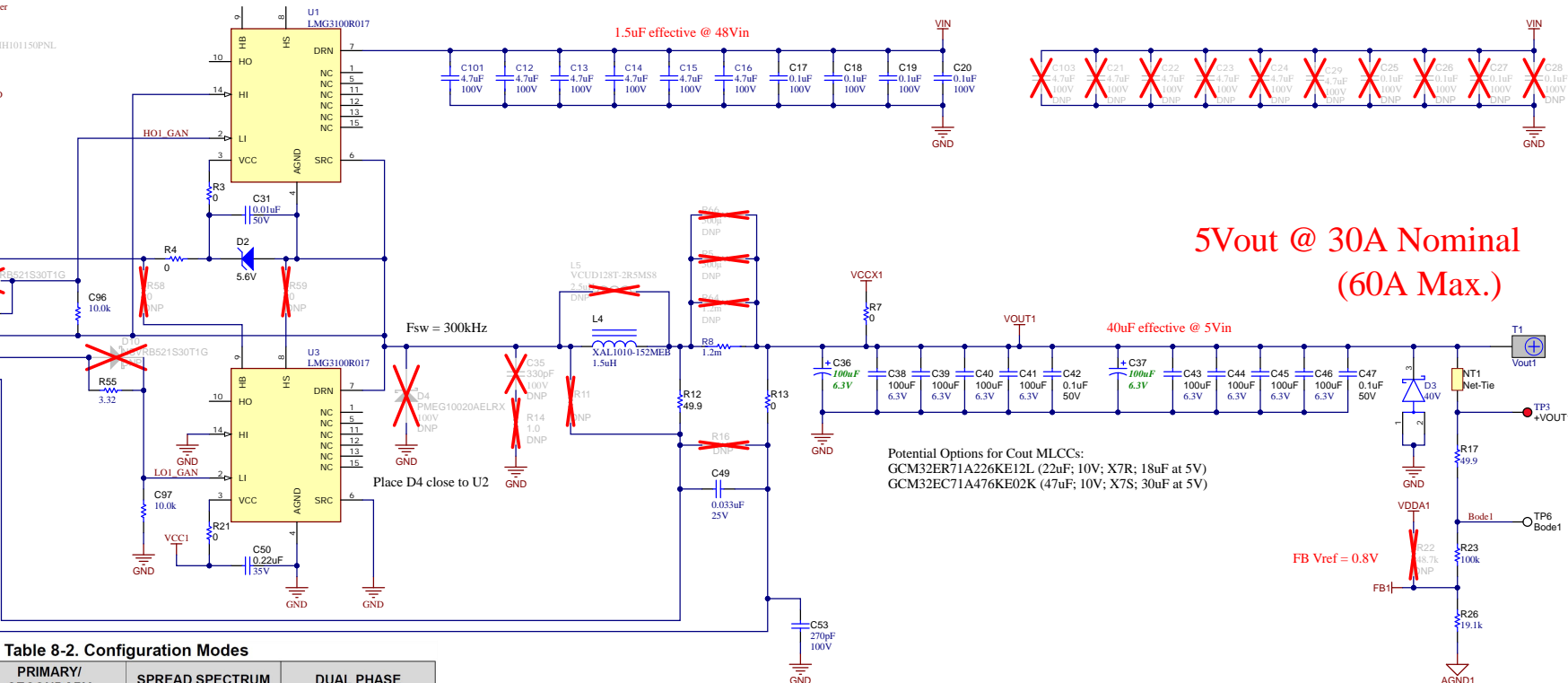
***NOTES:**

- D1 and D5 can be removed. The LM5148-Q1 contains internal bootstrap diodes.
- D3 and D7 protect the circuit from potential large negative voltages caused by short circuit applications using long lead wires on the output. These diodes may be omitted on a final system design.

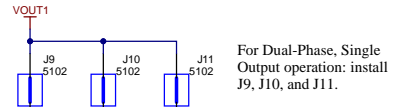
Table 8-2. Configuration Modes

R _{CNFg}	PRIMARY/SECONDARY	SPREAD SPECTRUM	DUAL PHASE
29.9 kΩ	Primary	OFF	Disabled
41.2 kΩ	Primary	ON	Disabled
54.9 kΩ	Primary	OFF	Enabled
71.5 kΩ	Primary	ON	Enabled
90.9 kΩ	Secondary	N/A	Enabled

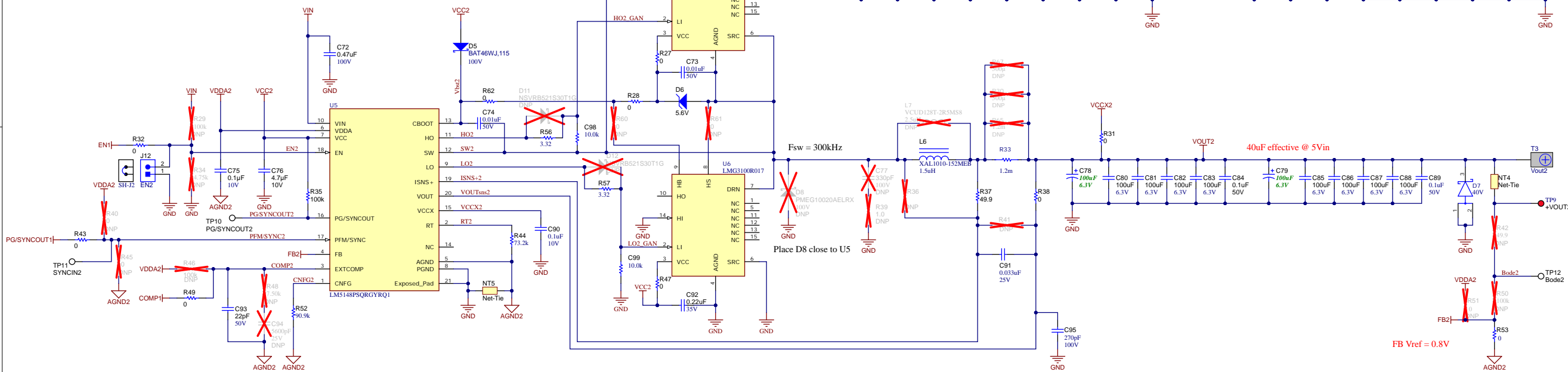
5Vout @ 30A Nominal
(60A Max.)



Potential Options for Cout MLCCs:
GCM32ER71A226KE12L (22uF; 10V; X7R; 18uF at 5V)
GCM32EC71A476KE02K (47uF; 10V; X7S; 30uF at 5V)



For Dual-Phase, Single Output operation: install J9, J10, and J11.



H1 NY PMS 440 0025 PH
 H2 NY PMS 440 0025 PH
 H3 NY PMS 440 0025 PH
 H4 NY PMS 440 0025 PH

H5 1902C
 H6 1902C
 H7 1902C
 H8 1902C

~~FID1~~ ~~FID2~~ ~~FID3~~ ~~FID4~~ ~~FID5~~ ~~FID6~~

PCB Number: PMP23392
 PCB Rev: A



PCB LOGO
 FCC disclaimer

PCB LOGO
 WEEE logo

Variant/Label Table

Variant	Label Text
001	

LBL1
 PCB Label
 THT-14-423-10
 Size: 0.65" x 0.20 "

Orderable: ChangeMe in variant	Designed for:	Mod. Date: 8/9/2023
TID #: PMP23392	Project Title: Dual-Phase LM5148-Q1 Buck Using GaN FETs	
Number: PMP23392	Rev: -1	Sheet Title:
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 2 of 2
Drawn By:	File: PMP23392_Hardware.SchDoc	Size: B
Engineer: Hrag Kasparian	Contact: http://www.ti.com/support	

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