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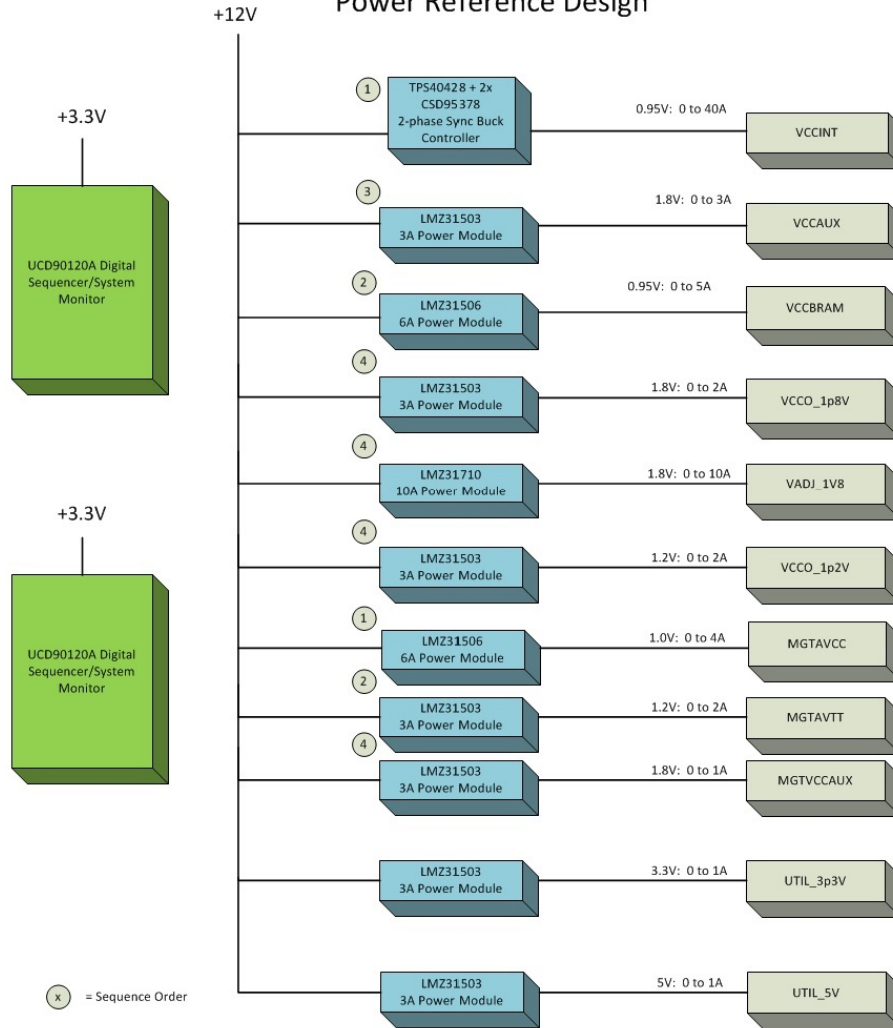
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(x) = Sequence Order

PMP9444 Ultrascale Kintex FPGA

Power Reference Design



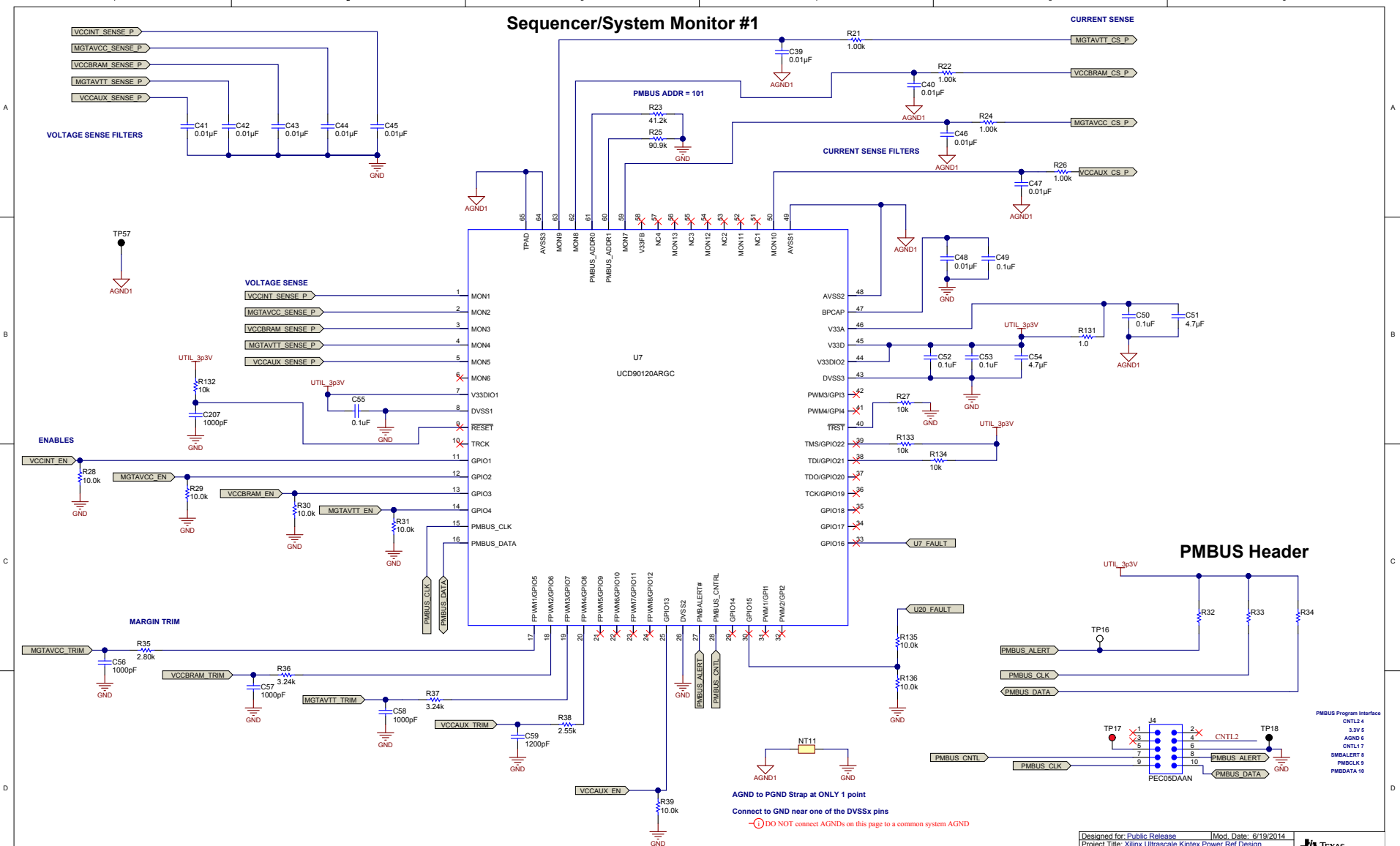
| Revision History | |
|------------------|-------|
| Revision | Notes |
| | |

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| | | |
|--|--|---------------------|
| Number: PMP9444 | Rev: E2 | Mod Date: 6/27/2014 |
| Project Title: Xilinx Ultrascale Kintex Power Ref Design | | |
| Sheet Title: Cover Sheet | | |
| SVN Rev: Not in version control | Assembly Variant: (No Variations) | Sheet: 1 of 15 |
| Drawn By: Sami Sirhan | File: SA1011E2_Cover_SchDoc | Size: B |
| Engineer: Sami Sirhan | Contact: http://www.ti.com/support | |

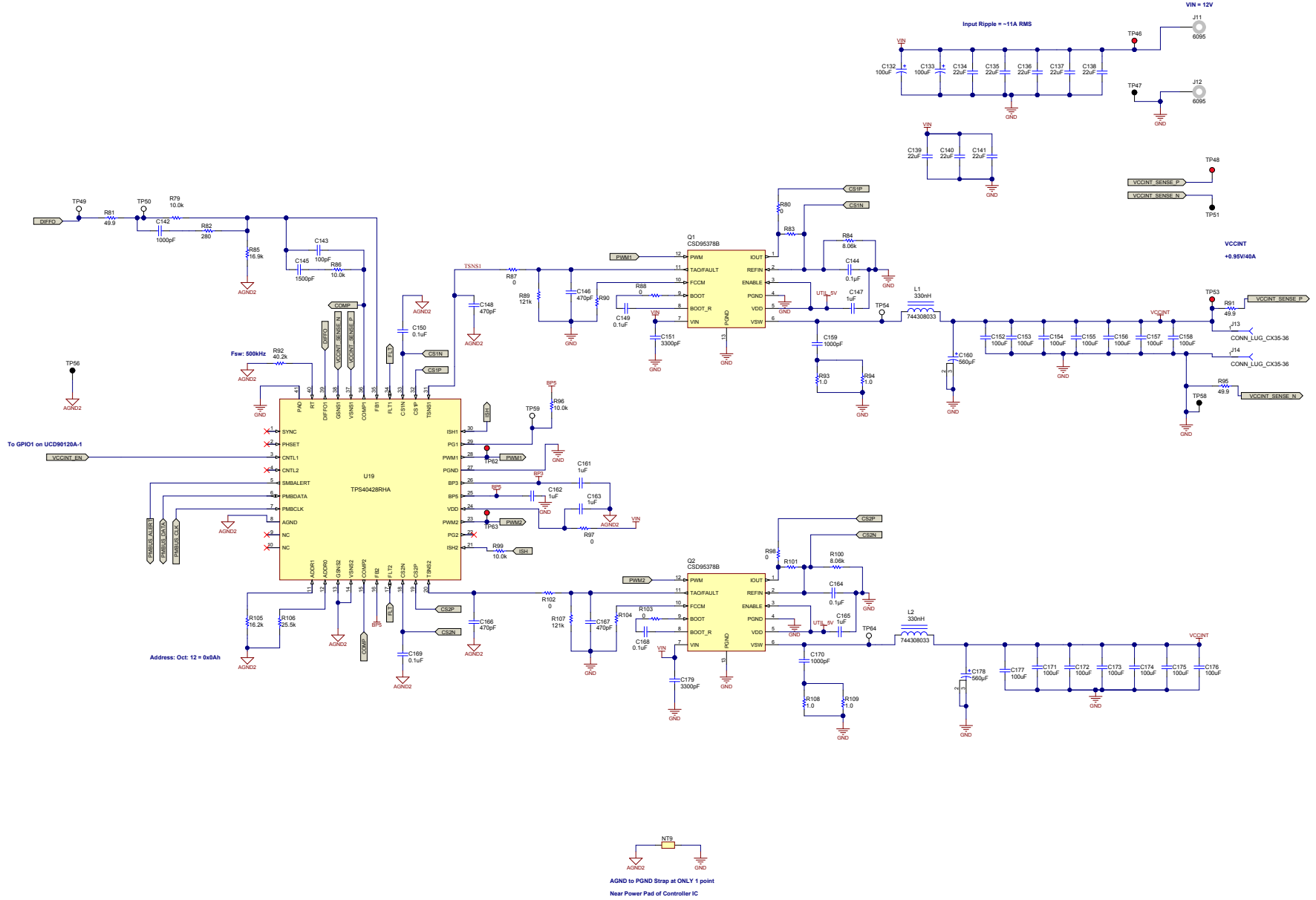


Sequencer/System Monitor #1



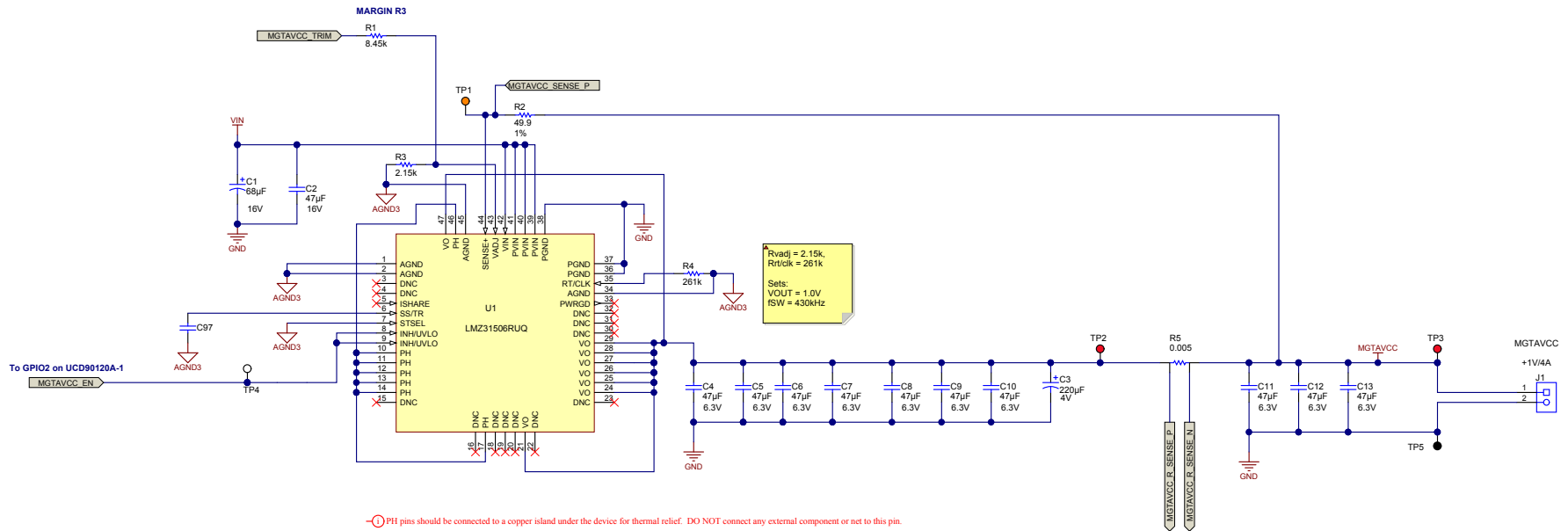
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VCCINT: 0.95V@40A

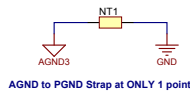


AGND to PGND Strap at ONLY 1 point
Near Power Pad of Controller IC

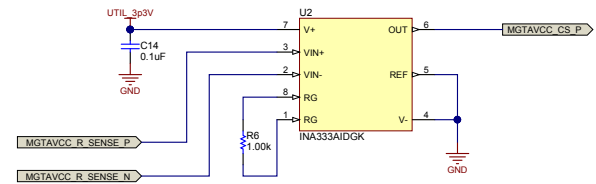
MGTAVCC 1.0V @ 4A



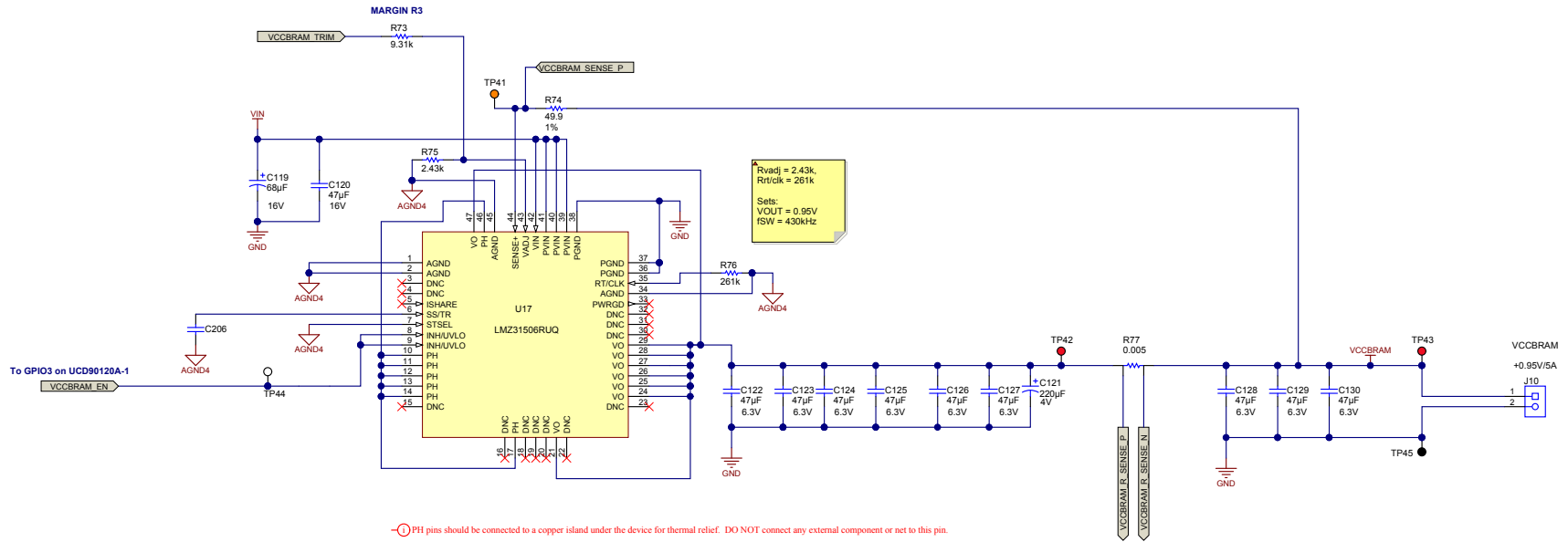
- ⊖ PH pins should be connected to a copper island under the device for thermal relief. DO NOT connect any external component or net to this pin.
- ⊖ DO NOT connect AGNDs on this page to a common system AGND



MGTAVCC 0A-4A => CS = 0V - 2.015V
G = 100.75, Rg = 1k

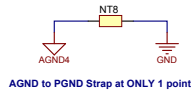


VCCBRAM 0.95V @ 5A

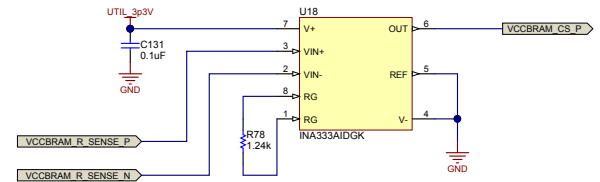


$R_{\text{vadj}} = 2.43\text{k}$
 $R_{\text{rt}/\text{clk}} = 261\text{k}$
 Sets:
 $V_{\text{OUT}} = 0.95\text{V}$
 $f_{\text{SW}} = 430\text{kHz}$

- Ⓢ PH pins should be connected to a copper island under the device for thermal relief. DO NOT connect any external component or net to this pin.
- Ⓢ DO NOT connect AGNDs on this page to a common system AGND



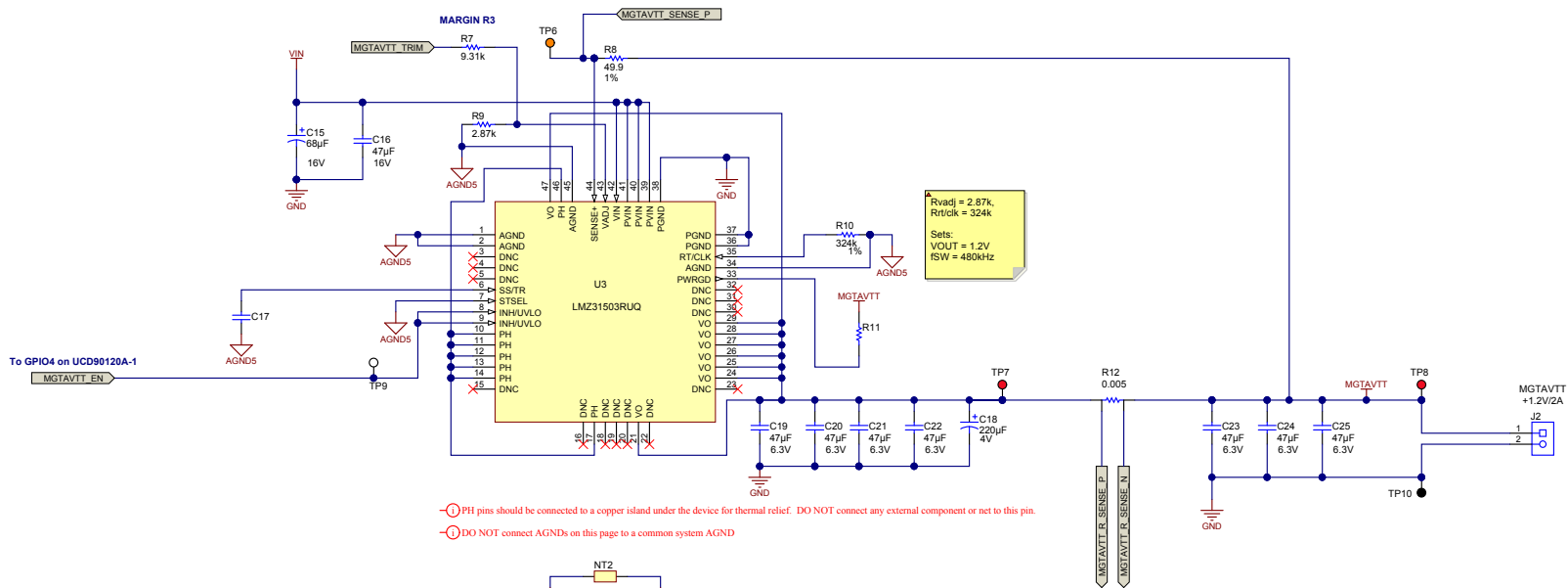
VCCBRAM 0A-5A => CS = 0V - 2.015V
 $G = 80.6$, $R_g = 1.24\text{k}$



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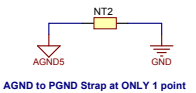
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| Number: PMP9444 | Rev: E2 | Designed for: Public Release | Mod. Date: 6/19/2014 |
| SVN Rev.: Not in version control | | Project Title: Xilinx Ultrascale Kintex Power Ref Design | |
| Drawn By: Sami Sirhan | | Sheet Title: VCCBRAM | Sheet 5 of 15 |
| Engineer: Sami Sirhan | File: SA17101E2_VCCBRAM_0p95V_5A_SchDoc | Assembly Variant: (No Variations) | Size: B |
| Contact: http://www.ti.com/support | | http://www.ti.com | |

MGTAVTT: 1.2V @ 2A

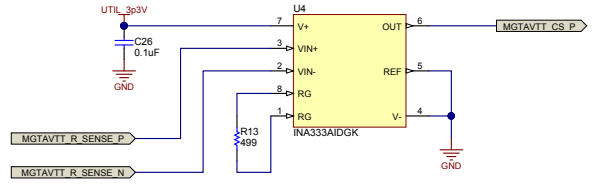


$R_{vadj} = 2.87k$
 $R_{rtick} = 324k$
 Sets:
 $V_{OUT} = 1.2V$
 $f_{SW} = 480kHz$

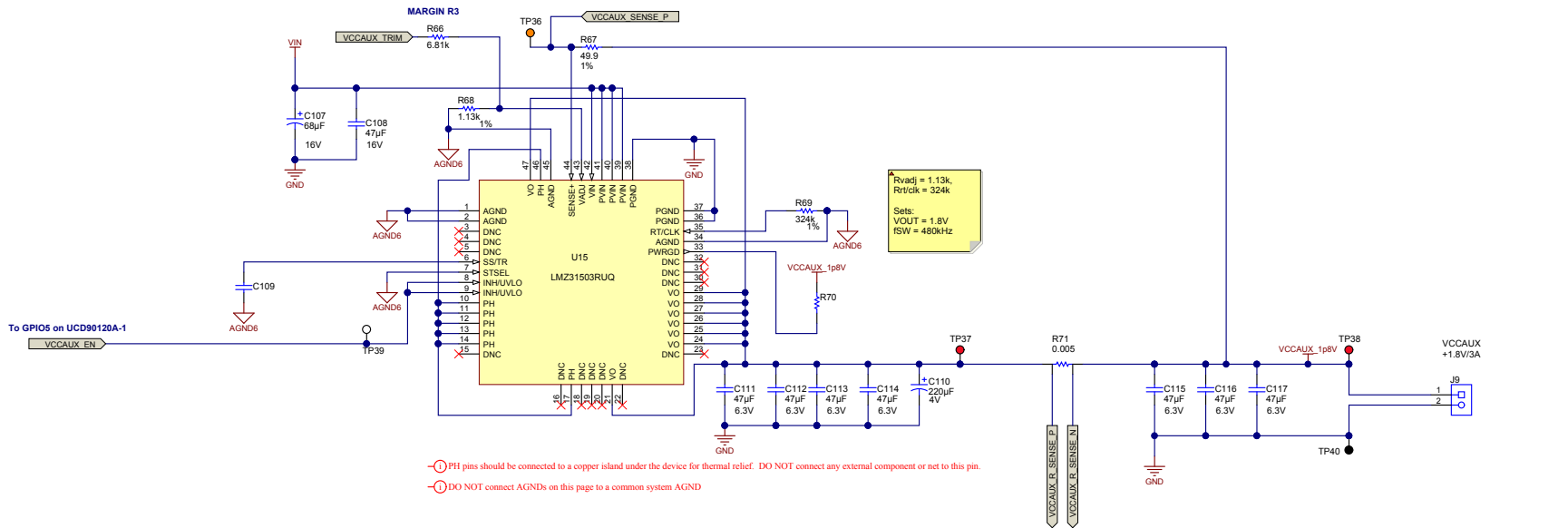
- ⊖ PH pins should be connected to a copper island under the device for thermal relief. DO NOT connect any external component or net to this pin.
- ⊖ DO NOT connect AGNDs on this page to a common system AGND



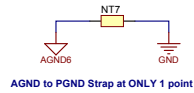
MGTAVTT 0A-2A => CS = 0V - 2.015V
 $G = 201.5, R_g = 499$



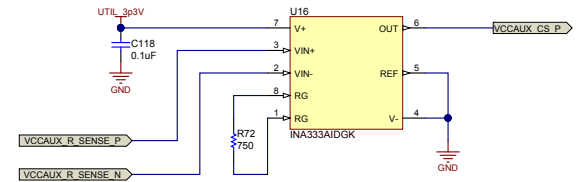
VCCAUX: 1.8V @ 3A



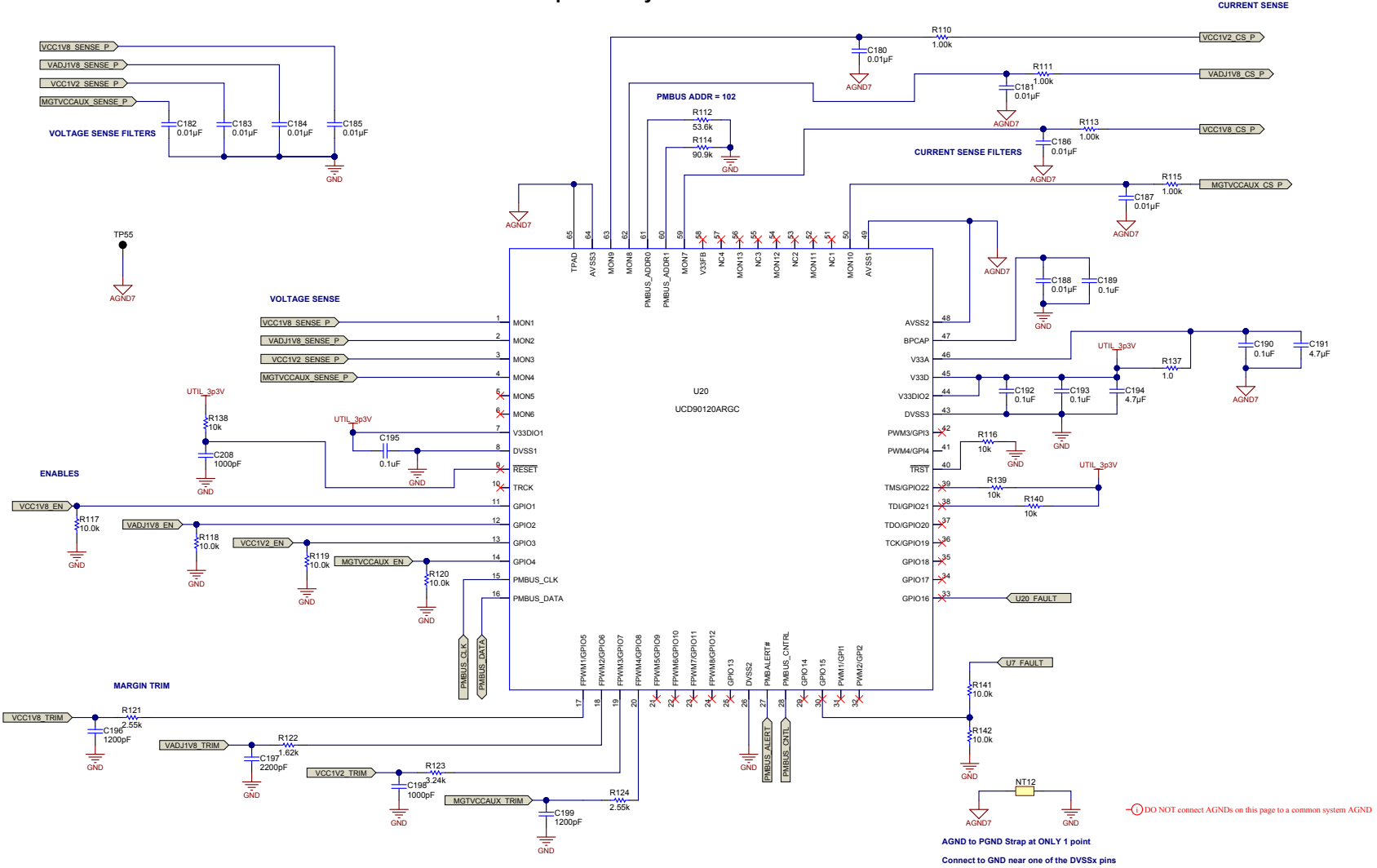
- PH pins should be connected to a copper island under the device for thermal relief. DO NOT connect any external component or net to this pin.
- DO NOT connect AGNDs on this page to a common system AGND



VCCAUX 0A-3A => CS = 0V - 2.015V
G = 134.3, Rg = 750



Sequencer/System Monitor #2



AGND to PGND Strap at ONLY 1 point
Connect to GND near one of the DVSSx pins

DO NOT connect AGNDs on this page to a common system AGND

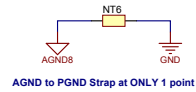
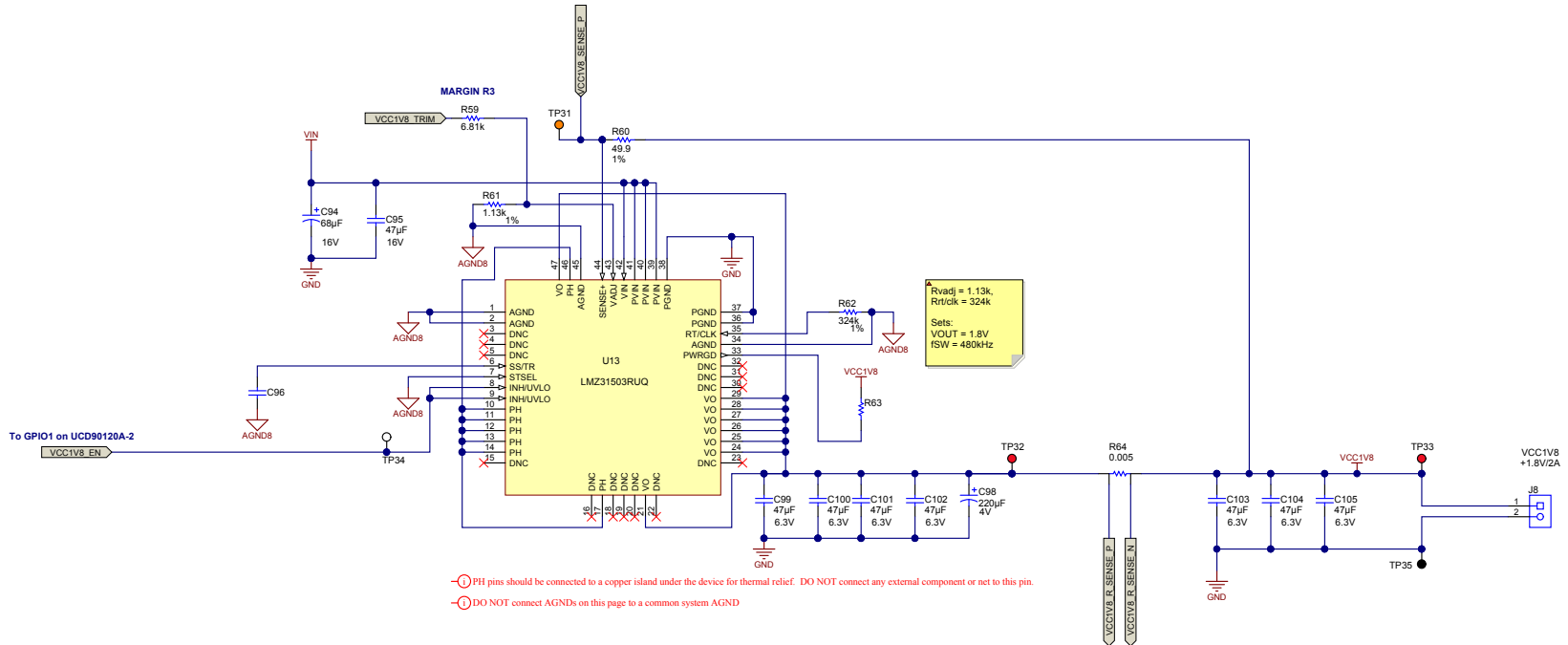
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|---------------------------------|-----------------------|--|---|
| Number: PMP9444 | Rev: E2 | Designed for: Public Release | Mod. Date: 6/19/2014 |
| SVN Rev: Not in version control | Drawn By: Sami Sirhan | Project Title: Xilinx Ultrascale Kintex Power Ref Design | Sheet Title: Sequencer 2 |
| Engineer: Sami Sirhan | | Assembly Variant: (No Variations) | File: SA1011E2_Sequencer-2_SchDoc |
| | | Sheet 8 of 15 | Size: B |
| | | Contact: http://www.ti.com/support | http://www.ti.com |

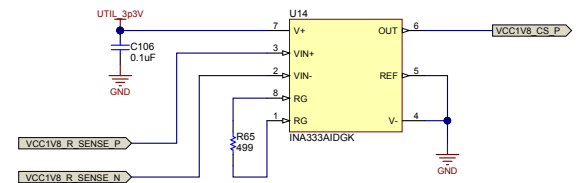


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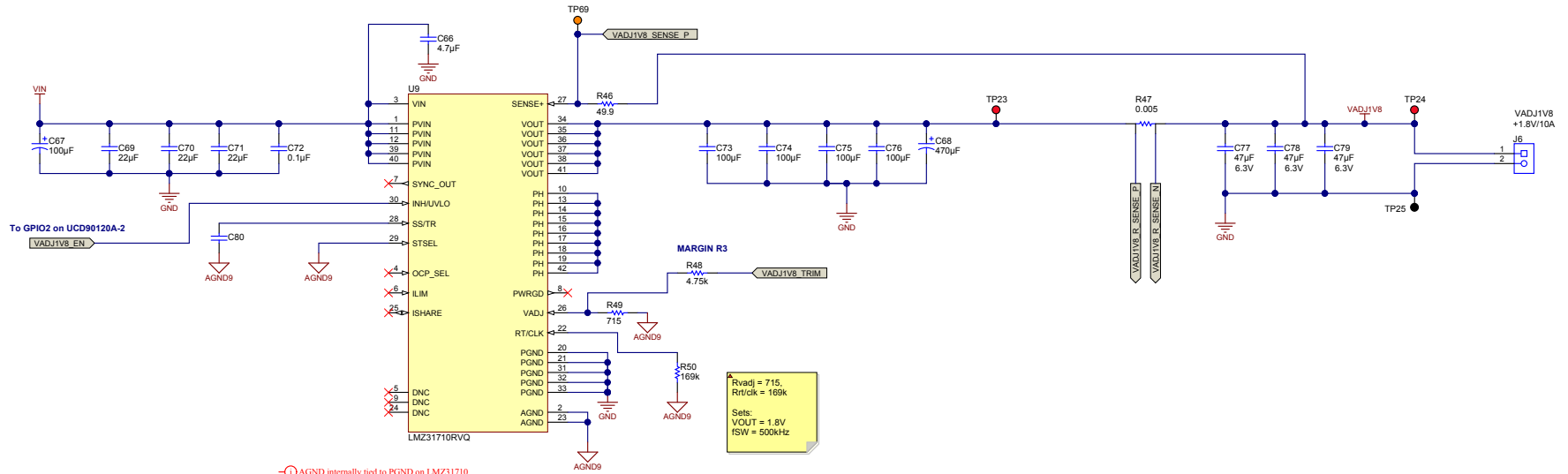
VCC1V8: 1.8V @ 2A



VCC1V8 0A-2A => CS = 0V - 2.015V
G = 201.5, Rg = 499

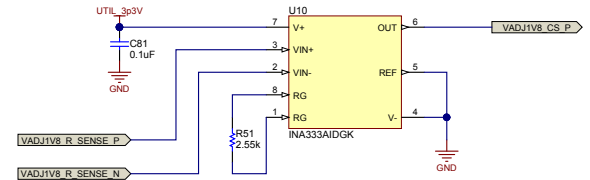


VADJ1V8: 1.8V @ 10A

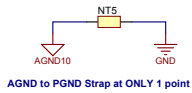
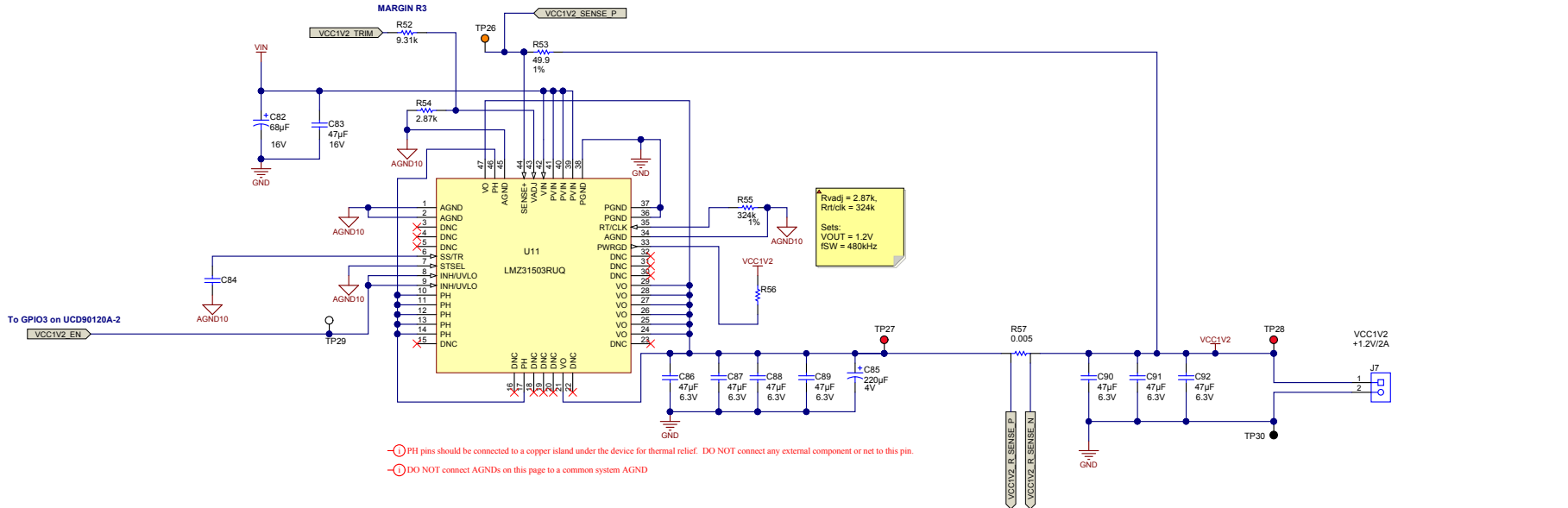


- AGND internally tied to PGND on LMZ31710
- PH pins should be connected to a copper island under the device for thermal relief. DO NOT connect any external component or net to this pin.
- DO NOT connect AGNDs on this page to a common system AGND

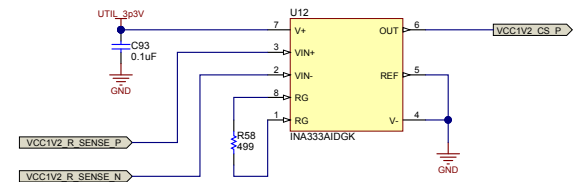
VADJ1V8 0A-10A => CS = 0V - 2.015V
 G = 40.3, Rg = 2.55k



VCC1V2: 1.2V @ 2A

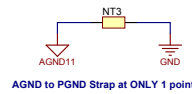
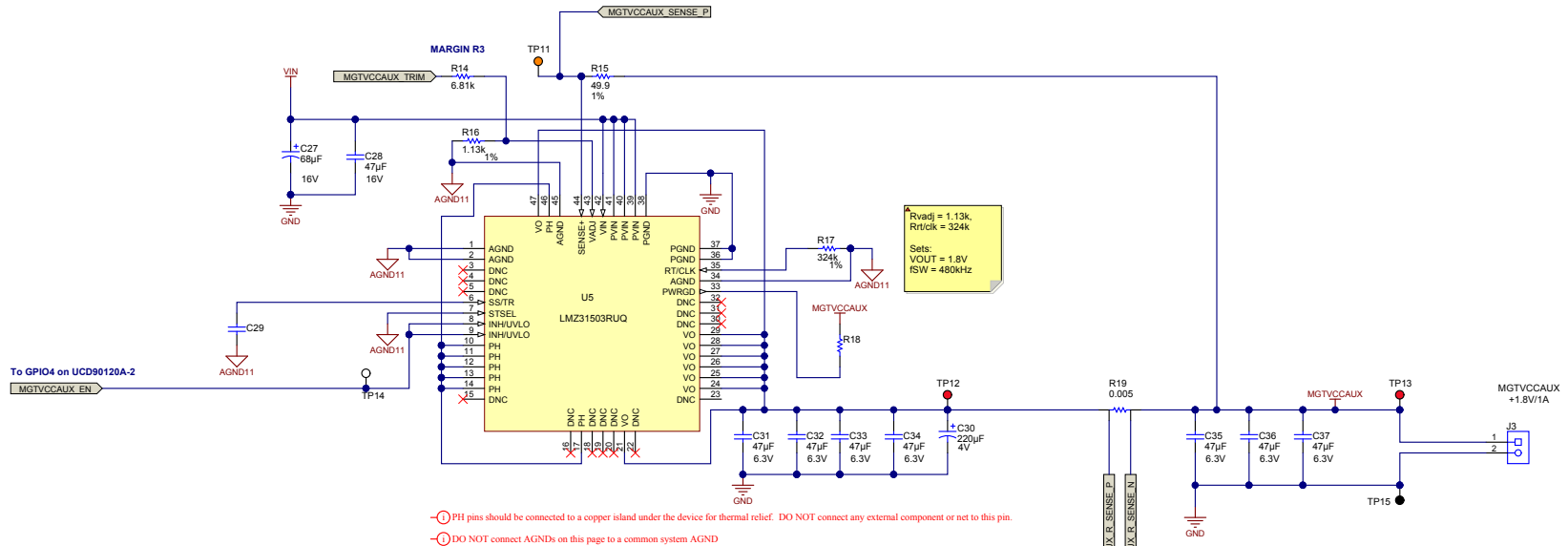


VCC1V2 0A-2A => CS = 0V - 0.015V
G = 201.5, Rg = 499

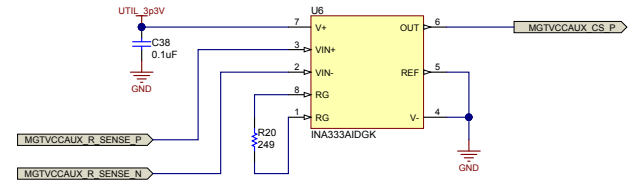


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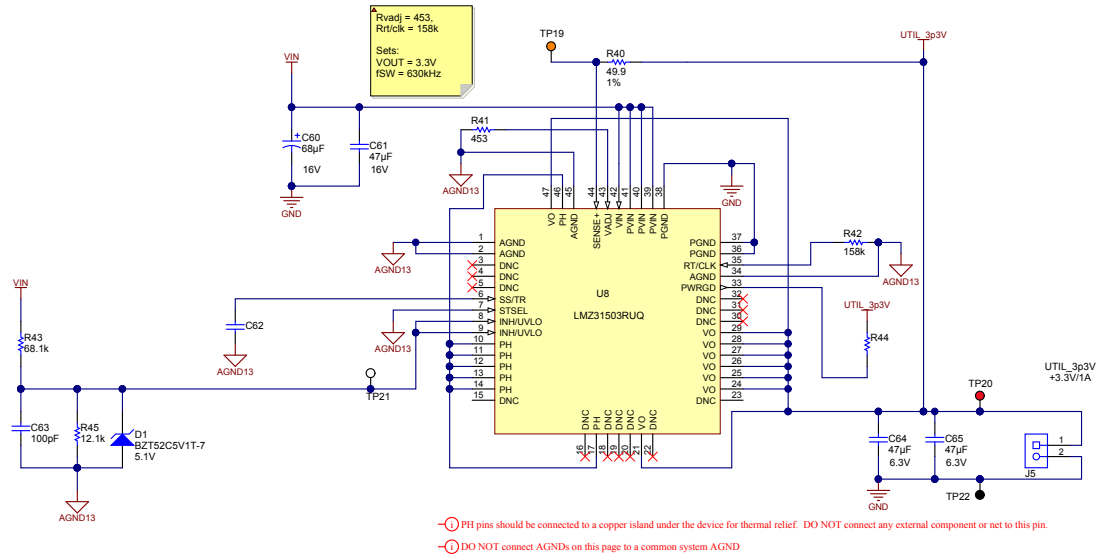
MGTVCCAUX: 1.8V @ 1A



MGTVCCAUX 0A-2A => CS = 0V - 2.015V
G = 403, Rg = 249

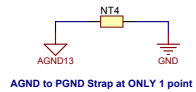


UTIL_3p3V: 3.3V @ 1A



R_{vadj} = 453,
R_{t/cik} = 158k
Sets:
V_{OUT} = 3.3V
f_{SW} = 630kHz

⓪ PH pins should be connected to a copper island under the device for thermal relief. DO NOT connect any external component or net to this pin.
⓪ DO NOT connect AGNDs on this page to a common system AGND

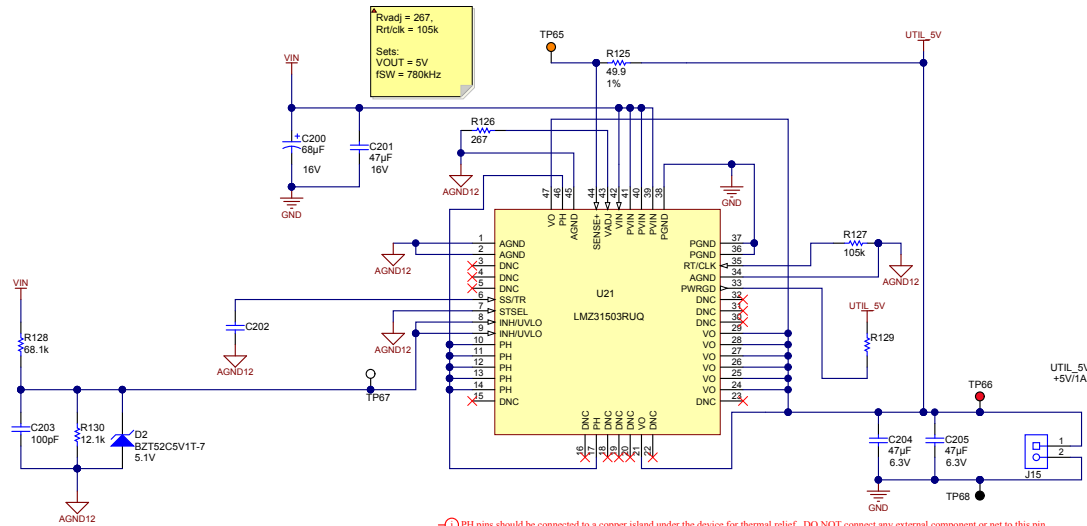


AGND to PGND Strap at ONLY 1 point

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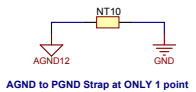
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| Number: PMP9444 | Rev: E2 | Designed for: Public Release | Mod. Date: 6/19/2014 | |
| SVN Rev.: Not in version control | Assembly Variant: (No Variations) | Project Title: Xilinx Ultrascale Kintex Power Ref Design | Sheet Title: UTIL_3p3V | |
| Drawn By: Sami Sirhan | File: SA/T101E2_UTIL_3p3V_1A.SchDoc | | Sheet: 13 of 15 | |
| Engineer: Sami Sirhan | Contact: http://www.ti.com/support | | Size: B | |

UTIL_5V: 5V @ 1A



Rvadj = 267
Rt/cik = 105k
Sets:
VOUT = 5V
ISW = 780kHz

- ⊖ PH pins should be connected to a copper island under the device for thermal relief. DO NOT connect any external component or net to this pin.
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| Number: PMP9444 | Rev: E2 | Sheet Title: UTIL_5V | | |
| SVN Rev.: Not in version control | | Assembly Variant: (No Variations) | Sheet: 14 of 15 | |
| Drawn By: Sami Sirhan | | File: SA10101E2_UTIL_5V_1A.SchDoc | Size: B | |
| Engineer: Sami Sirhan | | Contact: http://www.ti.com/support | | |

H1 NY PMS 440 0025 PH H2 NY PMS 440 0025 PH H3 NY PMS 440 0025 PH H4 NY PMS 440 0025 PH

H5 1902C H6 1902C H7 1902C H8 1902C

FID1 FID2 FID3
FID4 FID5 FID6

PCB Number: PMP9444
PCB Rev: E2

PCB
LOGO
Texas Instruments

| Label Table | |
|-------------|------------|
| Variant | Label Text |
| 001 | ChangeMe! |
| 002 | ChangeMe! |
| | |
| | |
| | |
| | |
| | |

222
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

223
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

224
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

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| Project Title: Xilinx Ultrascale Kintex Power Ref Design | | | |
| Number: PMP9444 | Rev: E2 | Sheet Title: Hardware | |
| SVN Rev.: Not in version control | | Assembly Variant: (No Variations) | Sheet: 15 of 15 |
| Drawn By: Sami Sirhan | | File: SA101101E2_Hardware.SchDoc | Size: B |
| Engineer: Sami Sirhan | | Contact: http://www.ti.com/support | |

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