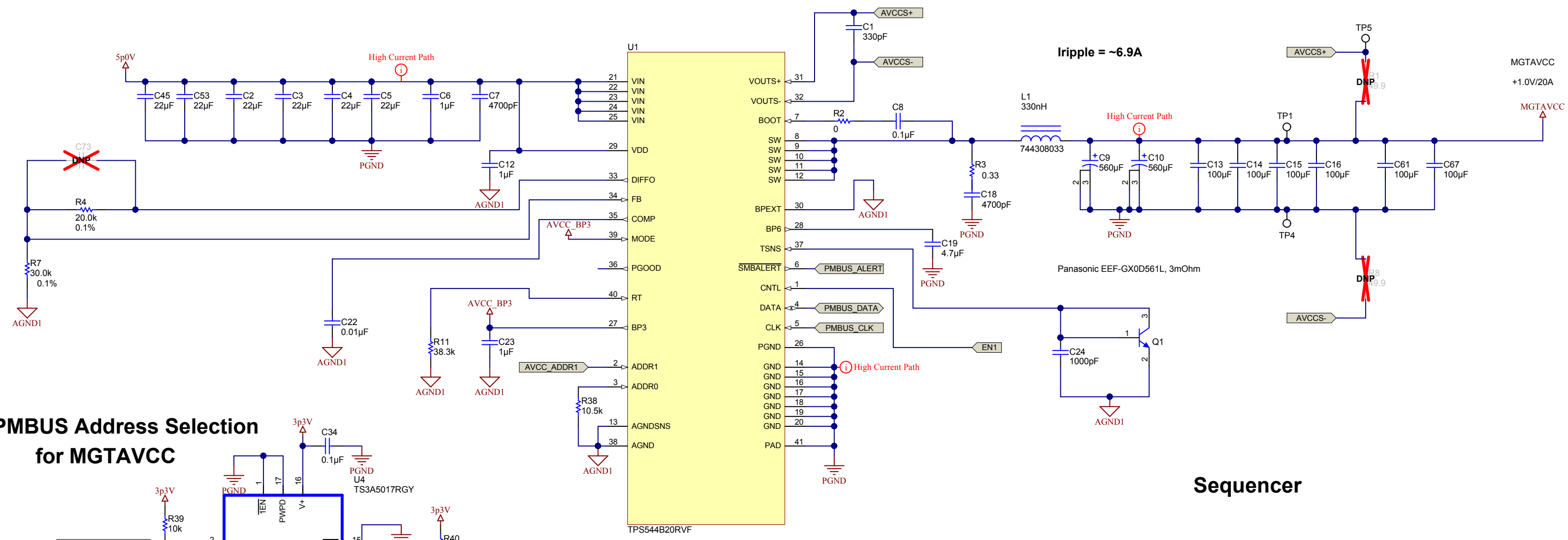
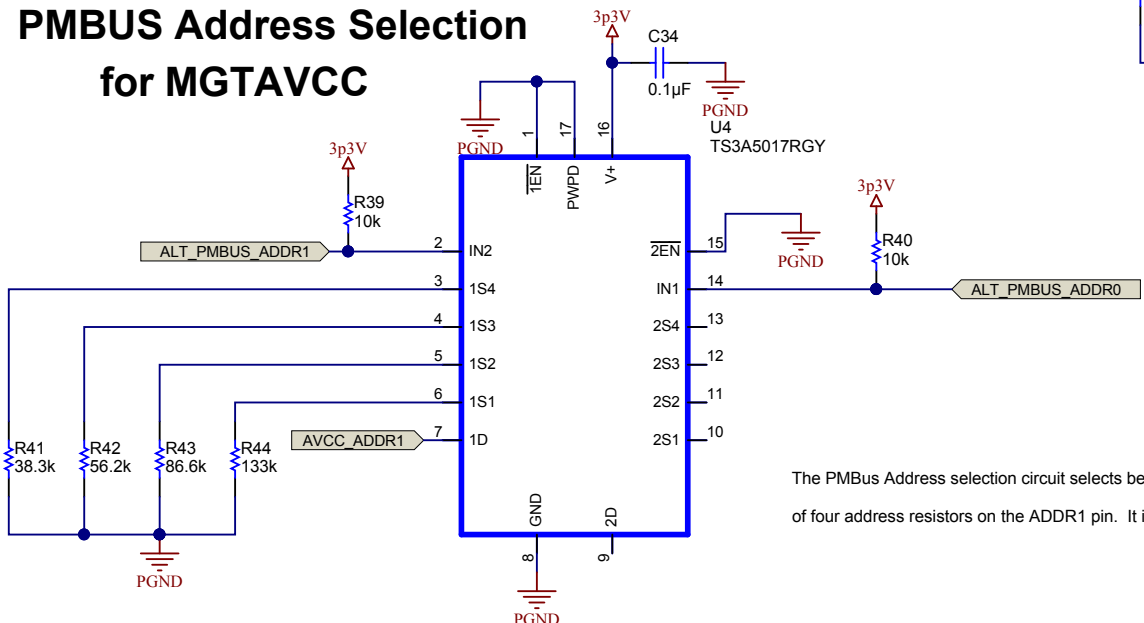


# MGTAVCC - 1.0V@20A



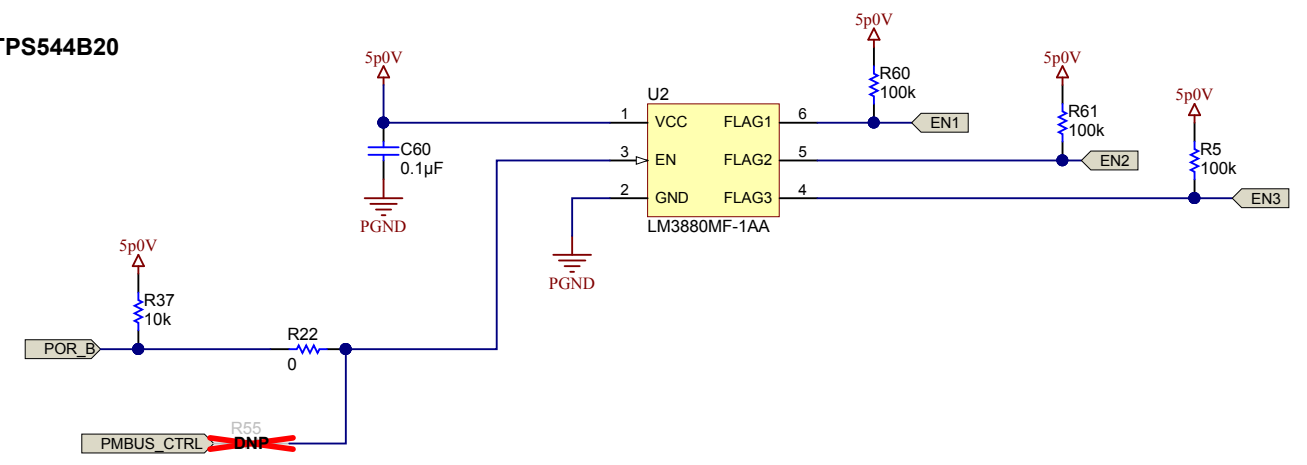
## PMBUS Address Selection for MGTAVCC



AGND internally connected to GND on TPS544B20

The PMBus Address selection circuit selects between one of four address resistors on the ADDR1 pin. It is not required in an end application.

## Sequencer



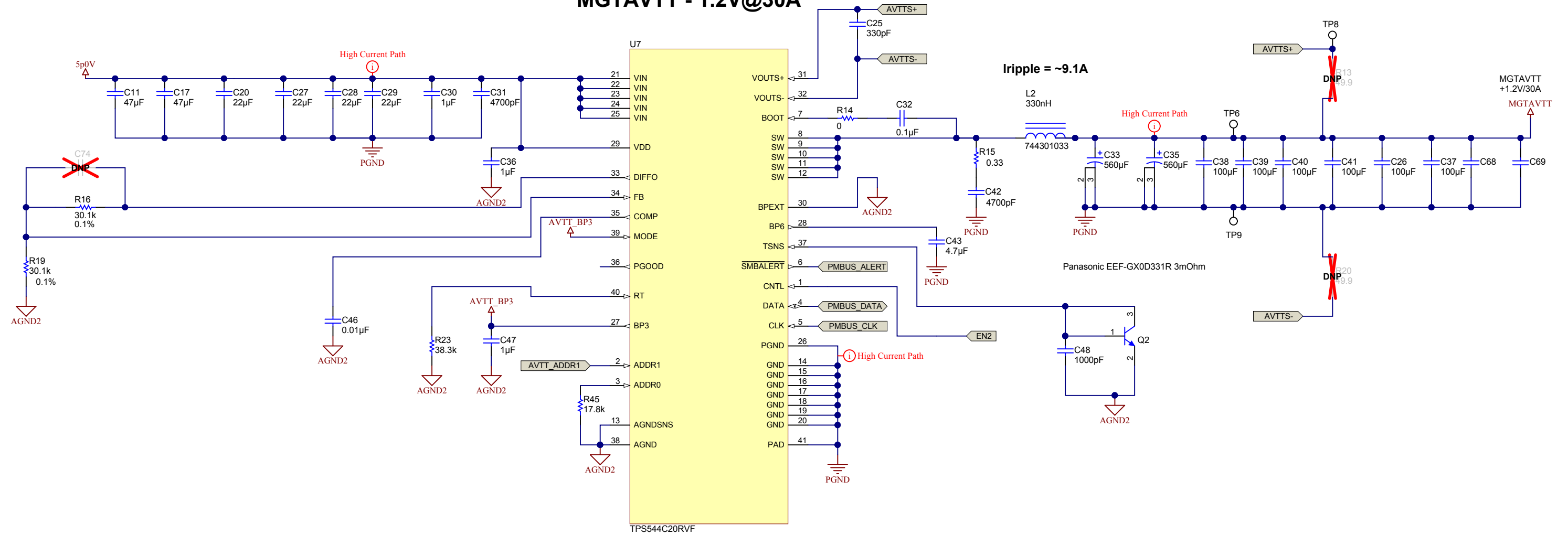
### FUNCTION TABLE

IN2	IN1	D TO S, S TO D
L	L	D = S <sub>1</sub>
L	H	D = S <sub>2</sub>
H	L	D = S <sub>3</sub>
H	H	D = S <sub>4</sub>

ALT_PMBUS_1	ALT_PMBUS_0	HEX	OCTAL	Raddr1 (kohm)	Raddr0 (kohm)
GND	GND	0x30	60	133	10.5
GND	OPEN	0x28	50	86.6	10.5
OPEN	GND	0x20	40	56.2	10.5
OPEN	OPEN	0x18	30	38.3	10.5

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# MGTAVTT - 1.2V@30A



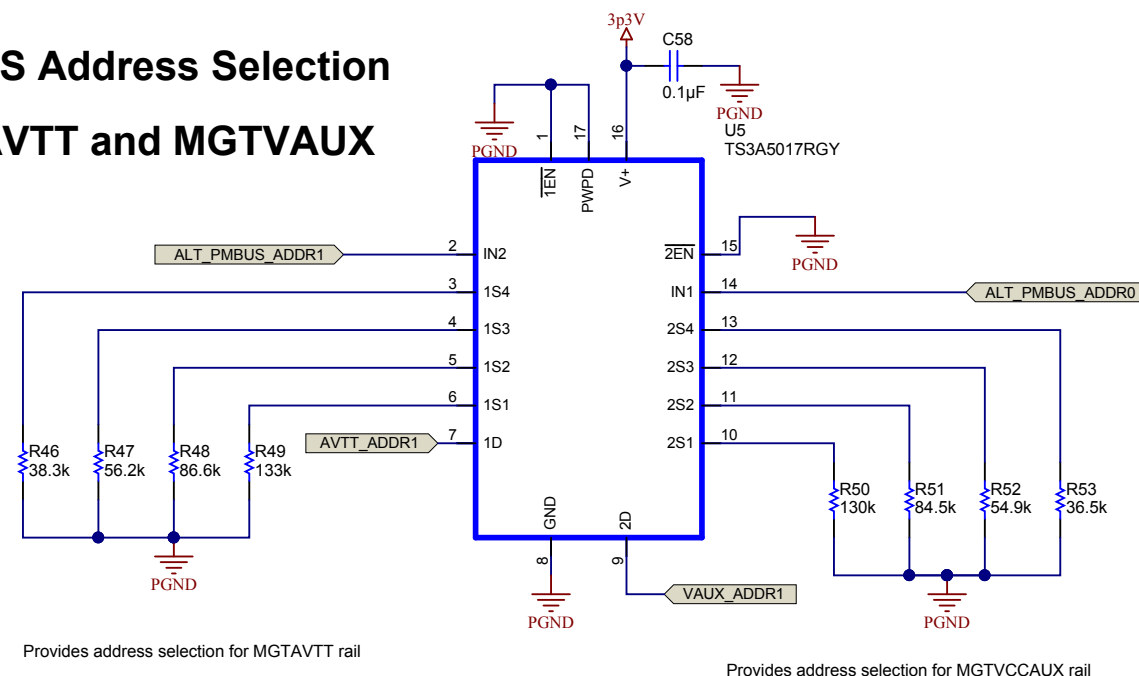
AGND internally connected to GND on TPS544C20

## PMBUS Address Selection for MGTAVTT and MGTVAUX

FUNCTION TABLE

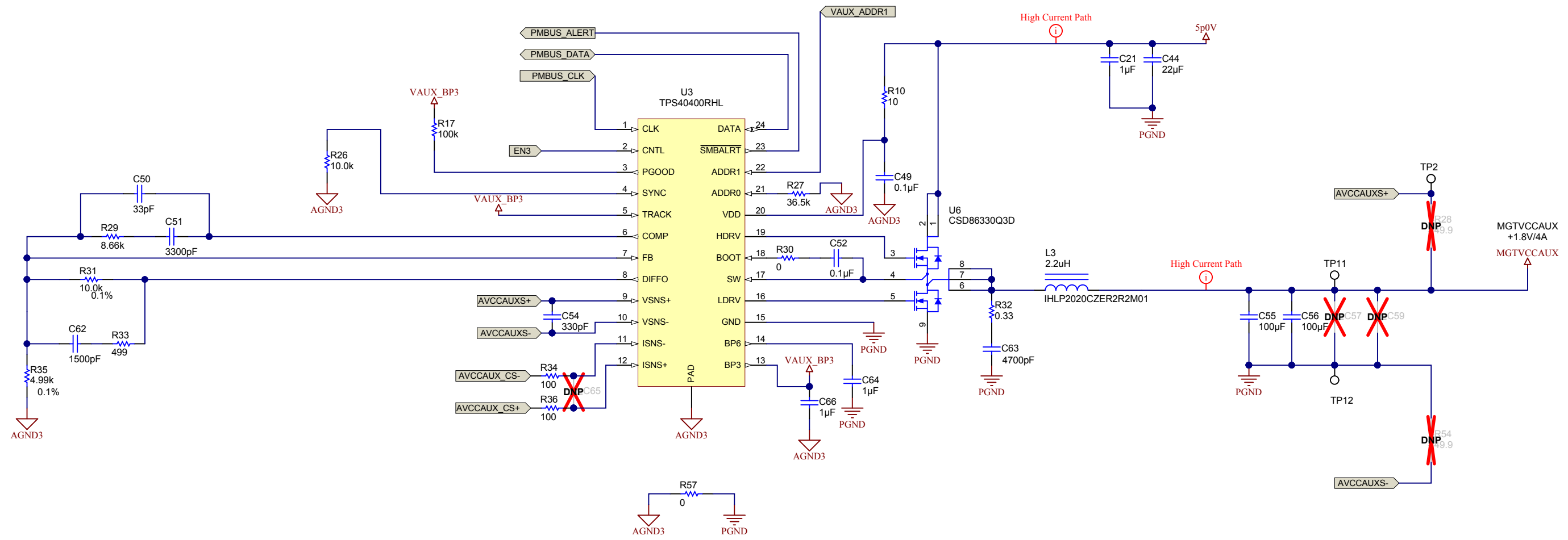
IN2	IN1	D TO S, S TO D
L	L	D = S <sub>1</sub>
L	H	D = S <sub>2</sub>
H	L	D = S <sub>3</sub>
H	H	D = S <sub>4</sub>

ALT_PMBUS_1	ALT_PMBUS_0	HEX	OCTAL	Raddr1 (kohm)	Raddr0 (kohm)
GND	GND	0x31	61	133	17.8
GND	OPEN	0x29	51	86.6	17.8
OPEN	GND	0x21	41	56.2	17.8
OPEN	OPEN	0x19	31	38.3	17.8



The PMBUS Address selection circuit selects between one of four address resistors on the ADDR1 pin. It is not required in an end application.

# MGTVCCAUX - 1.8V@4A



**FUNCTION TABLE**

IN2	IN1	D TO S, S TO D
L	L	D = S <sub>1</sub>
L	H	D = S <sub>2</sub>
H	L	D = S <sub>3</sub>
H	H	D = S <sub>4</sub>

ALT_PMBUS_1	ALT_PMBUS_0	HEX	OCTAL	Raddr1 (kohm)	Raddr0 (kohm)
GND	GND	0x33	63	130	36.5
GND	OPEN	0x2B	53	84.5	36.5
OPEN	GND	0x23	43	54.9	36.5
OPEN	OPEN	0x1B	33	36.5	36.5

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Number: PMP10520	Rev: E1	Designed for: Public Release	Mod. Date: 8/6/2014
SVN Rev: Version control disabled	Drawn By: Sami Sirhan	Project Title: PMP10520	Sheet Title: MGTVCCAUX
Engineer: Sami Sirhan	File: Page3.SchDoc	Assembly Variant: 001	Sheet: 3 of 5
	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	Size: B	© Texas Instruments 2014



A

B

C

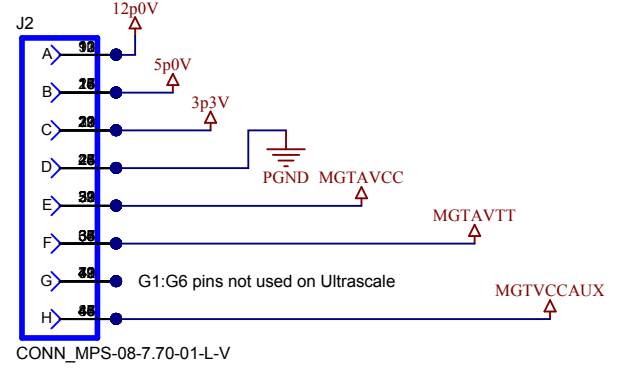
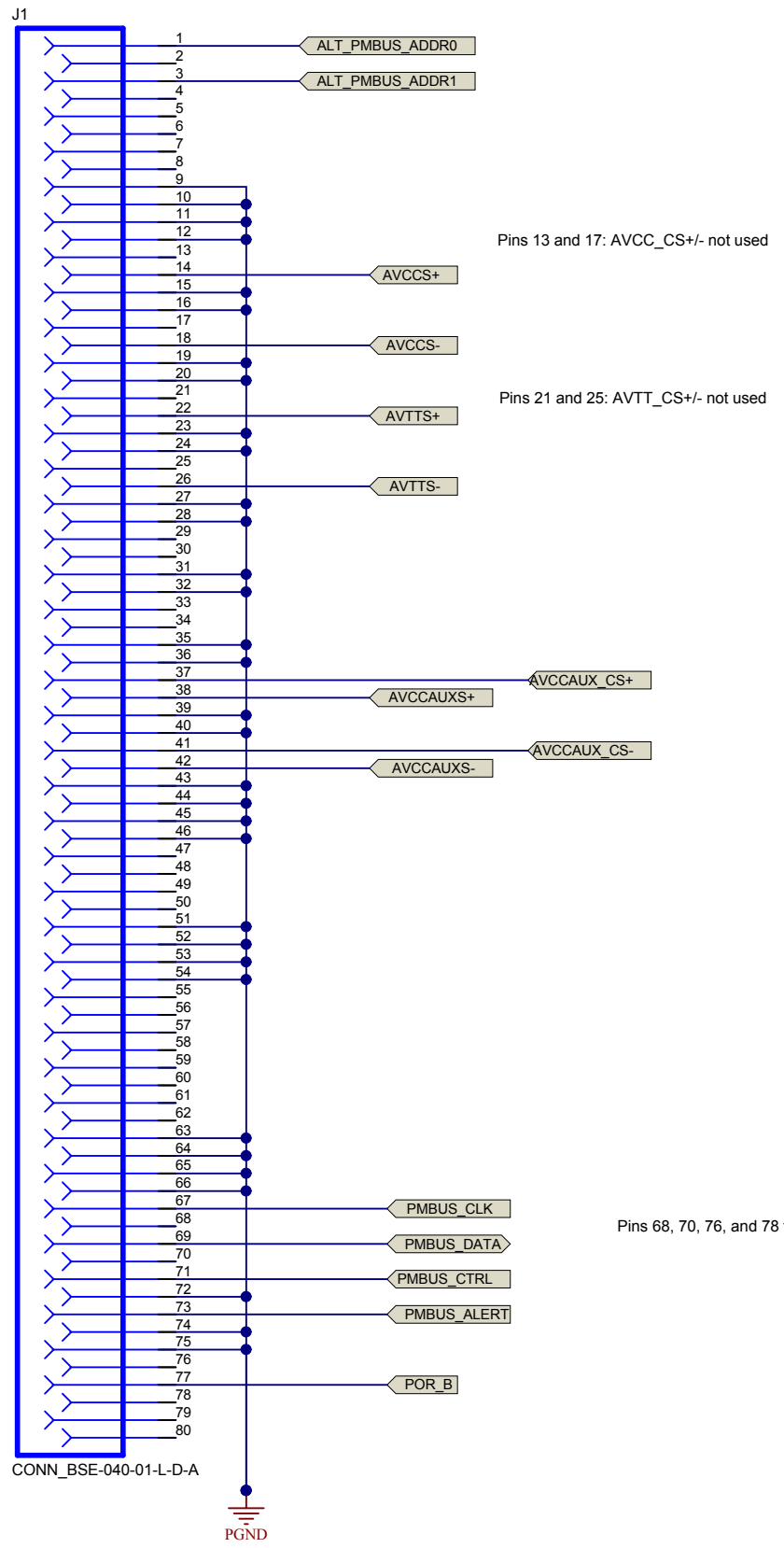
D

A

B

C

D



MGTAVCC on Ultrascale. Previously called MGTHAVCC on Gen 6 and 7-series

MGTAVTT on Ultrascale. Previously called MGTAVCCR on Gen 6 and MGTHAVTT on 7-series

Pins 29, 30, 33, and 34 not used for Ultrascale. Previously called MGTHAVTT on Gen 6.

MGTAVCCAUX on Ultrascale. Previously called MGTAVCCPLL on Gen 6 and MGTHVCCAUX on 7-series

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PCB Number: PMP10520  
PCB Rev: E1

PCB  
LOGO  
Texas Instruments


Label Table	
Variant	Label Text
001	ChangeMe!
002	ChangeMe!

~~Z72~~ ~~DNP~~  
These assemblies are ESD sensitive, ESD precautions shall be observed.

~~Z73~~ ~~DNP~~  
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

~~Z74~~ ~~DNP~~  
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

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Number: <a href="#">PMP10520</a>	Rev: <a href="#">E1</a>	Designed for: <a href="#">Public Release</a>	Mod. Date: <a href="#">8/8/2014</a>
SVN Rev: <a href="#">Version control disabled</a>	Assembly Variant: <a href="#">001</a>	Sheet: <a href="#">5</a> of <a href="#">5</a>	 <a href="http://www.ti.com">http://www.ti.com</a> <small>© Texas Instruments 2014</small>
Drawn By: <a href="#">Sami Sirhan</a>	File: <a href="#">Hardware_ANSI-B_SchDoc</a>	Size: <a href="#">B</a>	
Engineer: <a href="#">Sami Sirhan</a>	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>		

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