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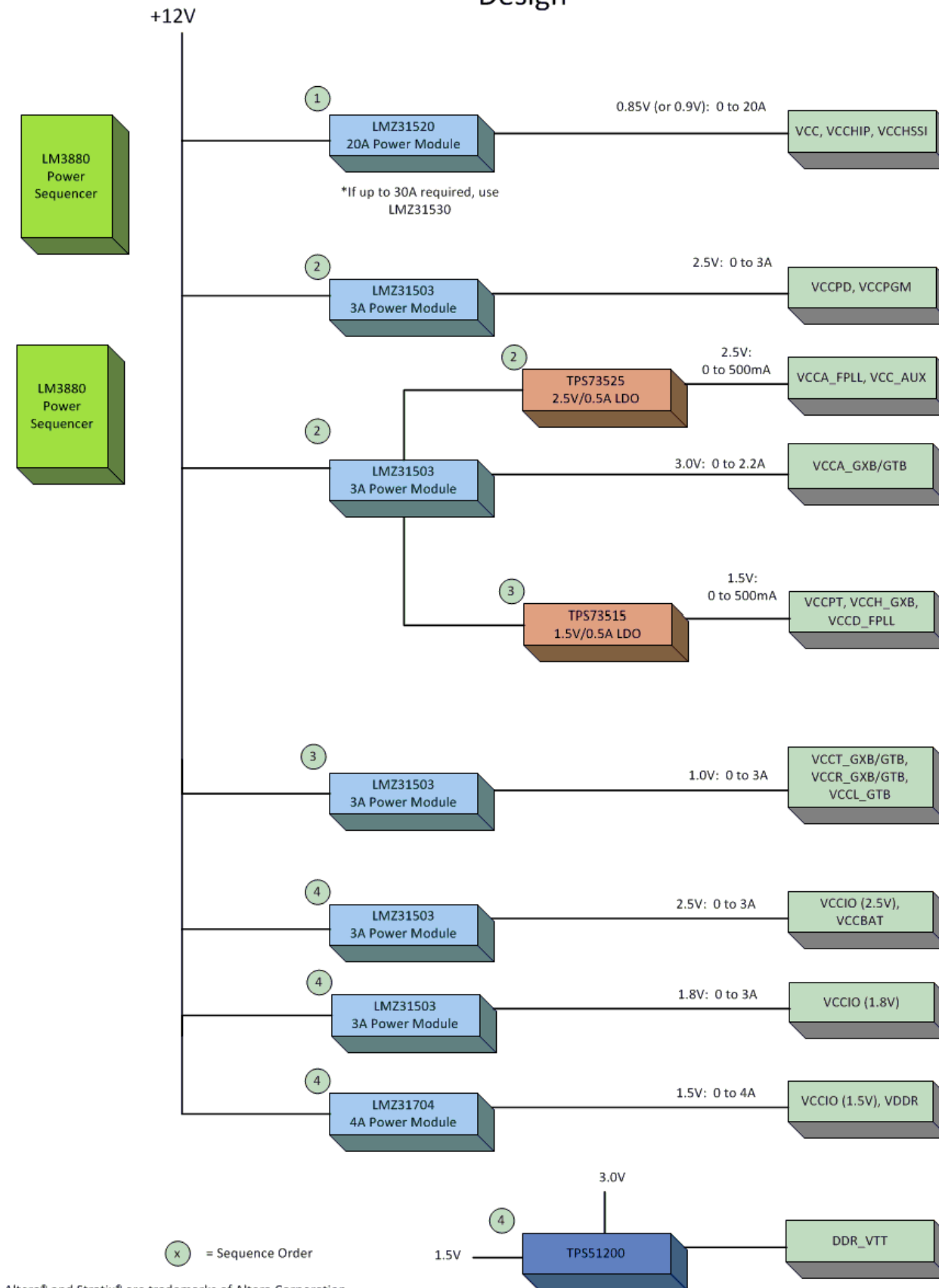
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Stratix® V FPGA Power Reference Design



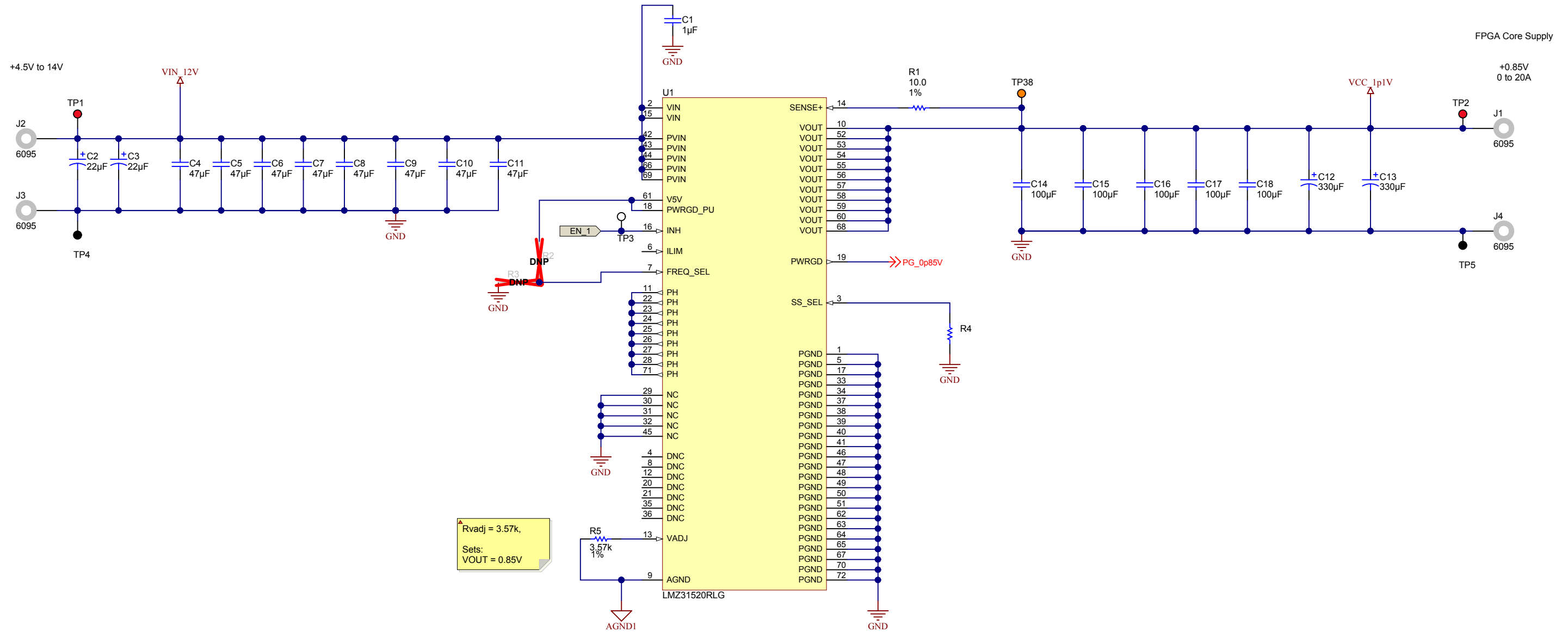
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Number: PMP9365	Rev: E1	Designed for: Public Release	Mod. Date: 10/15/2014
SVN Rev: Version control disabled		Project Title: Altera® Stratix® V FPGA Power Solution	
Drawn By:	Engineer: Sami Sirhan	Assembly Variant: 001	Sheet: 1 of 7
File: Cover Sheet_ANSI-B_SchDoc		Size: B	
Contact: http://www.ti.com/support		© Texas Instruments 2014	



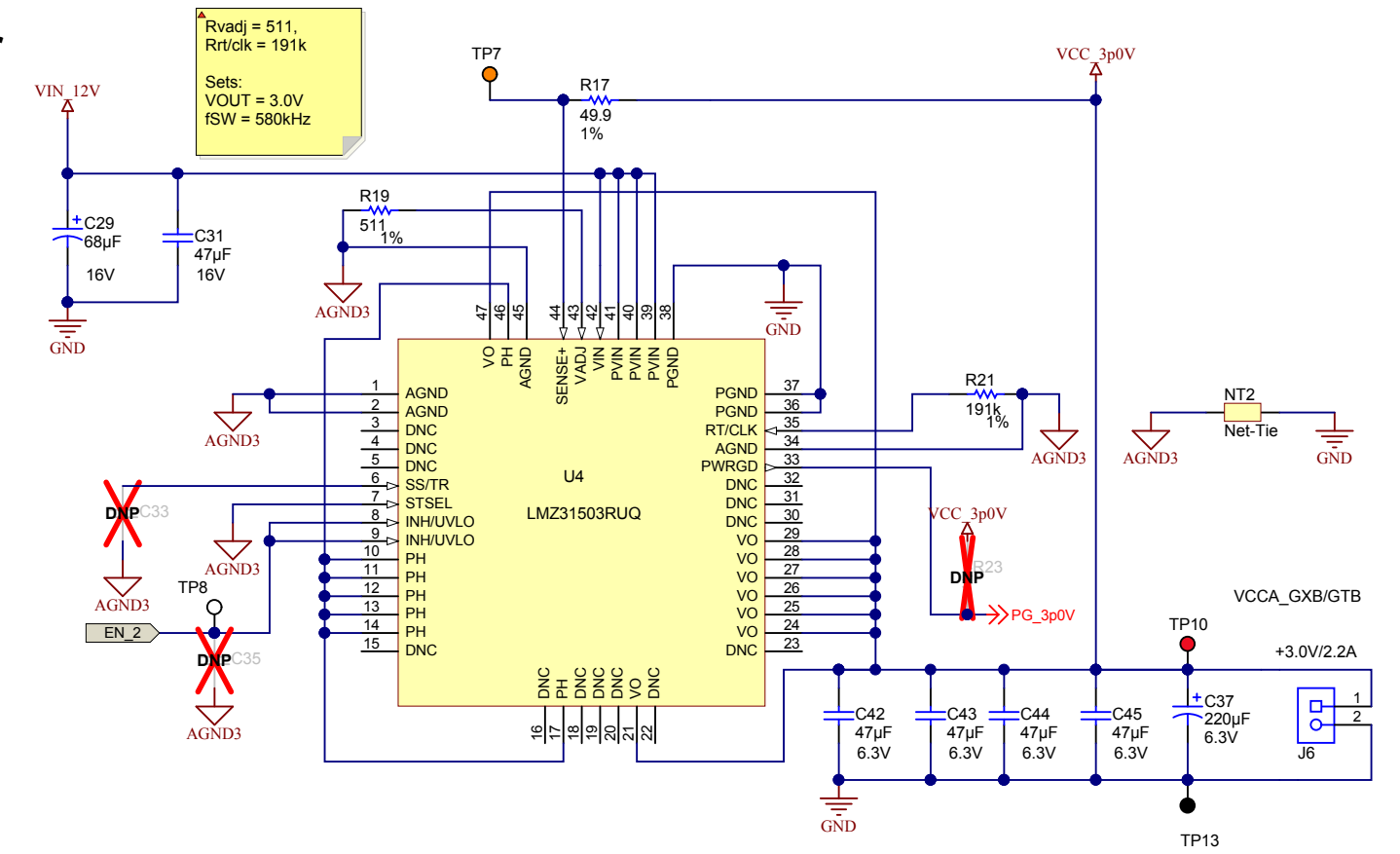
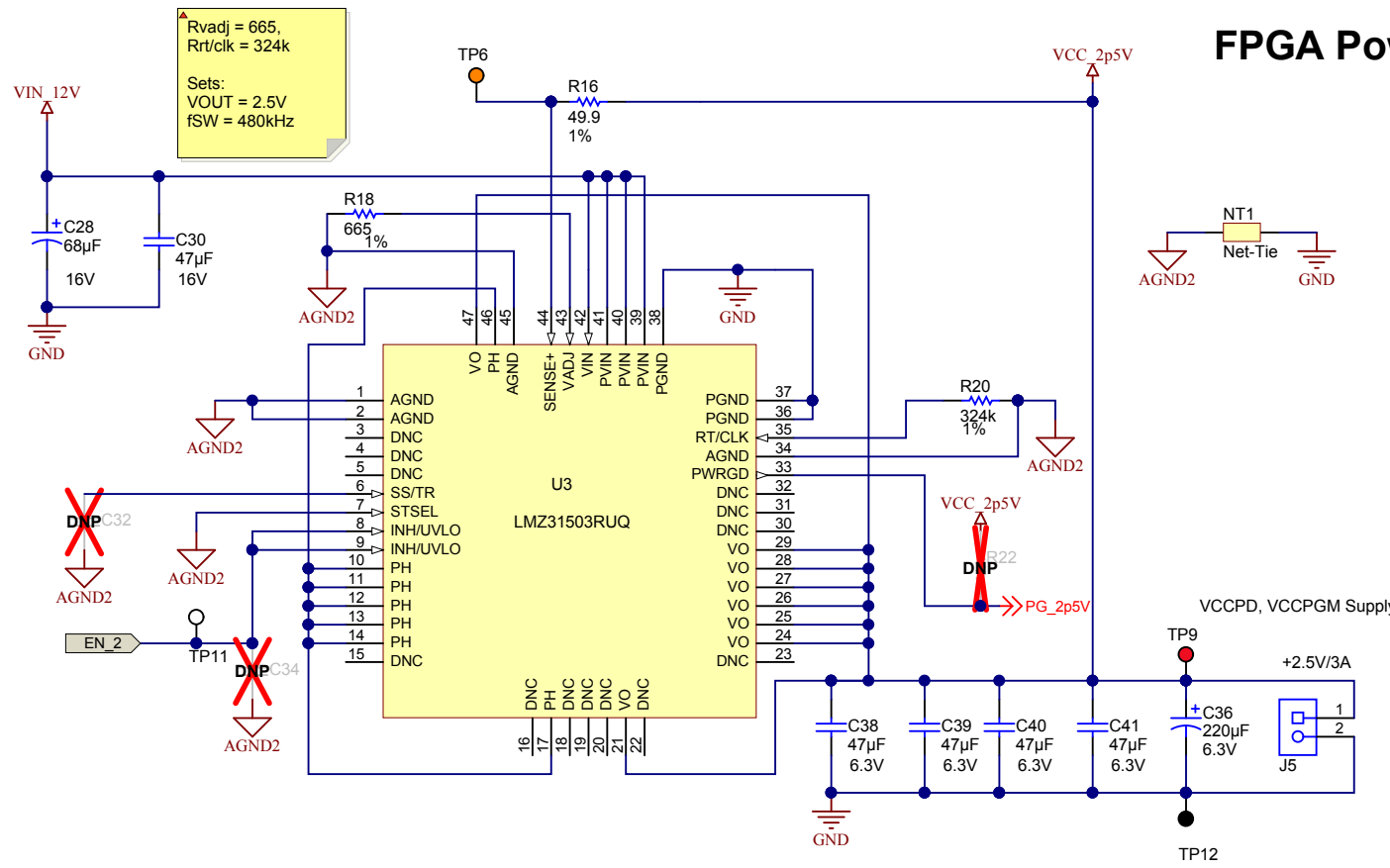
FPGA Core Power Supply



R_{vadj} = 3.57k,
Sets:
V_{OUT} = 0.85V

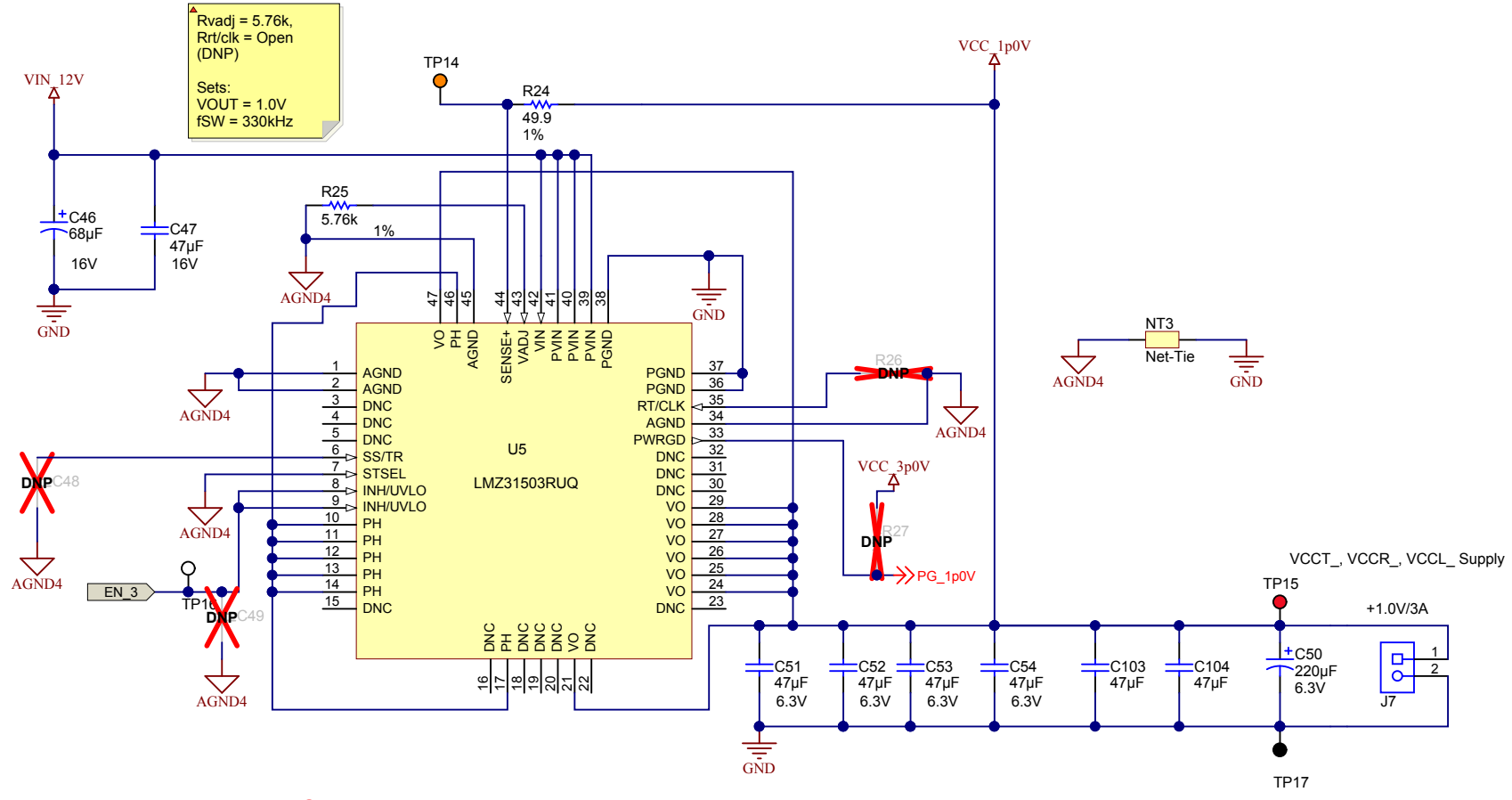
- i AGND internally tied to PGND on LMZ3 series modules
- i PH pins should be connected to a copper island under the device for thermal relief. DO NOT connect any external component or net to this pin.

FPGA Power



ⓘ PH pins should be connected to a copper island under the device for thermal relief. DO NOT connect any external component or net to this pin.

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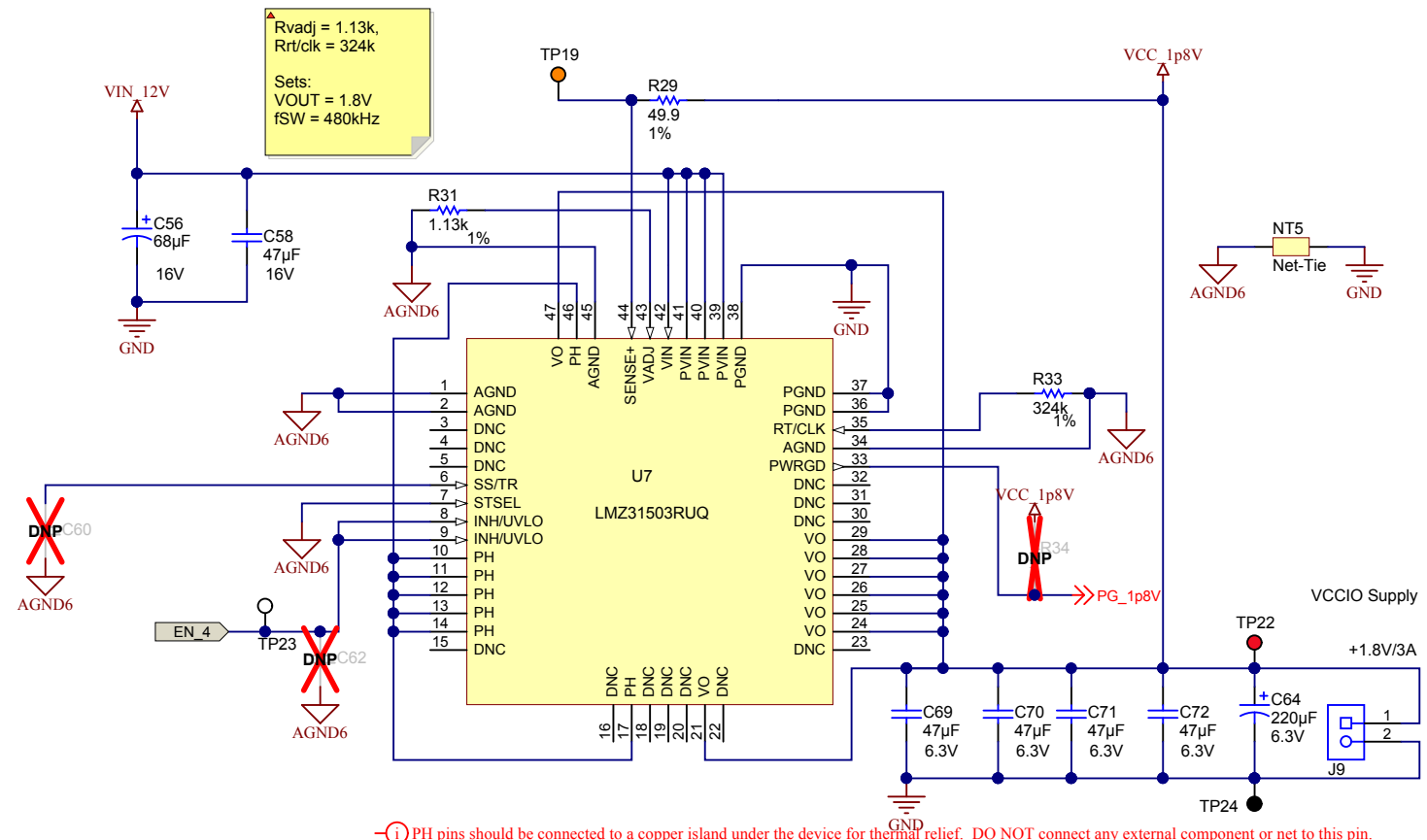
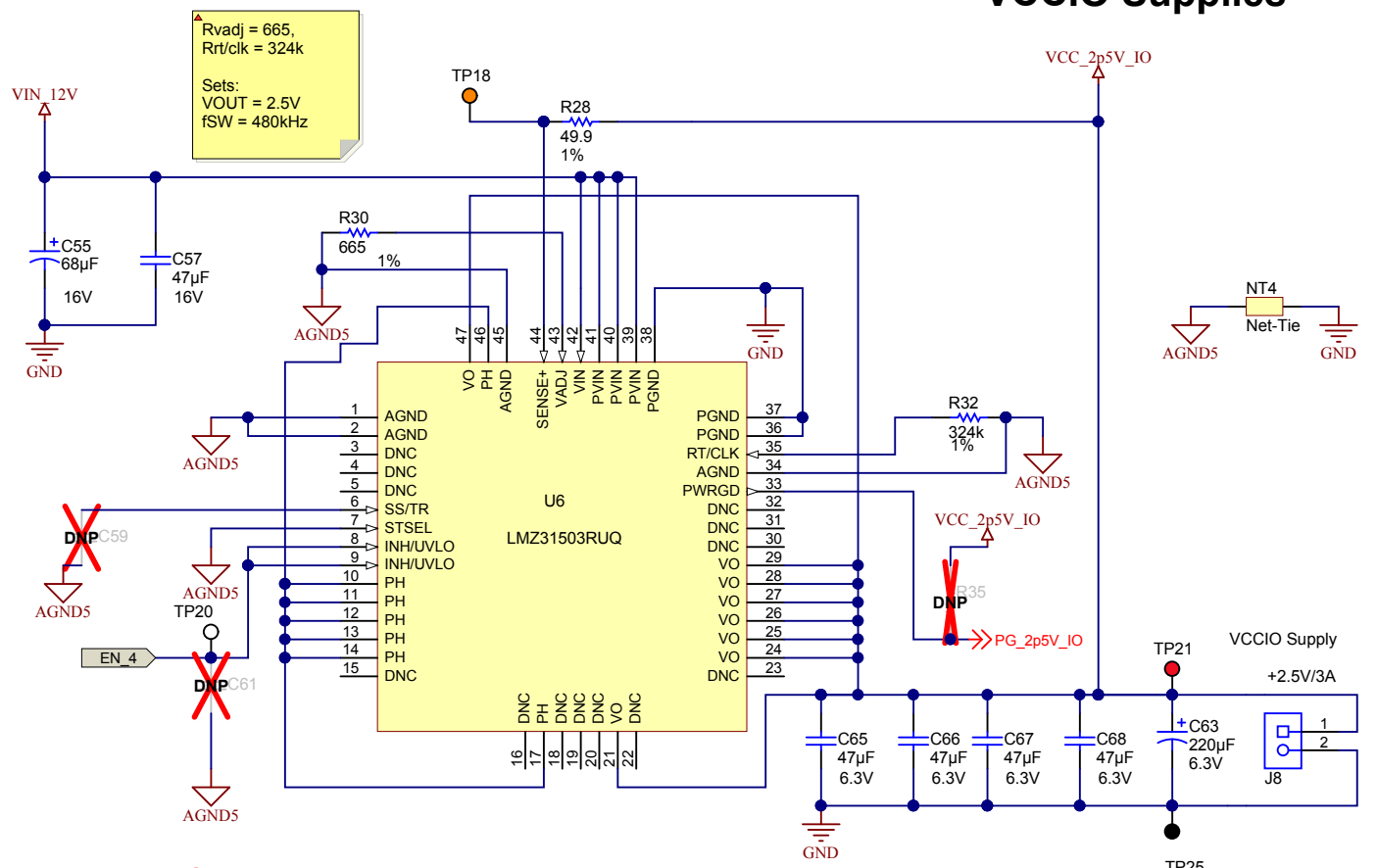


ⓘ PH pins should be connected to a copper island under the device for thermal relief. DO NOT connect any external component or net to this pin.

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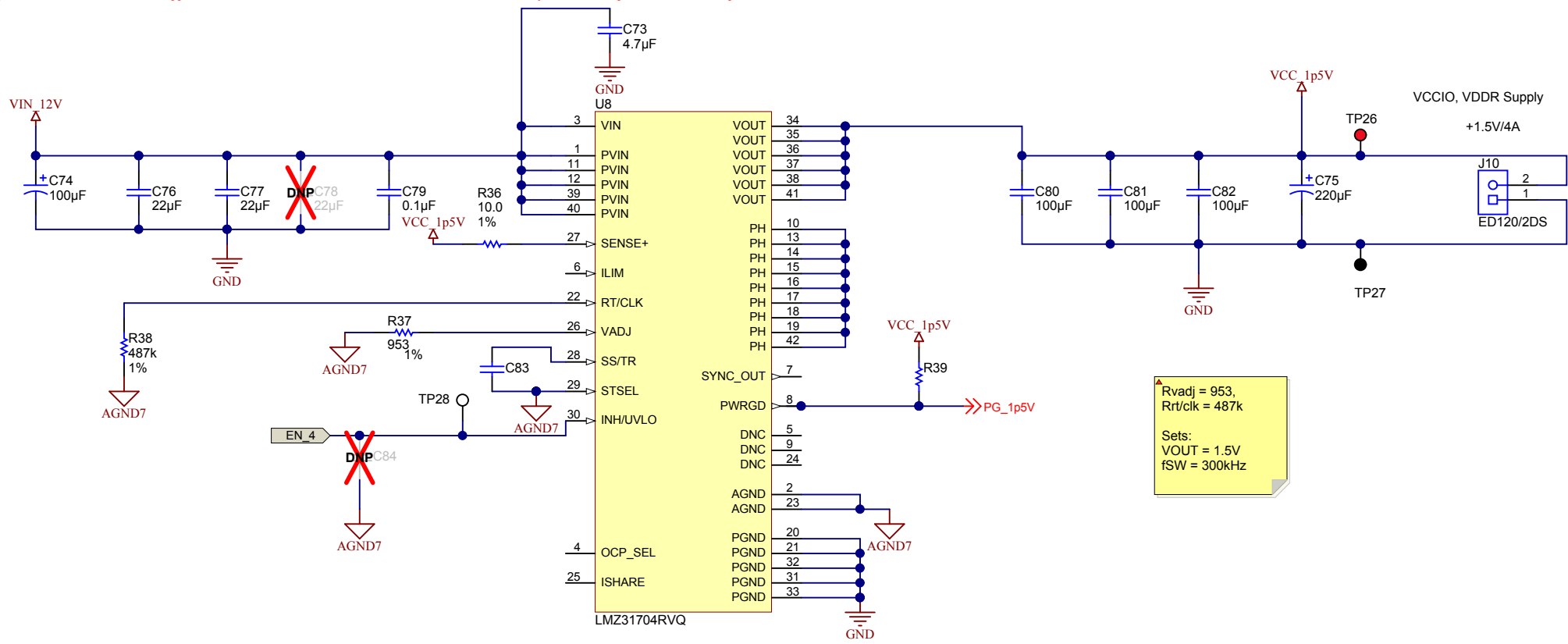
Number: PMP9365	Rev: E1	Designed for: Public Release	Mod. Date: 7/10/2014
SVN Rev: Version control disabled		Project Title: Altera® Stratix® V FPGA Power Solution	
Drawn By:	Engineer: Sami Sirhan	Sheet: 3 of 7	Size: B
File: Page2.SchDoc		Contact: http://www.ti.com/support	
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VCCIO Supplies



ⓘ PH pins should be connected to a copper island under the device for thermal relief. DO NOT connect any external component or net to this pin.

ⓘ PH pins should be connected to a copper island under the device for thermal relief. DO NOT connect any external component or net to this pin.



ⓘ AGND internally tied to PGND

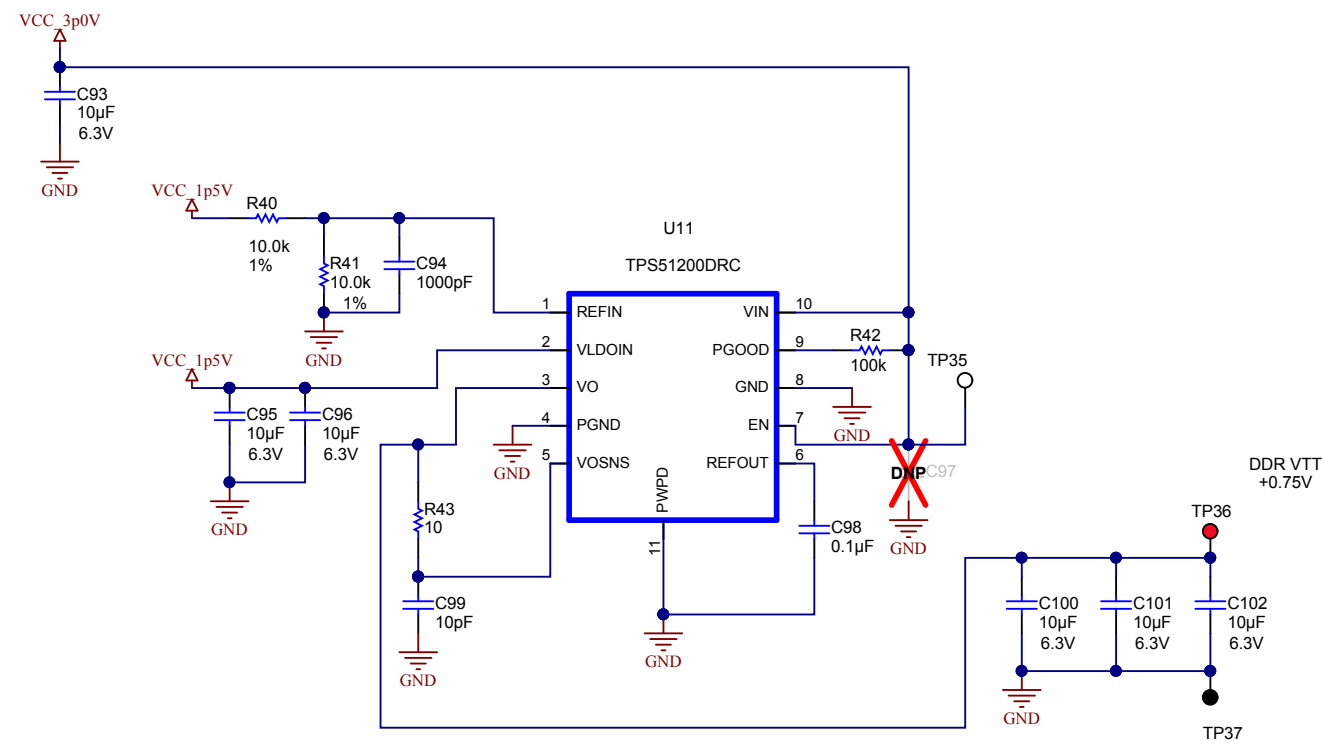
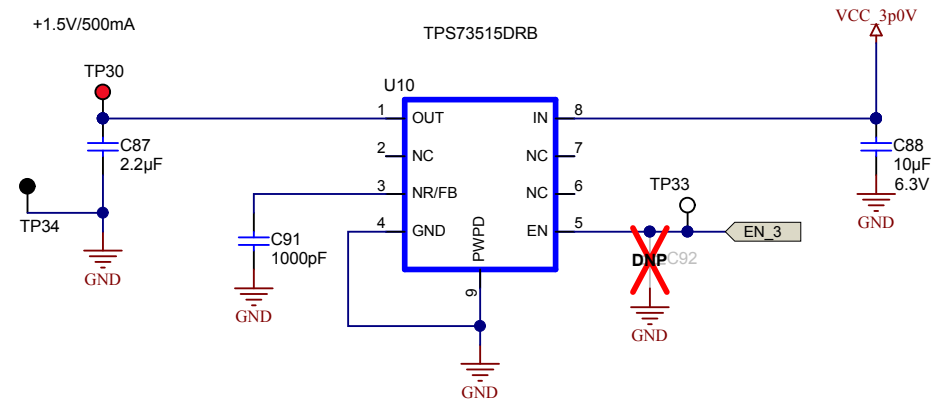
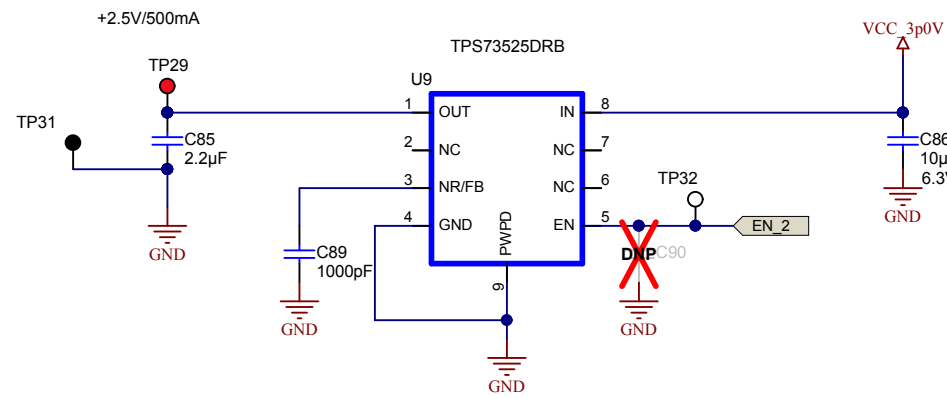
ⓘ PH pins should be connected to a copper island under the device for thermal relief. DO NOT connect any external component or net to this pin.

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SVN Rev: Version control disabled		Project Title: Altera® Stratix® V FPGA Power Solution	
Drawn By:	Engineer: Sami Sirhan	Sheet: 4 of 7	Size: B
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LDOs and DDR Termination



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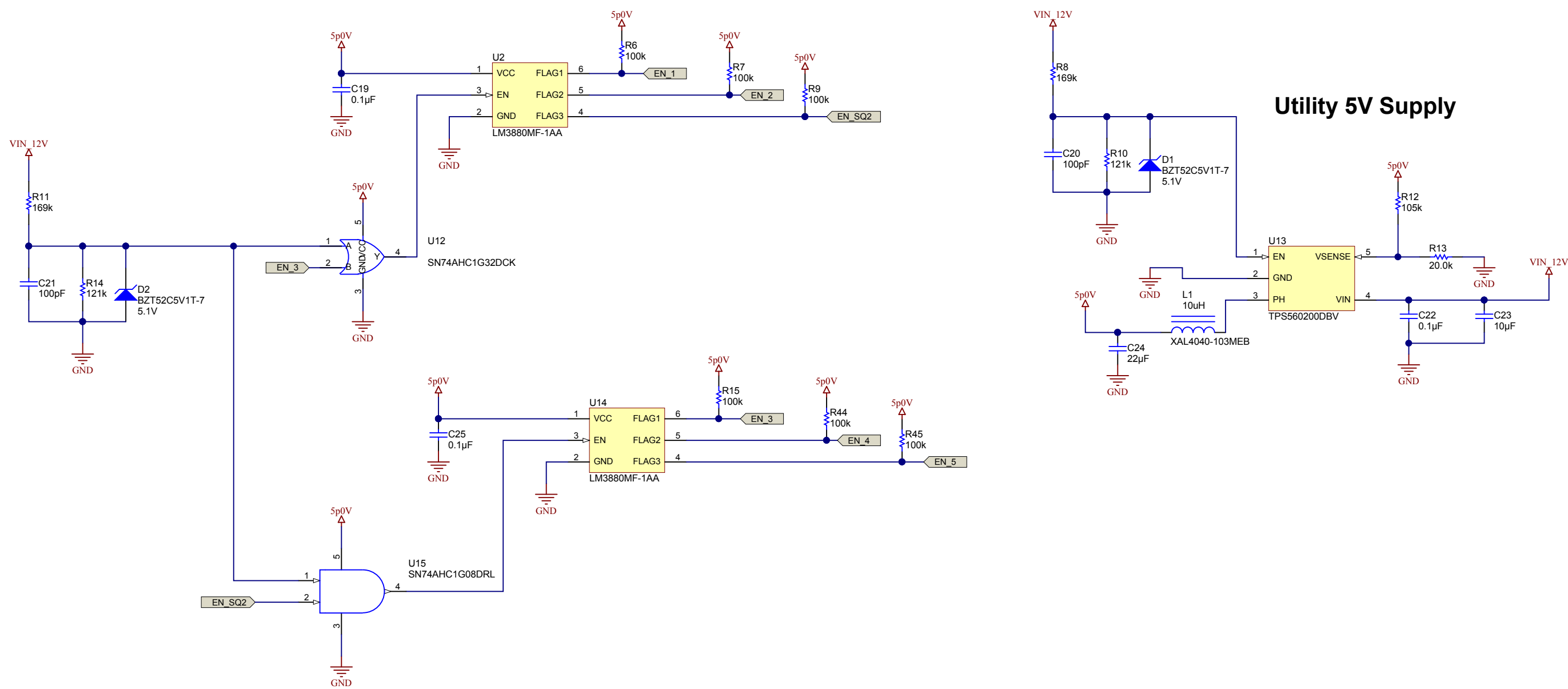
Number: PMP9365 Rev: E1
 SVN Rev: Version control disabled
 Drawn By:
 Engineer: Sami Sirhan

Designed for: Public Release Mod. Date: 7/8/2014
 Project Title: Altera® Stratix® V FPGA Power Solution
 Sheet Title:
 Assembly Variant: 001 Sheet: 5 of 7
 File: Page4.SchDoc Size: B
 Contact: <http://www.ti.com/support>



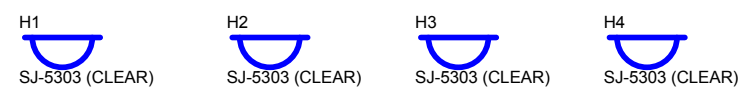
Sequencers

Utility 5V Supply



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Drawn By: Sami Sirhan	Engineer: Sami Sirhan	File: Page5.SchDoc	Contact: http://www.ti.com/support
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PCB Number: PMP9365
PCB Rev: E1

PCB
LOGO
Texas Instruments

Label Table	
Variant	Label Text
001	ChangeMe!
002	ChangeMe!

LBL1
PCB Label
Size: 0.65" x 0.20"


ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

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Drawn By: Sami Sirhan		Assembly Variant: 001	Sheet: 7 of 7	
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