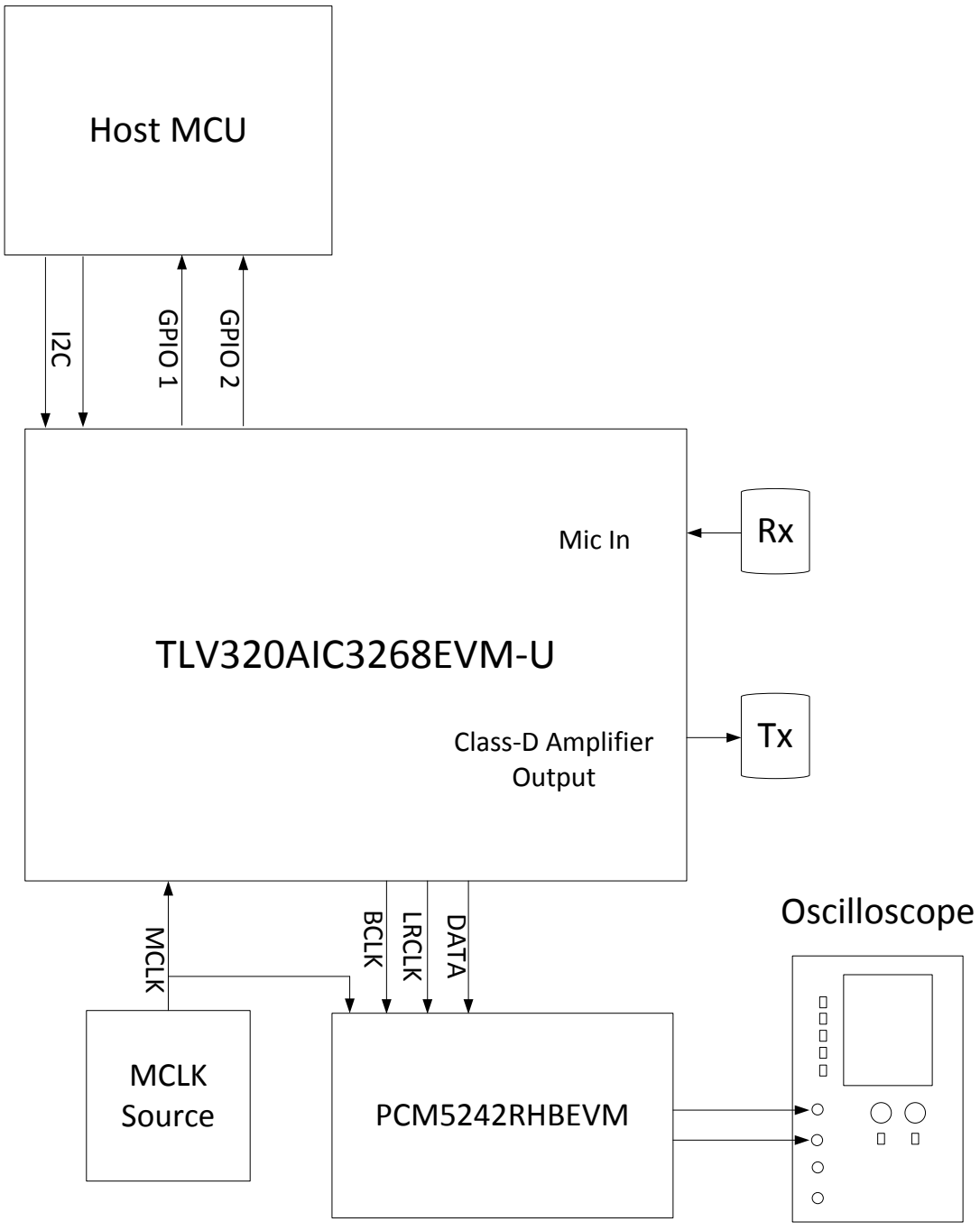
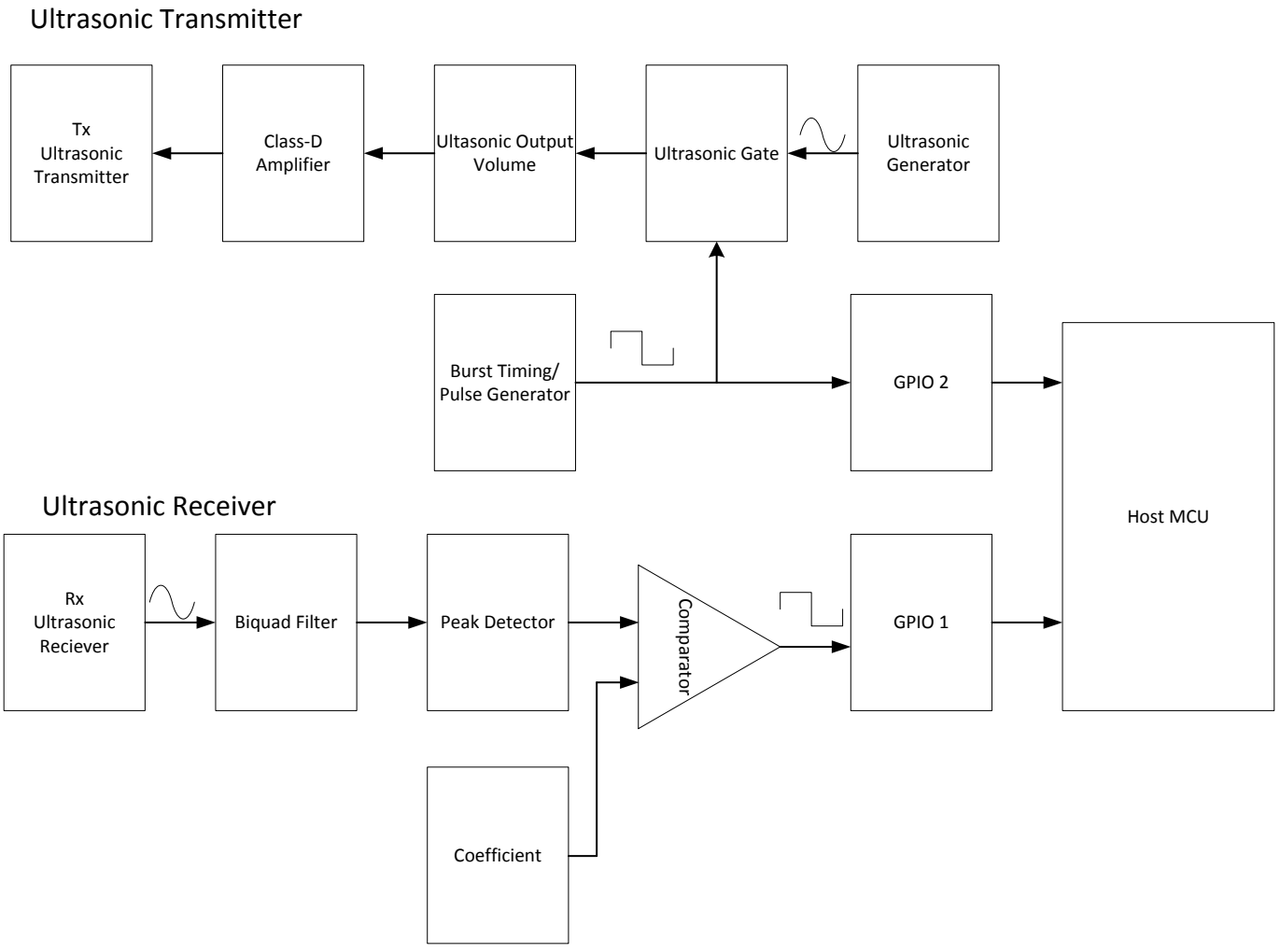
Hardware Block Diagram

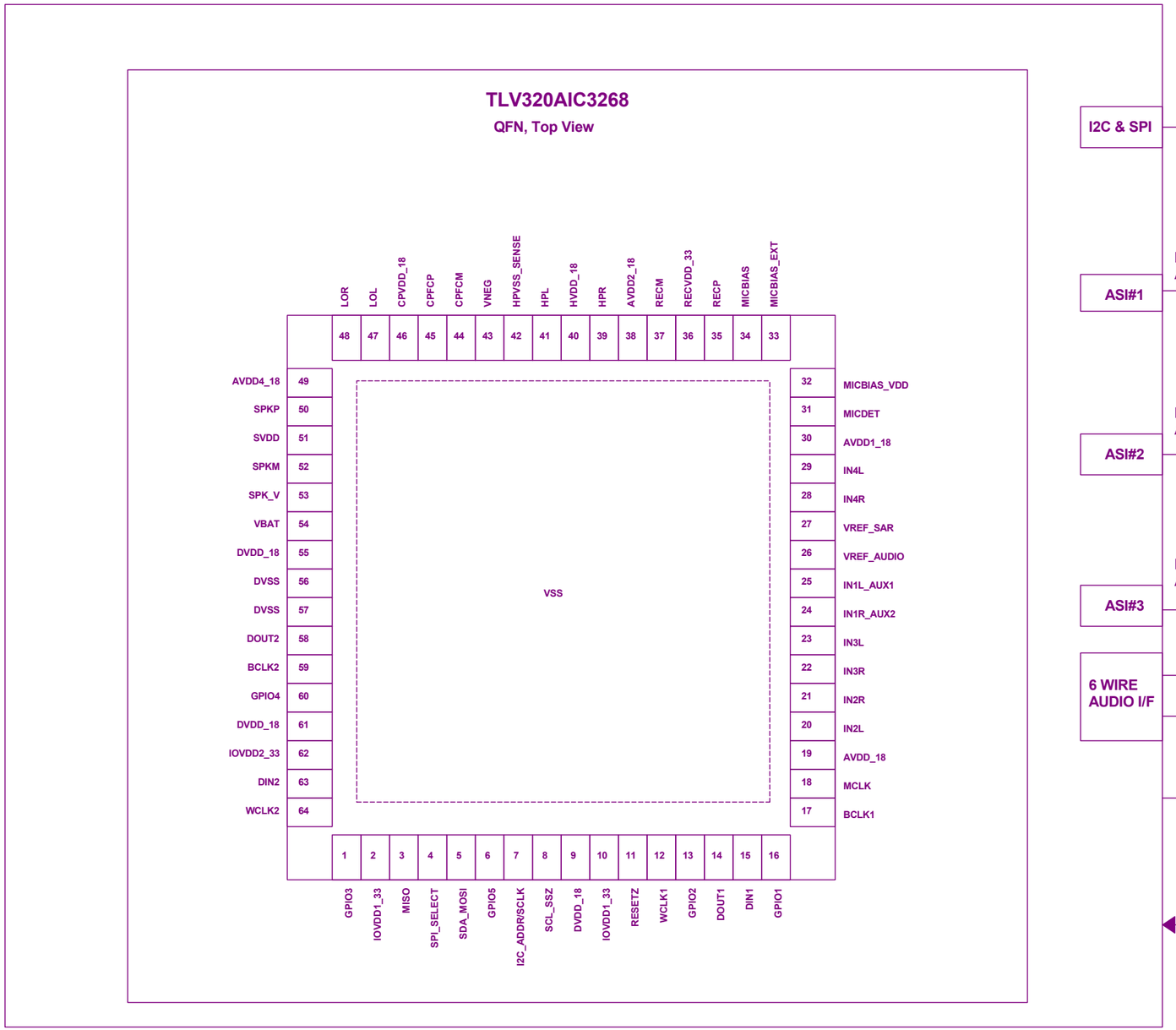


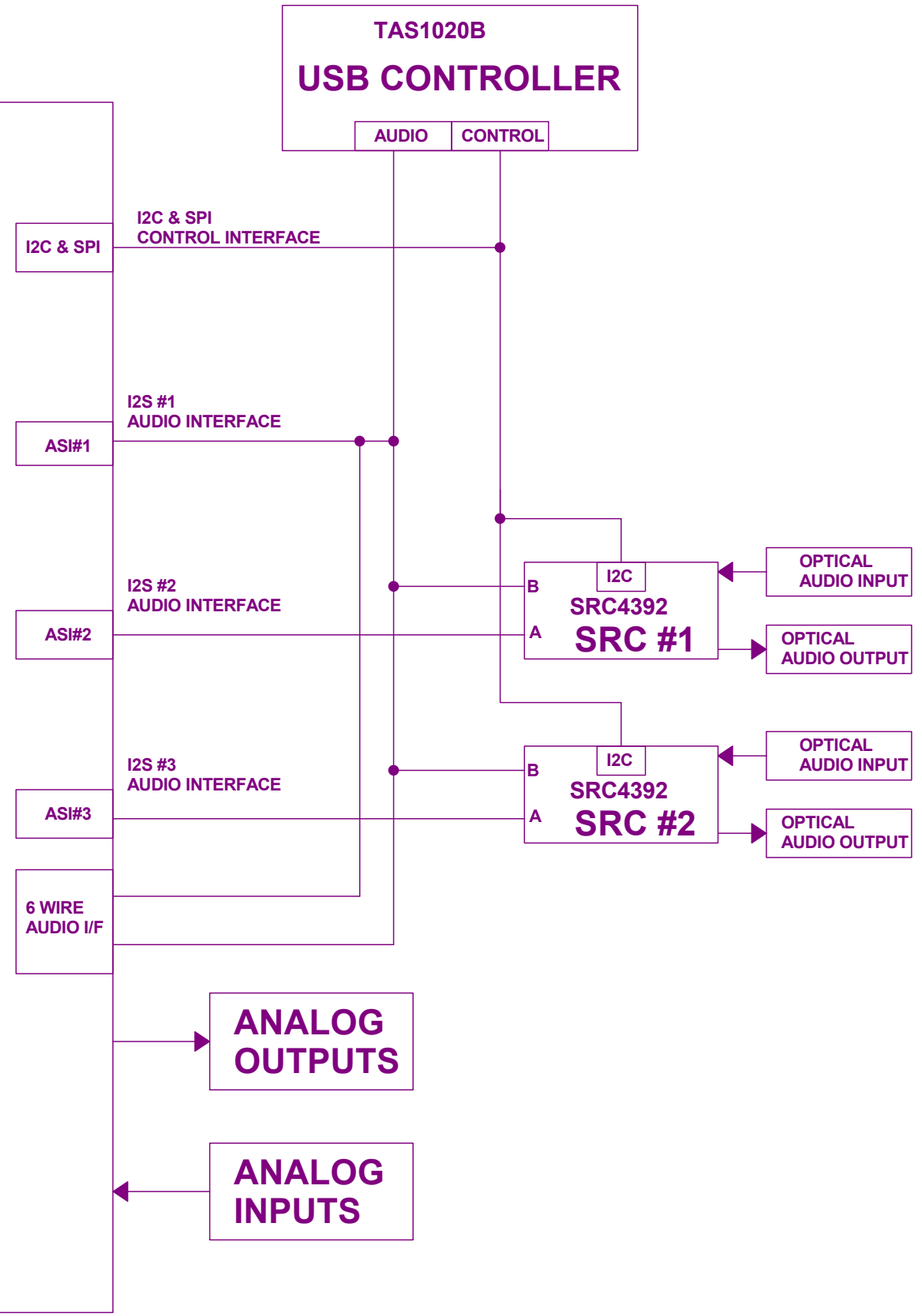
Ultrasonic Measurement Block Diagram



TIDA-00403

TLV320AIC3268RGC EVALUATION BOARD



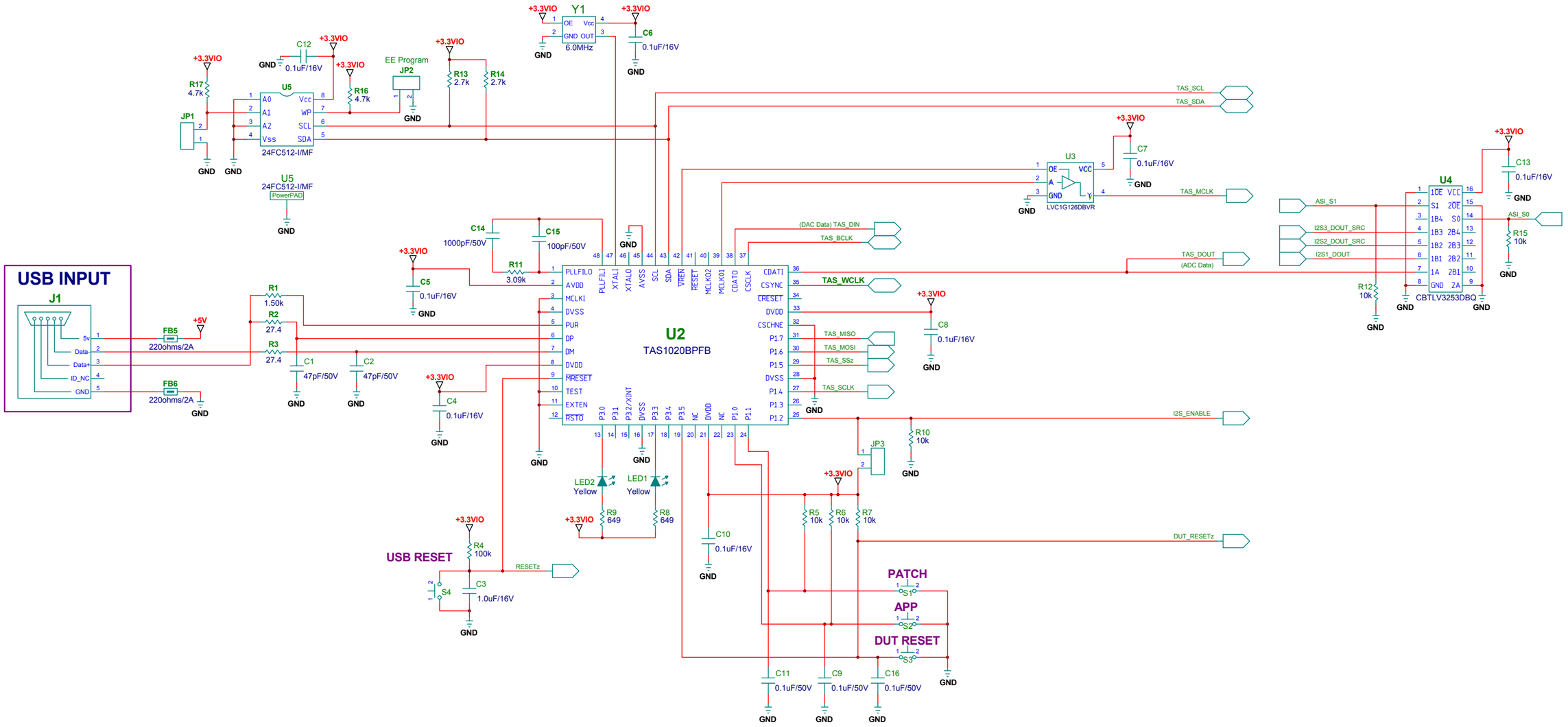


TIDA-00403

TEXAS INSTRUMENTS			SCH REV C
			PCB REV C
PAGE INFO: BLOCK DIAGRAM		DATE JANUARY 31, 2014	SHEET 1 OF 11
DESIGN LEAD JOHN FEDAK IV		FILENAME AIP013C_Schematic.sbk	DRAWN BY L;DN

TLV320AIC3268RGC EVALUATION BOARD

TAS1020B USB HOST ADAPTER

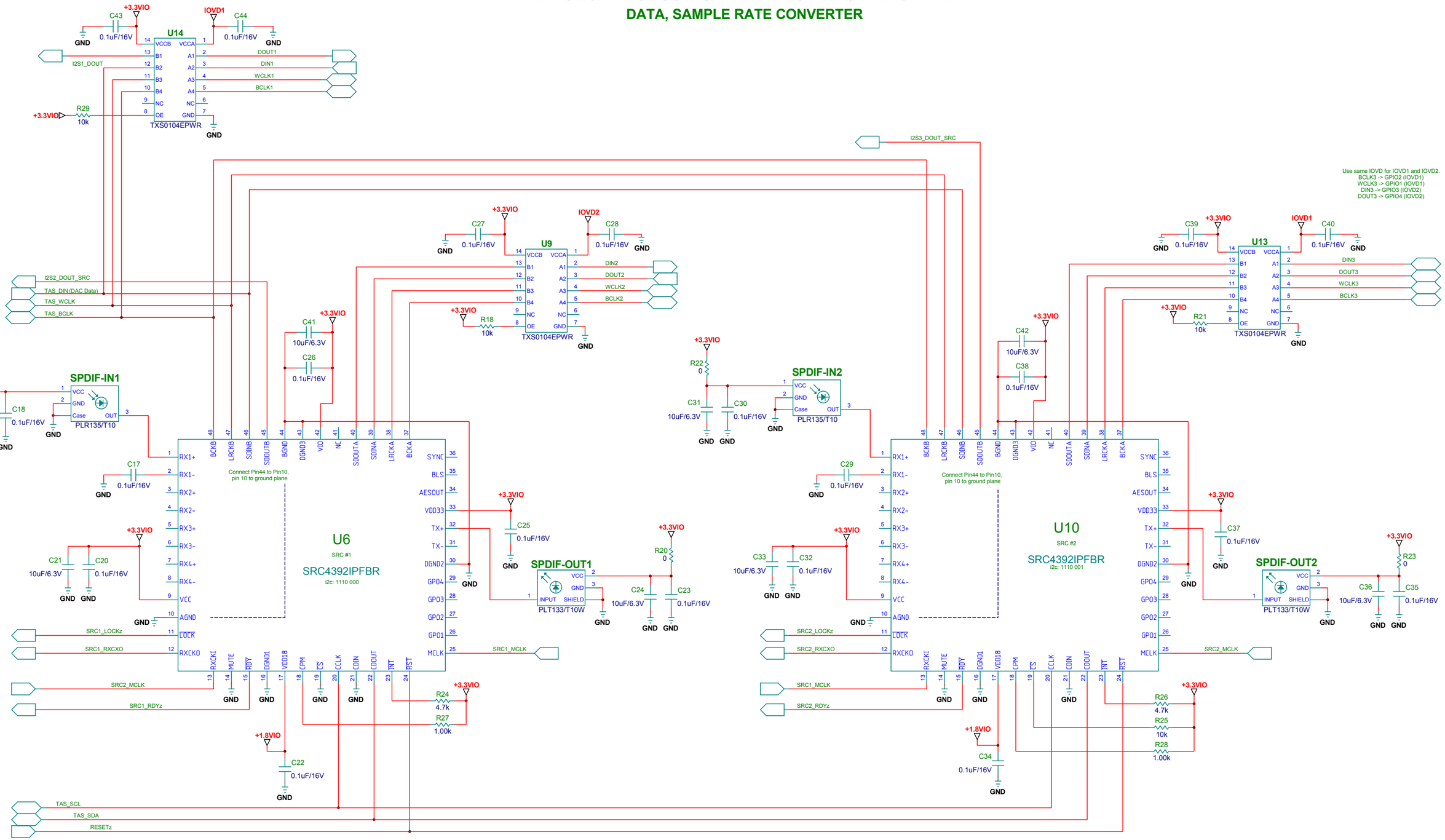


TIDA-00403

TEXAS INSTRUMENTS			SCH REV C
			PCB REV C
PAGE INFO: USB CONTROLLER		DATE JANUARY 31, 2014	SHEET 2 OF 11
DESIGN LEAD JOHN FEDAK IV		FILENAME AIP013C_Schematic.sbk	DRAWN BY L;DN

TLV320AIC3268RGC EVALUATION BOARD

DATA, SAMPLE RATE CONVERTER

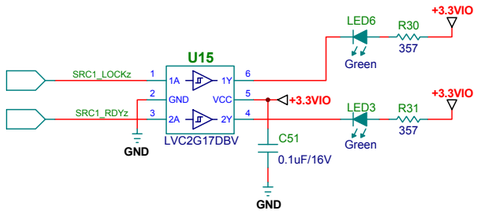


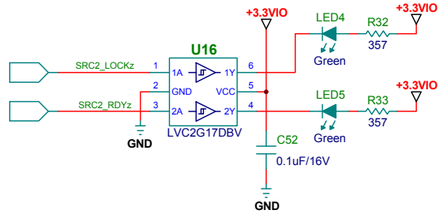
TIDA-00403

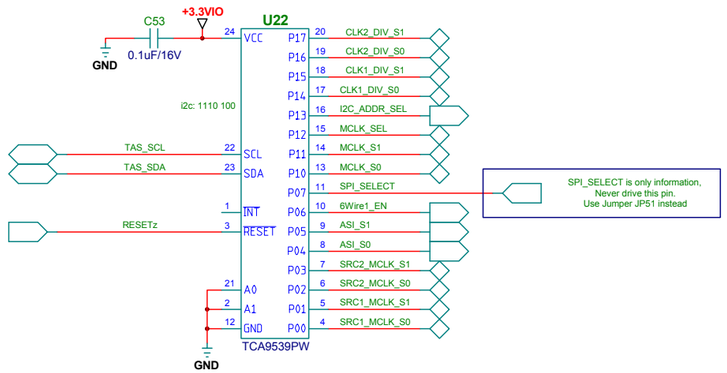
PAGE INFO: SAMPLE RATE CONVERTERS FOR ASIs		DATE JANUARY 31, 2014	SCH REV C
DESIGN LEAD JOHN FEDAK IV		FILENAME AIP013C_Schematic.sbk	PCB REV C
			SHEET 3 OF 11
			DRAWN BY L;DN

TLV320AIC3268RGC EVALUATION BOARD

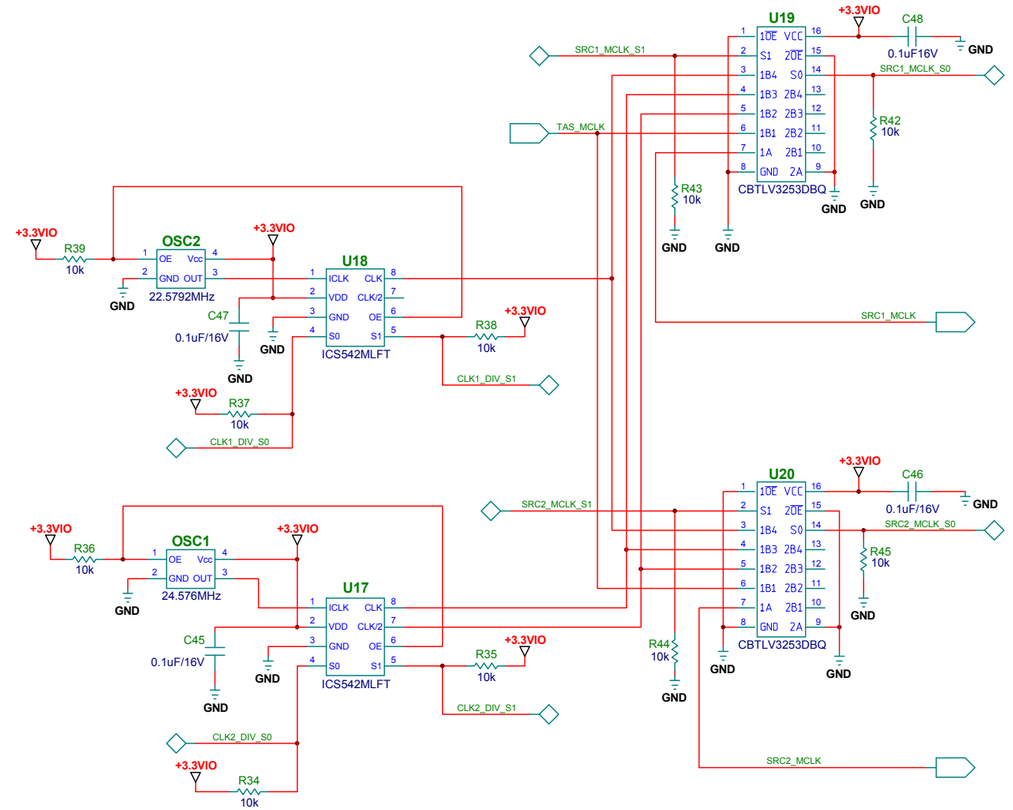
DATA

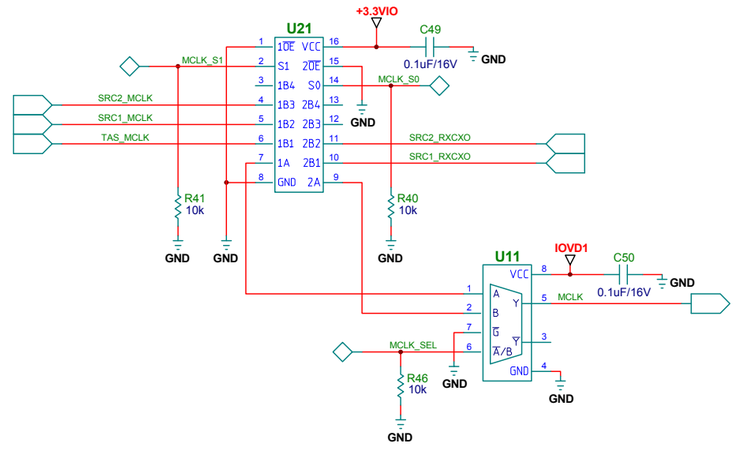






CLOCKS





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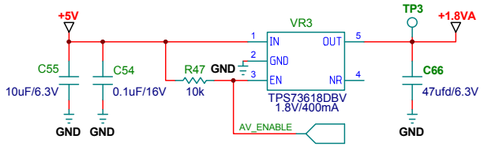
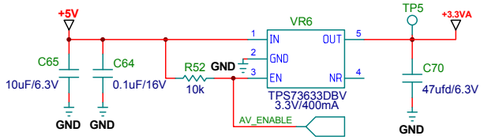
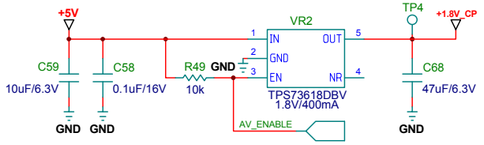
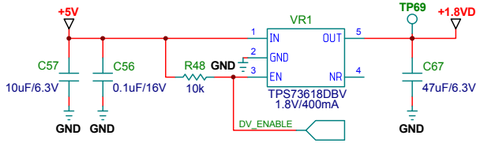
TLV320AIC3268RGC EVALUATION BOARD

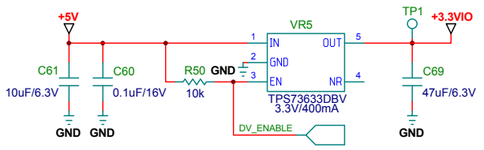
LDO SUPPLIES

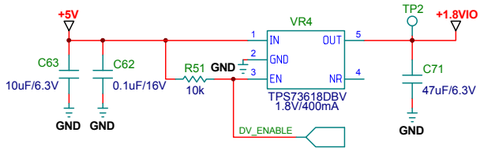


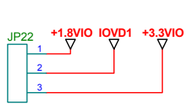


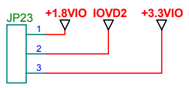


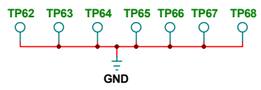


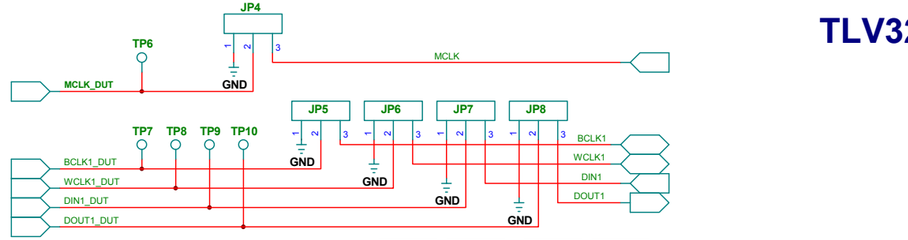


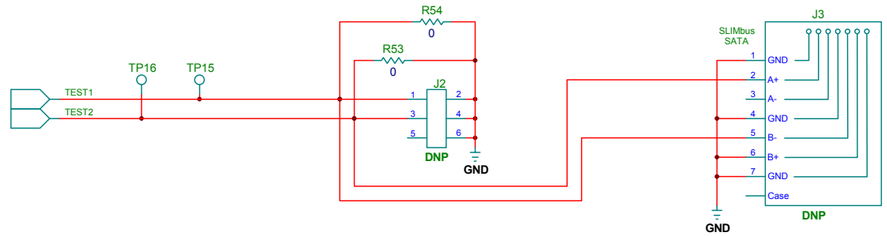


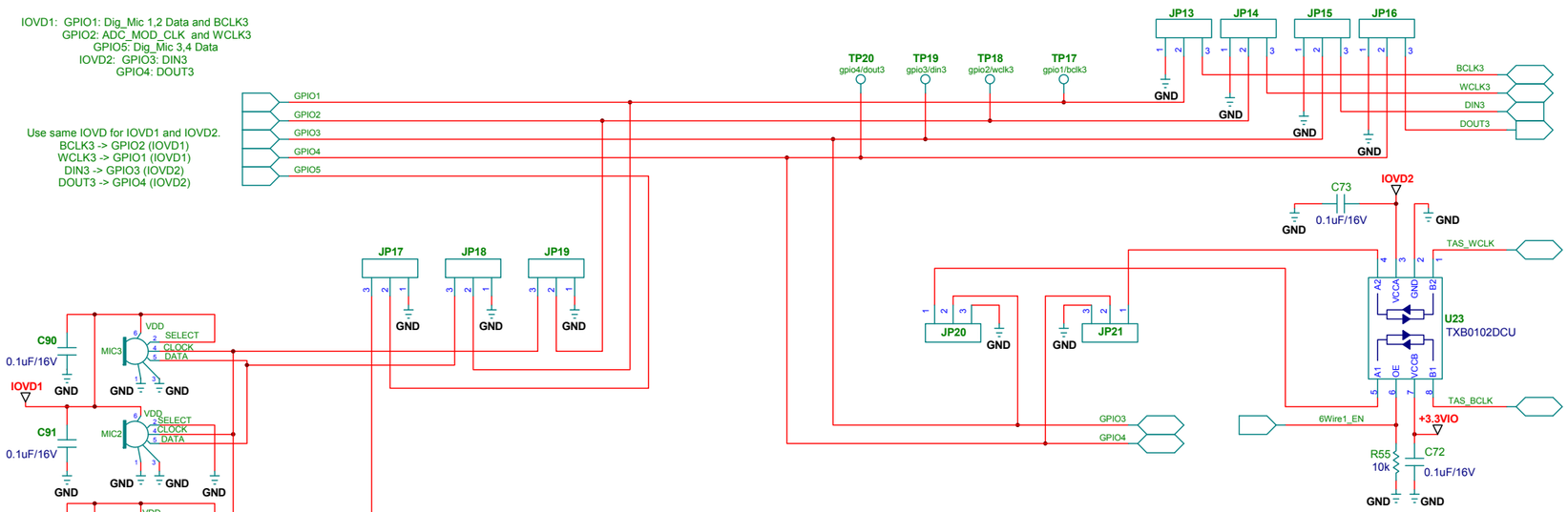








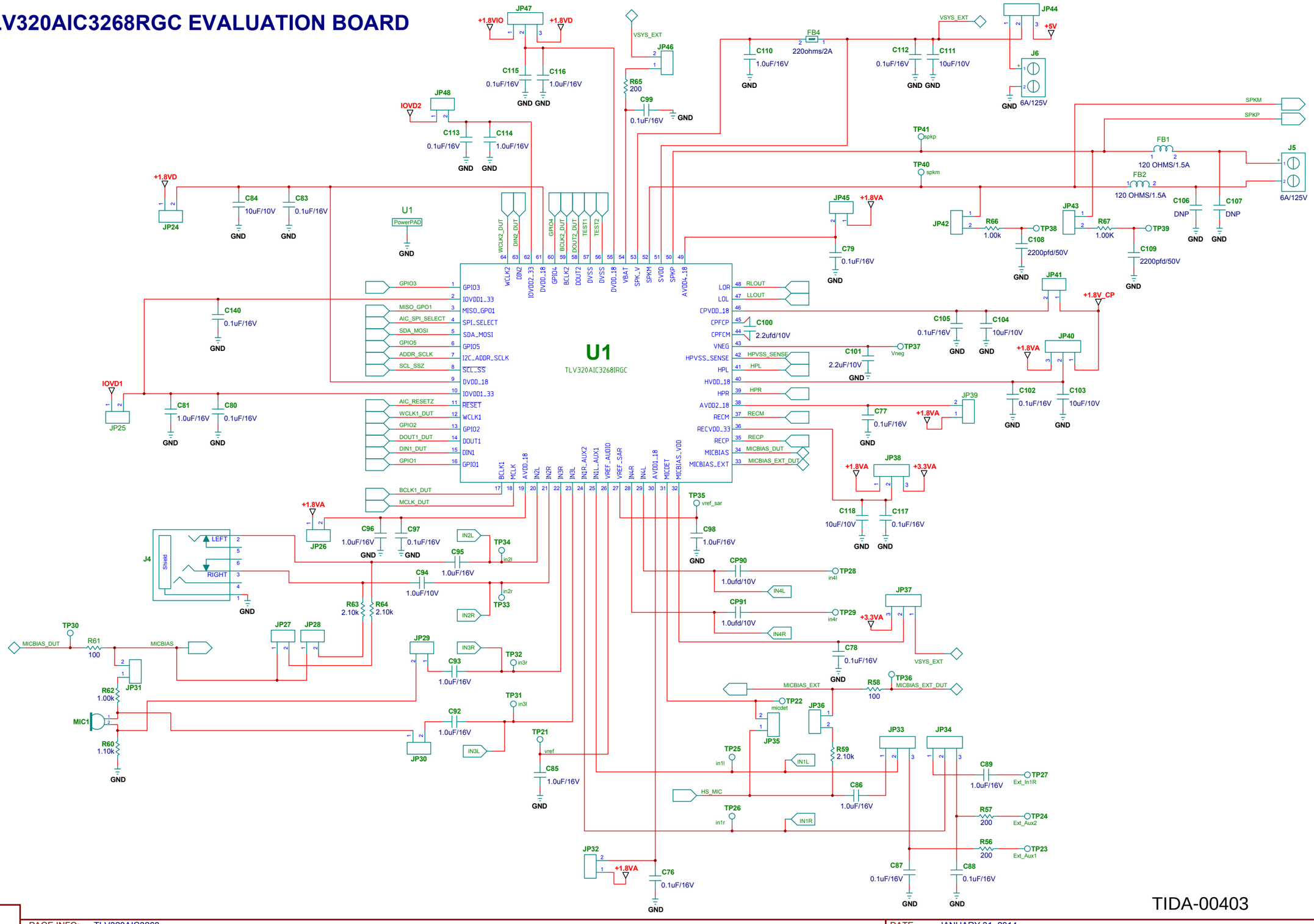




TIDA-00403

PAGE INFO: LDOs & AIC3268 ANALOG OUTPUTS		DATE JANUARY 31, 2014	SCH REV C
DESIGN LEAD JOHN FEDAK IV		FILENAME AIP013C_Schematic.sbk	PCB REV C
			SHEET 5 OF 11
			DRAWN BY L;DN

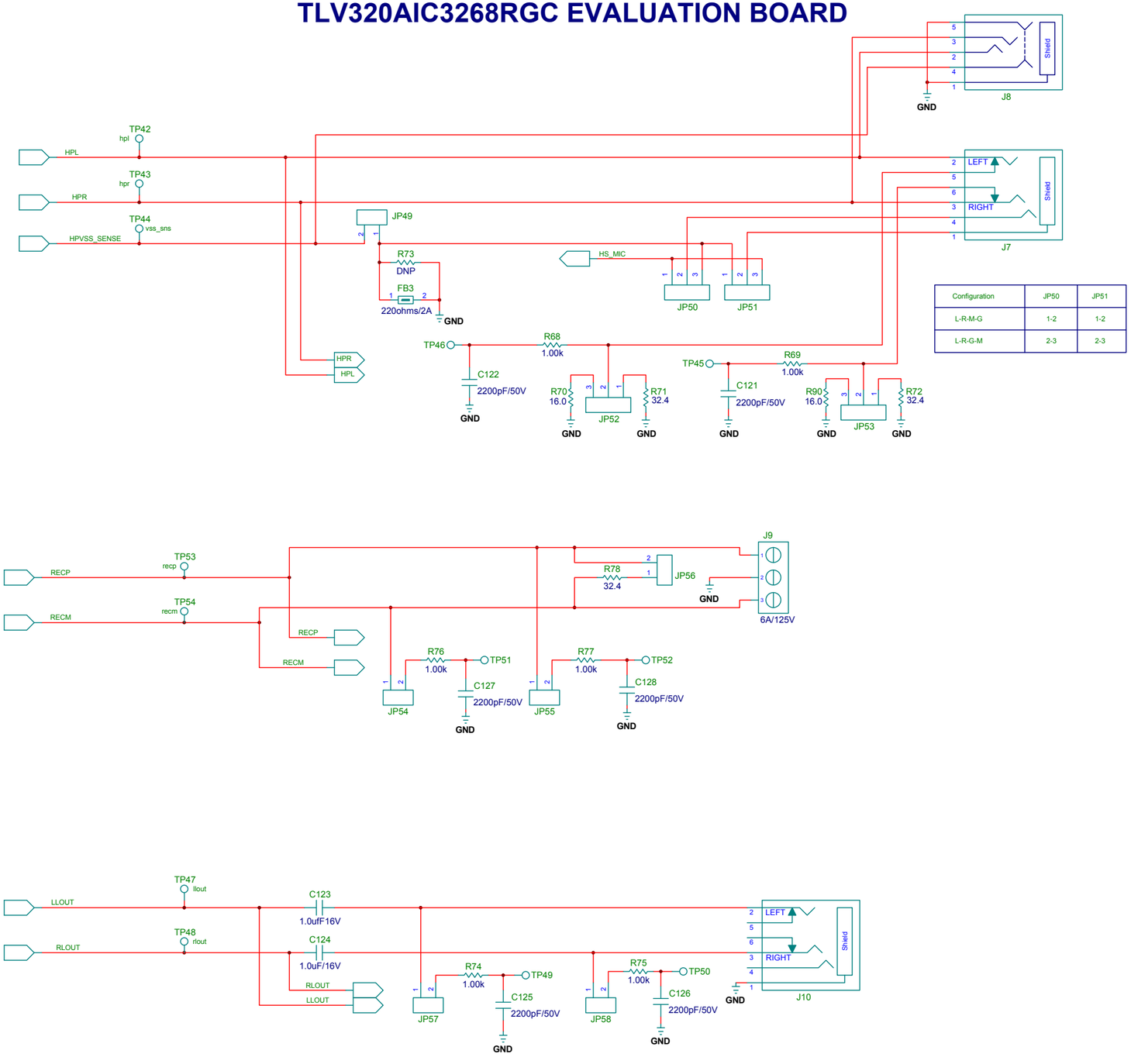
TLV320AIC3268RGC EVALUATION BOARD



TIDA-00403

PAGE INFO: TLV320AIC3268		DATE JANUARY 31, 2014	SCH REV C
DESIGN LEAD JOHN FEDAK IV		FILENAME AIP013C_Schematic.sbk	PCB REV C
			SHEET 6 OF 11
			DRAWN BY L;DN

TLV320AIC3268RGC EVALUATION BOARD



Configuration	JP50	JP51
L-R-M-G	1-2	1-2
L-R-G-M	2-3	2-3

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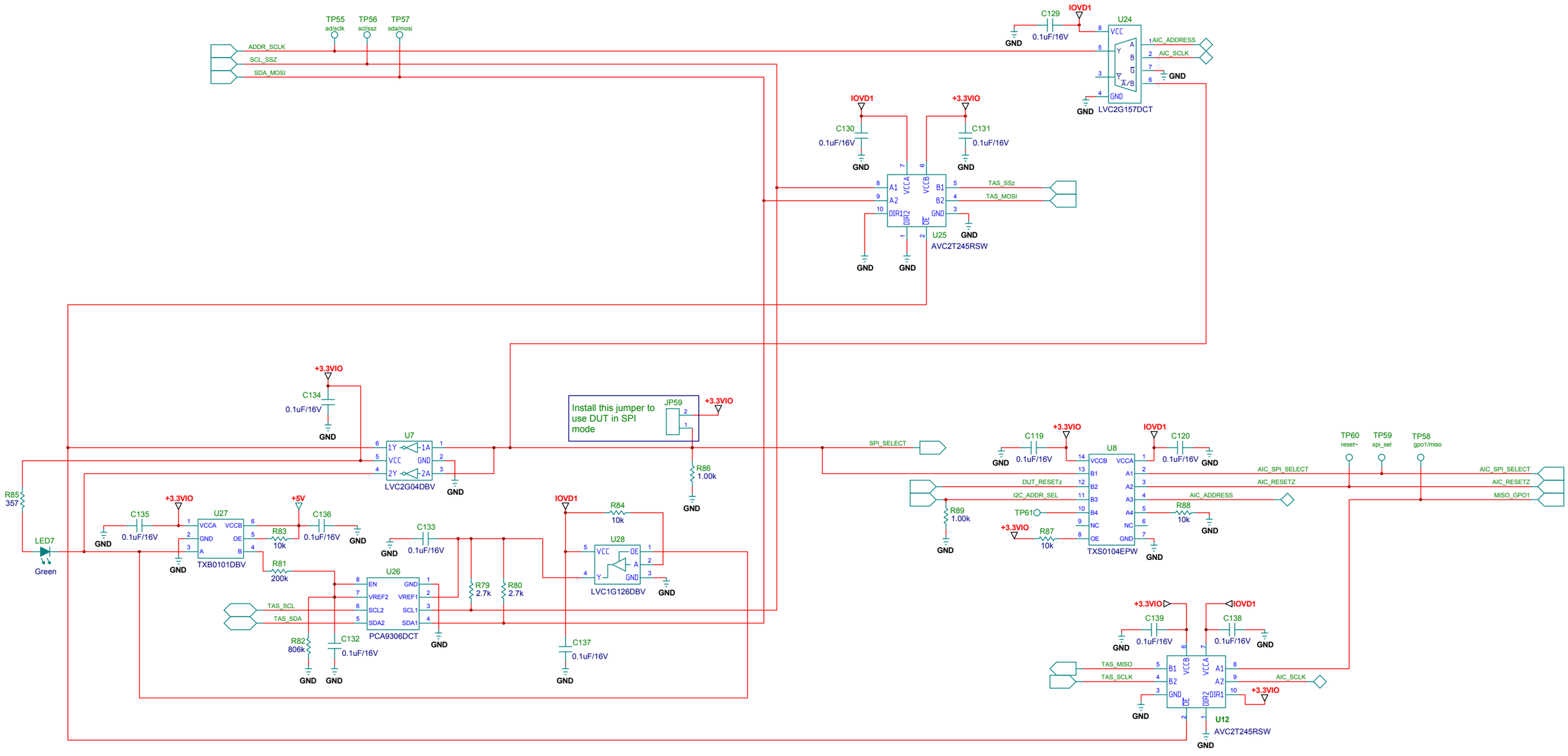
PAGE INFO: AUDIO CONNECTORS		DATE JANUARY 31, 2014	SCH REV C
DESIGN LEAD JOHN FEDAK IV		FILENAME AIP013C_Schematic.sbk	PCB REV C
			SHEET 7 OF 11
			DRAWN BY L;DN

TLV320AIC3268RGC EVALUATION BOARD



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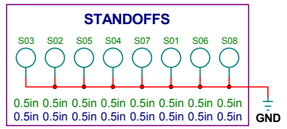
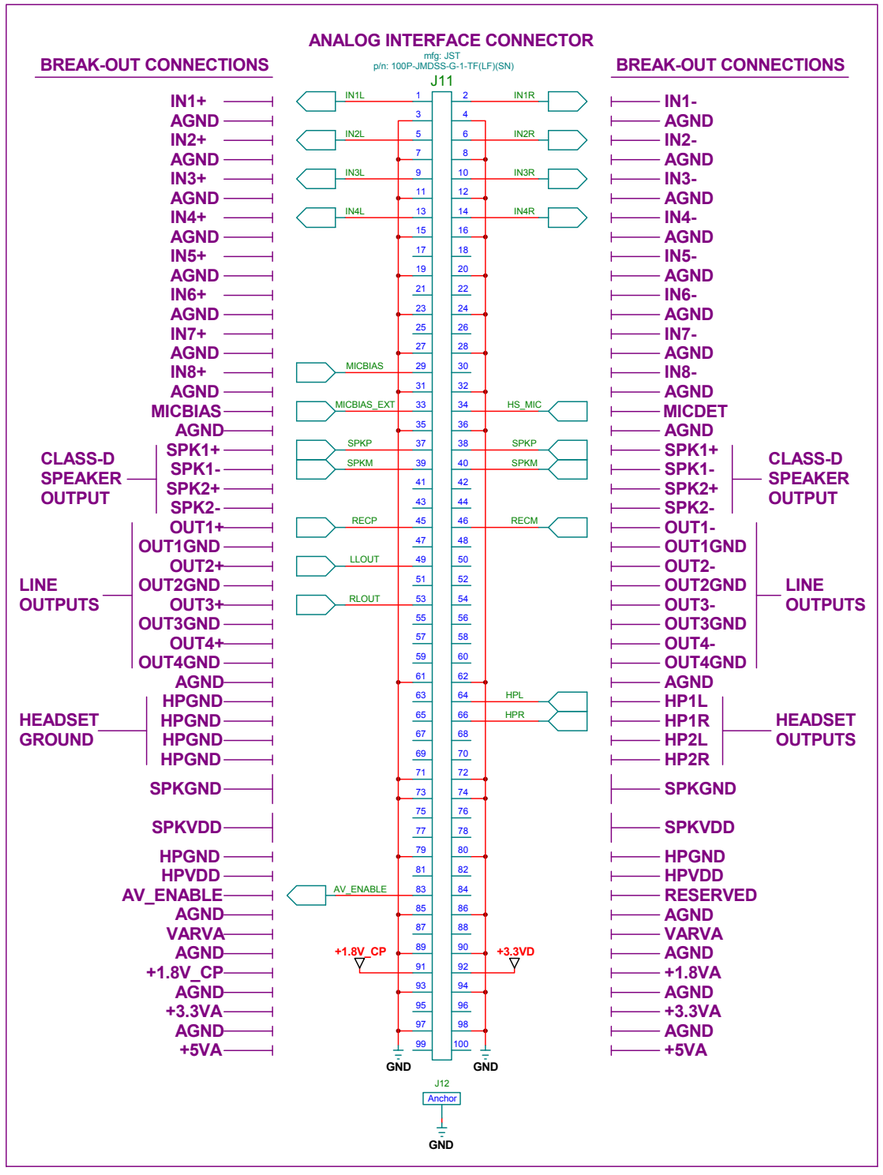
PAGE INFO: I2C TRANSLATION AND SELECTION		DATE JANUARY 31, 2014	SCH REV C
DESIGN LEAD JOHN FEDAK IV		FILENAME AIP013C_Schematic.sbk	PCB REV C
			SHEET 8 OF 11
			DRAWN BY L;DN

TLV320AIC3268RGC EVALUATION BOARD

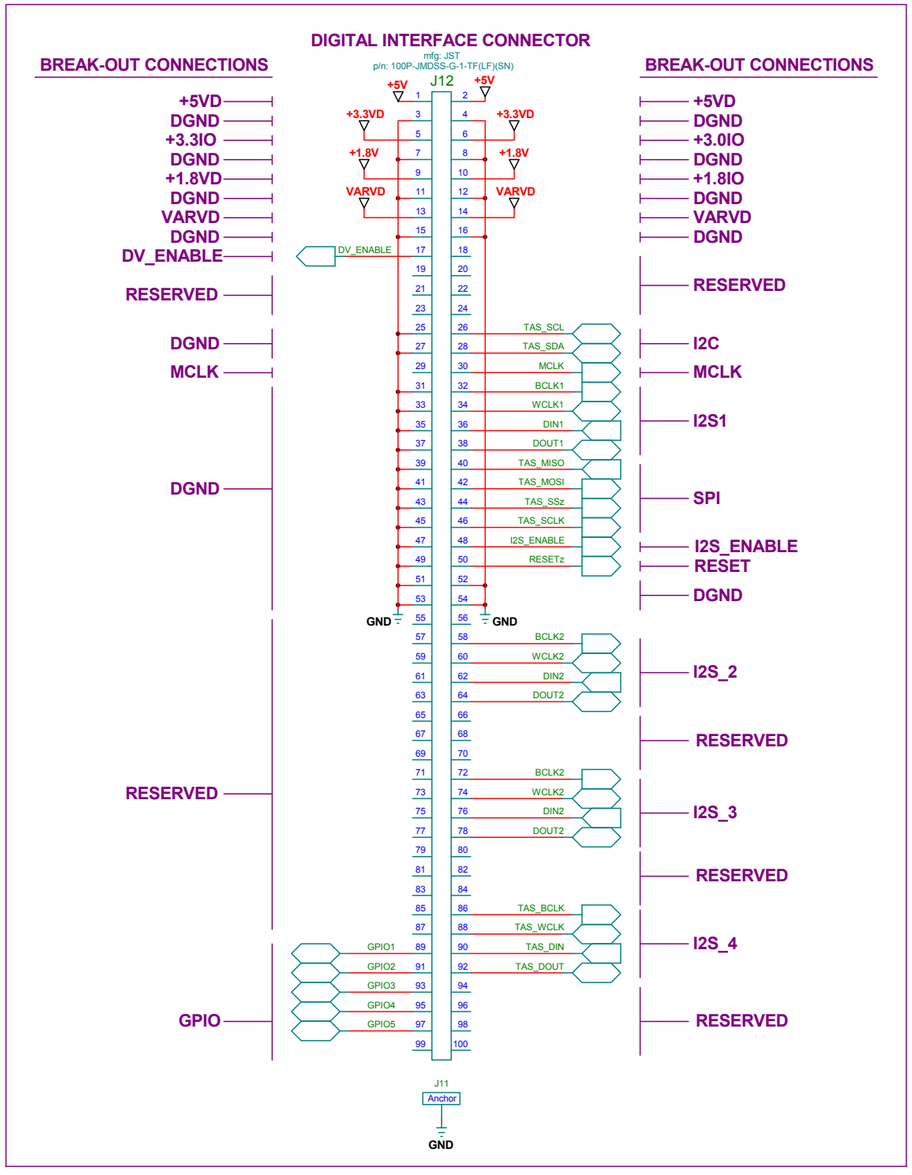
STANDOFFS



ANALOG INTERFACE CONNECTOR



DIGITAL INTERFACE CONNECTOR



TIDA-00403

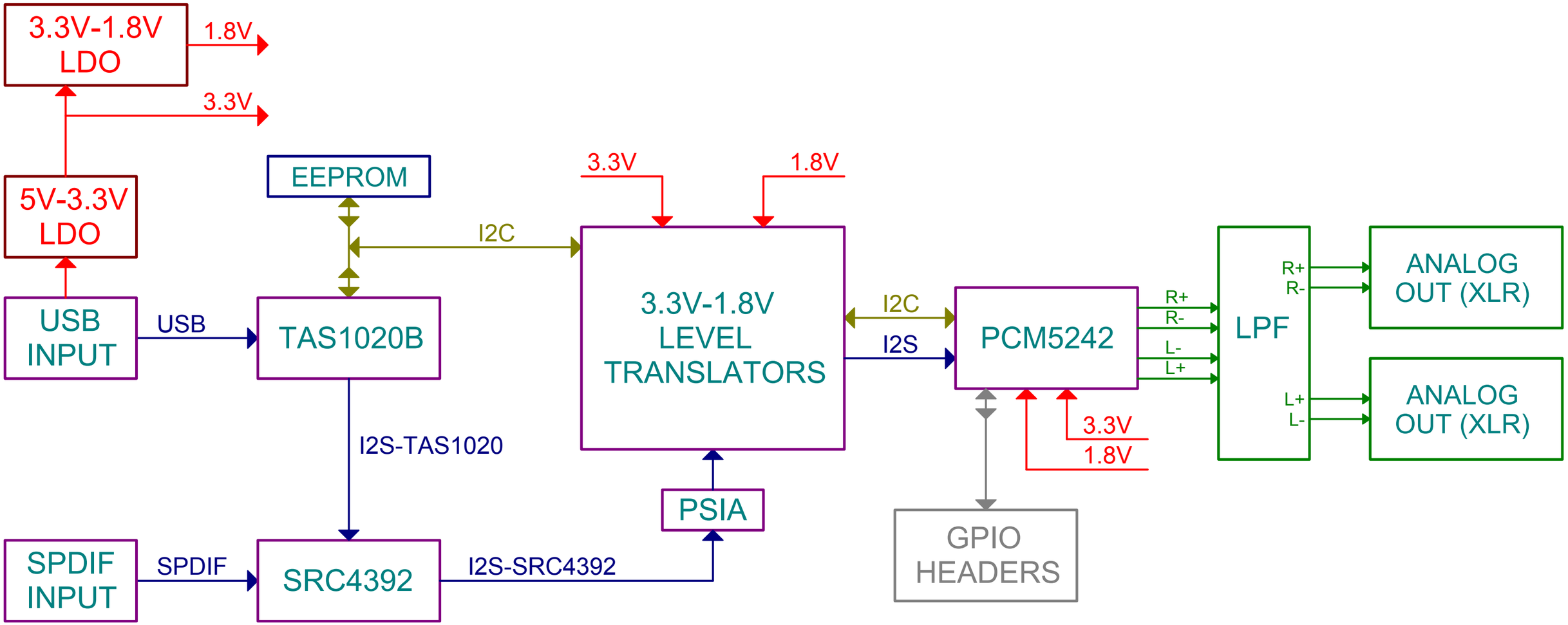
TEXAS INSTRUMENTS			SCH REV C
			PCB REV C
PAGE INFO: BREAKOUT BOARD CONNECTIONS		DATE JANUARY 31, 2014	SHEET 9 OF 11
DESIGN LEAD JOHN FEDAK IV		FILENAME AIP013C_Schematic.sbk	DRAWN BY L;DN

TLV320AIC3268RGC EVALUATION BOARD

REVISION HISTORY

REVISION	DESCRIPTION	DATE	APPROVED BY
A	- Initial Release.	MARCH 1, 2013	JA
B	Schematic: - Renamed and reorganized jumper reference designators. All named JPx. - Fixed I2S jumper short circuits. - DUT DVSS pins 56 and 57 connected to GND via 0-ohm. PCB: - Replaced TI logo. - Fixed S3 and S4 labels. - Applied DNPs to BOM. - Added silk labels to clarify jack and terminal functionality. - Updated invalid part numbers,	DECEMBER 20, 2013	JF4
C	Schematic: - Replaced OSC1 and OSC2. - Replaced Y1. - Corrected IOVD1 net connection to MIC1/2/3. - Updated U12 part number. PCB: - Routed changes above. - Moved J4/J7/J10 closer to edge of board.	JANUARY 31, 2014	JF4

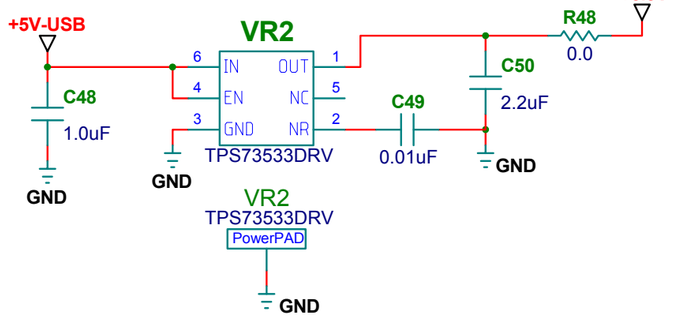
PCM5242RHB EVM BLOCK DIAGRAM



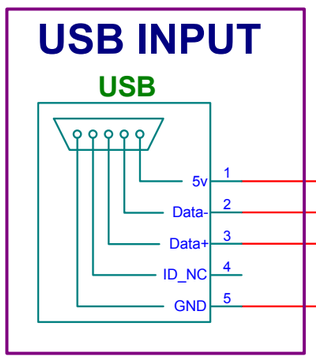
TEXAS INSTRUMENTS		TIDA-00403	SCH REV A
			PCB REV A
PAGE INFO: BLOCK DIAGRAM		DATE JULY 30, 2014	SHEET 1 OF 6
DESIGN LEAD DAVID K. WILSON		FILENAME AIP024A_Schematic.sbk	DRAWN BY LDN

PCM5242RHB EVALUATION MODULE

5V to 3.3V LDO

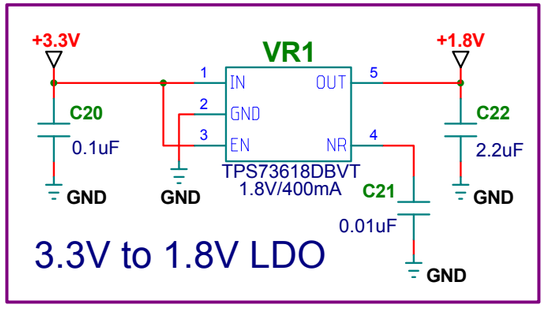


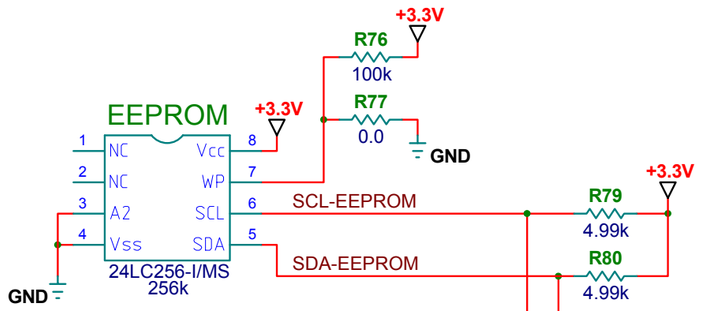
USB INPUT

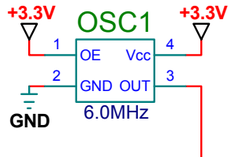


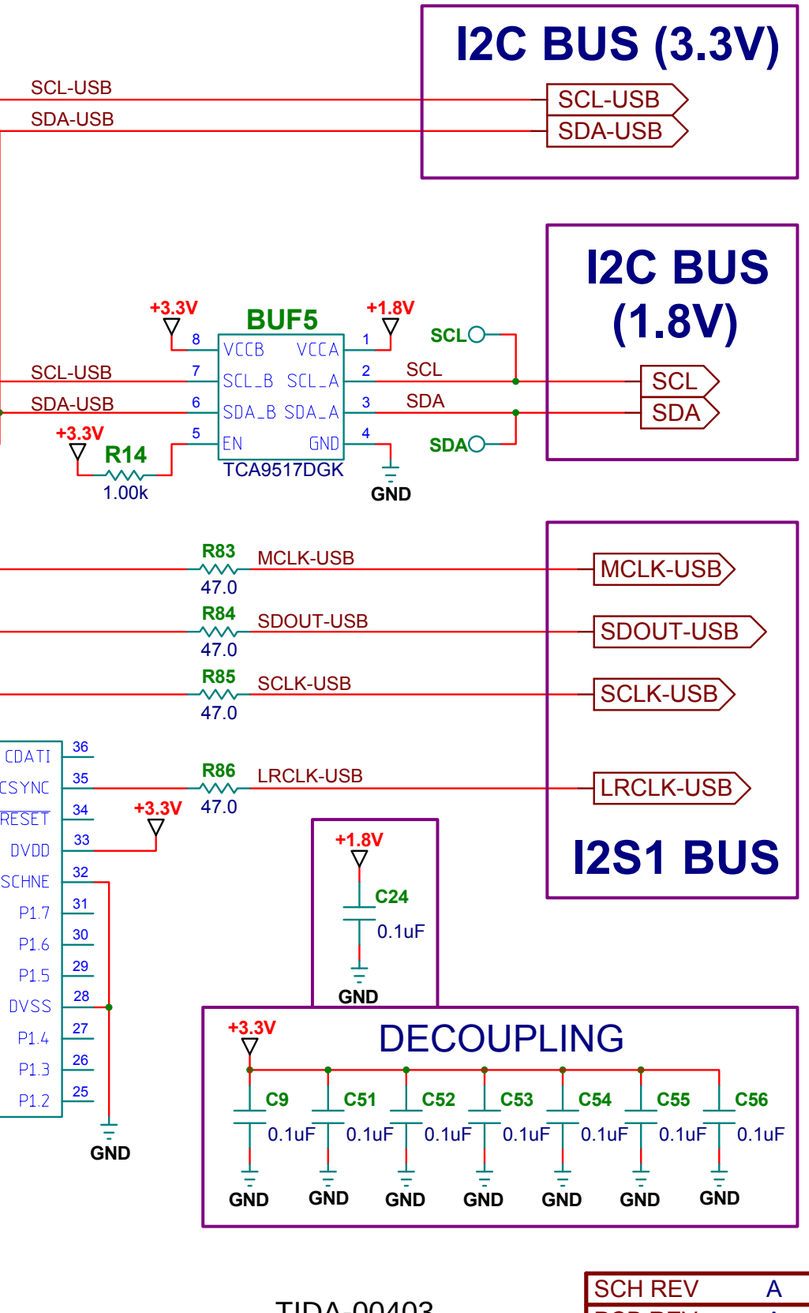
RESET

3.3V to 1.8V LDO









TIDA-00403

TEXAS INSTRUMENTS			SCH REV A
PAGE INFO:	USB TO I2C/I2S CONVERTER	DATE JULY 30, 2014	PCB REV A
DESIGN LEAD	DAVID K. WILSON	FILENAME AIP024A_Schematic.sbk	SHEET 2 OF 6
			DRAWN BY LDN

PCM5242RHB EVALUATION MODULE

SPDIF INPUT

+3.3V
C63 0.1uF
GND
OPTO-IN
VCC
GND
Case
OUT
PLR135/T10
OPTO-IN
SPDIF
Shield
Signal
Black
GND
R50 75
C30 0.1uF
RX2+
C31 0.1uF
RX2-
GND

DECOUPLING

+1.8V
C17 0.1uF
C18 0.1uF
C19 0.1uF
C23 0.1uF
GND GND GND GND

+3.3V
3.3V
R47 360
Green/2.0V
GND

HARDWARE

HWB1 HWB2 HWB3 HWB4
GND GND GND GND
BUMPONS

I2C BUS (3.3V)

SCL-USB
SDA-USB

RESET

RESET
GND
+3.3V
R69 10.0k
C41 0.1uF
GND

U3

SRC4392IPFBR

SCL-USB
SDA-USB
+3.3V
R51 1.00k
R52 4.99k
RESET
MCLK-USB
SRC-READY
R53 22.1
Blue/3.3V
GND
RXCKI
+1.8V
C32 0.1uF
RXCKO
RX-LOCK
R55 22.1
Blue/3.3V
+3.3V
GND
C38 0.1uF
C37 10uF
GND GND
RX2-
RX2+
C64 0.1uF
GND
OPTO-IN
+3.3V
C33 0.1uF
GND
+3.3V
C34 10uF
C35 0.1uF
GND GND
GND GND
SCLK-SRC
LRCLK-SRC
SDOUT-SRC
SCLK-USB
LRCLK-USB
SDOUT-USB

Pin	Name	Pin	Name
24	RST	48	BCKB
23	INT	47	LRCKB
22	CDOUT	46	SDINB
21	CDIN	45	SDOUTB
20	CCLK	44	BGND
19	CCS	43	DGND3
18	CPM	42	VIO
17	VDD18	41	NC
16	DGND1	40	SDOUTA
15	RDY	39	SDINA
14	MUTE	38	LRCKA
13	RXCKI	37	BCKA
12	RXCKO	36	SYNC
11	LOCK	35	BLS
10	AGND	34	AESOUT
9	VCC	33	VDD33
8	RX4-	32	TX+
7	RX4+	31	TX-
6	RX3-	30	DGND2
5	RX3+	29	GPO4
4	RX2-	28	GPO3
3	RX2+	27	GPO2
2	RX1-	26	GPO1
1	RX1+	25	MCLK

PSIA CLOCK SELECT

PSIA IN = 2-3
JUMPER 1-2
FOR PASS-THRU

MCLK-USB 1 JP10 2
RXCKO 3
MCLK-SRC 1 JP1 2 MCLK-PSIA
GND 3
SCLK-SRC 1 JP2 2 SCLK-PSIA
GND 3
LRCLK-SRC 1 JP3 2 LRCLK-PSIA
GND 3
SDOUT-SRC 1 JP4 2 SDOUT-PSIA
GND 3

TRANSLATORS

BUF1 +1.8V
OE VCC
A Y
GND
74AUP1G125DRL
R5 47.0
SCK

BUF2
74AUP1G125DRL
R6 47.0
BCK

BUF3
74AUP1G125DRL
R7 47.0
LRCK

BUF4
74AUP1G125DRL
GND
R8 47.0
DIN

I2S2 BUS

SCK
BCK
LRCK
DIN

I2S1 BUS

MCLK-USB
SCLK-USB
LRCLK-USB
SDOUT-USB

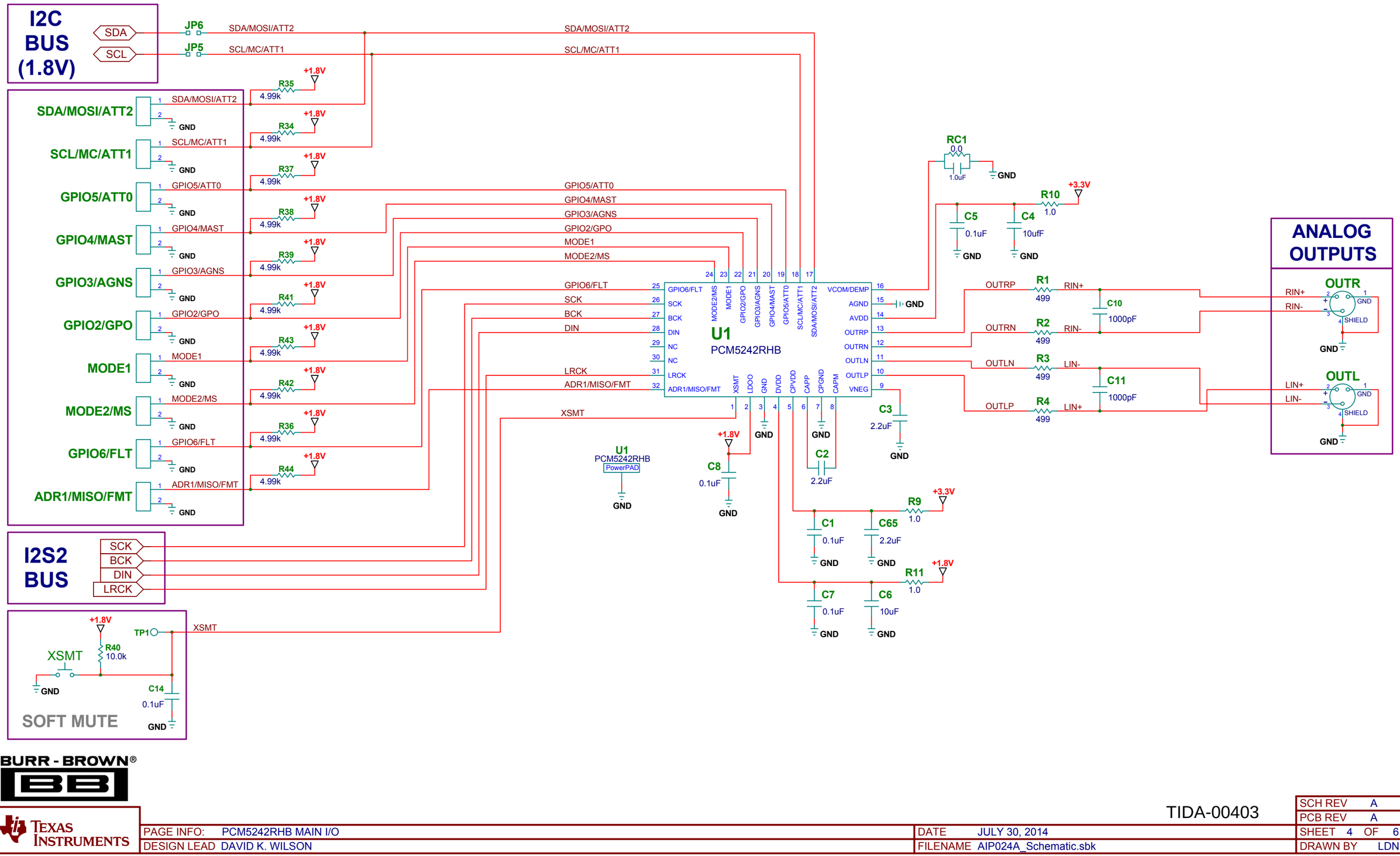
RESET

RESET

TIDA-00403

TEXAS INSTRUMENTS			
PAGE INFO: SAMPLE RATE CONVERTER		DATE JULY 30, 2014	SCH REV A
DESIGN LEAD DAVID K. WILSON		FILENAME AIP024A_Schematic.sbk	PCB REV A
			SHEET 3 OF 6
			DRAWN BY LDN

PCM5242RHB EVALUATION MODULE



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TEXAS INSTRUMENTS			SCH REV A
			PCB REV A
PAGE INFO: PCM5242RHB MAIN I/O		DATE JULY 30, 2014	SHEET 4 OF 6
DESIGN LEAD DAVID K. WILSON		FILENAME AIP024A_Schematic.sbk	DRAWN BY LDN

PCM5242RHB EVALUATION MODULE

REVISION HISTORY

REVISION	DESCRIPTION	DATE	APPROVAL
A	INITIAL RELEASE	JULY 30, 2014	DKW

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