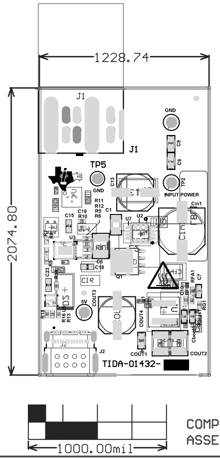
Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				▨
2	Top Solder	Solder Resist	0.40mil	3.5	▨
3	Top Layer	Copper	1.40mil		▨
4	Dielectric1	FR-4	6.00mil	4.8	▨
5	Signal Layer 1	Copper	1.40mil		▨
6	Dielectric2		44.00mil	4.2	▨
7	Signal Layer 2	Copper	1.40mil		▨
8	Dielectric 3		6.00mil	4.2	▨
9	Bottom Layer	Copper	1.40mil		▨
10	Bottom Solder	Solder Resist	0.40mil	3.5	▨
11	Bottom Overlay				▨

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 8 MIL
MIN. VIA PAD SIZE: 16 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
☐ FR-408 ☒ FR-4 High Tg ☐ OTHER ______
THICKNESS: ☒ 62 MIL (1.6mm) +/-10% ☐ OTHER ______
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- ______
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- ______

DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER ______

BOARD FINISH:
SILKSCREEN: ☒ TOP ☒ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER ______
SOLDER RESIST COLOR: ☒ GREEN ☐ OTHER ______
☒ MATTE ☐ SEMI-GLOSS

SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENEPIG
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER ______

ARRAY/PANEL: ☐ CUT AND TRIM PER M1 BOARD OUTLINE
☒ N.C. ROUTE ☐ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ RoHS ☐ OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER

TEXAS INSTRUMENTS

PROJECT TITLE:
TIDA-01432

DESIGNED FOR:
Not for Public Release

FILE NAME:
TIDA-01432_E1.PcbDoc

ENGINEER:
H.Bovenzi

LAYOUT BY:
Bovenzi/Clanin

SCALE: 1.00

ALTIUM DESIGNER VERSION:
17.1.5.472

PCB VIEWED FROM TOP SIDE
BOARD #: TIDA-01432
REV #: E1
SVN REV: Not In VersionControl
LAYER NAME =
TID #: N/A
PLOT NAME = Top Layer Assembly Drawing
GENERATED 9/18/2017 3:22:03 PM
TEXAS INSTRUMENTS

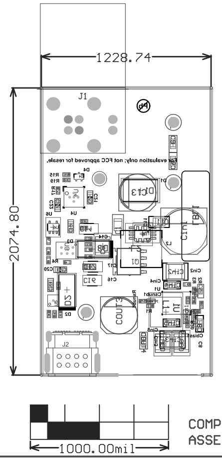
Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				▨
2	Top Solder	Solder Resist	0.40mil	3.5	▨
3	Top Layer	Copper	1.40mil		▨
4	Dielectric1	FR-4	6.00mil	4.8	▨
5	Signal Layer 1	Copper	1.40mil		▨
6	Dielectric2		44.00mil	4.2	▨
7	Signal Layer 2	Copper	1.40mil		▨
8	Dielectric 3		6.00mil	4.2	▨
9	Bottom Layer	Copper	1.40mil		▨
10	Bottom Solder	Solder Resist	0.40mil	3.5	▨
11	Bottom Overlay				▨

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 8 MIL
MIN. VIA PAD SIZE: 16 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
☐ FR-408 ☒ FR-4 High Tg ☐ OTHER ______
THICKNESS: ☒ 62 MIL (1.6mm) +/-10% ☐ OTHER ______
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- ______
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- ______

DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER ______

BOARD FINISH:
SILKSCREEN: ☒ TOP ☒ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER ______
SOLDER RESIST COLOR: ☒ GREEN ☐ OTHER ______
☒ MATTE ☐ SEMI-GLOSS

SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENEPIG
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER ______

ARRAY/PANEL: ☐ CUT AND TRIM PER M1 BOARD OUTLINE
☒ N.C. ROUTE ☐ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ RoHS ☐ OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER

TEXAS INSTRUMENTS

PROJECT TITLE: TIDA-01432	
DESIGNED FOR: Not for Public Release	
FILE NAME: TIDA-01432_E1.PcbDoc	
ENGINEER: H.Bovenzi	LAYOUT BY: Bovenzi/Clanin
SCALE: 1.00	ALTIUM DESIGNER VERSION: 17.1.5.472

PCB VIEWED FROM TOP SIDE		BOARD #:	TIDA-01432	E1	SVN REV: Not In VersionControl
LAYER NAME =		TID #:	N/A		
PLOT NAME =	Assembly Drawing	GENERATED	9/18/2017	3:22:10 PM	TEXAS INSTRUMENTS

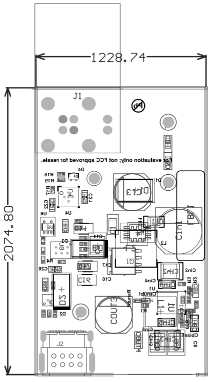
Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				▨
2	Top Solder	Solder Resist	0.40mil	3.5	▨
3	Top Layer	Copper	1.40mil		▨
4	Dielectric1	FR-4	6.00mil	4.8	▨
5	Signal Layer 1	Copper	1.40mil		▨
6	Dielectric2		44.00mil	4.2	▨
7	Signal Layer 2	Copper	1.40mil		▨
8	Dielectric 3		6.00mil	4.2	▨
9	Bottom Layer	Copper	1.40mil		▨
10	Bottom Solder	Solder Resist	0.40mil	3.5	▨
11	Bottom Overlay				▨

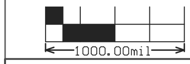
ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

ZZ2 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.





COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB VIEWED FROM TOP SIDE	SVN REV:	E1	BOARD #:	TIDA-01432	SVN REV: Not In VersionControl
LAYER NAME = Bottom Overlay			TID #:	N/A	
PLOT NAME = Signal Layer 2 Assembly Drawing	3:22:18 PM		GENERATED	9/18/2017	3:22:18 PM

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 8 MIL
MIN. VIA PAD SIZE: 16 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
☐ FR-408 ☒ FR-4 High Tg ☐ OTHER ____
THICKNESS: ☒ 62 MIL (1.6mm) +/-10% ☐ OTHER ____
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- ____
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- ____

DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER ____

BOARD FINISH:
SILKSCREEN: ☒ TOP ☒ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER ____
SOLDER RESIST COLOR: ☒ GREEN ☐ OTHER ____
☒ MATTE ☐ SEMI-GLOSS

SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENEPIG
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER ____

ARRAY/PANEL: ☐ CUT AND TRIM PER M1 BOARD OUTLINE
☒ N.C. ROUTE ☐ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ RoHS ☐ OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER

TEXAS INSTRUMENTS

PROJECT TITLE: TIDA-01432
DESIGNED FOR: Not for Public Release
FILE NAME: TIDA-01432_E1.PcbDoc
ENGINEER: H.Bovenzi
LAYOUT BY: Bovenzi/Clanin
SCALE: 1.00
ALTIUM DESIGNER VERSION: 17.1.5.472

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				▨
2	Top Solder	Solder Resist	0.40mil	3.5	▨
3	Top Layer	Copper	1.40mil		▨
4	Dielectric1	FR-4	6.00mil	4.8	▨
5	Signal Layer 1	Copper	1.40mil		▨
6	Dielectric2		44.00mil	4.2	▨
7	Signal Layer 2	Copper	1.40mil		▨
8	Dielectric 3		6.00mil	4.2	▨
9	Bottom Layer	Copper	1.40mil		▨
10	Bottom Solder	Solder Resist	0.40mil	3.5	▨
11	Bottom Overlay				▨

ZZ1 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.

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ZZ3 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 8 MIL
MIN. VIA PAD SIZE: 16 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
☐ FR-408 ☒ FR-4 High Tg ☐ OTHER ____________
THICKNESS: ☒ 62 MIL (1.6mm) +/-10% ☐ OTHER ____________
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- ____________
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- ____________

DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER ________

BOARD FINISH:
SILKSCREEN: ☒ TOP ☒ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER ____________
SOLDER RESIST COLOR: ☒ GREEN ☐ OTHER ____________
☒ MATTE ☐ SEMI-GLOSS

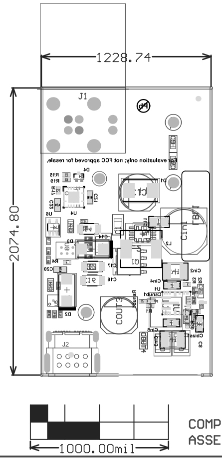
SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENEPIG
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER ____________

ARRAY/PANEL: ☐ CUT AND TRIM PER M1 BOARD OUTLINE
☒ N.C. ROUTE ☐ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ RoHS ☐ OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: [No Variations]

PCB VIEWED FROM TOP SIDE	SVN REV: E1	BOARD #:	TIDA-01432	E1	SVN REV: Not In VersionControl
LAYER NAME =	Bottom Overlay	TID #:	N/A		
PLOT NAME =	TEXAS INSTRUMENTS Assembly Drawing	GENERATED	9/18/2017	3:22:26 PM	

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TEXAS INSTRUMENTS

PROJECT TITLE:
TIDA-01432

DESIGNED FOR:
Not for Public Release

FILE NAME:
TIDA-01432_E1.PcbDoc

ENGINEER:	LAYOUT BY:
H.Bovenzi	Bovenzi/Clanin
SCALE: 1.00	ALTIUM DESIGNER VERSION: 17.1.5.472

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