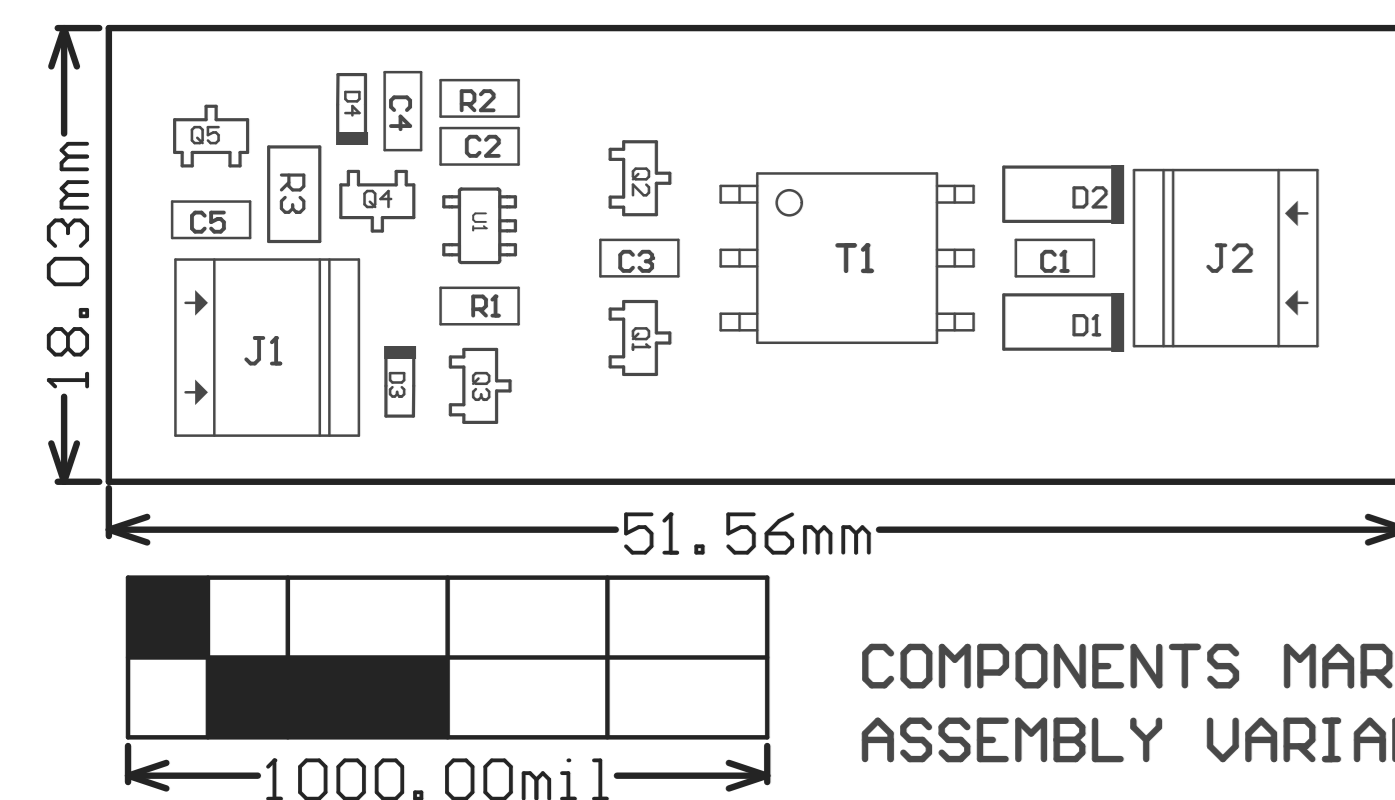


DESIGN INFORMATION	
MIN. TRACK WIDTH:	<u>8</u> MIL
MIN. CLEARANCE:	<u>0.2</u> mm
MIN. VIA PAD SIZE:	<u>24</u> MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- <u>5</u> MIL, HOLES +/- <u>3</u> MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- <u>3</u> MIL	
MATERIAL:	
<input type="checkbox"/> FR-408 <input checked="" type="checkbox"/> FR-4 High Tg <input type="checkbox"/> OTHER _____	
THICKNESS:	<input checked="" type="checkbox"/> 62 MIL (1.6mm) +/-10% <input type="checkbox"/> OTHER _____
TOLERANCE:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2 <input type="checkbox"/> OTHER +/- _____
BOW & TWIST:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2 <input type="checkbox"/> OTHER +/- _____
DRILLING:	
REFERENCE:	<input checked="" type="checkbox"/> AS SHOWN <input checked="" type="checkbox"/> NC_DRILL FILES
PTH COPPER THICKNESS:	<input checked="" type="checkbox"/> 20-30 um <input type="checkbox"/> OTHER _____
BOARD FINISH:	
SILKSCREEN:	<input checked="" type="checkbox"/> TOP <input checked="" type="checkbox"/> BOTTOM
SILKSCREEN COLOR:	<input checked="" type="checkbox"/> WHITE <input type="checkbox"/> OTHER _____
SOLDER RESIST COLOR:	<input checked="" type="checkbox"/> GREEN <input type="checkbox"/> OTHER _____ <input checked="" type="checkbox"/> MATTE <input type="checkbox"/> SEMI-GLOSS
SURFACE FINISH:	<input checked="" type="checkbox"/> IMMERSION GOLD (ENIG) <input type="checkbox"/> ENEPIG <input type="checkbox"/> IMM. TIN/SILVER OR EQUIV <input type="checkbox"/> OTHER _____
ARRAY/PANEL:	<input type="checkbox"/> CUT AND TRIM PER M1 BOARD OUTLINE <input type="checkbox"/> N.C. ROUTE <input checked="" type="checkbox"/> V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:	
<input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS -> <input type="checkbox"/> 1 <input checked="" type="checkbox"/> 2 <input type="checkbox"/> 3 <input checked="" type="checkbox"/> RoHS <input type="checkbox"/> OTHER PER ORDER	
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS. PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION:	<input type="checkbox"/> YES
BARE BOARD ELEC. TEST:	<input type="checkbox"/> NONE <input checked="" type="checkbox"/> REQUIRED <input type="checkbox"/> PER ORDER
<input type="checkbox"/> XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE	
<input type="checkbox"/> LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE	

The PMP30440 Rev\_B Reference Design has been built on PMP30440 Rev\_A PCB.

- M1 Board Outline
- M2 Board Dimensions
- M9 Title Sheet
- M10 Fab Notes



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.  
ASSEMBLY VARIANT: [No Variations]

PCB VIEWED FROM TOP SIDE	BOARD #: PMP30440	REV: A	SUN REV: Not In VersionControl	Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.	ENGINEER: R. Scibilia	LAYOUT BY: R. Scibilia
M18 Embedded Assembly	TID #: .TID				SCALE: 1.00	ALTIUM DESIGNER VERSION: 17.1.5.472
PLOT NAME = Top LayerAssembly Drawing	GENERATED : 11/23/2018 1:09:13 PM	TEXAS INSTRUMENTS				

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