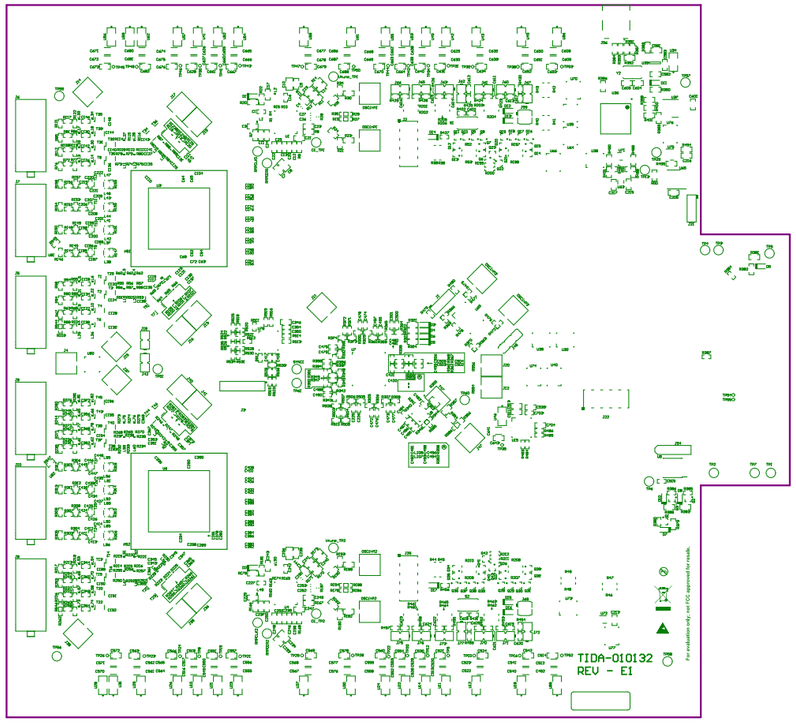
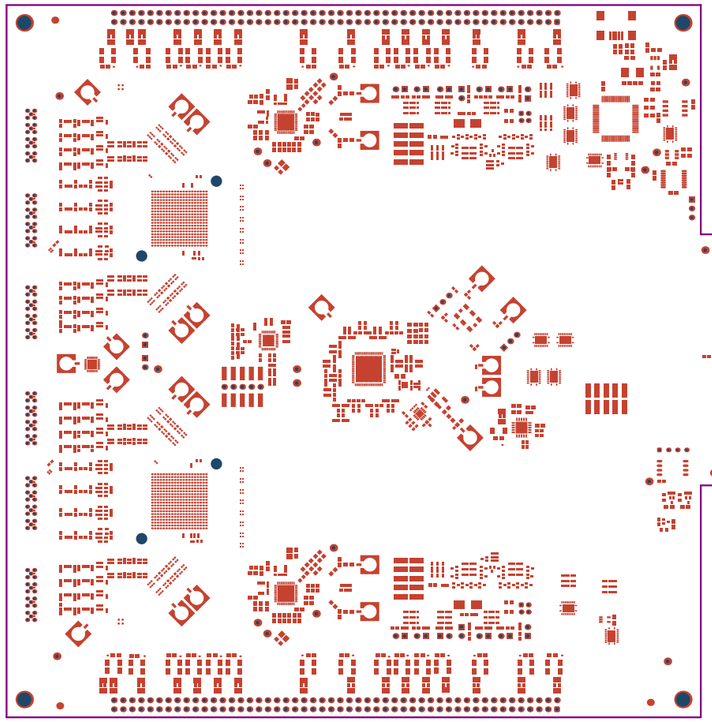
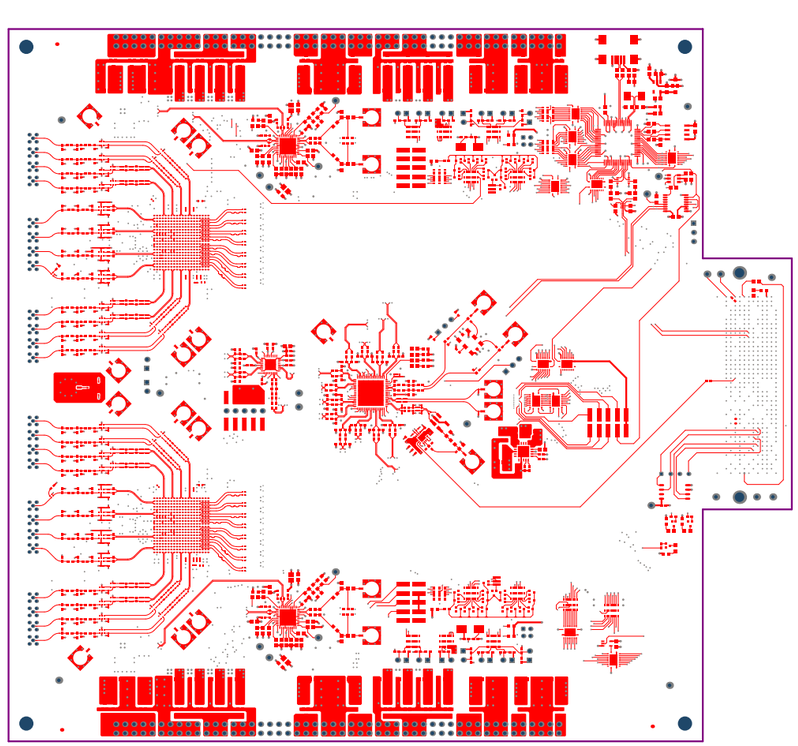


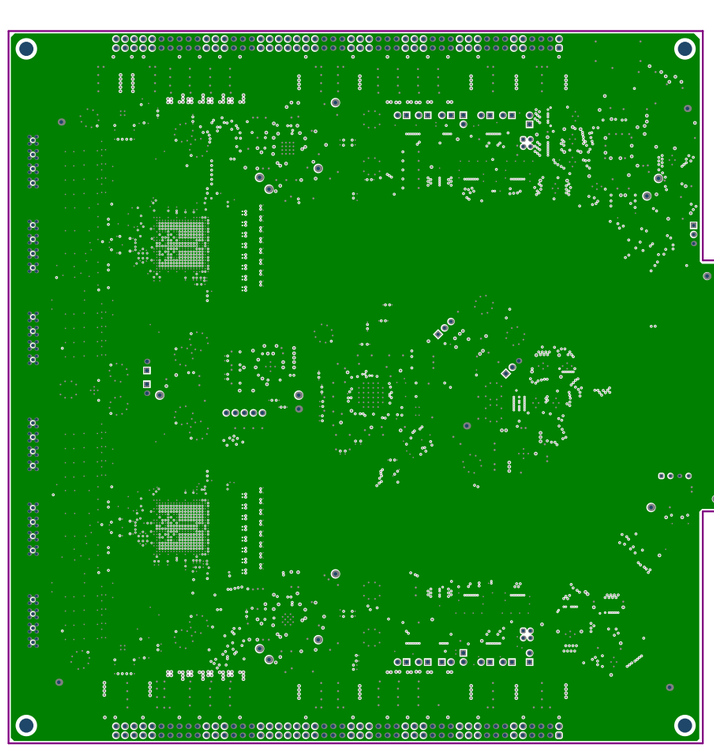
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-010132	REV: E1	SVN REV:	
LAYER NAME = Top Overlay	TID #:010132			
PLOT NAME = Top Overlay	GENERATED : 5/23/2019 11:52:51 AM			TEXAS INSTRUMENTS



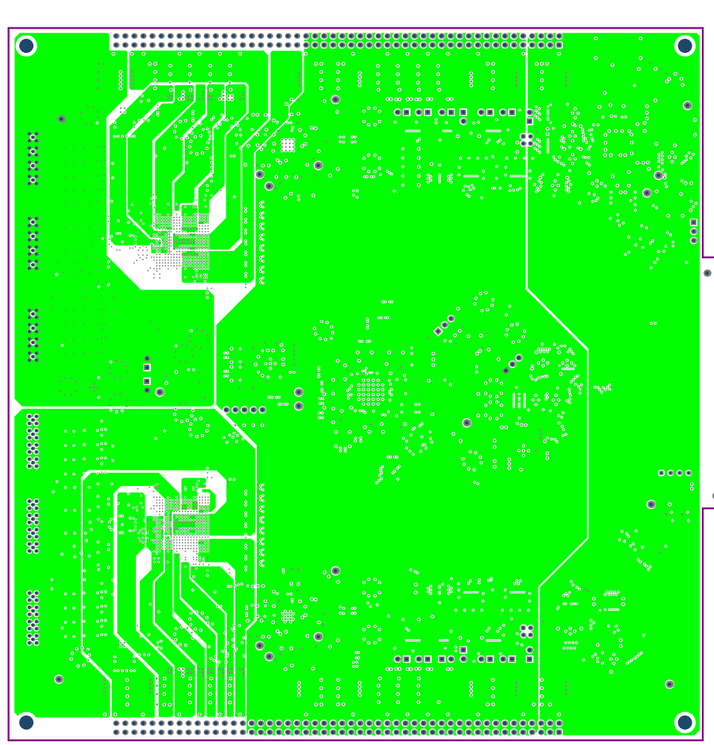
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-010132	REV: C:	SVN REV:
LAYER NAME = TOP SOLDER	TID #:010132		
PLOT NAME = Top Solder Mask	GENERATED : 5/23/2019 11:52:51 AM		TEXAS INSTRUMENTS



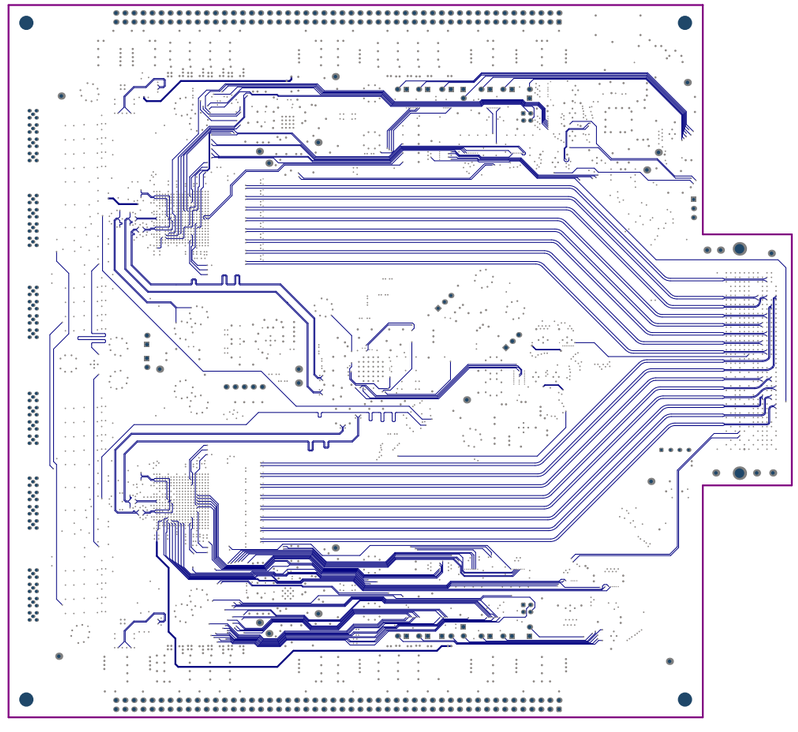
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01O132	REV: E:	SVN REV:
LAYER NAME = L1_Top Layer	TID #:01O132		
PLOT NAME = L1_Top Layer	GENERATED : 5/23/2019 11:52:51 AM		TEXAS INSTRUMENTS



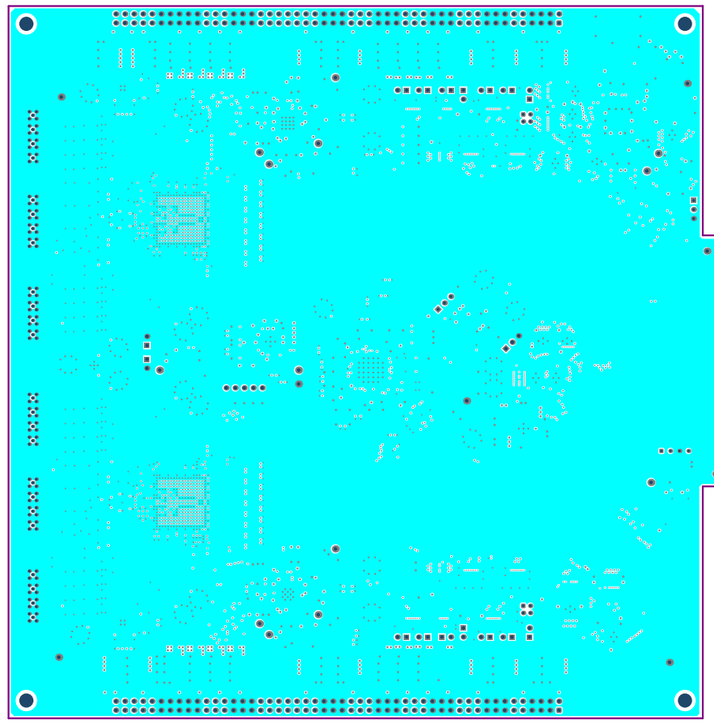
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01O132	REV: E	SVN REV:
LAYER NAME = L2_GNDPI Layer	TID #:01O132		
PLOT NAME = L2_GNDPI Layer	GENERATED : 5/23/2019 11:52:51 AM		TEXAS INSTRUMENTS



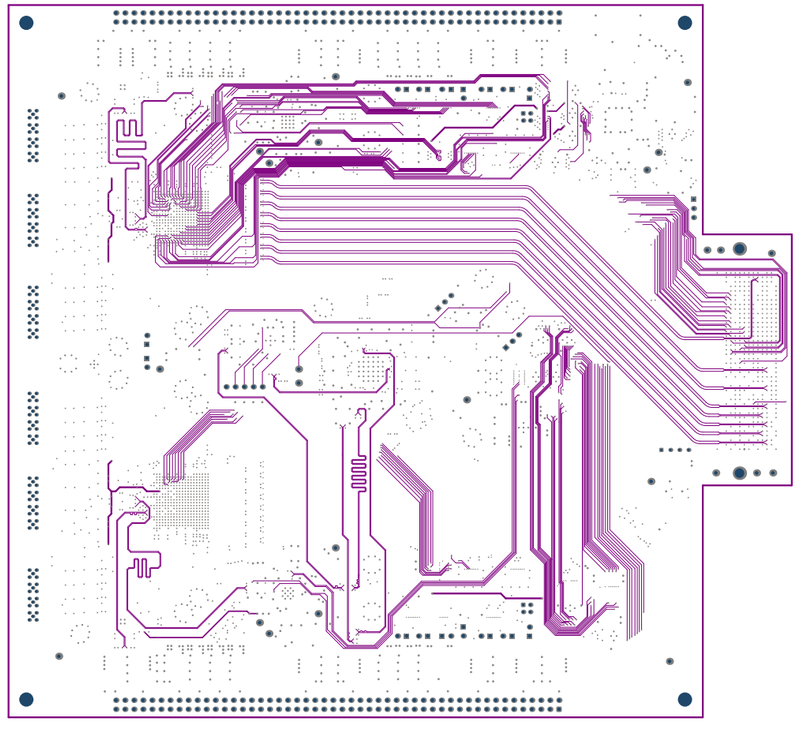
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01O132	REV: E	SVN REV:
LAYER NAME = L3_PWRPI Layer	TID #:01O132		
PLOT NAME = L3_PWRPI Layer	GENERATED : 5/23/2019 11:52:52 AM		TEXAS INSTRUMENTS



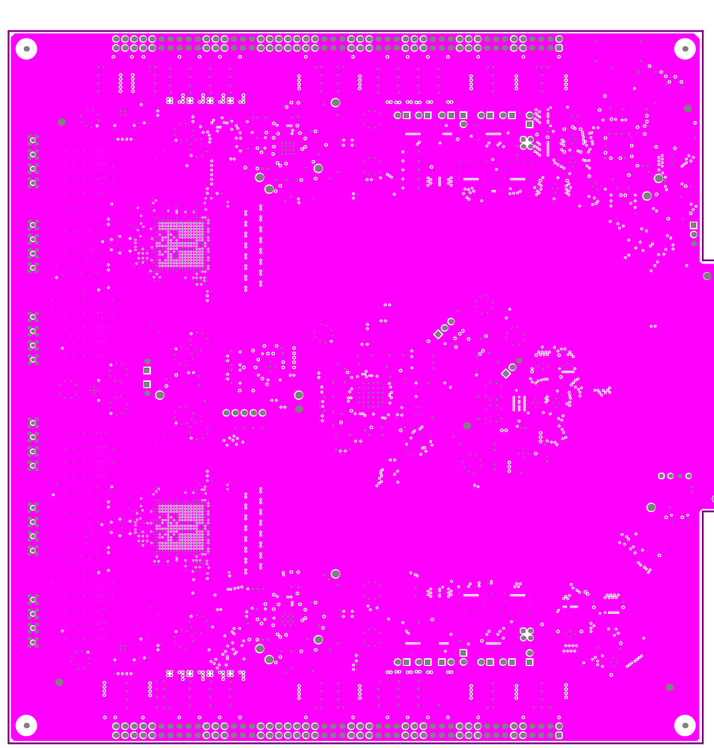
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-010132	REV: E1	SUN REV:
LAYER NAME = L4_SIGI Layer	TID #:010132		
PLOT NAME = L4_SIGI Layer	GENERATED : 5/23/2019 11:52:52 AM		TEXAS INSTRUMENTS



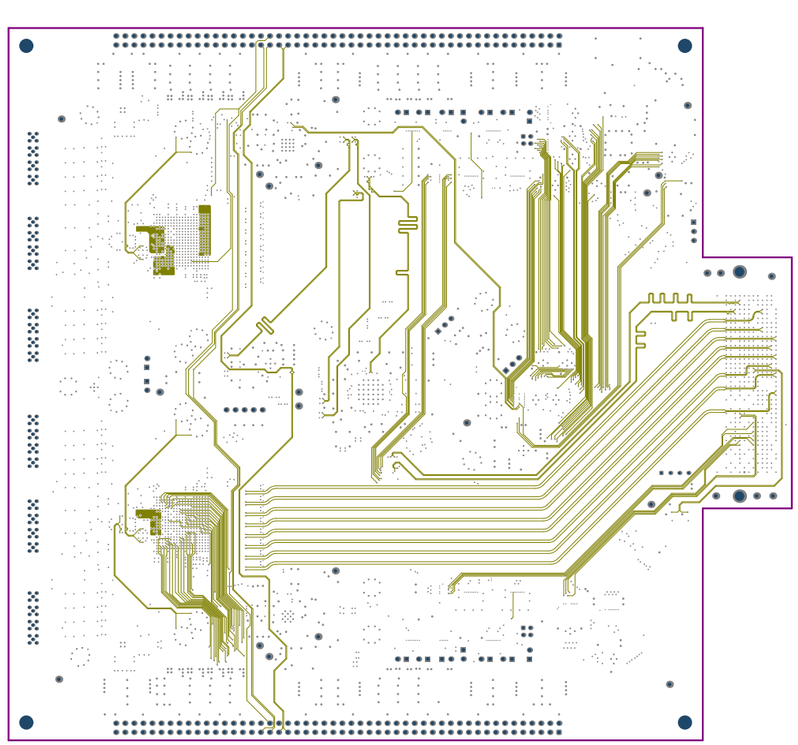
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-010132	REV: E1	SVN REV:
LAYER NAME = L5_GND Layer	TID #:010132		
PLOT NAME = L5_GND Layer	GENERATED : 5/23/2019 11:52:52 AM		TEXAS INSTRUMENTS



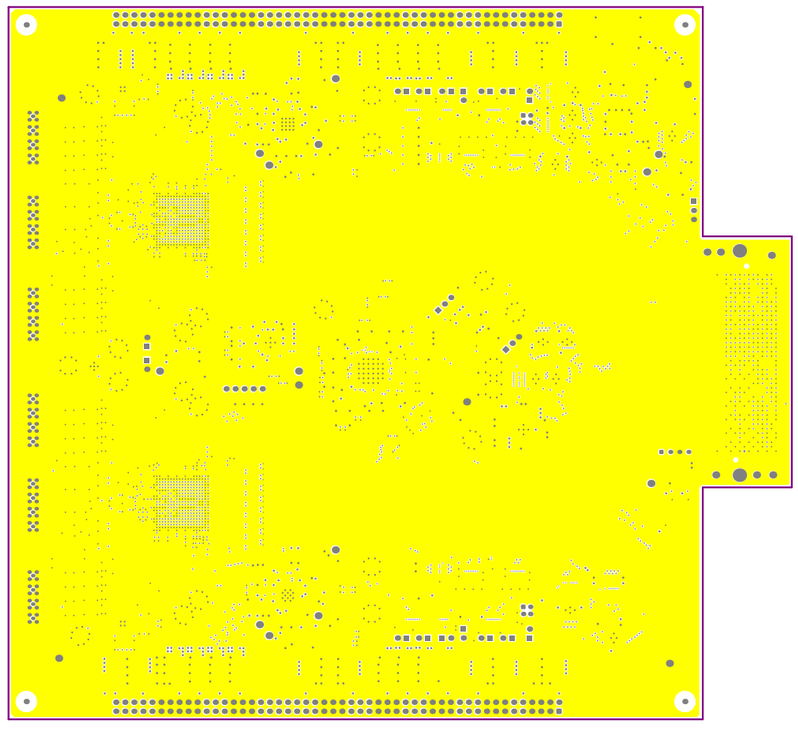
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-010132	REV: E1	SUN REV:
LAYER NAME = L6_SIG2 Layer	TID #:010132		
PLOT NAME = L6_SIG2 Layer	GENERATED : 5/23/2019 11:52:52 AM		TEXAS INSTRUMENTS



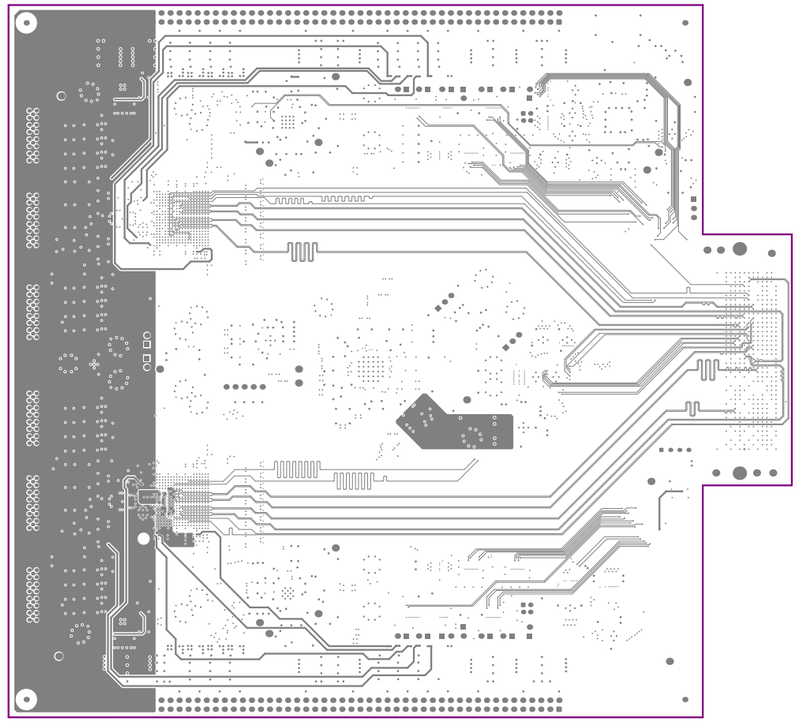
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-010132	REV: C1	SVN REV:
LAYER NAME = L7_GND Layer	TID #:010132		
PLOT NAME = L7_GND Layer	GENERATED : 5/23/2019 11:52:52 AM		TEXAS INSTRUMENTS



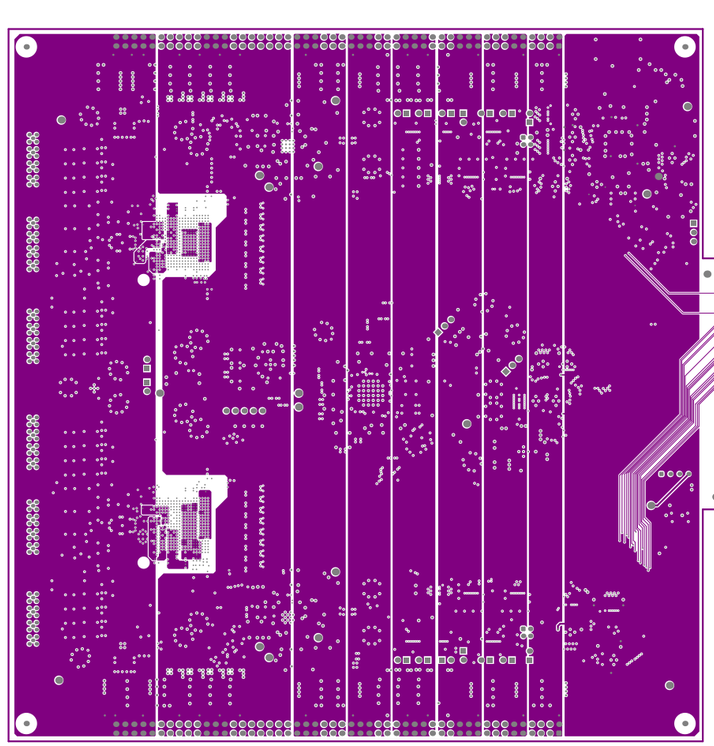
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01013 2	REV: E	SVN REV:
LAYER NAME = L8_SIG3 Layer	TID #:01013 2		
PLOT NAME = L8_SIG3 Layer	GENERATED : 5/23/2019 11:52:53 AM		TEXAS INSTRUMENTS



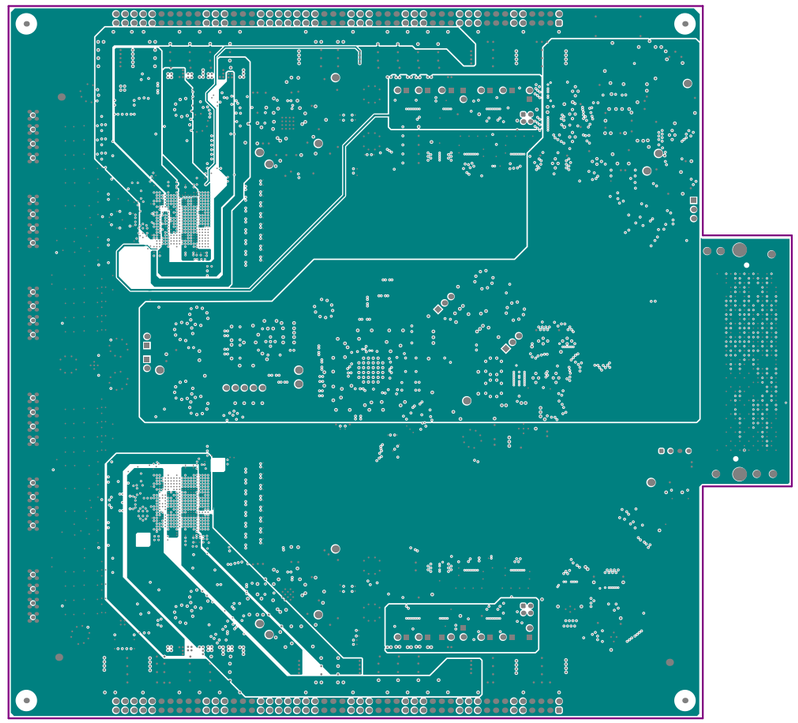
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-010132	REV: E1	SUN REV:
LAYER NAME = L9_GND Layer	TID #:010132		
PLOT NAME = L9_GND Layer	GENERATED : 5/23/2019 11:52:53 AM		TEXAS INSTRUMENTS



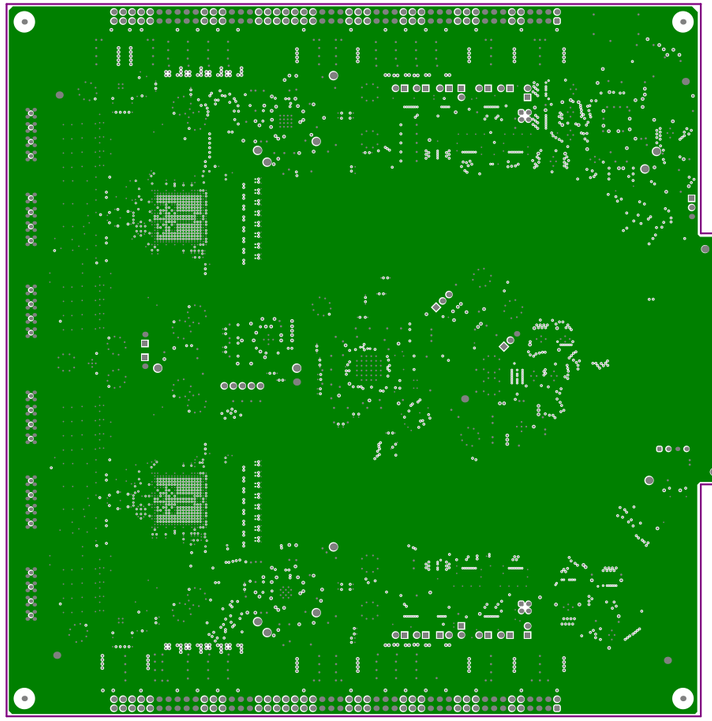
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01O132	REV: C:	SVN REV:
LAYER NAME = LIO_SIG4 Layer	TID #:01O132		
PLOT NAME = LIO_SIG4 Layer	GENERATED : 5/23/2019 11:52:53 AM		TEXAS INSTRUMENTS



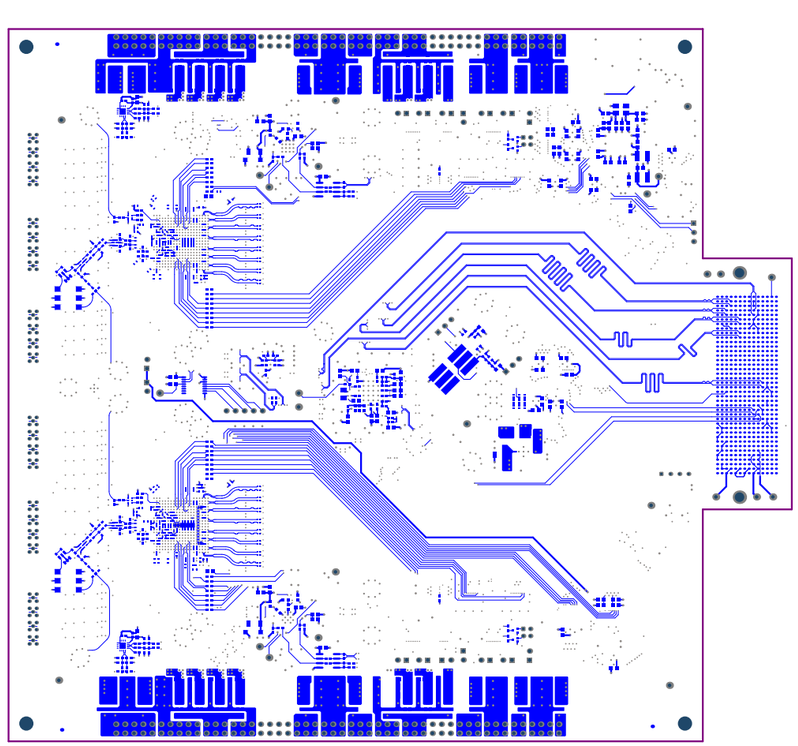
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01O132	REV: E	SVN REV:
LAYER NAME = LII_SIG/PWR Layer	TID #:01O132		
PLOT NAME = LII_SIG/PWR Layer	GENERATED : 5/23/2019 11:52:53 AM		TEXAS INSTRUMENTS



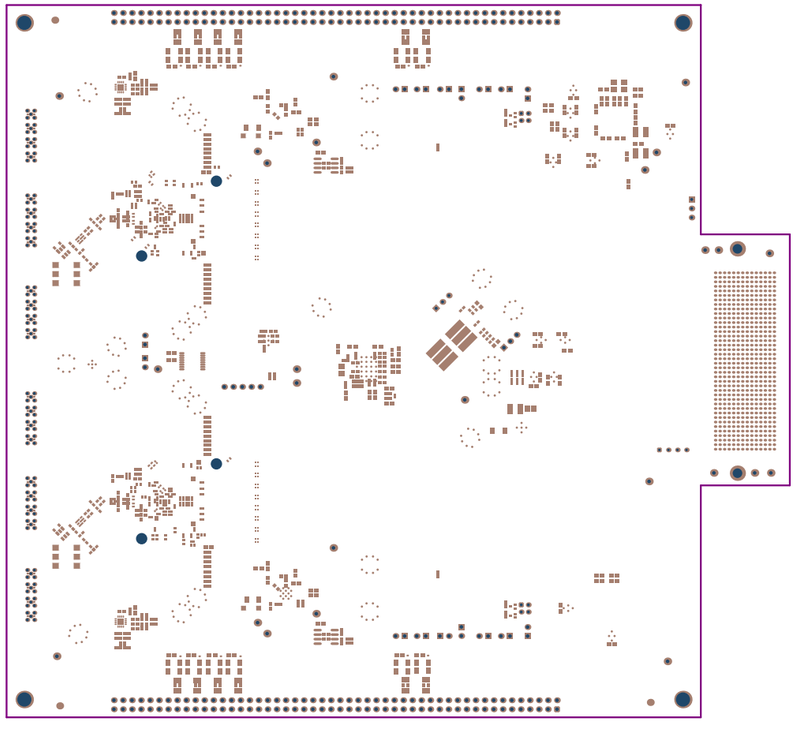
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01O132	REV: E:	SVN REV:
LAYER NAME = L12_PWRP2 Layer	TID #:01O132		
PLOT NAME = L12_PWRP2 Layer	GENERATED : 5/23/2019 11:52:53 AM		TEXAS INSTRUMENTS



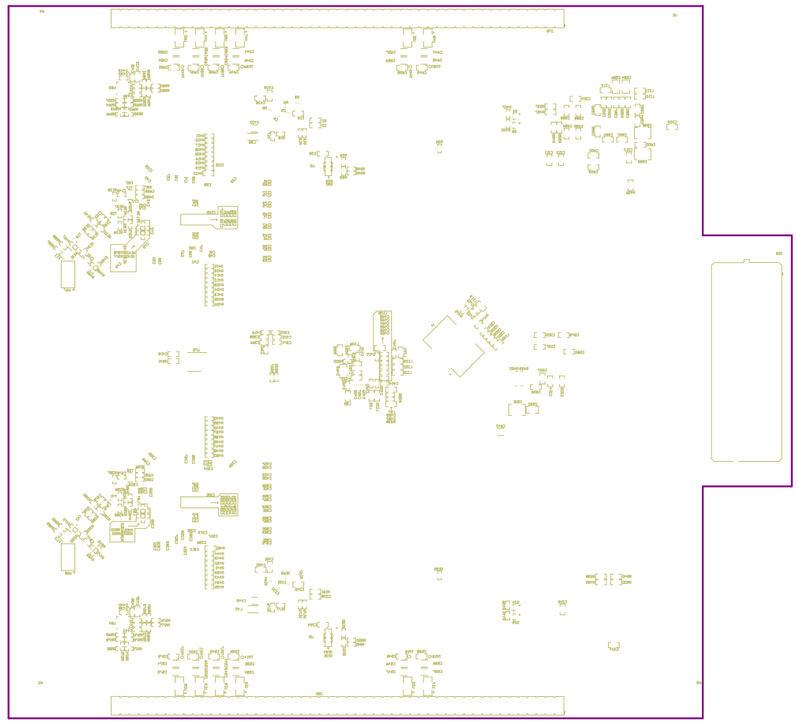
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-010132	REV: E:	SVN REV:
LAYER NAME = L13_GND2 Layer	TID #:010132		
PLOT NAME = L13_GND2 Layer	GENERATED : 5/23/2019 11:52:53 AM		TEXAS INSTRUMENTS



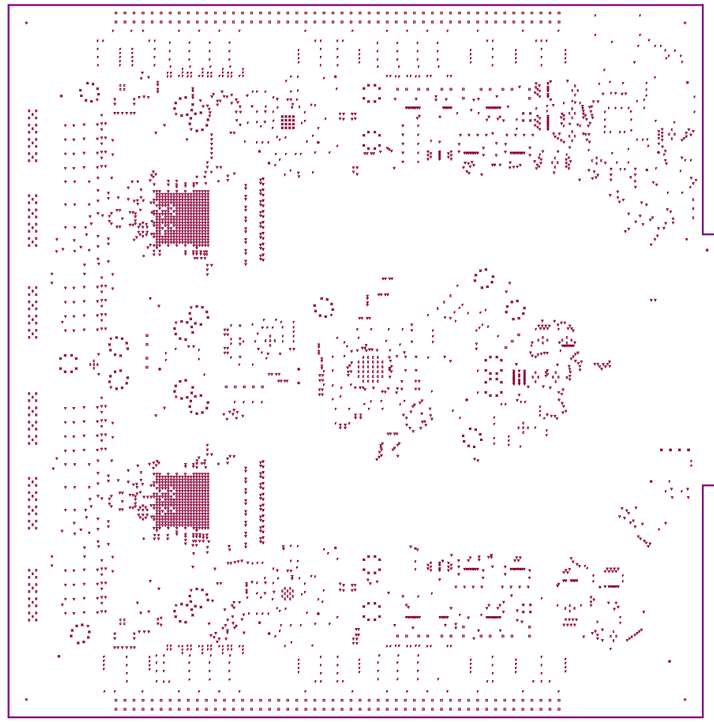
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-010132	REV: E	SVN REV:
LAYER NAME = L14_Bottom Layer	TID #:010132		
PLOT NAME = L14_Bottom Layer	GENERATED : 5/23/2019 11:52:54 AM		TEXAS INSTRUMENTS



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-010132	REV: E:	SUN REV:
LAYER NAME = BOTTOM SOLDER	TID #:010132		
PLOT NAME = Bottom Solder Mask	GENERATED : 5/23/2019 11:52:54 AM		TEXAS INSTRUMENTS



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-010132	REV: C1	SUN REV:
LAYER NAME = BOTTOM OVERLAY	TID #:010132		
PLOT NAME = Bottom Overlay	GENERATED : 5/23/2019 11:52:54 AM	TEXAS INSTRUMENTS	



Drill Table

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad
▼	189	6.00mil (0.152mm)	PTH	Round	L1_Top Layer - L14_Bottom Layer	Via
C	115	7.87mil (0.200mm)	PTH	Round	L1_Top Layer - L14_Bottom Layer	Via
▽	2320	8.00mil (0.203mm)	PTH	Round	L1_Top Layer - L14_Bottom Layer	Via
✖	200	10.00mil (0.254mm)	PTH	Round	L1_Top Layer - L14_Bottom Layer	Via
F	621	12.00mil (0.305mm)	PTH	Round	L1_Top Layer - L14_Bottom Layer	Via
⊠	4	27.56mil (0.700mm)	PTH	Round	L1_Top Layer - L14_Bottom Layer	Pad
D	120	31.00mil (0.787mm)	PTH	Round	L1_Top Layer - L14_Bottom Layer	Pad
⌘	8	31.50mil (0.800mm)	PTH	Round	L1_Top Layer - L14_Bottom Layer	Pad
E	6	33.47mil (0.850mm)	PTH	Round	L1_Top Layer - L14_Bottom Layer	Pad
⌬	25	40.00mil (1.016mm)	PTH	Round	L1_Top Layer - L14_Bottom Layer	Pad
□	240	40.16mil (1.020mm)	PTH	Round	L1_Top Layer - L14_Bottom Layer	Pad
⧈	2	50.00mil (1.270mm)	NPTH	Round	L1_Top Layer - L14_Bottom Layer	Pad
❁	2	106.00mil (2.692mm)	PTH	Round	L1_Top Layer - L14_Bottom Layer	Pad
◇	4	125.00mil (3.175mm)	PTH	Round	L1_Top Layer - L14_Bottom Layer	Pad
○	4	157.00mil (3.988mm)	NPTH	Round	L1_Top Layer - L14_Bottom Layer	Pad
	3860 Total					

FOR 6MIL DRILL +0/-6MIL
FOR 7.87MIL DRILL +0/-7.87MIL
FOR 8MIL DRILL +0/-8MIL
FOR 10MIL DRILL +0/-10MIL
FOR 12MIL DRILL +0/-12MIL
FOR PTH DRILL +/-3MIL
FOR NPTH DRILL +/-2MIL
NOTE:
1.7.874mil Vias are not tented.
2.Fill all on pad vias (with non conductive material) and flat the surface (except 7.874mil via).

Stack up

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.50mil	3.5	
3	L1_Top Layer	Copper	2.00mil		
4	Dielectric1	R-5670K	4.10mil	3.175	
5	L2_GNDPI Layer	Copper	2.50mil		
6	Dielectric 2	R-5775K	3.00mil	3.42	
7	L3_PWRPI Layer	Copper	2.50mil		
8	Dielectric 3	R-5670K	3.60mil	3.175	
9	L4_SIG1 Layer	Copper	0.60mil		
10	Dielectric 4	R-5775K	3.00mil	3.42	
11	L5_GND Layer	Copper	0.60mil		
12	Dielectric 5	R-5670K	4.20mil	3.175	
13	L6_SIG2 Layer	Copper	0.60mil		
14	Dielectric 6	R-5775K	3.00mil	3.42	
15	L7_GND Layer	Copper	0.60mil		
16	Dielectric 7	R-5670K	4.10mil	3.175	
17	L8_SIG3 Layer	Copper	0.60mil		
18	Dielectric 8	R-5775K	3.00mil	3.42	
19	L9_GND Layer	Copper	0.60mil		
20	Dielectric 9	R-5670K	4.20mil	3.175	
21	L10_SIG4 Layer	Copper	0.60mil		
22	Dielectric 10	R-5775K	3.00mil	3.42	
23	L11_SIG/PWR Layer	Copper	0.60mil		
24	Dielectric 11	R-5670K	3.90mil	3.175	
25	L12_PWRP2 Layer	Copper	2.50mil		
26	Dielectric 12	R-5775K	3.00mil	3.42	
27	L13_GNDP2 Layer	Copper	2.50mil		
28	Dielectric 13	R-5670K	4.10mil	3.175	
29	L14_Bottom Layer	Copper	2.00mil		
30	Bottom Solder	Solder Resist	0.50mil	3.5	
31	Bottom Overlay				

IMPEDANCE TABLE:-

Layer	50 OHM SE	90 OHM DIFF	100 OHM DIFF TIGHTLY COUPLED	100 OHM DIFF LOOSELY COUPLED	REFERENCE LAYER
	TRACE WIDTH (MILS) +/-8%	WIDTH/SPACING (MILS) +/-8%	WIDTH/SPACING (MILS) +/-8%	WIDTH/SPACING (MILS) +/-8%	
L1_Top Layer	8 MILS	7.25 MILS TRACE/ 6.95 MILS SPACE	5.25 MILS TRACE/ 5.75 MILS SPACE	7.5 MILS TRACE/ 20.5 MILS SPACE	L2_GNDPI Layer
L4_SIG1 Layer	3.5 MILS	NA	3.4 MILS TRACE/ 8.6 MILS SPACE	3.4 MILS TRACE/ 24.6 MILS SPACE	L5_GND Layer
L6_SIG2 Layer	3.75 MILS	NA	3.5 MILS TRACE/ 6.5 MILS SPACE	3.5 MILS TRACE/ 24.5 MILS SPACE	L7_GND Layer
L8_SIG3 Layer	3.5 MILS	NA	3.25 MILS TRACE/ 6.75 MILS SPACE	3.5 MILS TRACE/ 24.5 MILS SPACE	L9_GND Layer
L10_SIG4 Layer	3.55 MILS	NA	3.55 MILS TRACE/ 8.45 MILS SPACE	3.6 MILS TRACE/ 24.4 MILS SPACE	L9_GND Layer
L11_SIG/PWR Layer	3.5 MILS	NA	3.4 MILS TRACE/ 8.6 MILS SPACE	3.4 MILS TRACE/ 24.6 MILS SPACE	L12_PWRP2 Layer
L14_Bottom Layer	8 MILS	7.25 MILS TRACE/ 6.95 MILS SPACE	5.25 MILS TRACE/ 5.75 MILS SPACE	7.5 MILS TRACE/ 20.5 MILS SPACE	L13_GNDP2 Layer

DESIGN INFORMATION

BOARD SIZE (REFER ALSO ARRAY/PANEL PROFILING INFORMATION)
220MM X 200MM
Number of Layers : 14
MIN. TRACK WIDTH: 3.25 MIL
MIN. CLEARANCE: 5 MIL
MIN. VIA PAD SIZE: 12 MIL
MINIMUM ANNULAR RING 3MIL EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

MATERIAL:
[ ] FR-408 [ ] FR-4 High Tg [X] OTHER R-5670K AND R-5775K
THICKNESS: [X] 63 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
COPPER THICKNESS (FINISHED):
OUTER: [ ] 1.4MIL (1oz) [X] 2MIL (1.4oz) [ ] 2.8MIL (2oz)
INNER SIGNAL: [X] 0.6MIL (1/2oz) [X] 2.8MIL (2oz) [ ] N/A
DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH MIN COPPER THICKNESS: [X] 1MIL [ ] OTHER
BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR:
[X] GREEN [ ] BLUE [ ] OTHER
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TN/SILVER OR EQUIV [ ] OTHER
ARRAY/PANEL: [ ] CUT AND TRIM PER MECH LAYER 1
[ ] N.C. ROUTE [X] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS --> [ ] 1 [X] 2 [ ] 3
[X] UL 94V-0 [X] RoHS [ ] OTHER PER ORDER
ADDITIONAL REQUIREMENTS: VIA TENTING: YES [X] NO [ ]
MICROSECTION: [ ] YES IMPEDANCE CONTROL: YES [X] NO [ ]
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
MANUFACTURER'S UL: [ ] RAIL [ ] METAL [X] SILK

TEXAS INSTRUMENTS

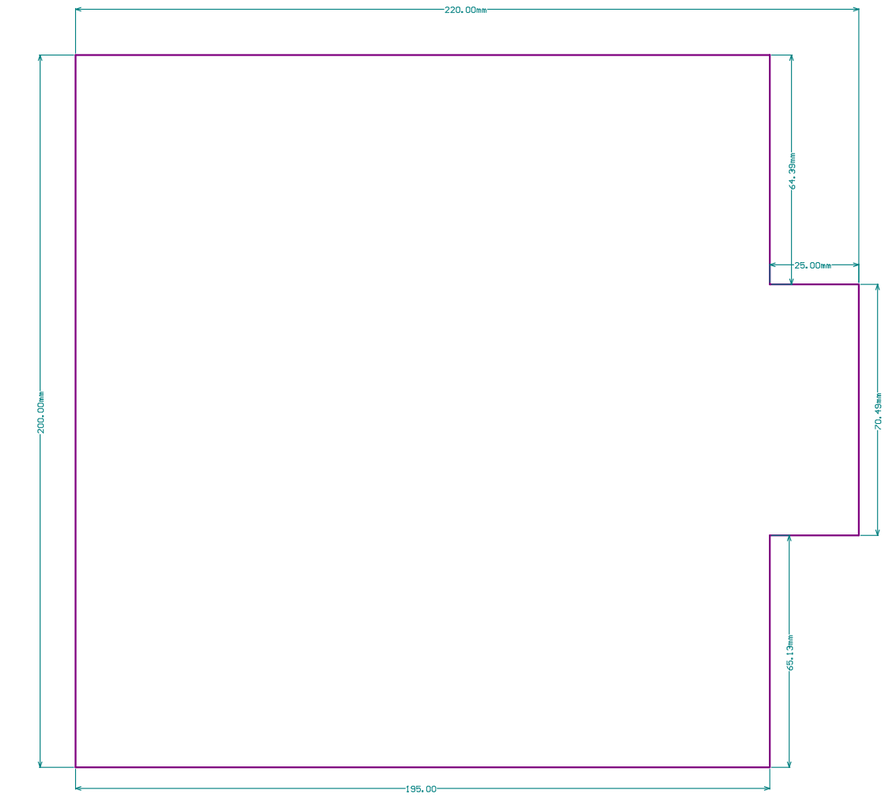
TIDA-010132

DESIGNED FOR: Public Release

FILE NAME: TIDA-010132.PcbDoc

ENGINEER: Sankar Sadasivam	LAYOUT BY: Avinash
SCALE: 0.60	ALTIUM DESIGNER VERSION: 18.1.9.240

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-010132	REV: E:	SVN REV:
LAYER NAME = DRILL DRAWING	TID #:010132		
PLOT NAME = Drill Drawing	GENERATED : 5/23/2019 11:52:54 AM		TEXAS INSTRUMENTS



25.4 (mm)

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-010132	REV: C1	SVN REV:
LAYER NAME =	TID #:010132		
PLOT NAME = Board Dimensions	GENERATED : 5/23/2019 11:53:12 AM		TEXAS INSTRUMENTS

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265