

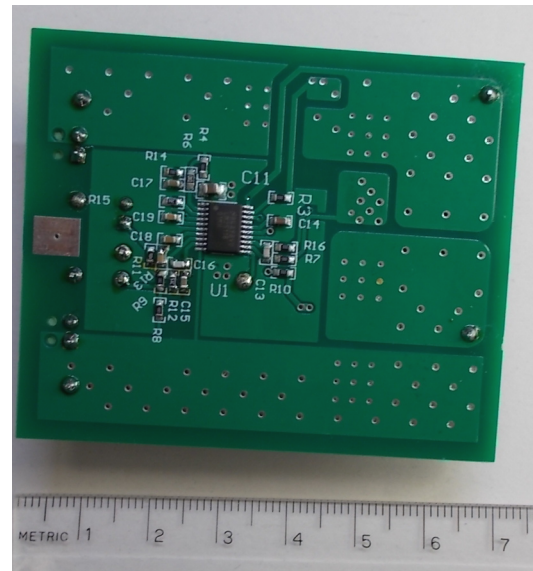
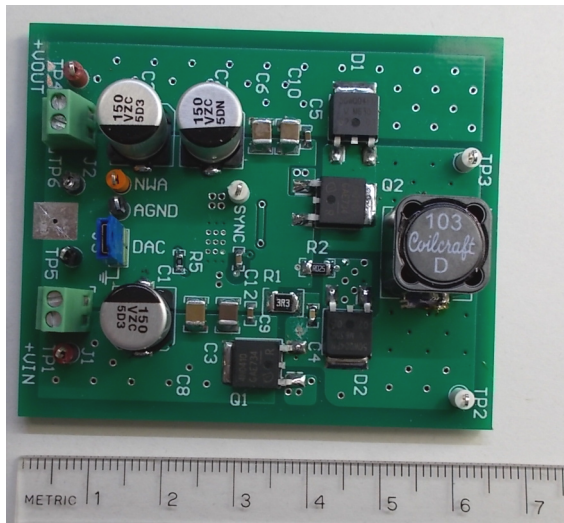
Test Report: PMP30520

20-W, 2-Switch Buck Boost Reference Design With Variable Output Voltage



Description

This design uses the LM25118-Q1. The input voltage is between 9 V and 16 V (withstanding pulse to 32 V). The output voltage is variable from 2 V to 18 V by means of a DAC control input. If the DAC control input is left open the output voltage is about 13.26 V. With shorted DAC control input the output voltage is around 18 V.



An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1. Voltage and Current Requirements

PARAMETER	SPECIFICATIONS
V_{IN}	9 V to 16 V (surge 32 V)
V_{OUT}	2 V to 18 V (default 13.3 V)
Nominal switching frequency	350 kHz

1.2 Considerations

The measured switching frequency is around 347 kHz. Unless otherwise mentioned a resistor was used as load. The circuit switches on around 8.4 V and off around 7.7 V.

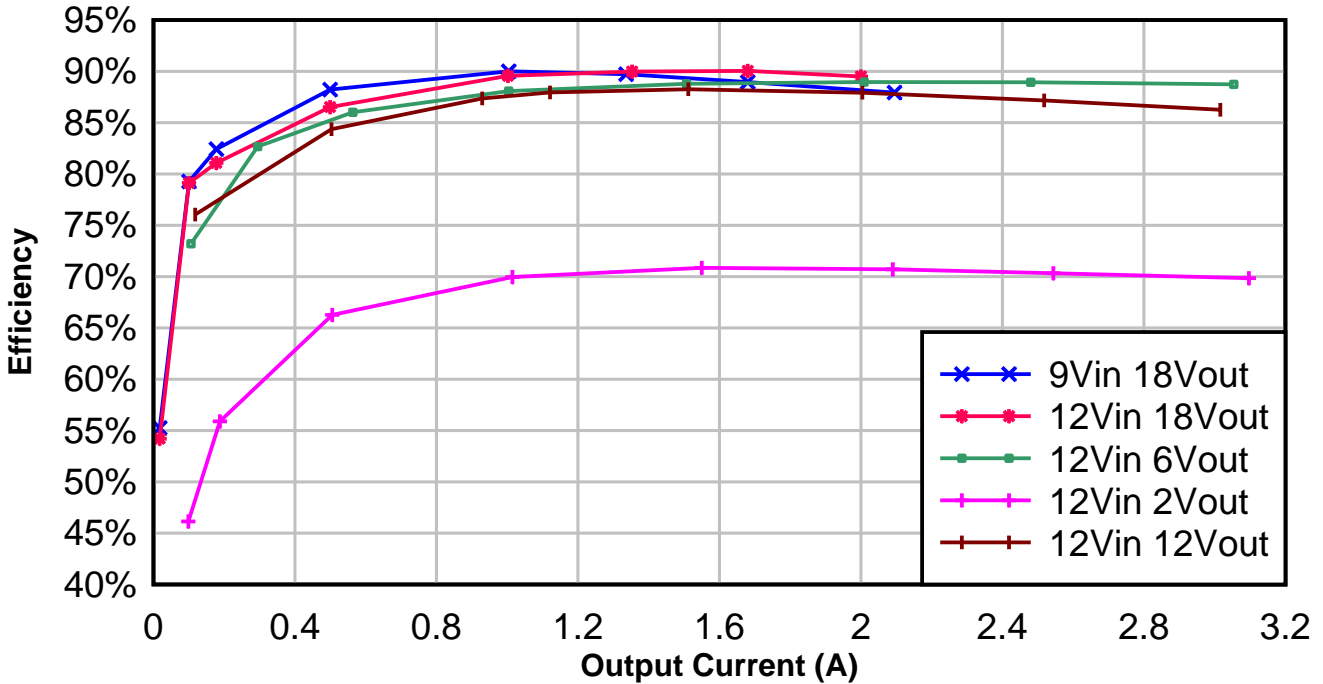
With increasing the DAC control voltage the output voltage is decreasing.

2 Testing and Results

2.1 Efficiency and Regulation Graphs

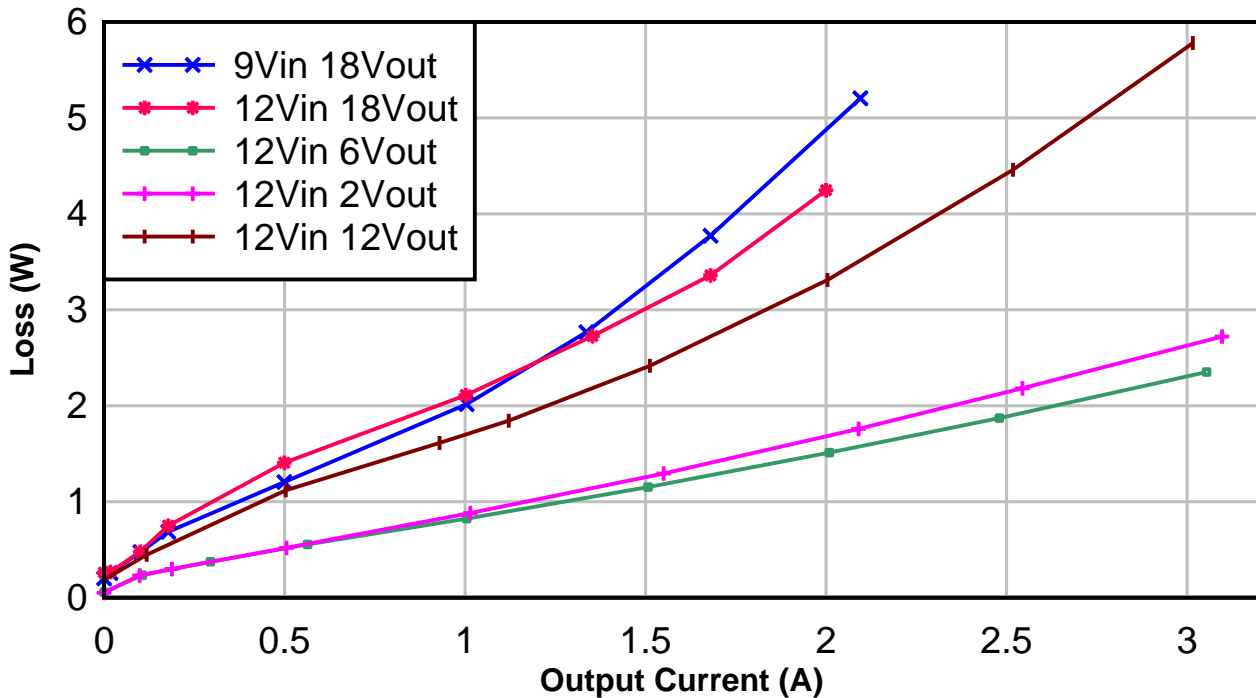
Figure below shows the efficiency graphs with different input/output voltage settings.

Figure 1. Efficiency vs Output Current



D001

Figure 2. Loss vs Output Current

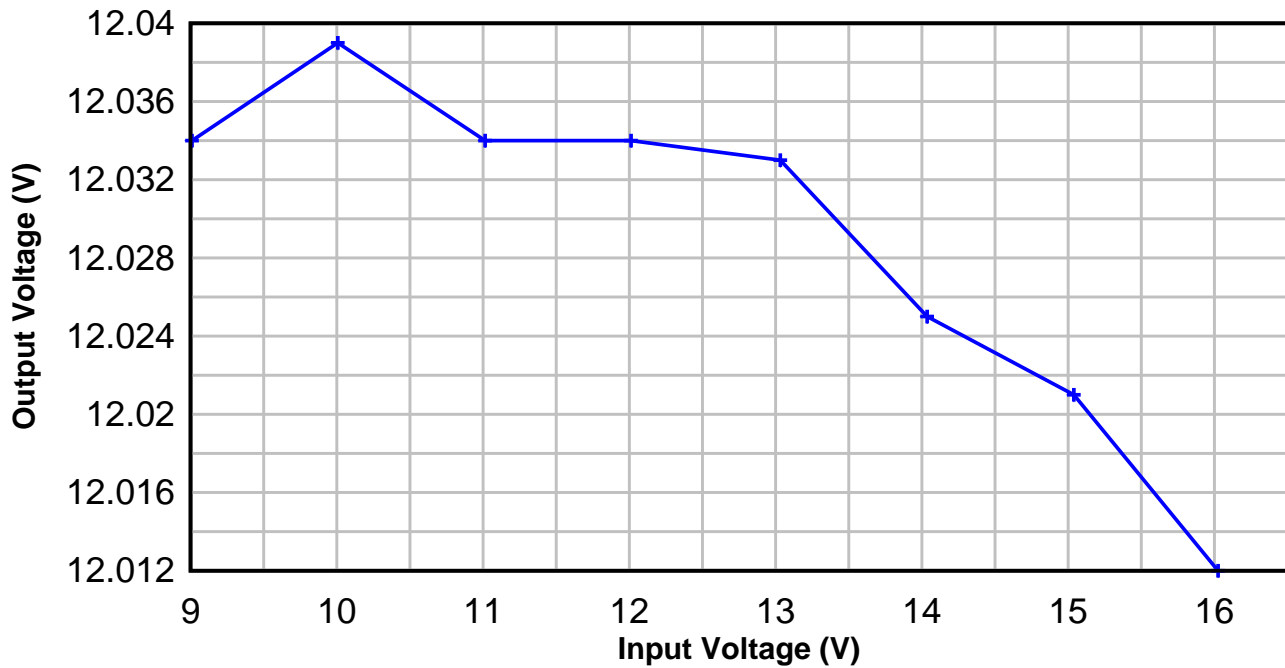


D002

2.2 Line Regulation

The image below shows the line regulation for 3-A output current and 12-V output voltage.

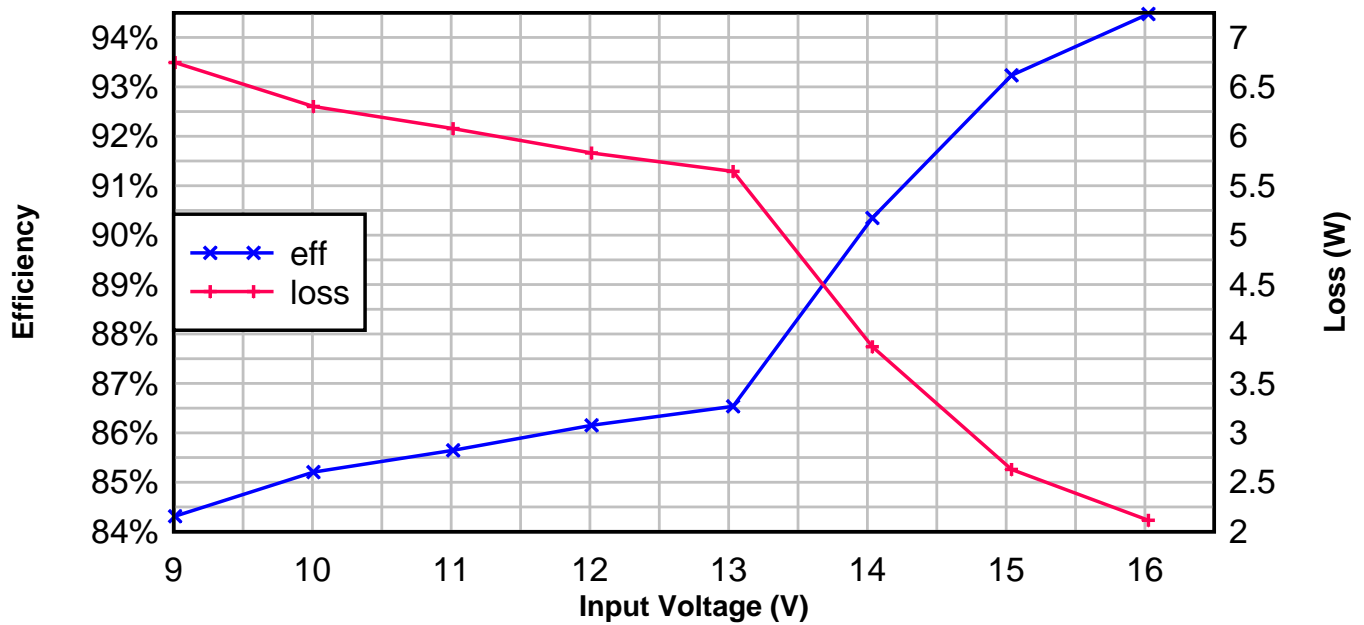
Figure 3. Output Voltage vs Input Voltage



D003

Also the efficiency and losses are calculated. This is shown in the image below.

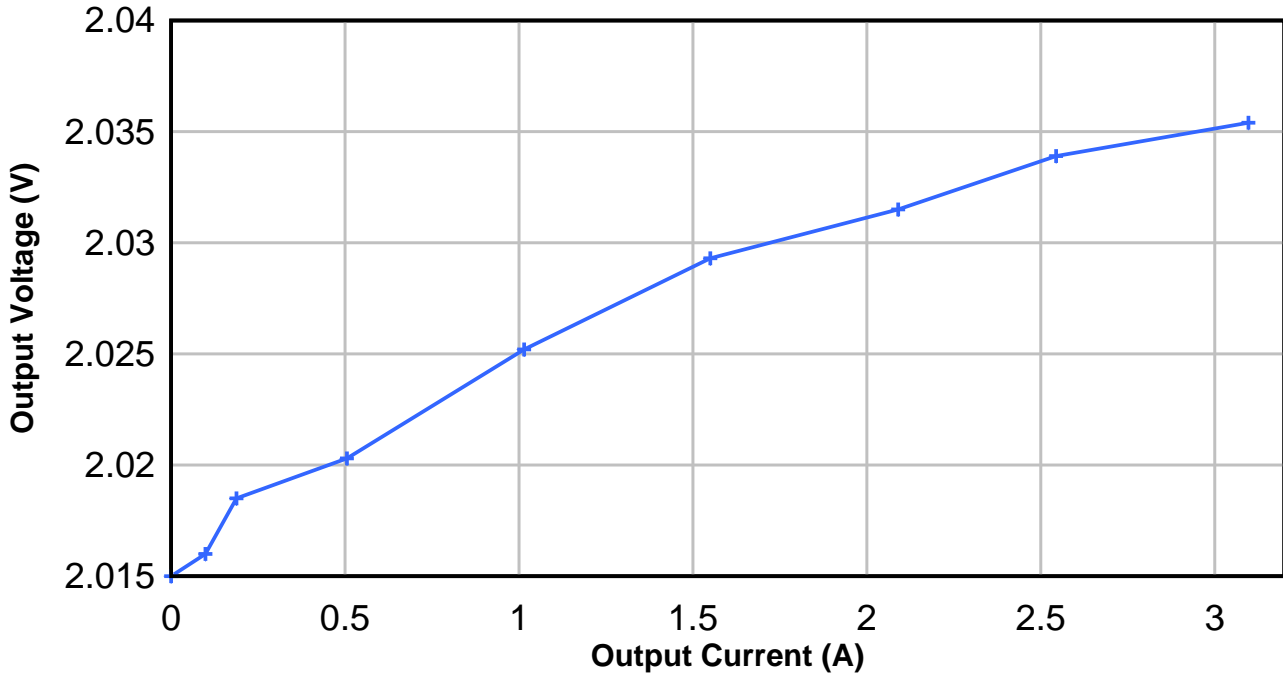
Figure 4. Efficiency and Loss vs Input Voltage



D004

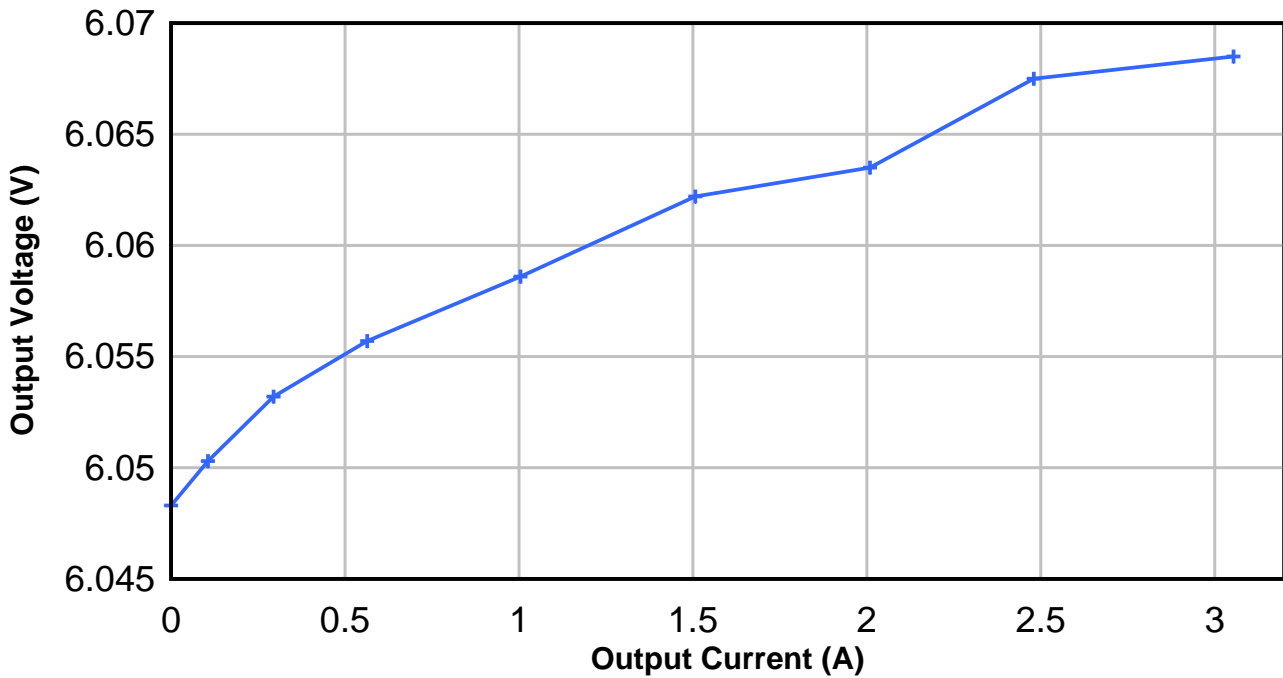
2.3 Load Regulation

Figure 5. Load Regulation for 12 Vin and 2 Vout (DAC:4.05 V)



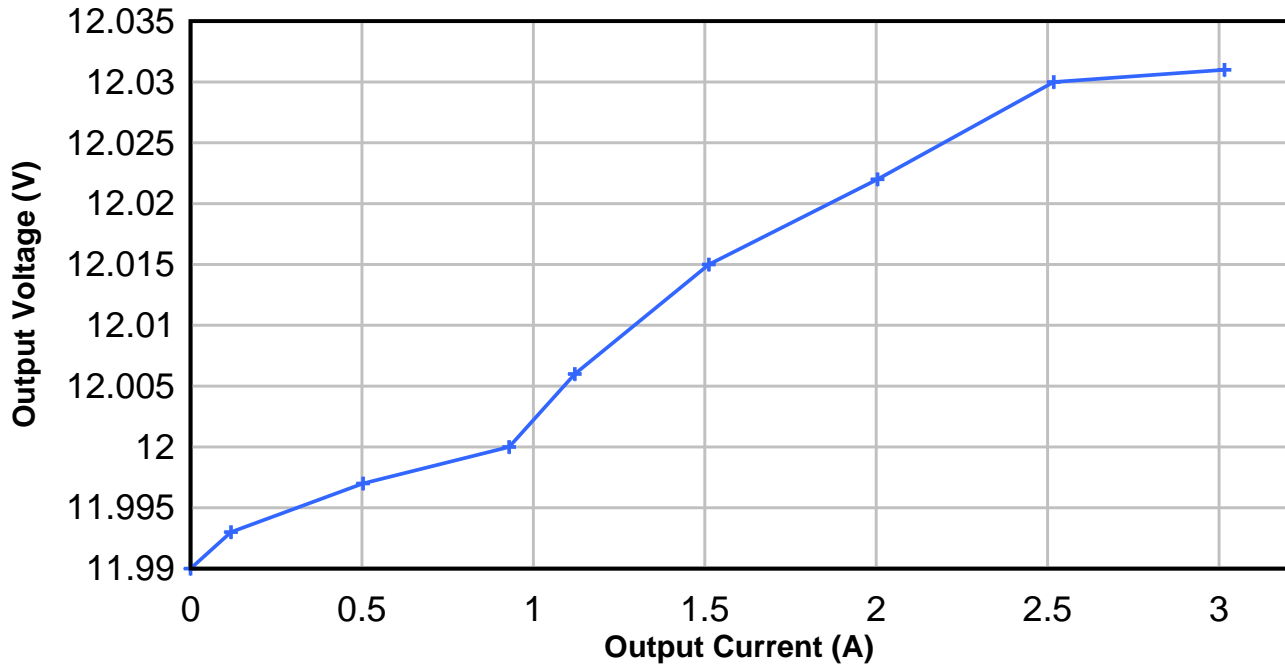
D005

Figure 6. Load Regulation for 12 Vin and 6 Vout (DAC:3.03 V)



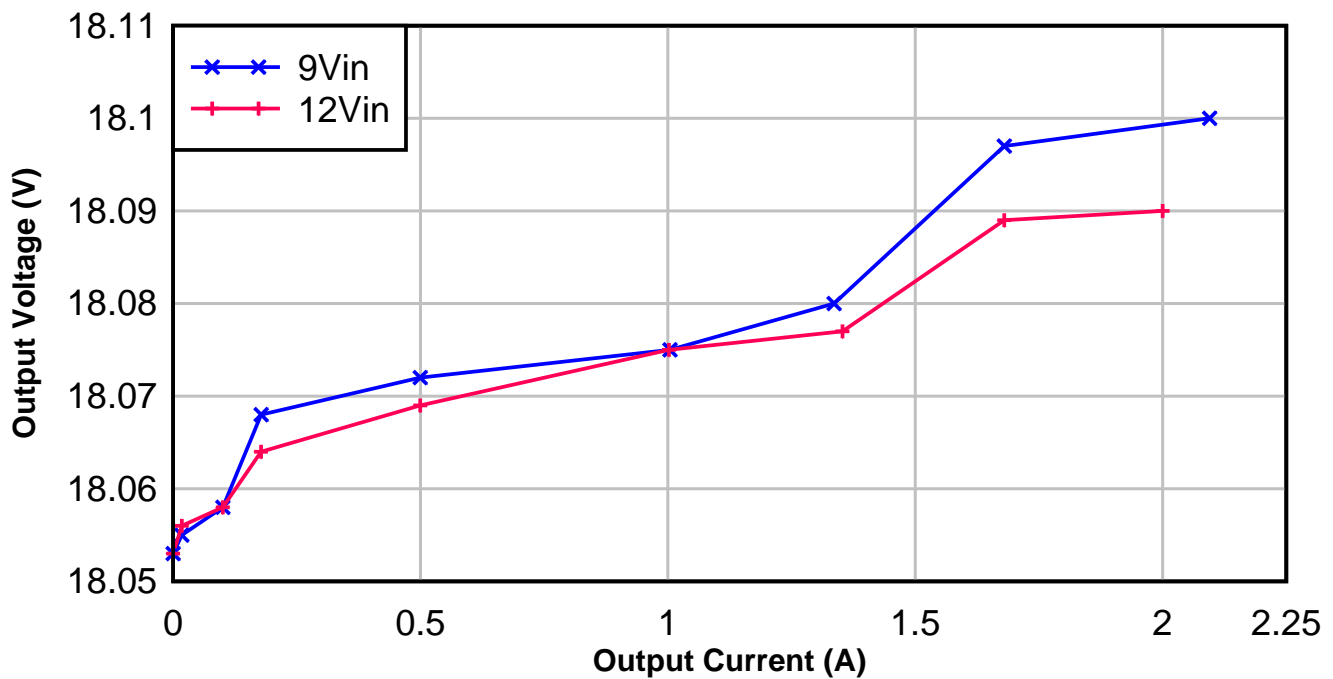
D006

Figure 7. Load Regulation for 12 Vin and 12 Vout (DAC:1.53 V)



D007

Figure 8. Load Regulation for 12 Vin and 9Vin with 18 Vout (DAC:shorted)

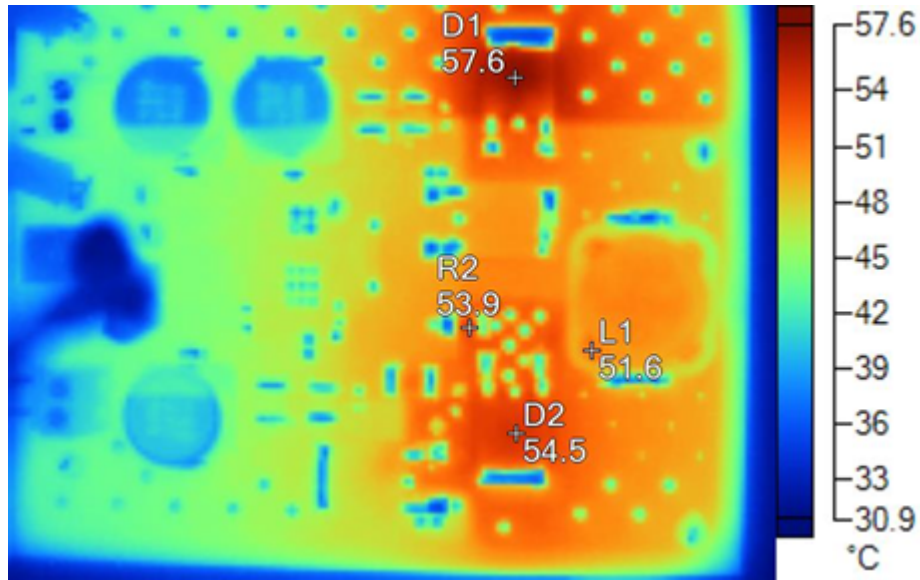


D008

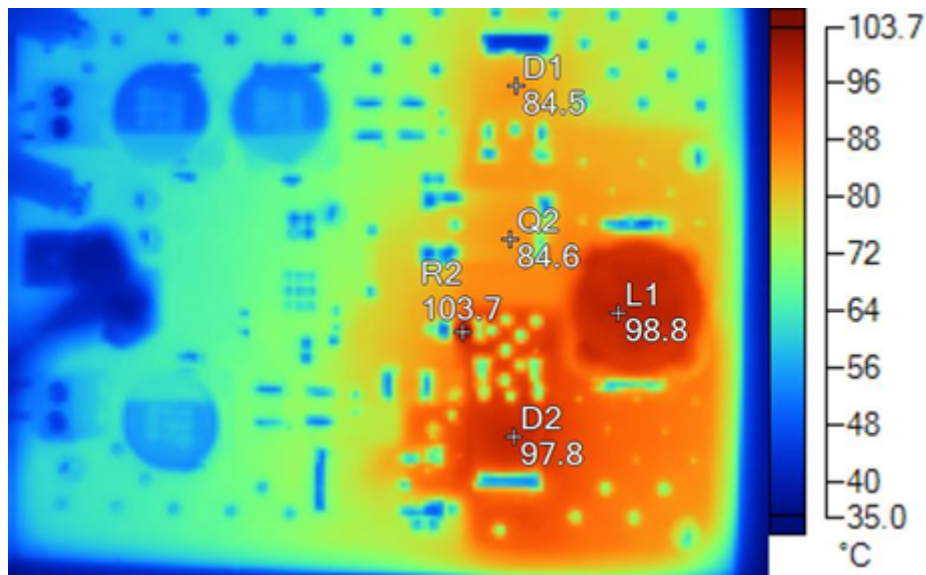
2.4 Thermal Images

2.4.1 Input Voltage 12 V, Output Voltage 6 V and 3-A Output Current

Figure 9. Thermal Image for 12 Vin and 6 Vout at 3 A



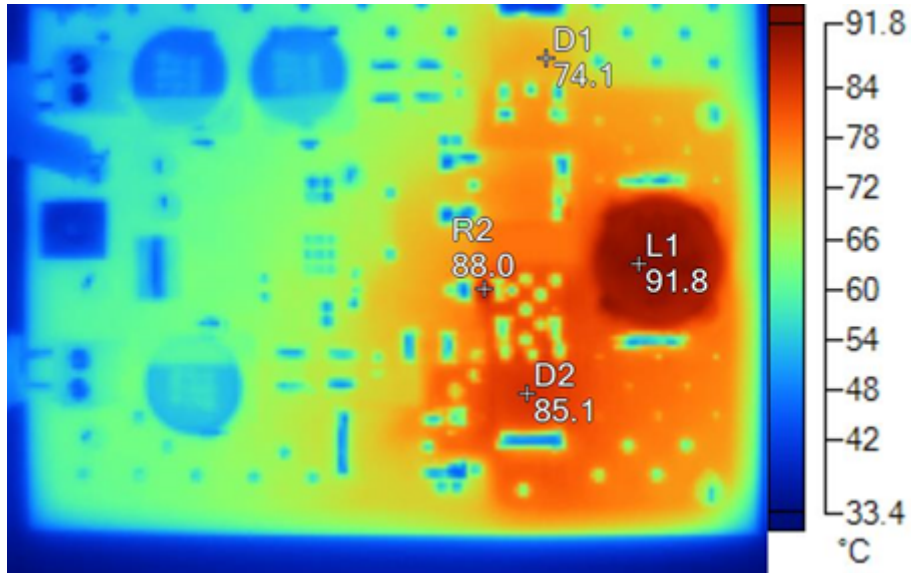
NAME	TEMPERATURE
D1	57.6°C
D2	54.5°C
L1	51.6°C
R2	53.9°C

2.4.2 Input Voltage 12 V, Output Voltage 12 V and 3-A Output Current
Figure 10. Thermal Image for 12 Vin and 12 Vout at 3 A


NAME	TEMPERATURE
D1	84.5°C
D2	97.8°C
L1	98.8°C
Q2	84.6°C
R2	103.7°C

2.4.3 Input Voltage 9 V, Output Voltage 18 V and 2-A Output Current

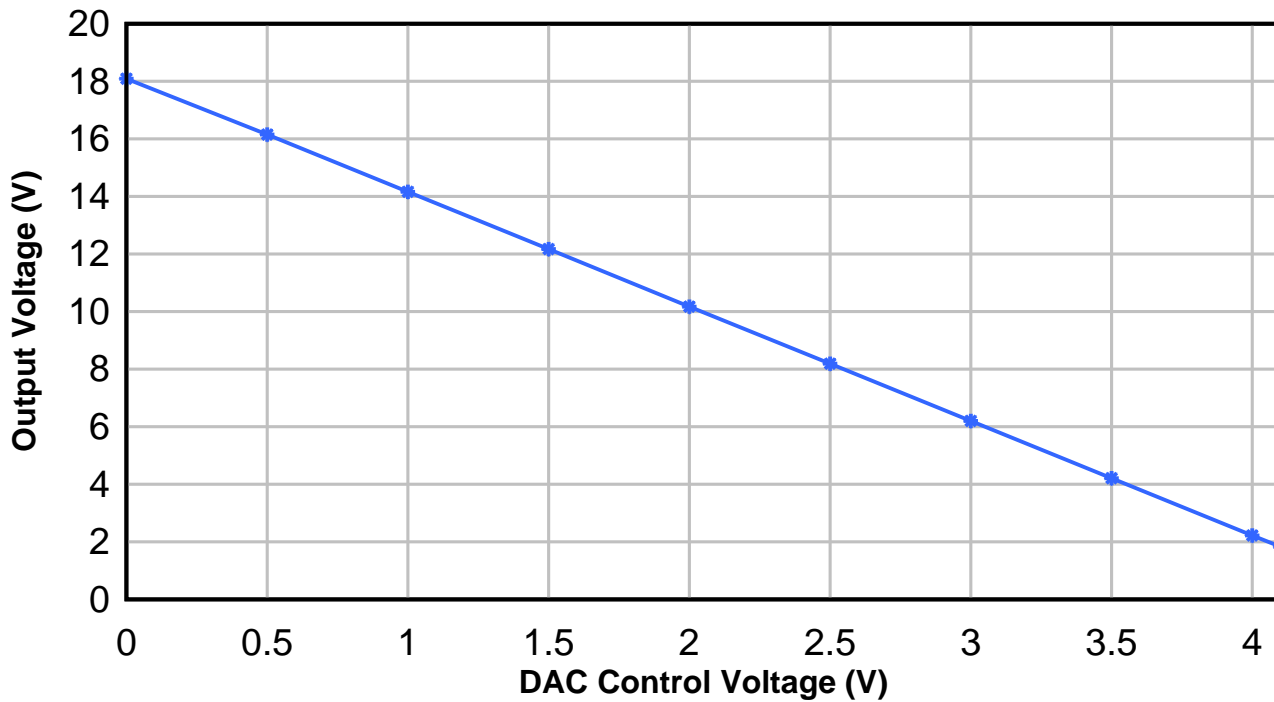
Figure 11. Thermal Image for 9 Vin and 18 Vout at 2 A



NAME	TEMPERATURE
D1	74.1°C
D2	85.1°C
L1	91.8°C
R2	88.0°C

3 DAC Control Input

Figure 12. Output Voltage vs DAC Control Voltage



D012

Table below show the values from the graph above.

VDAC	VOUT
0 V	18.09 V
0.5 V	16.15 V
1 V	14.16 V
1.5 V	12.17 V
2 V	10.17 V
2.5 V	8.19 V
3 V	6.2 V
3.5 V	4.21 V
4 V	2.22 V
4.1 V	1.83 V

4 Waveforms

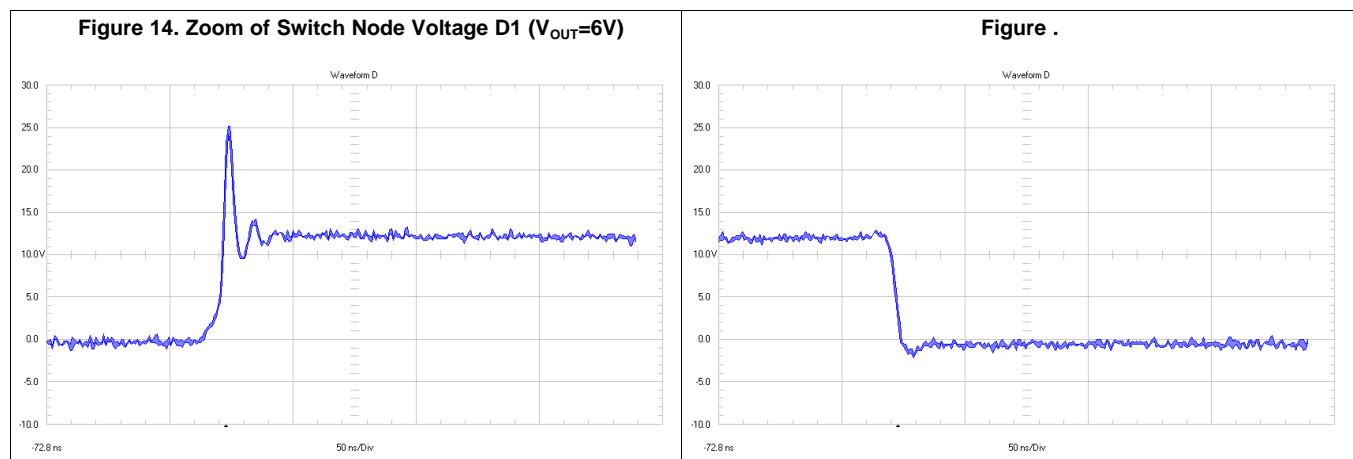
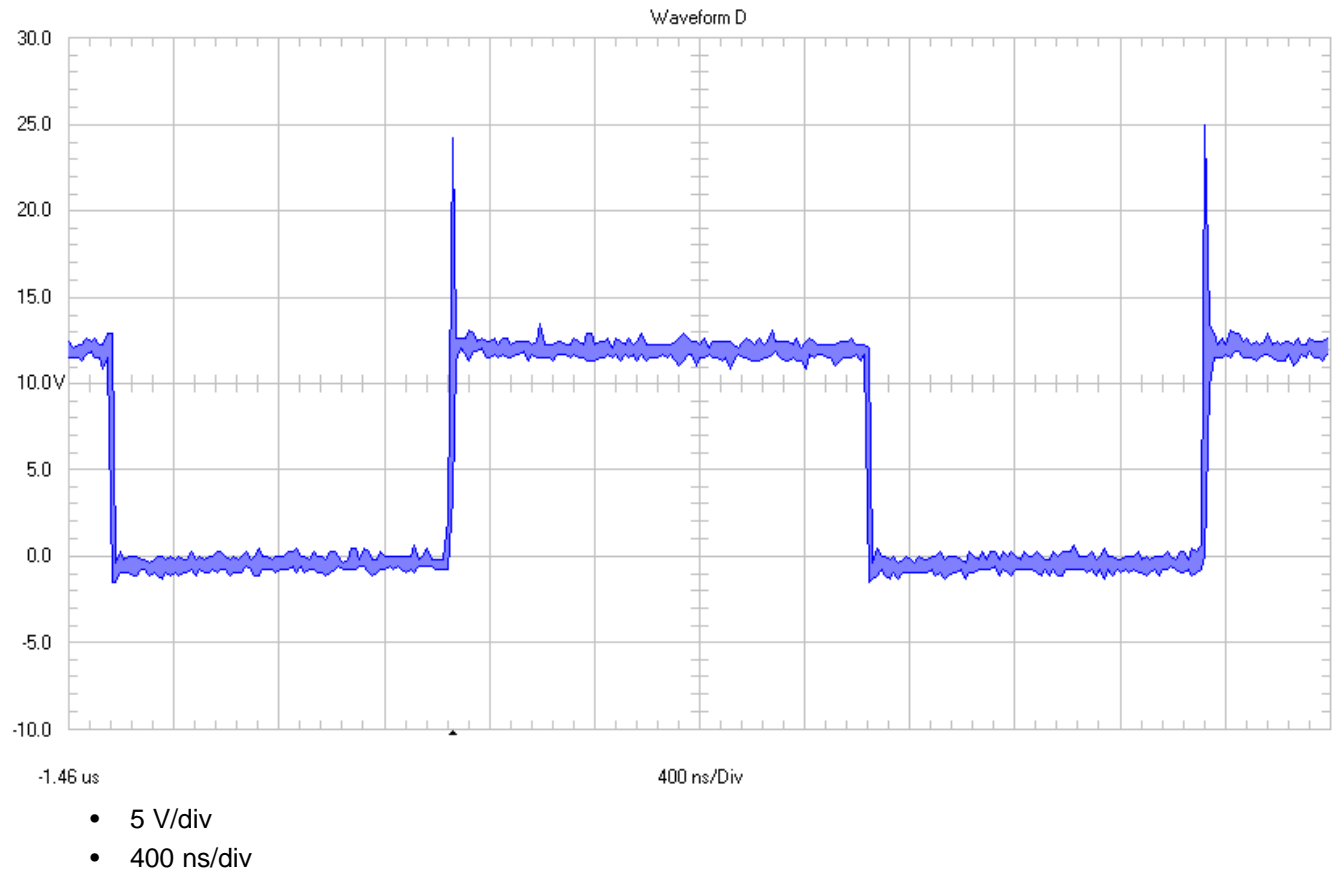
4.1 Switching

Unless otherwise mentioned: All switching waveforms are measured with full bandwidth setting.

4.1.1 12-V Input Voltage, 6-V Output Voltage at 3 A

4.1.1.1 Diode D2

Figure 13. Switch Node Voltage D2 ($V_{OUT}=6V$)

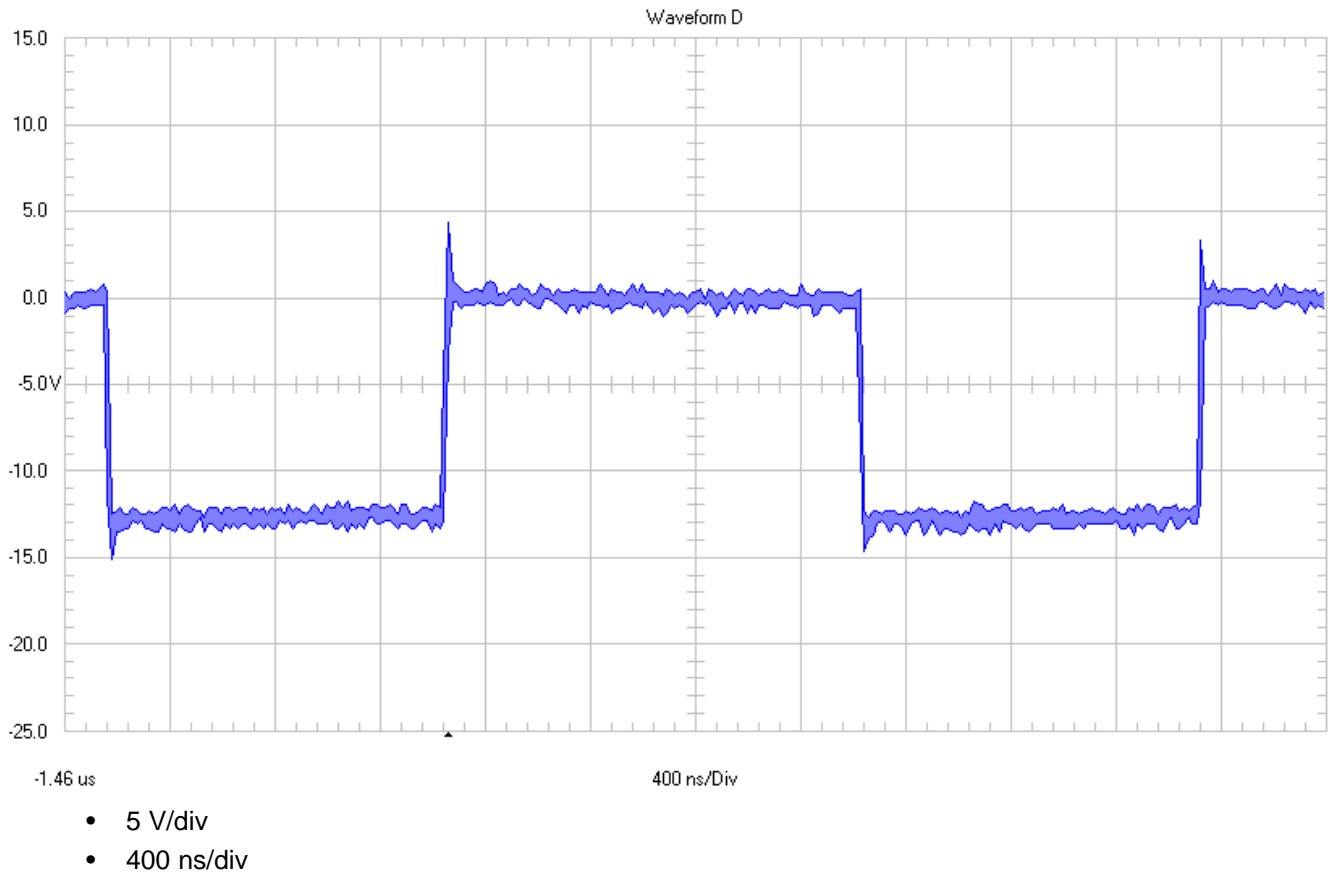


- 50 ns/ major div

4.1.1.2 Transistor Q1 referenced to VIN

4.1.1.2.1 Drain to Source

Figure 15. Switch Node Voltage Q1 Drain to Source ($V_{OUT}=6V$)



- 5 V/div
- 400 ns/div

Figure 16. Zoom of Switch Node Voltage Q1 ($V_{OUT}=6V$)

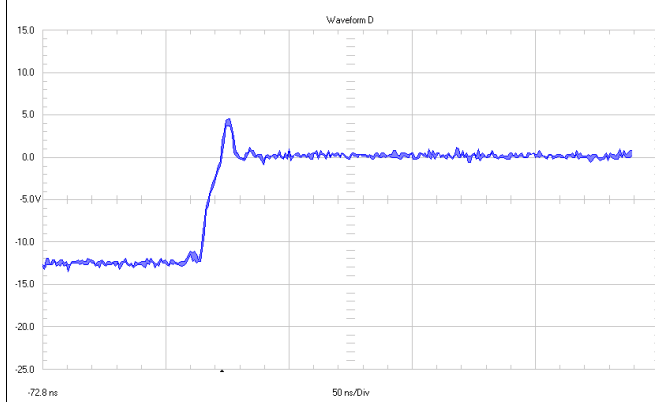
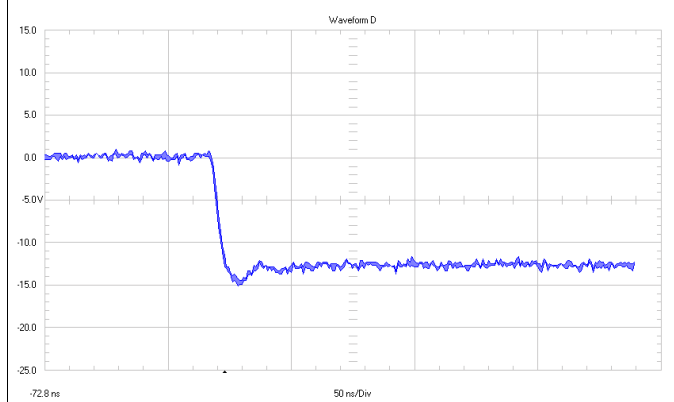


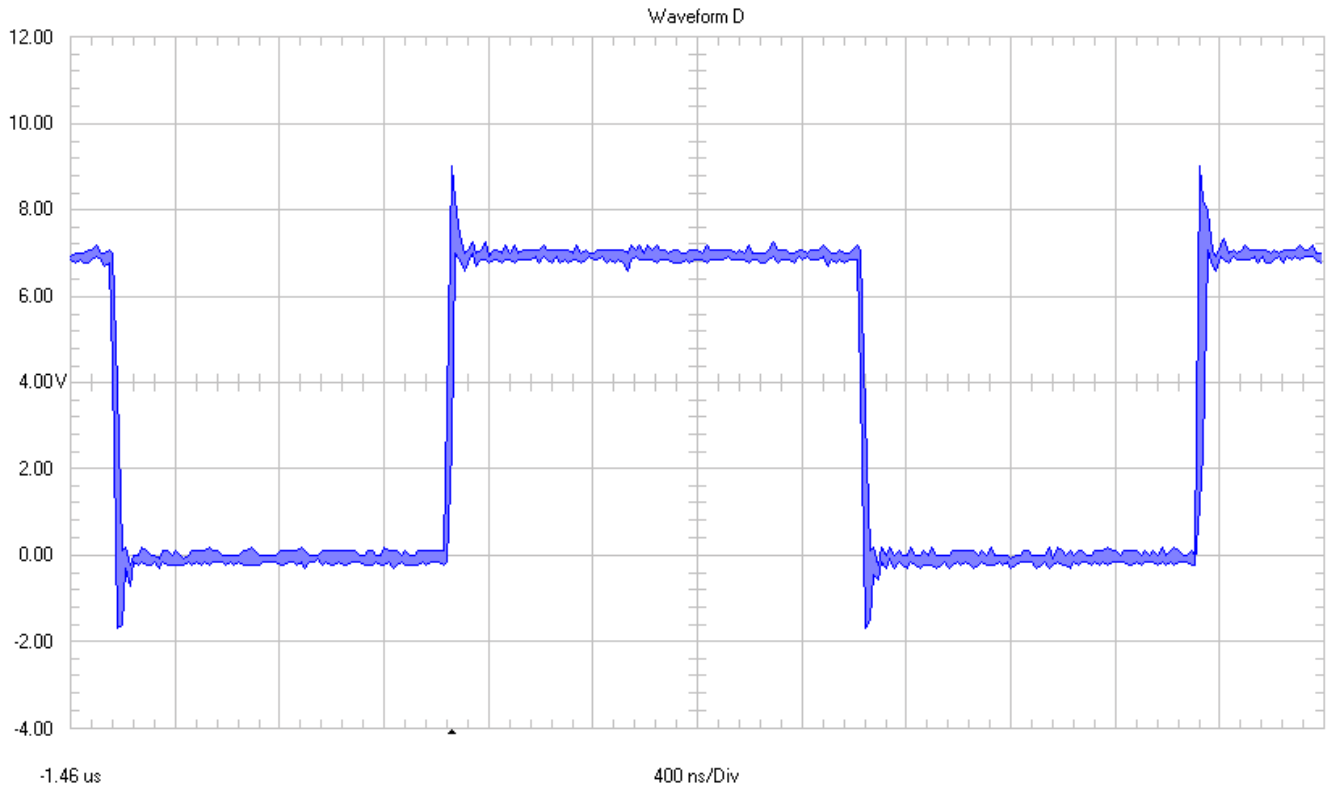
Figure .



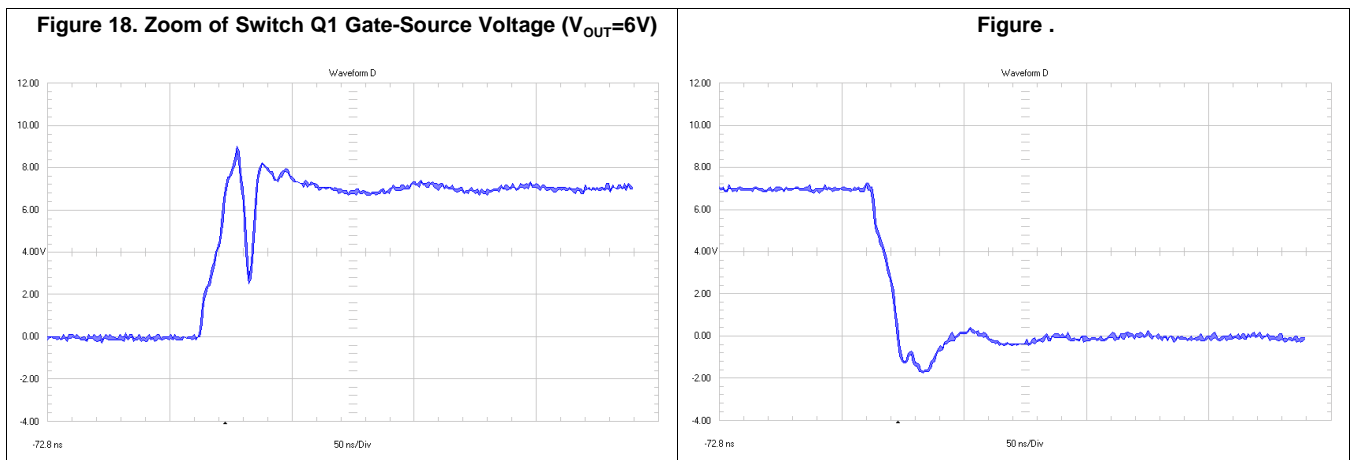
- 50 ns/div

4.1.1.2.2 Gate to Source

Figure 17. Gate to Source Voltage Q1 ($V_{OUT}=6V$)



- 2 V/div
- 400 ns/div

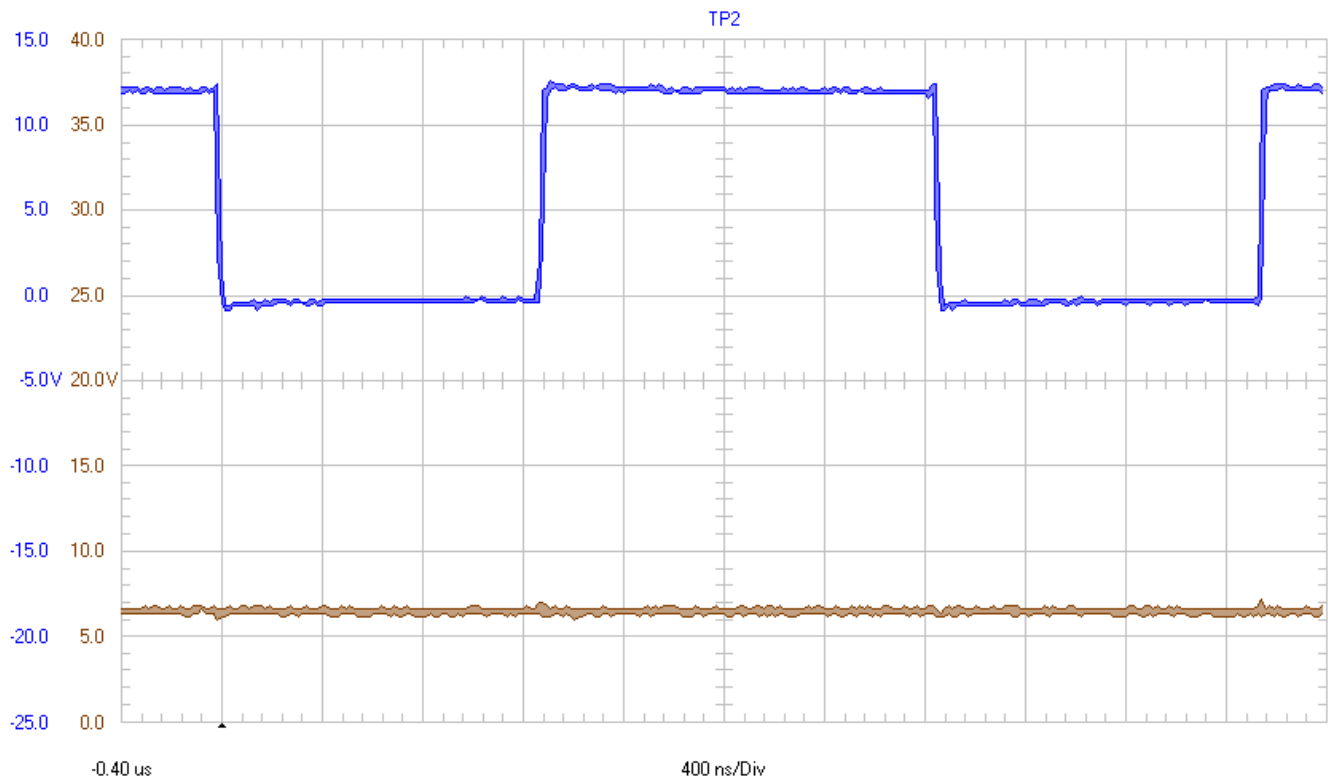


- 50 ns/div

4.1.1.3 Waveforms at TP2 and TP3

The waveforms below are measured with 20-MHz bandwidth filter.

Figure 19. Pure Buck Operation

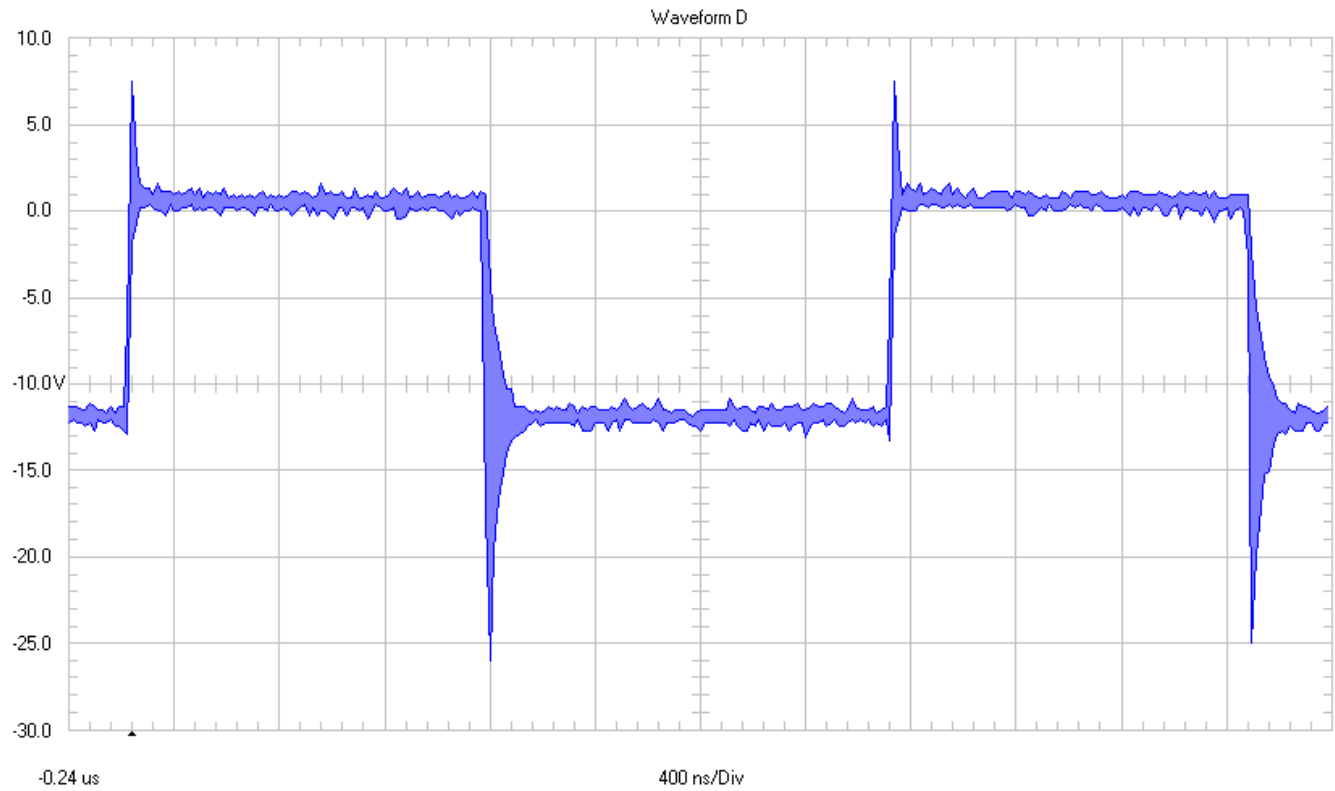


- channel 1 (blue): TP2 to GND => 5 V/div
- channel 2 (brown): TP3 to GND => 5 V/div
- 400 ns/div

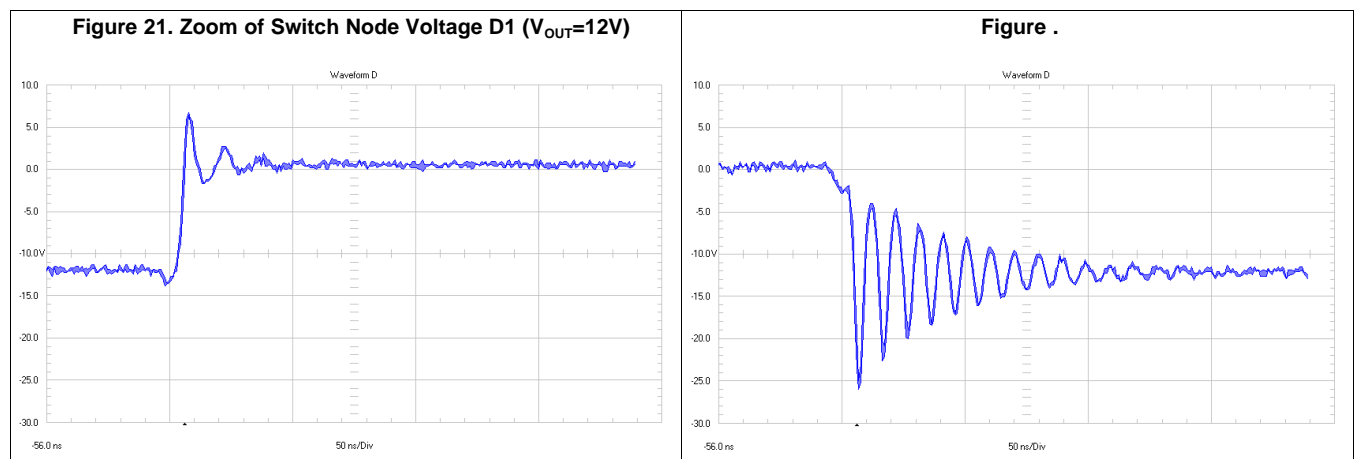
4.1.2 12-V Input Voltage, 12-V Output Voltage at 3 A

4.1.2.1 Diode D1 (Referenced to VOUT)

Figure 20. Switch Node Voltage D1 ($V_{OUT}=12V$)



- 5 V/div
- 400 ns/div

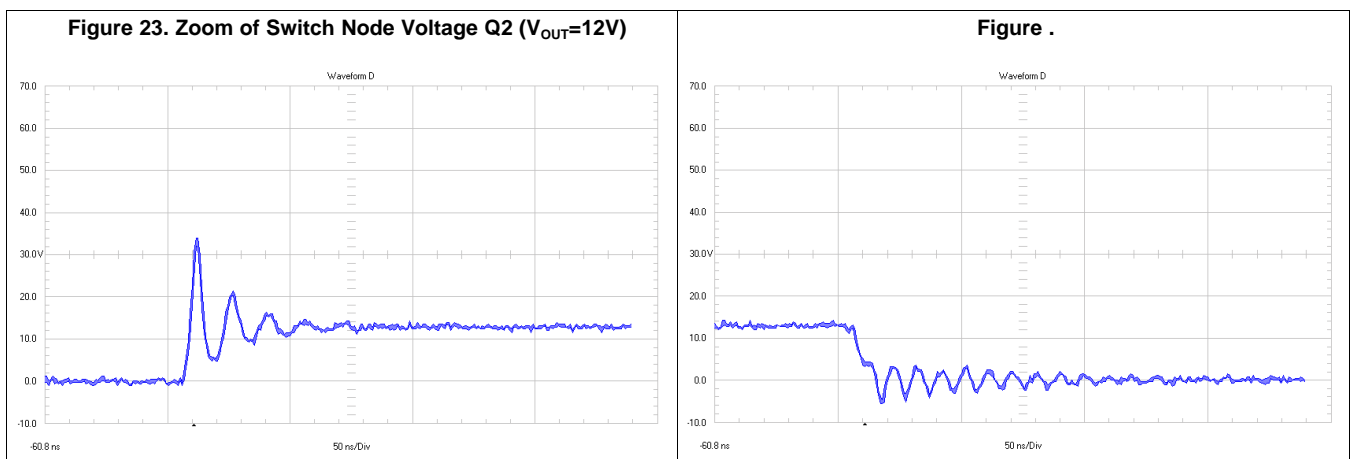
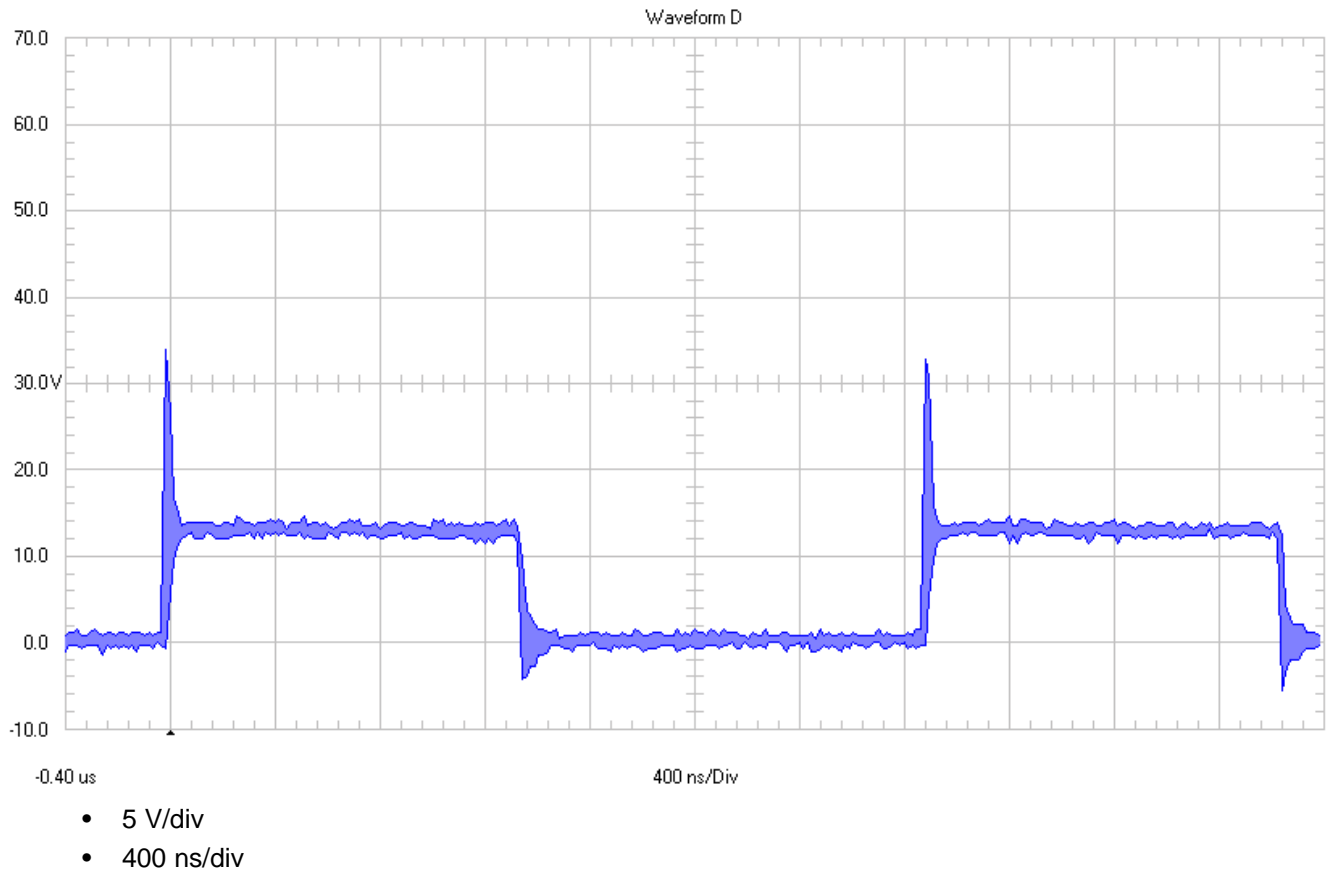


- 50 ns/div

4.1.2.2 Transistor Q2

4.1.2.2.1 Drain to Source (GND)

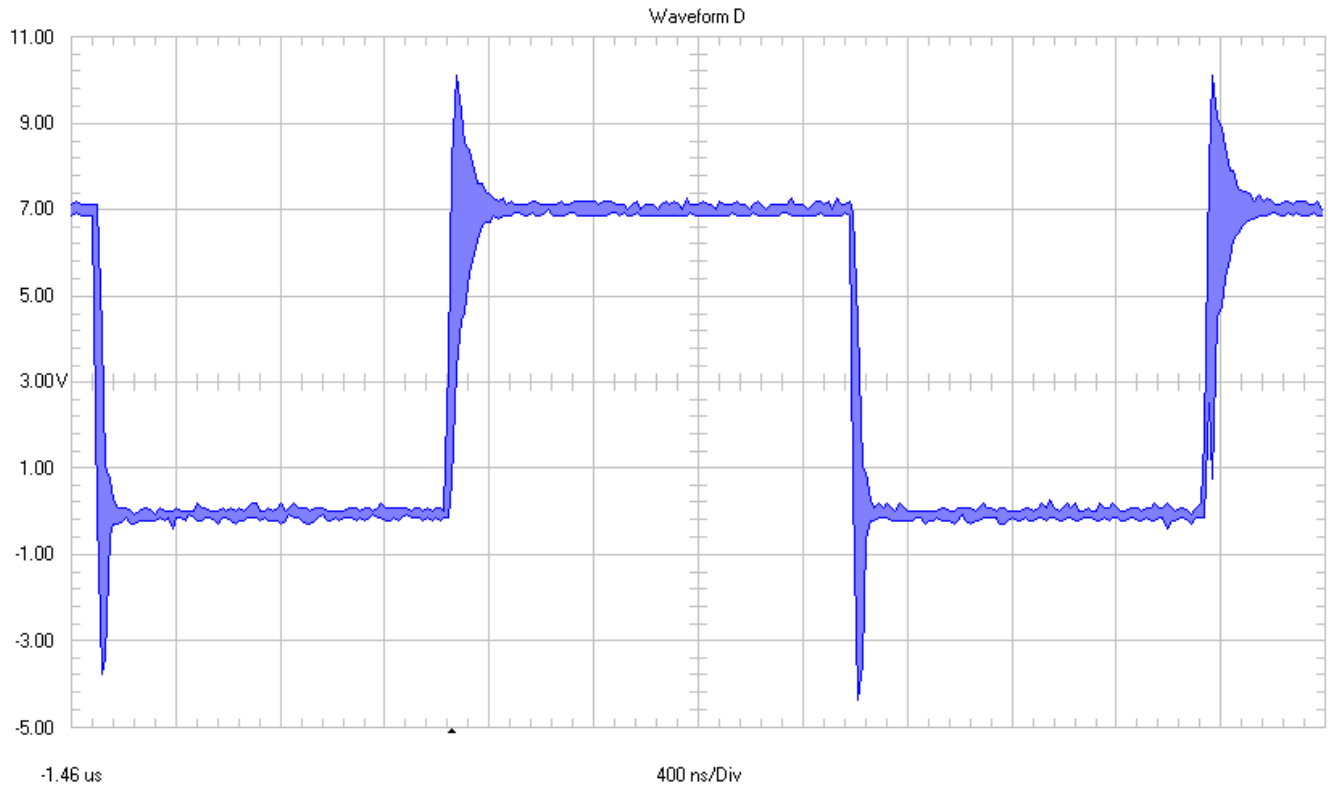
Figure 22. Switch Node Voltage Q2 Drain-Source ($V_{OUT}=12V$)



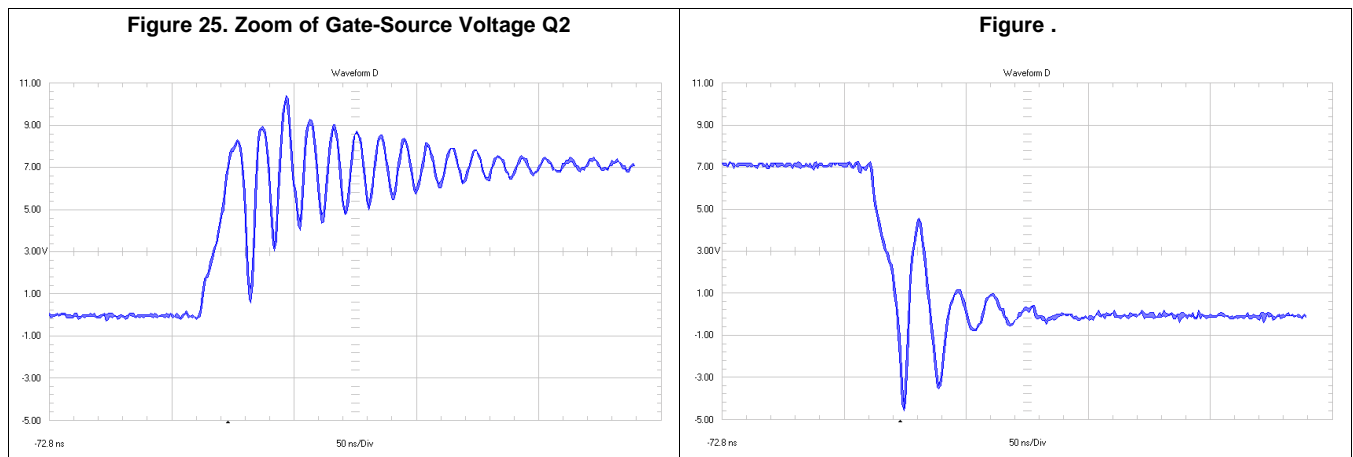
- 50 ns/div

4.1.2.2.2 Gate to Source (GND)

Figure 24. Gate to Source Voltage Q2 ($V_{OUT}=12V$)



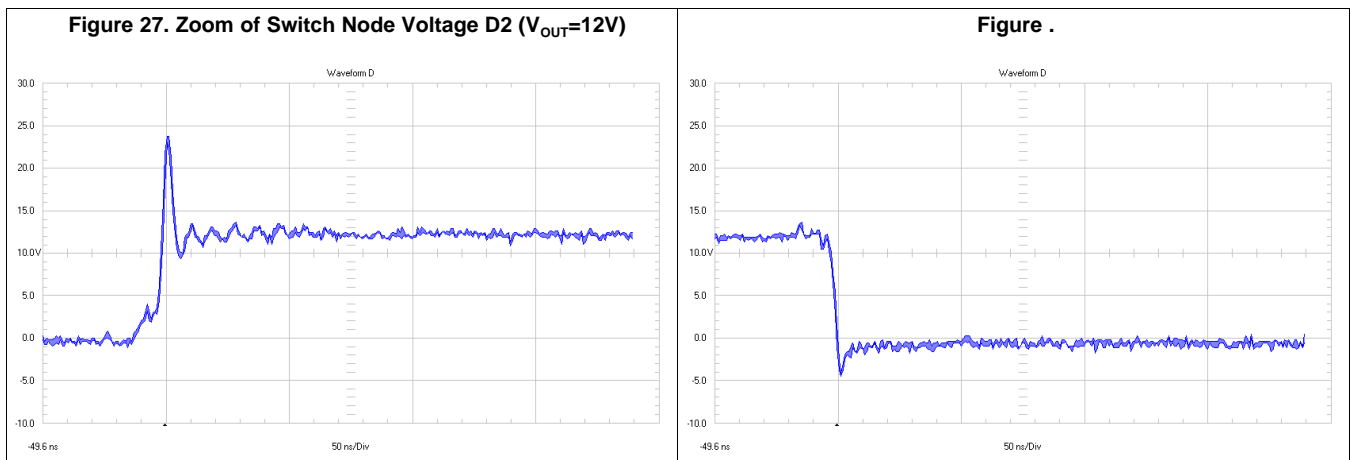
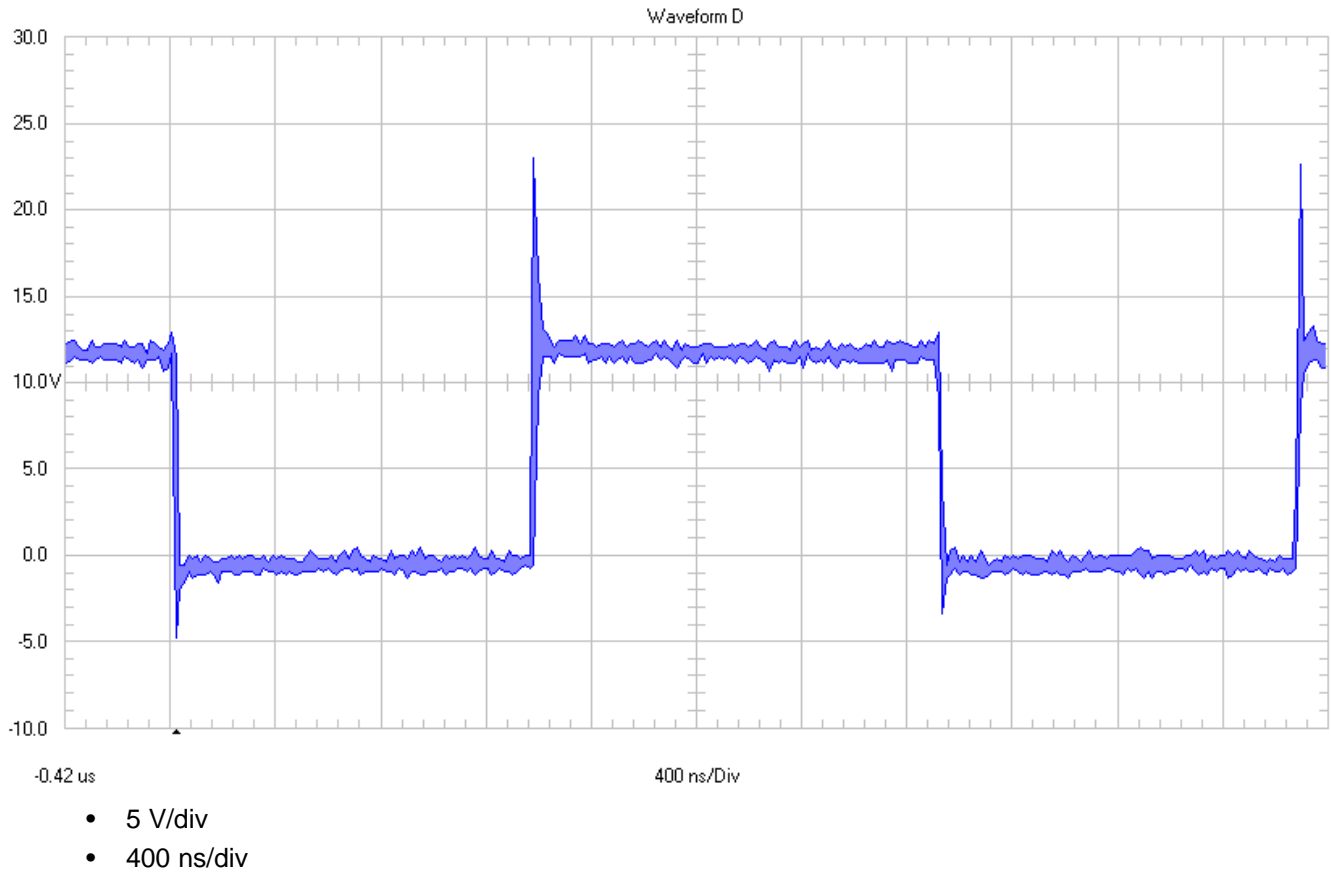
- 2 V/div
- 400 ns/div



- 50 ns/div

4.1.2.3 Diode D2

Figure 26. Switch Node Voltage D2 ($V_{OUT}=12V$)



50 ns/major div

4.1.2.4 Transistor Q1

4.1.2.4.1 Drain to Source (Referenced to VIN)

Figure 28. Switch Node Voltage Q1 ($V_{OUT}=12V$)

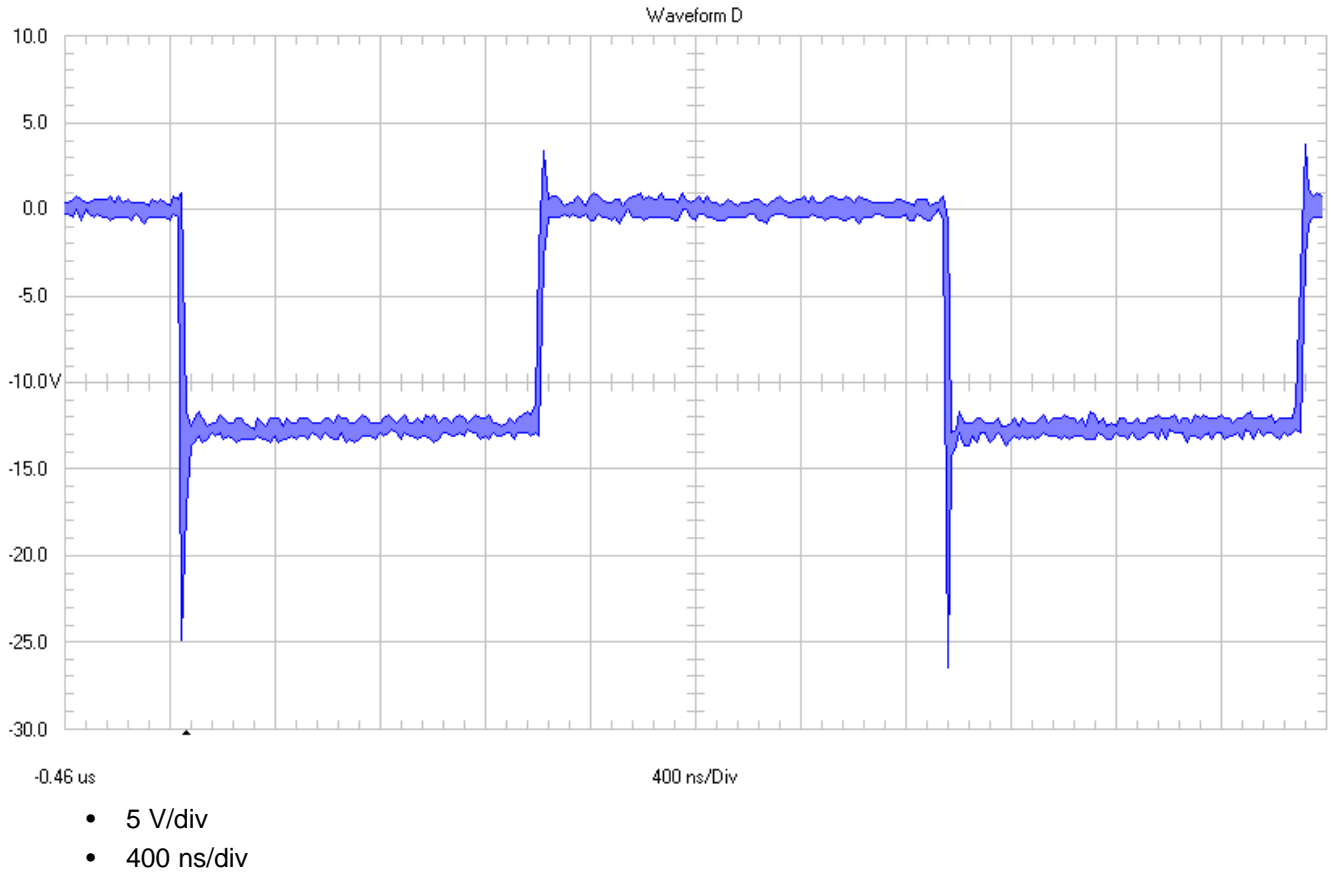


Figure 29. Zoom of Switch Node Voltage Q1 ($V_{OUT}=12V$)

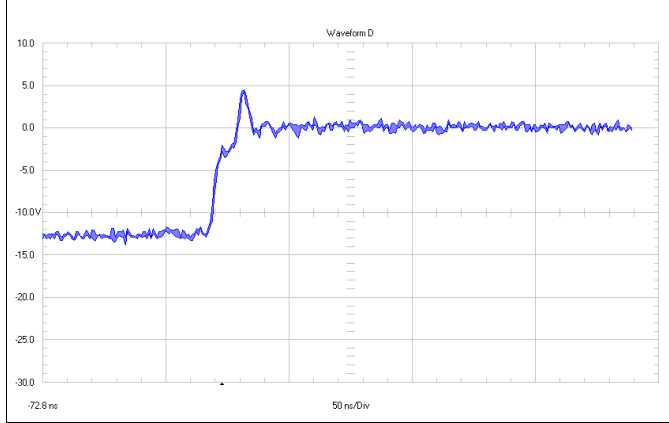
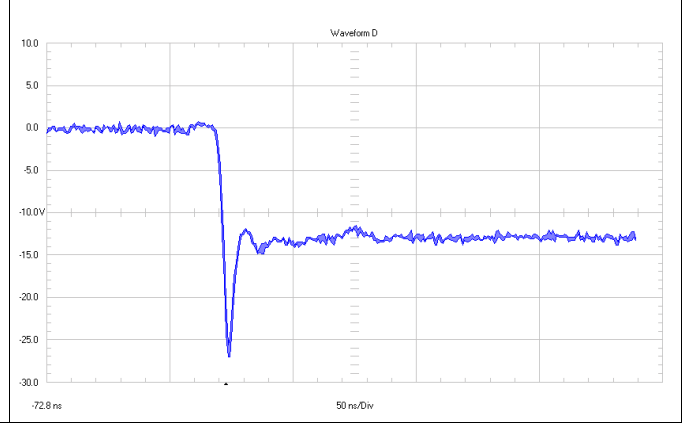


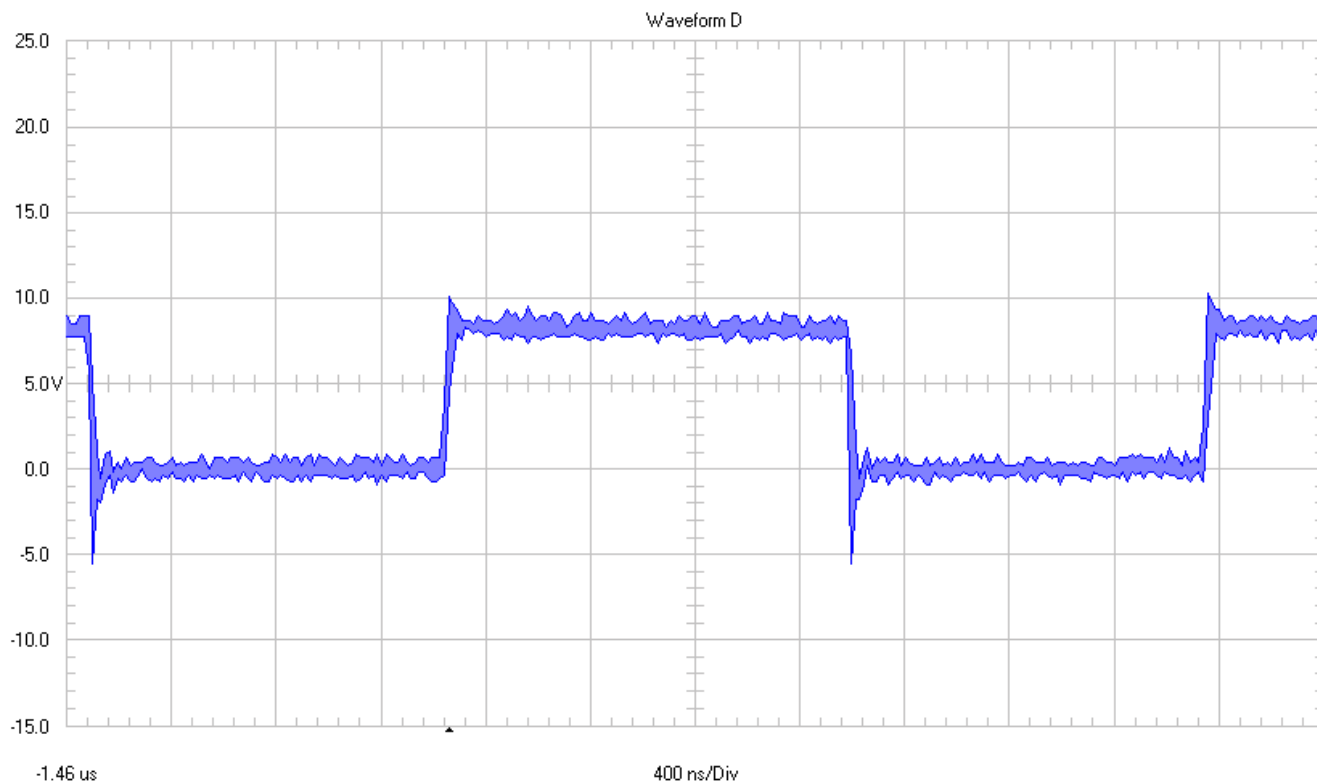
Figure .



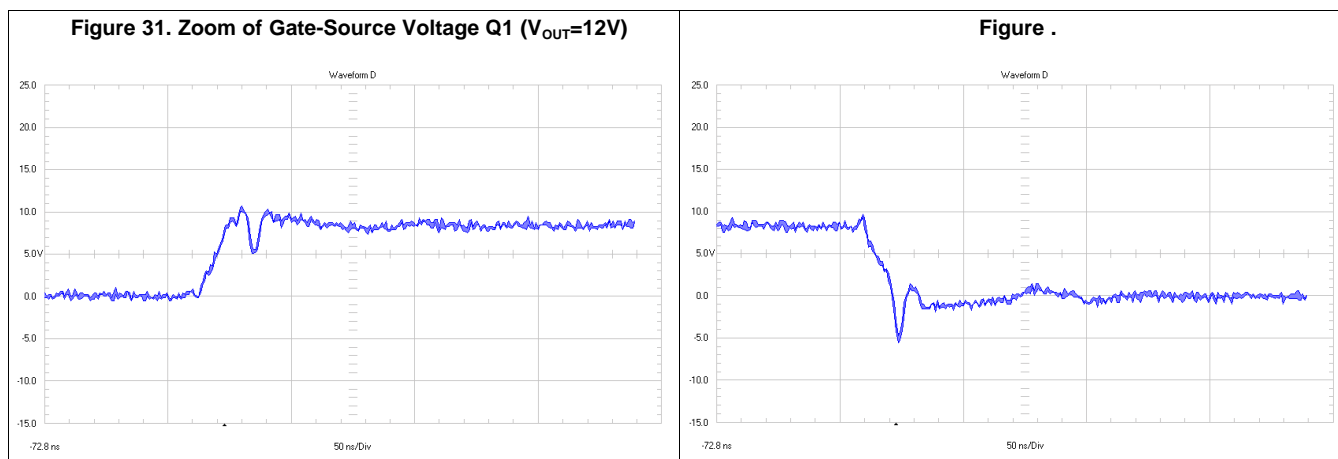
- 50 ns/major div

4.1.2.4.2 Gate to Source

Figure 30. Gate-Source Voltage Q1 ($V_{OUT}=12V$)



- 5 V/div
- 400 ns

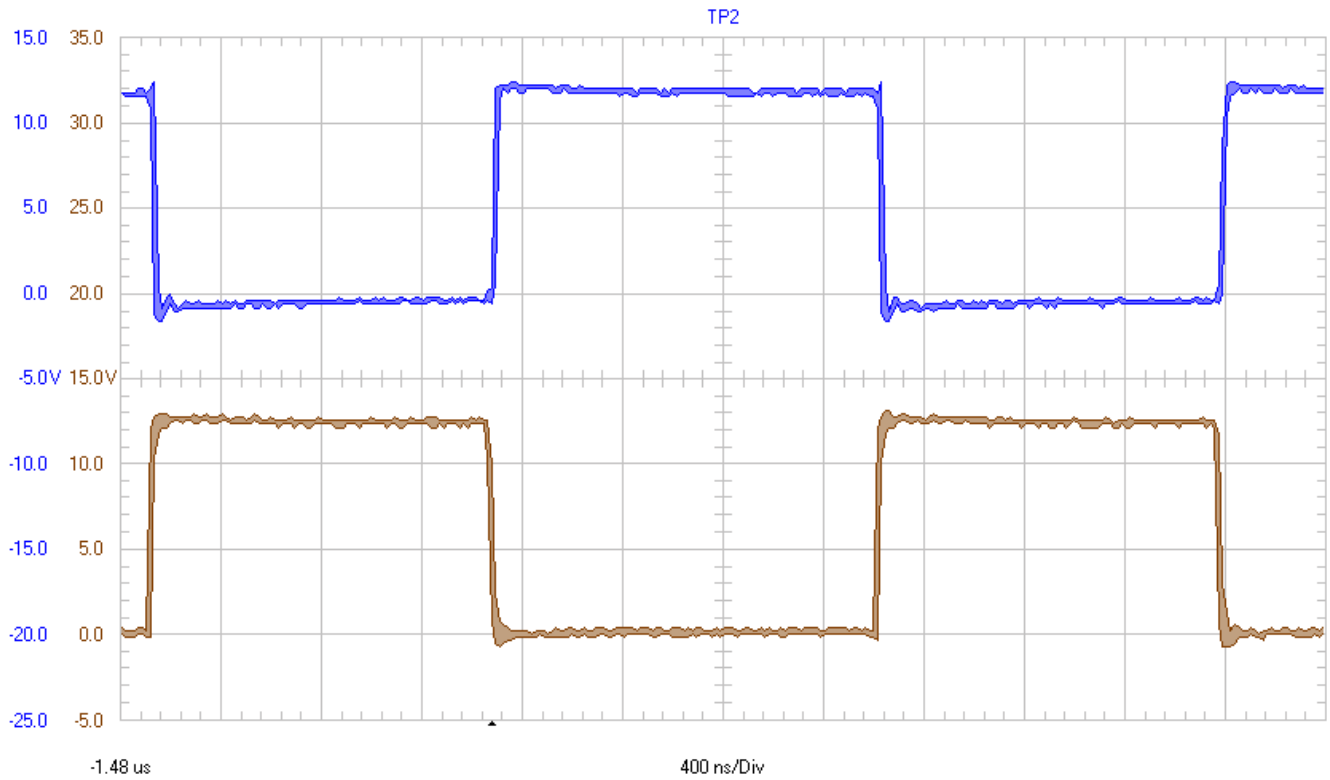


- 50 ns/major div

4.1.2.5 Waveforms at TP2 and TP3

The waveforms below are measured with 20-MHz bandwidth filter.

Figure 32. Buck-Boost Operation ($V_{OUT}=12V$)

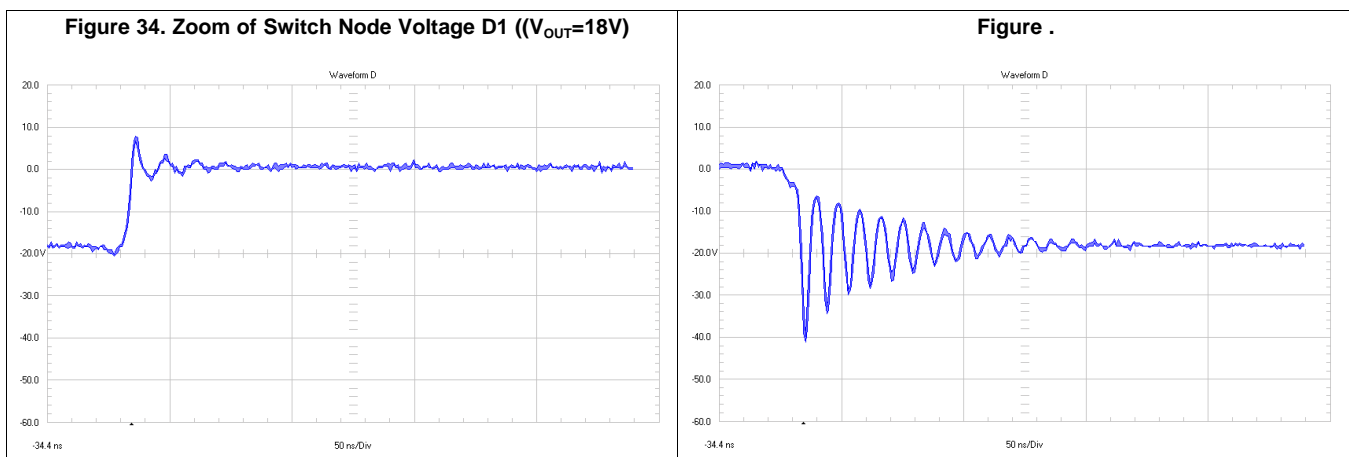
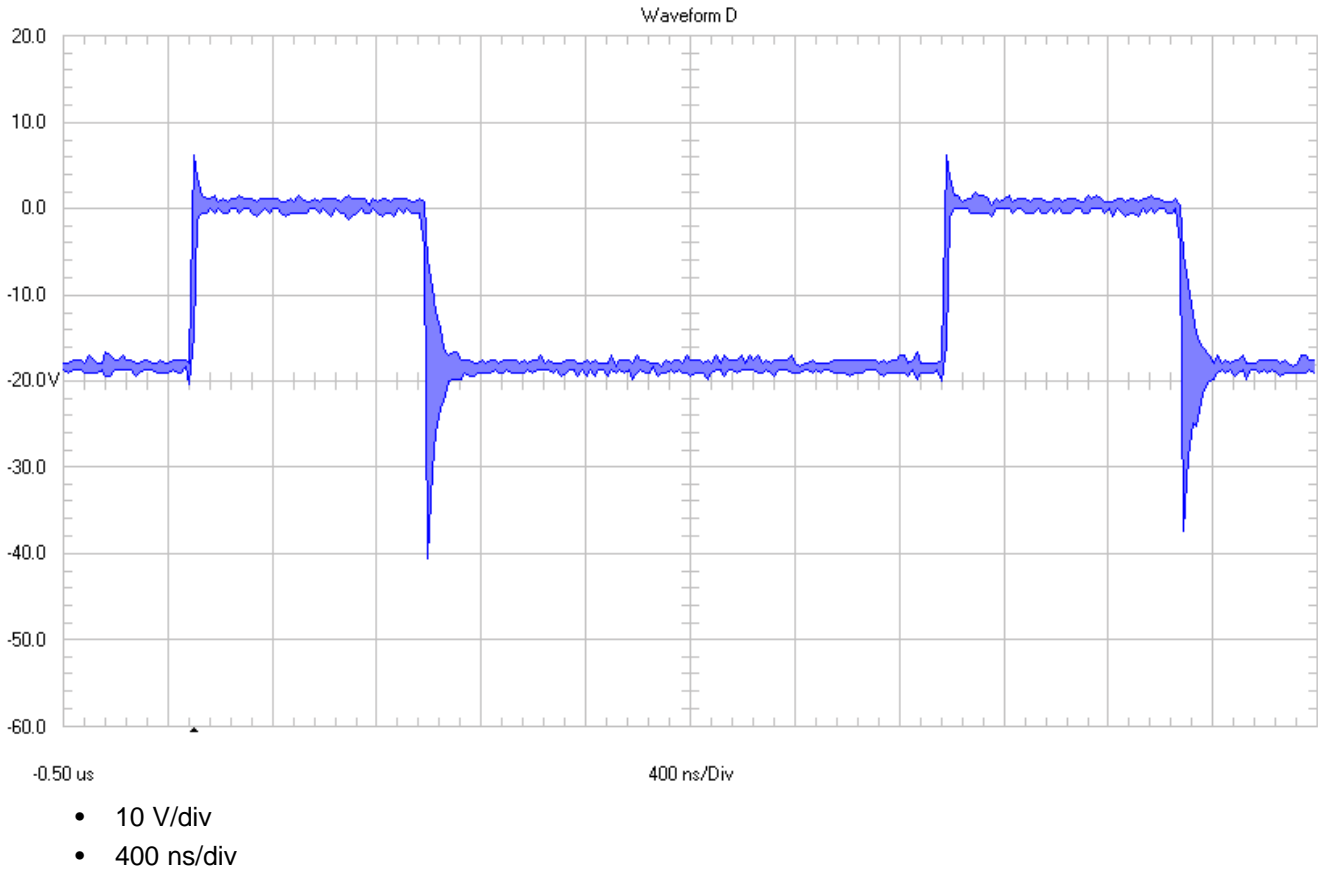


- channel 1 (blue): TP2 to GND => 5 V/div
- channel 2 (brown): TP3 to GND => 5 V/div
- 400 ns/div

4.1.3 9-V Input Voltage, 18-V Output Voltage at 2 A

4.1.3.1 Diode D1 (Referenced to VOUT)

Figure 33. Switch Node Voltage D1 ($V_{OUT}=18V$)

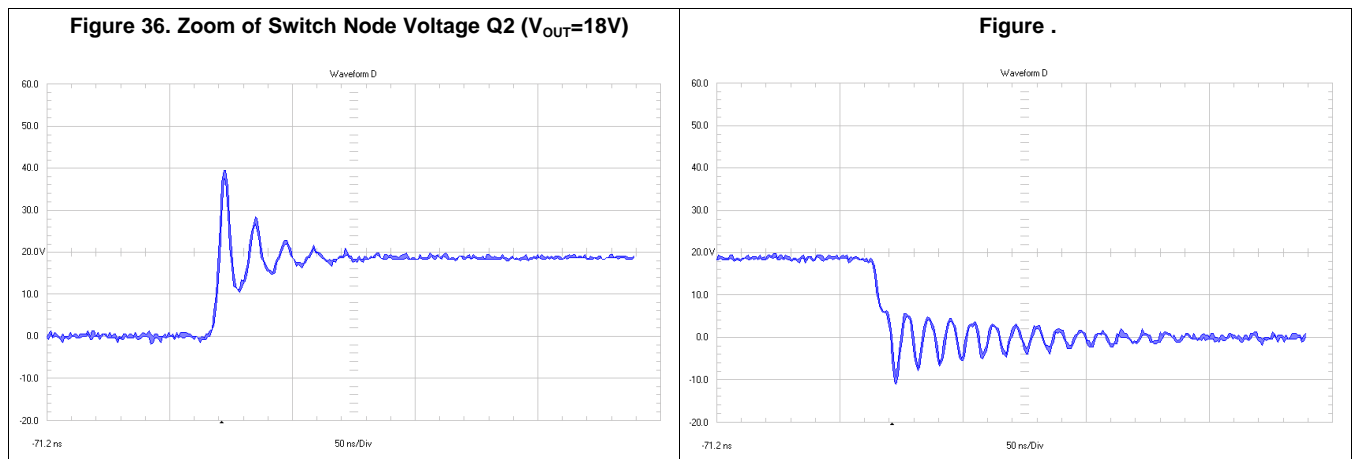
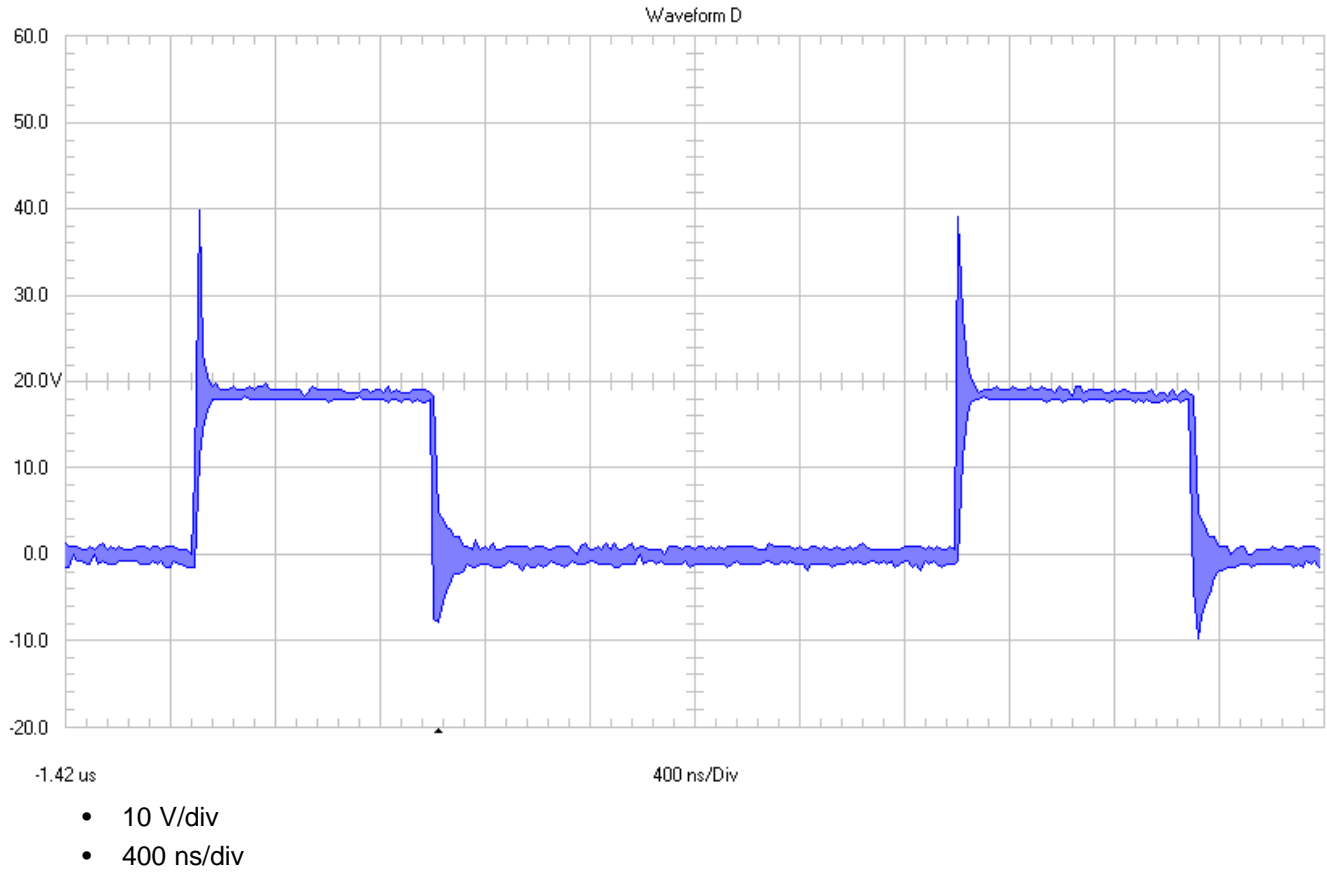


- 50 ns/div

4.1.3.2 Transistor Q2

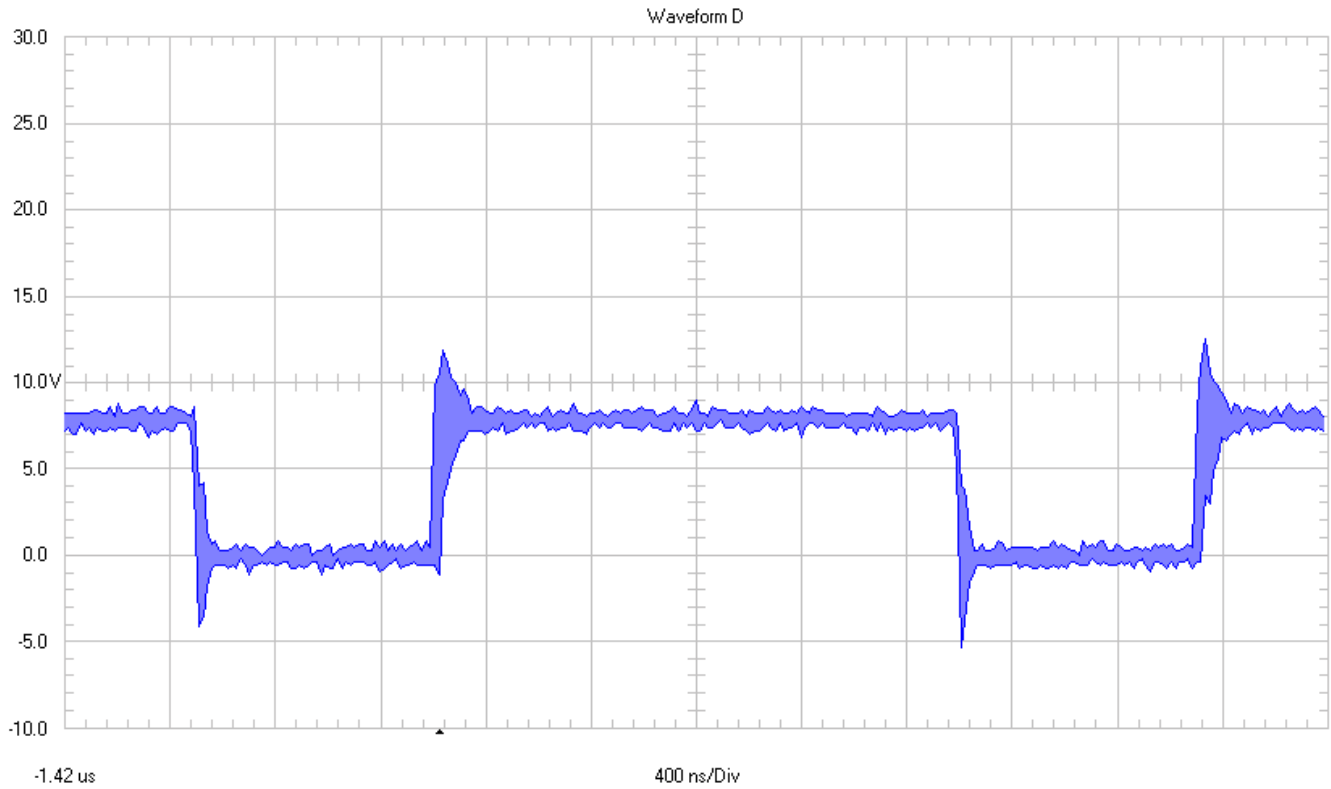
4.1.3.2.1 Drain to Source (Referenced to VOUT)

Figure 35. Switch Node Voltage Q2 ($V_{OUT}=18V$)

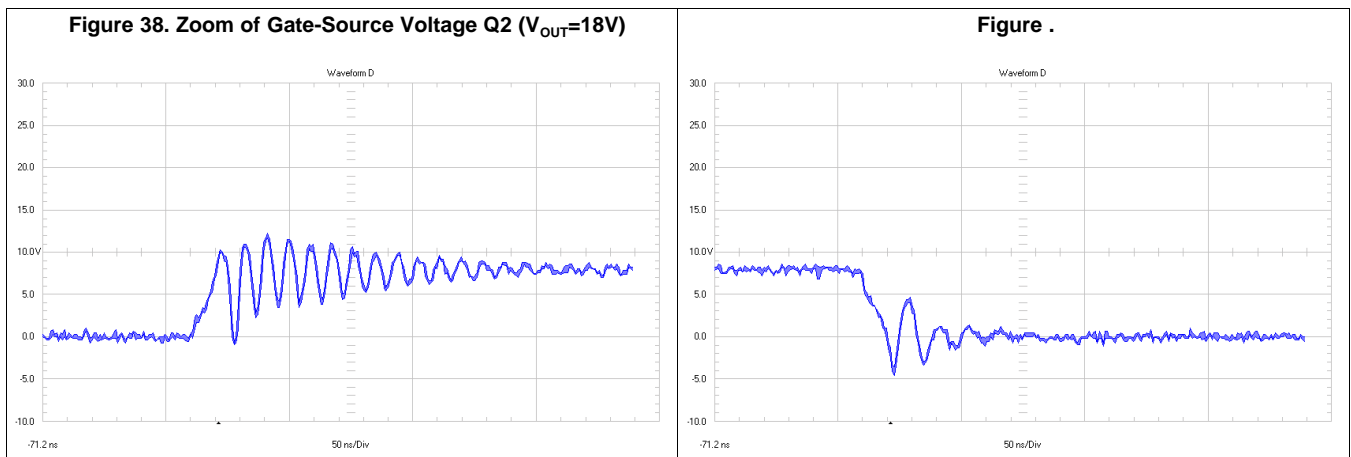


4.1.3.2.2 Gate to Source

Figure 37. Gate-Source Voltage Q2 ($V_{OUT}=18V$)



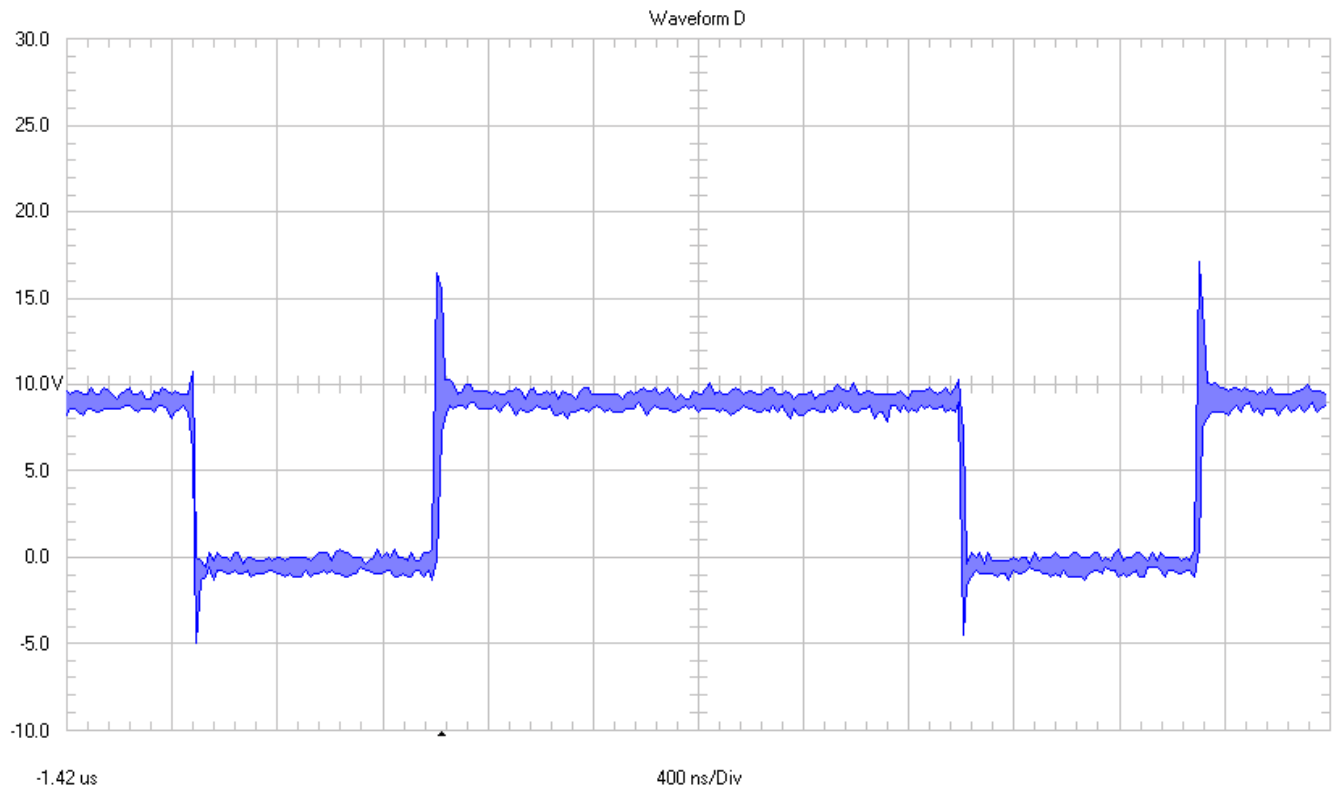
- 5 V/div
- 400 ns/div



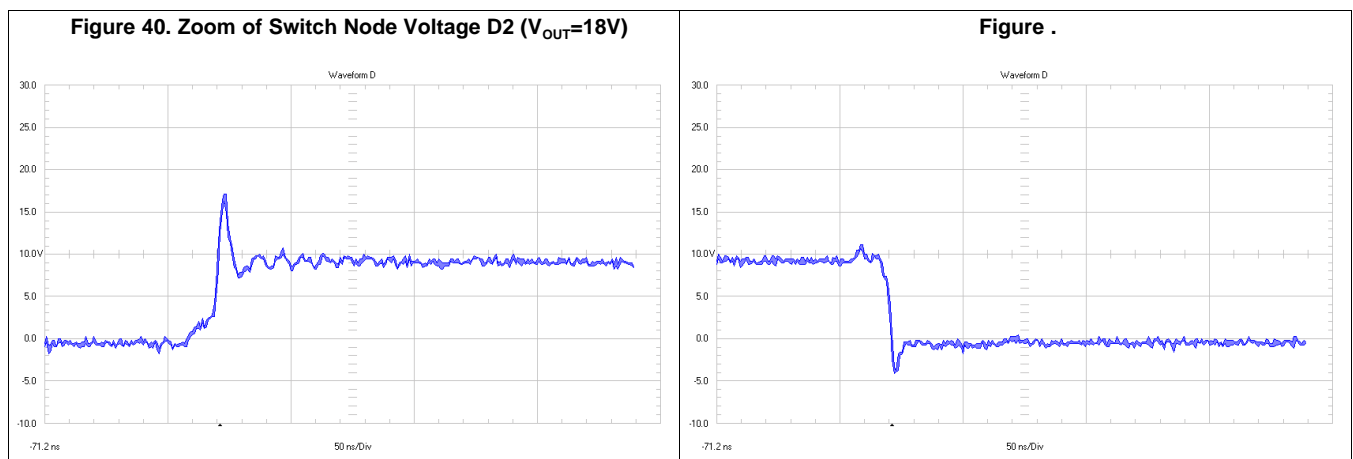
- 50 ns/div

4.1.3.3 Diode D2

Figure 39. Switch Node Voltage D2 ($V_{OUT}=18V$)



- 5 V/div
- 400 ns/div

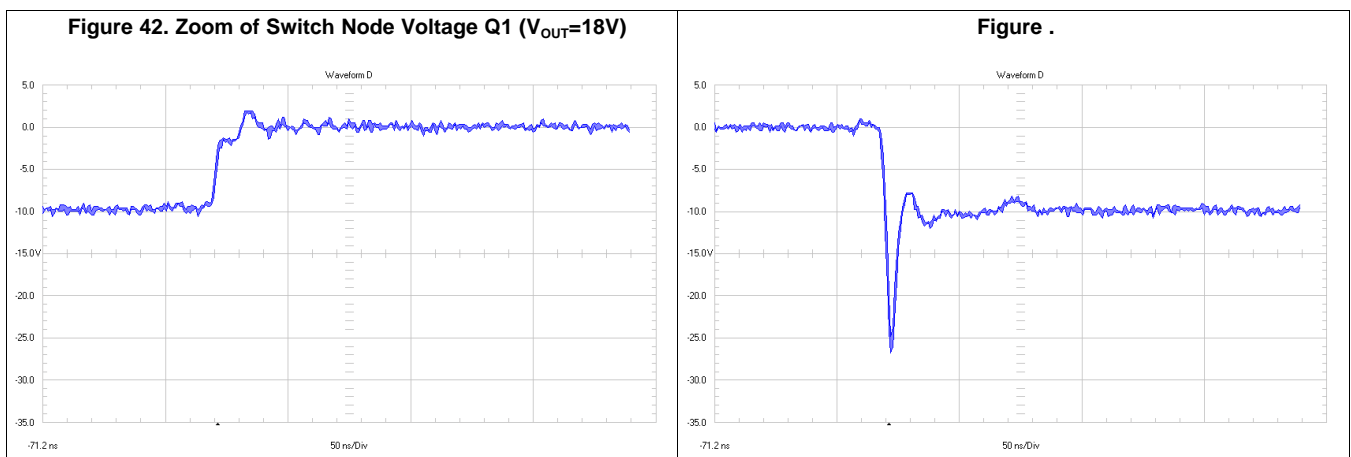
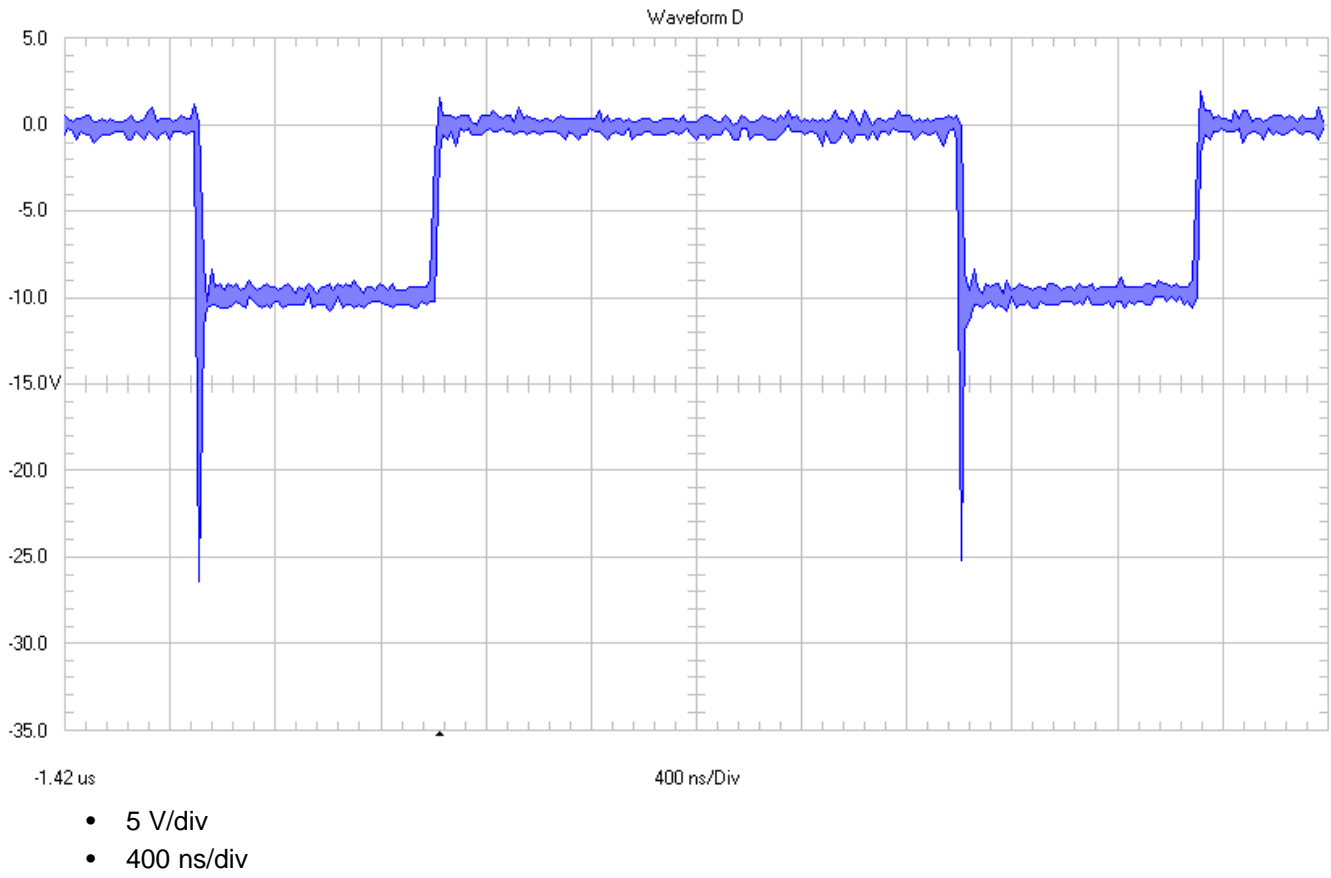


- 50 ns/major div

4.1.3.4 Transistor Q1 (Referenced to VIN)

4.1.3.4.1 Drain to Source

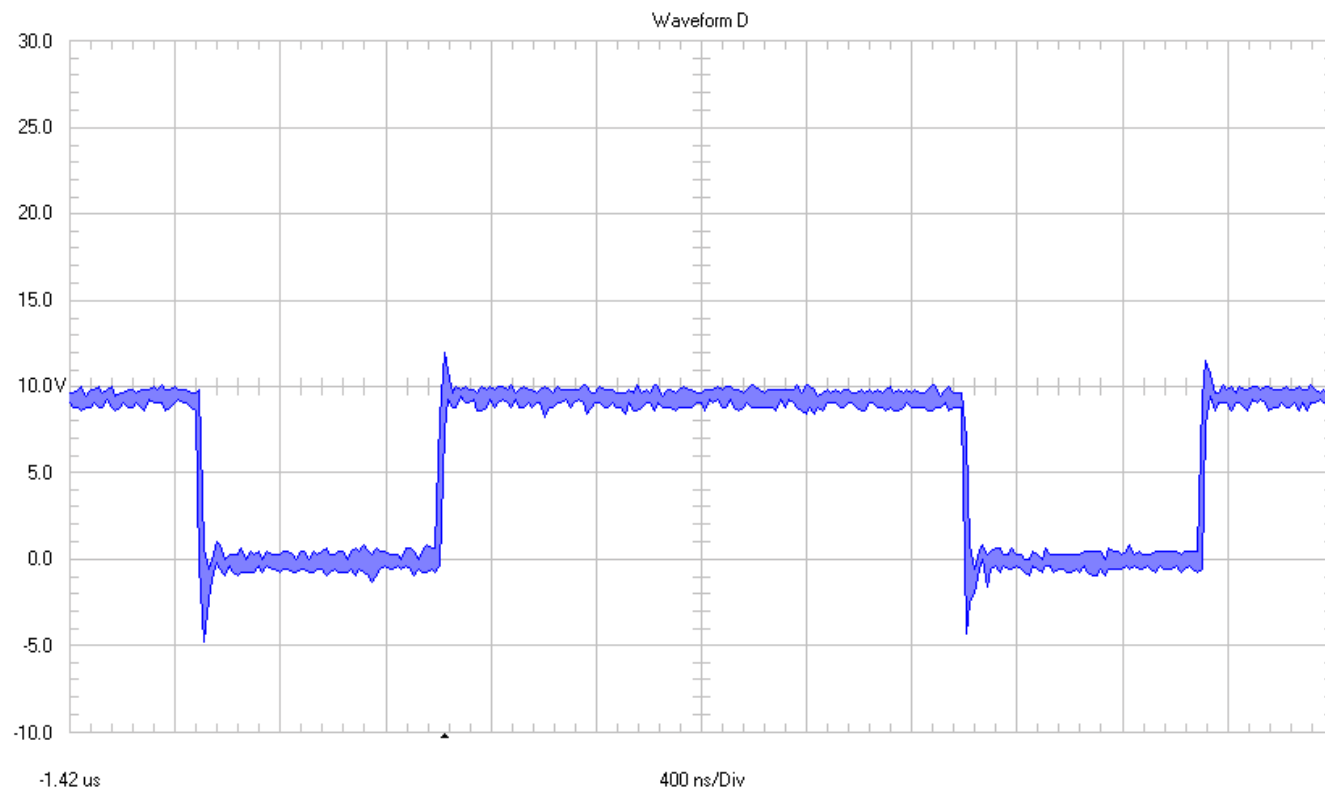
Figure 41. Switch Node Voltage Q1 ($V_{OUT}=18V$)



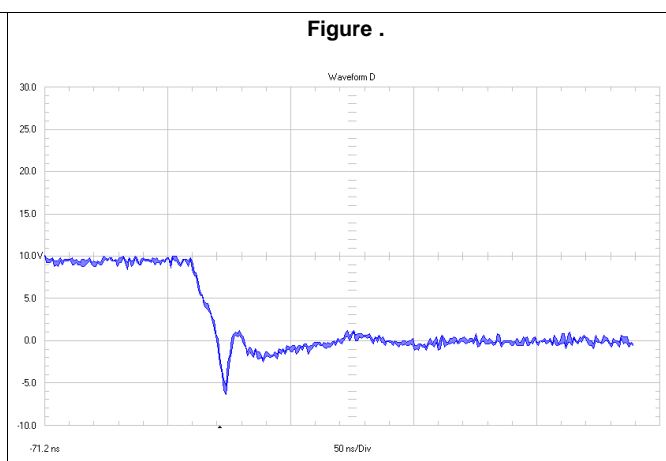
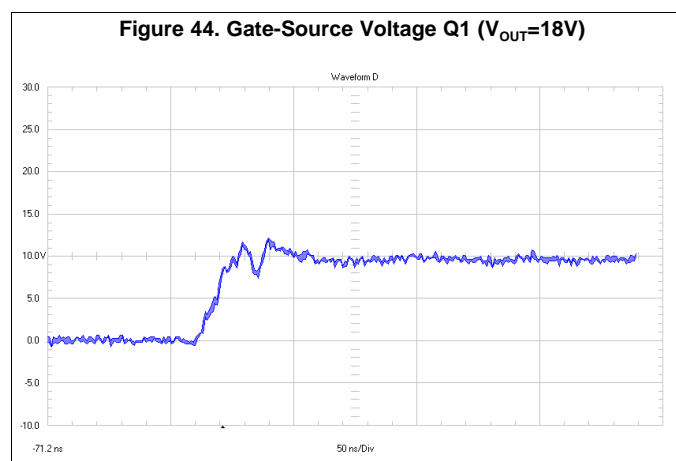
- 50 ns/major div

4.1.3.4.2 Gate to Source

Figure 43. Gate-Source Voltage Q1 (V_{OUT}=18V)



- 5 V/div
- 400 ns/div

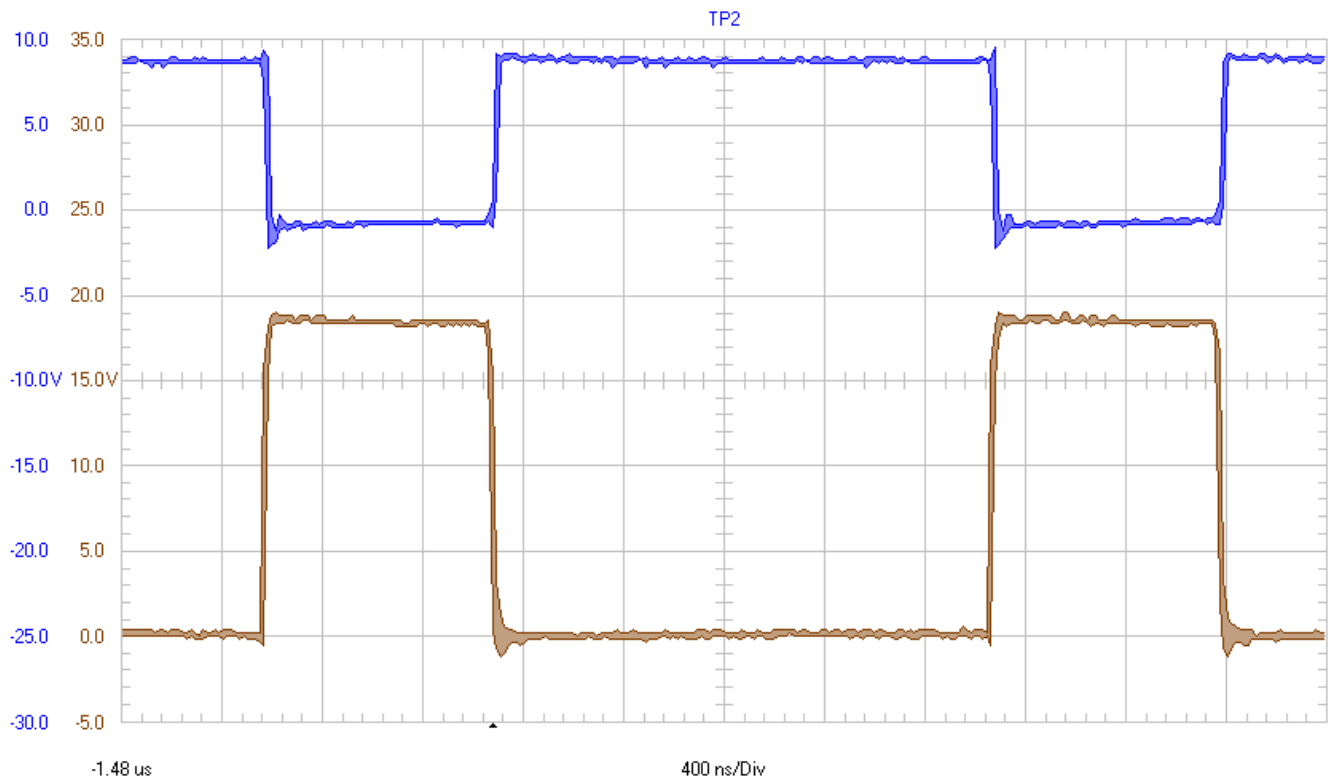


- 50 ns/major div

4.1.3.5 Waveforms at TP2 and TP3

The waveforms below are measured with 20-MHz bandwidth filter.

Figure 45. Buck-Boost Operation ($V_{OUT}=18V$)



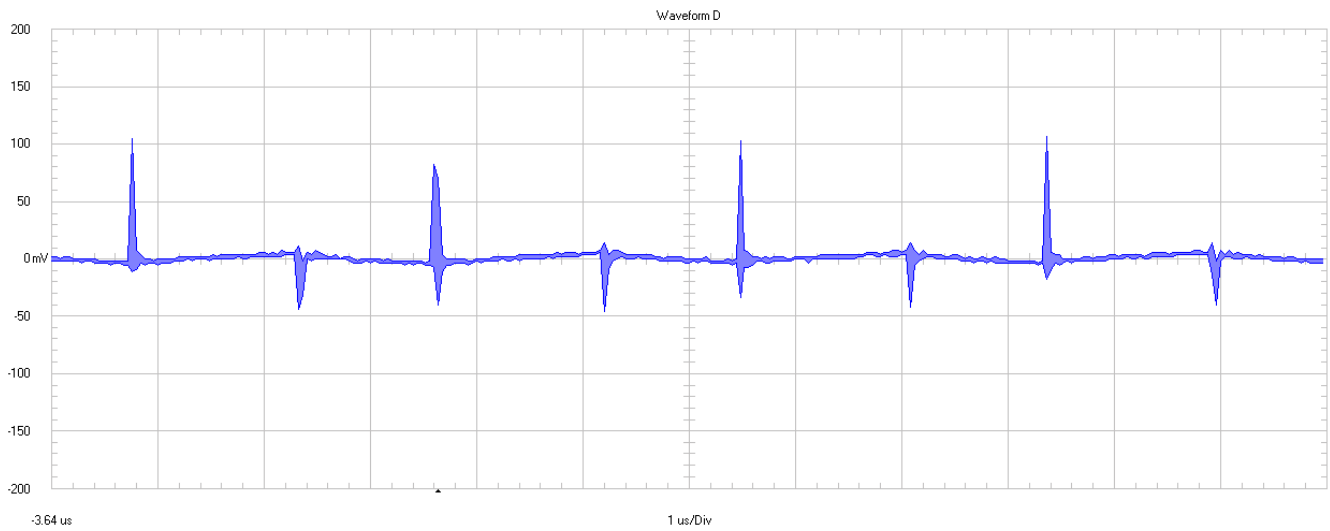
- channel 1 (blue): TP2 to GND => 5 V/div
- channel 2 (brown): TP3 to GND => 5 V/div
- 400 ns/div

4.2 Output Voltage Ripple

Waveforms are measured with 20-MHz bandwidth filter.

4.2.1 12-V Input Voltage, 6-V Output Voltage at 3 A

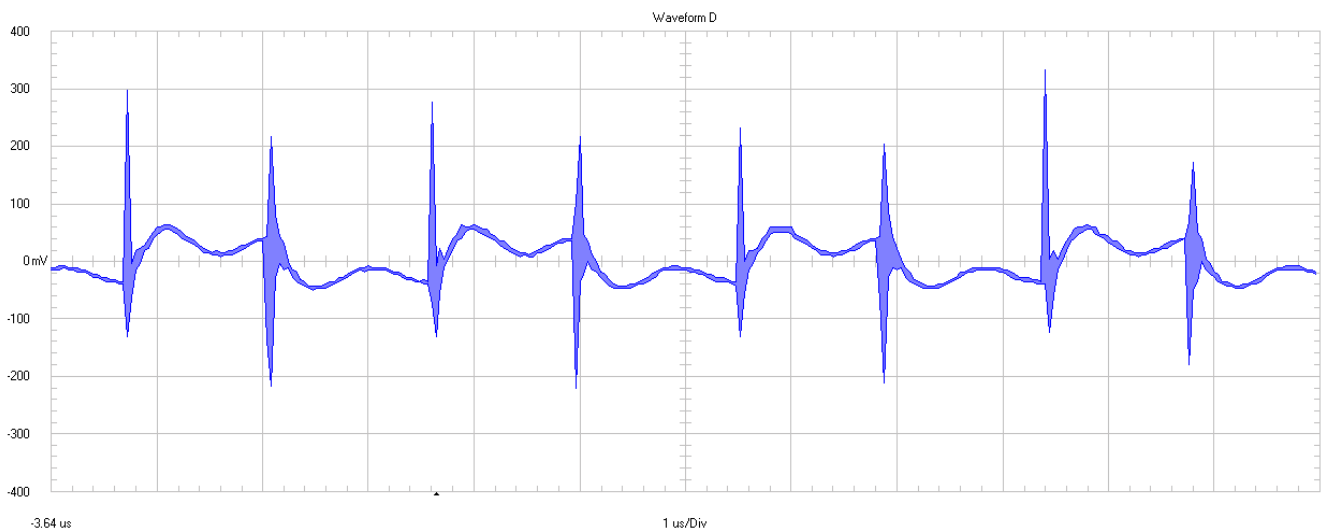
Figure 46. Output Voltage Ripple ($V_{OUT}=6V$)



- 50 mV/div
- 1 μ s/div

4.2.2 12-V Input Voltage, 12-V Output Voltage at 3 A

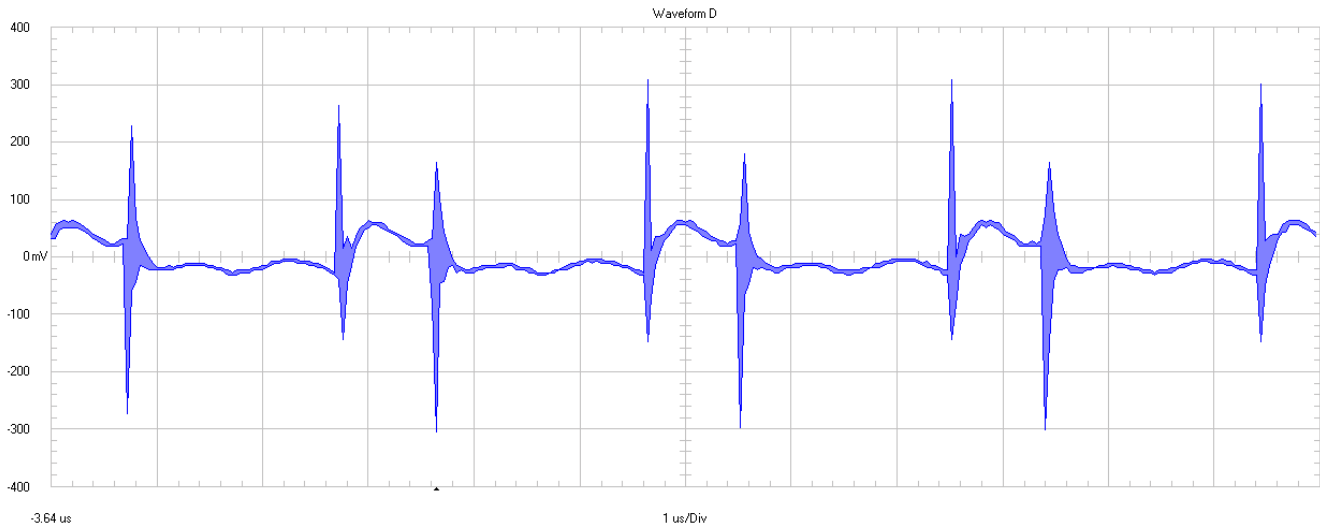
Figure 47. Output Voltage Ripple ($V_{OUT}=12V$)



- 100 mV/div
- 1 μ s/div

4.2.3 9-V Input Voltage, 18-V Output Voltage at 2 A

Figure 48. Output Voltage Ripple ($V_{OUT}=18V$)

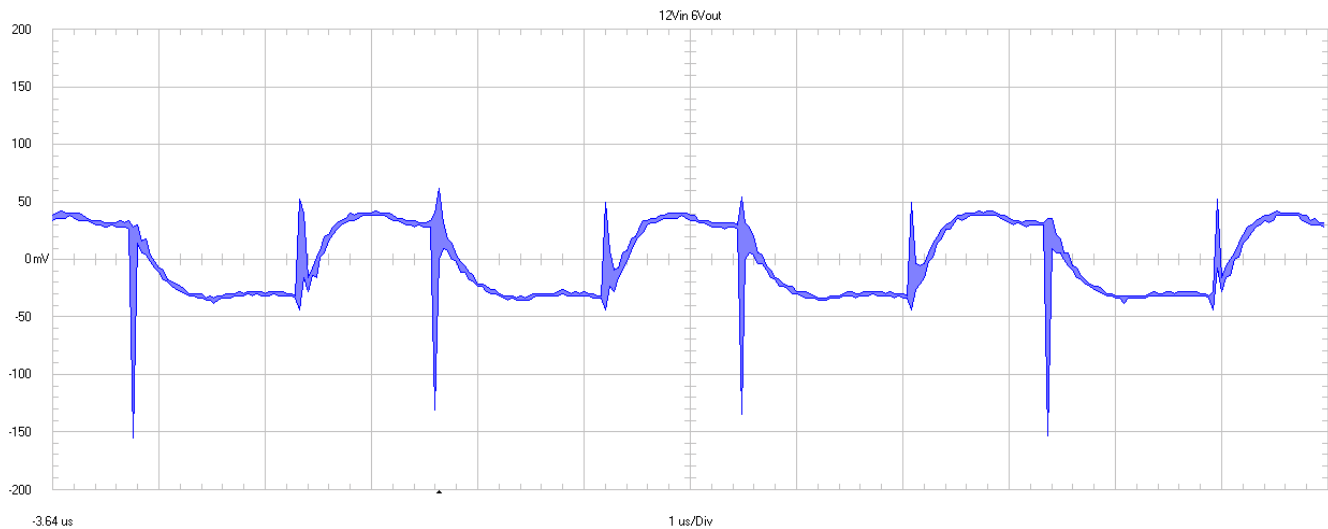


- 100 mV/div
- 1 μ s

4.3 Input Voltage Ripple

4.3.1 12-V Input Voltage, 6-V Output Voltage at 3 A

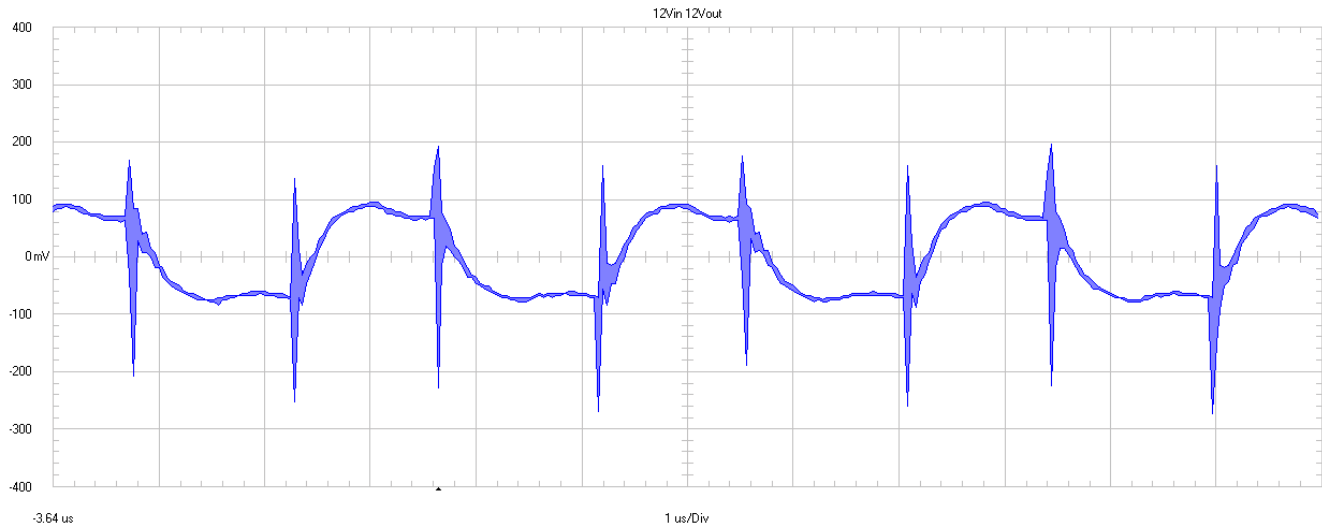
Figure 49. Input Voltage Ripple ($V_{OUT}=6V$)



- 50 mV/div
- 1 μ s/div

4.3.2 12-V Input Voltage, 12-V Output Voltage at 3 A

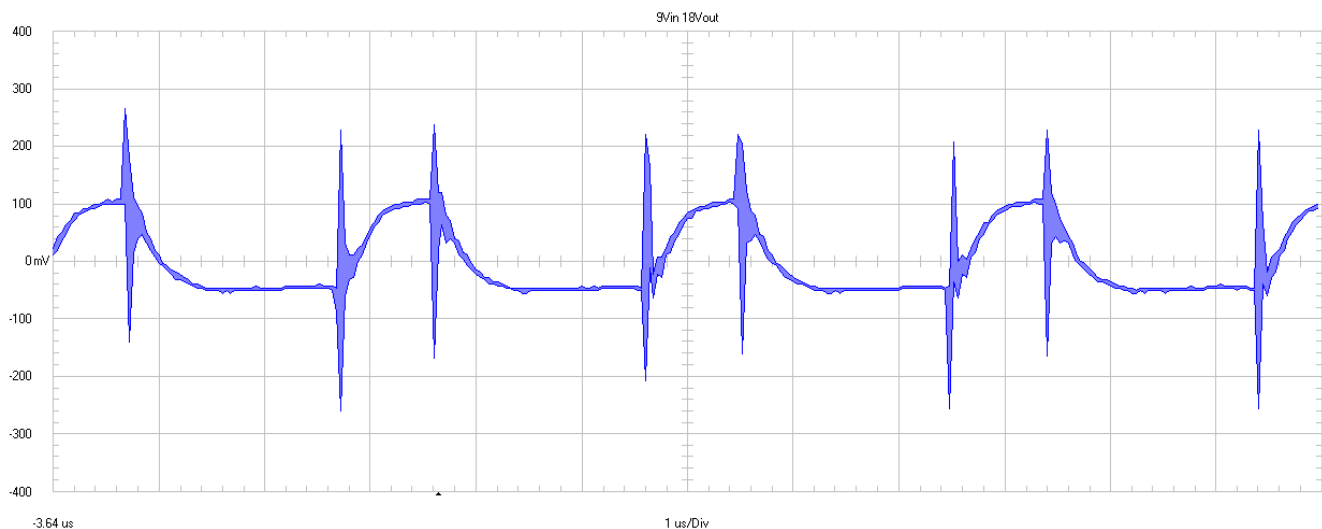
Figure 50. Input Voltage Ripple ($V_{OUT}=12V$)



- 100 mV/div
- 1 μ s/div

4.3.3 9-V Input Voltage, 18-V Output Voltage at 2 A

Figure 51. Input Voltage Ripple ($V_{OUT}=18V$)



- 100 mV/div
- 1 μ s/div

4.4 Bode Plot

Figure 52. Bode Plot for 8 Vin and 18 Vout at 2 A

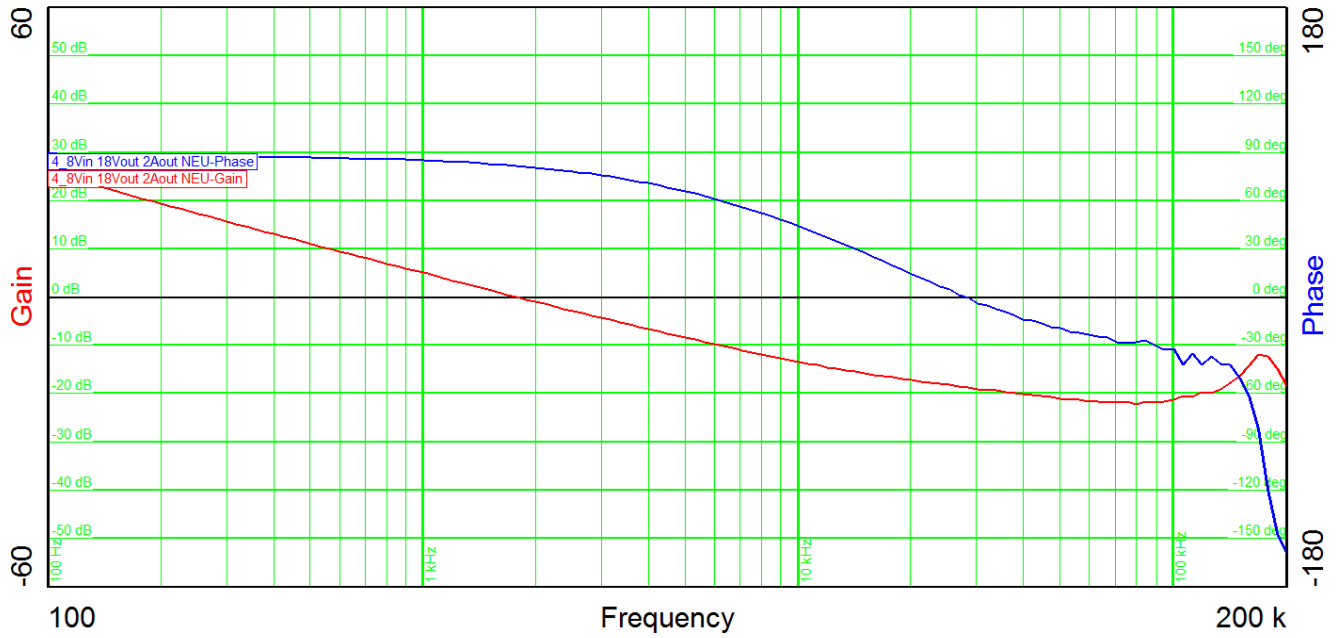
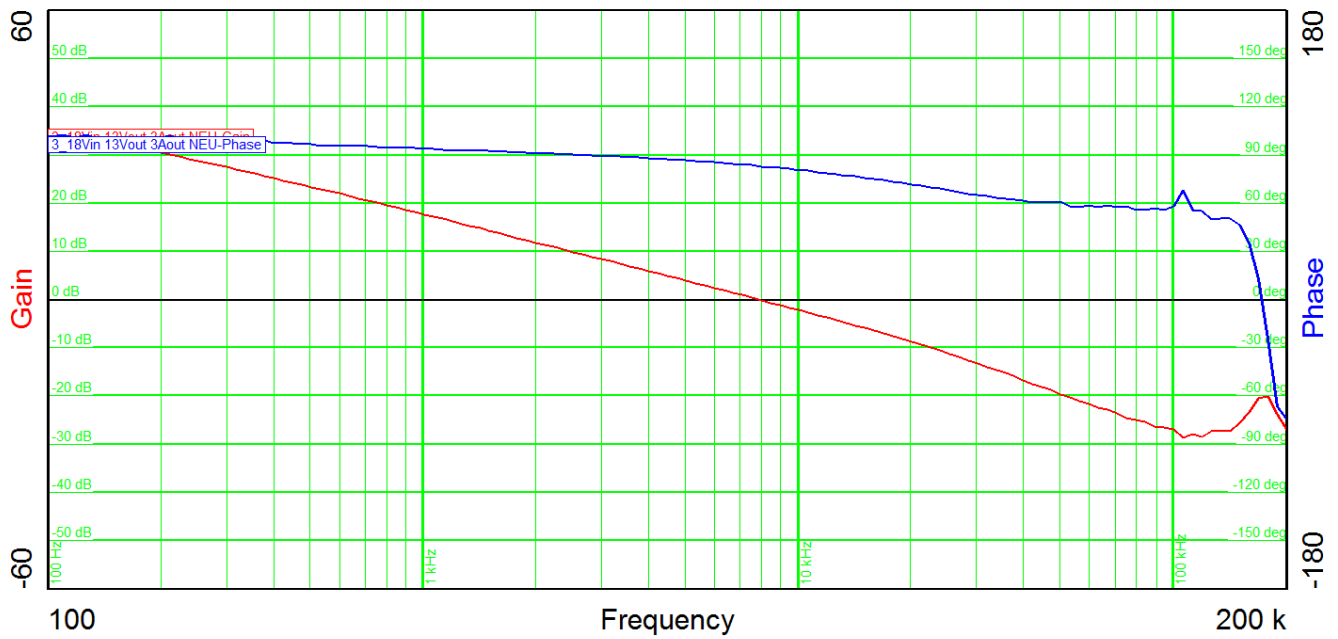


Figure 53. Bode Plot for 18 Vin and 13.3 Vout at 3 A



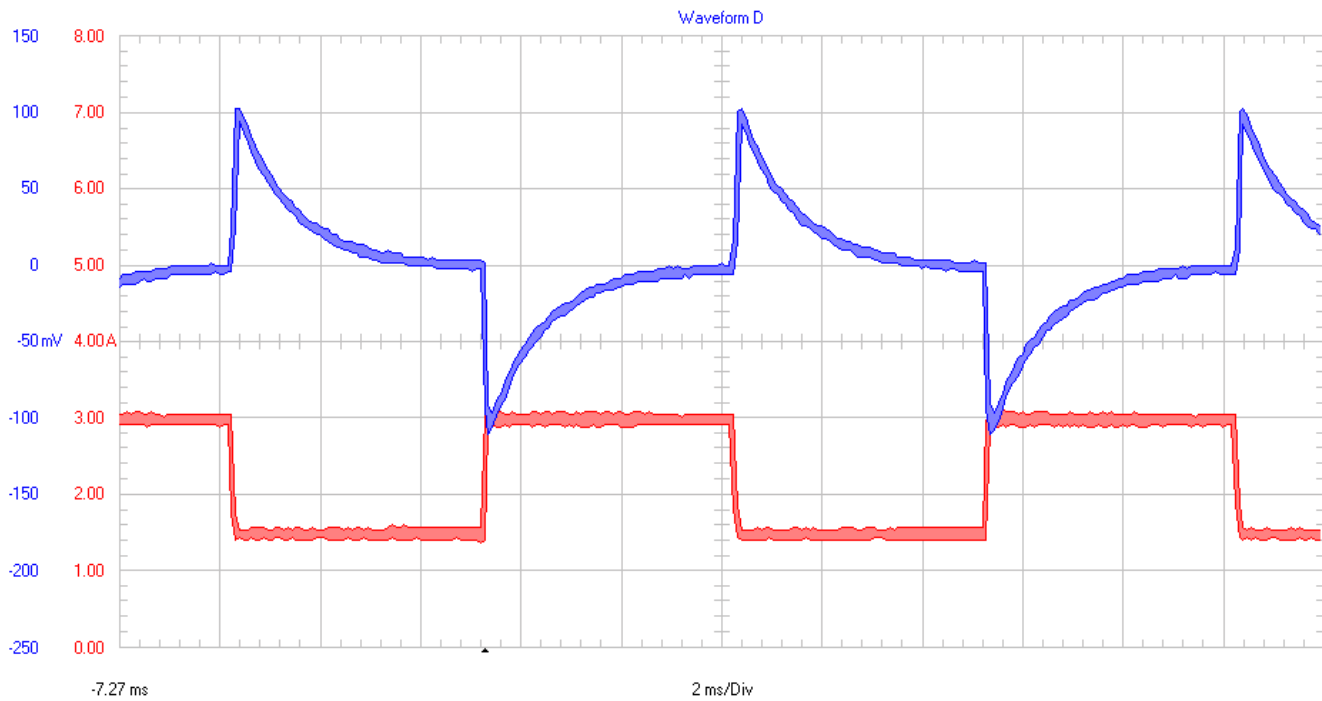
	8 Vin/18 Vout/3 Aout	18 Vin/13.3 Vout/3 Aout
Bandwidth (kHz)	1.8	7.9
Phase margin	81.4°	83
slope (20 dB/decade)	-1	-1
gain margin (dB)	-18.6	-20.3
slope (20 dB/decade)	-0.55	+0.5
freq (kHz)	27.6	172

4.5 Load Transients

The voltage waveforms were measured AC-coupled with 10-kHz bandwidth filter. The current waveforms were done with 20-MHz bandwidth filter.

4.5.1 12-V Input Voltage, 6-V Output Voltage

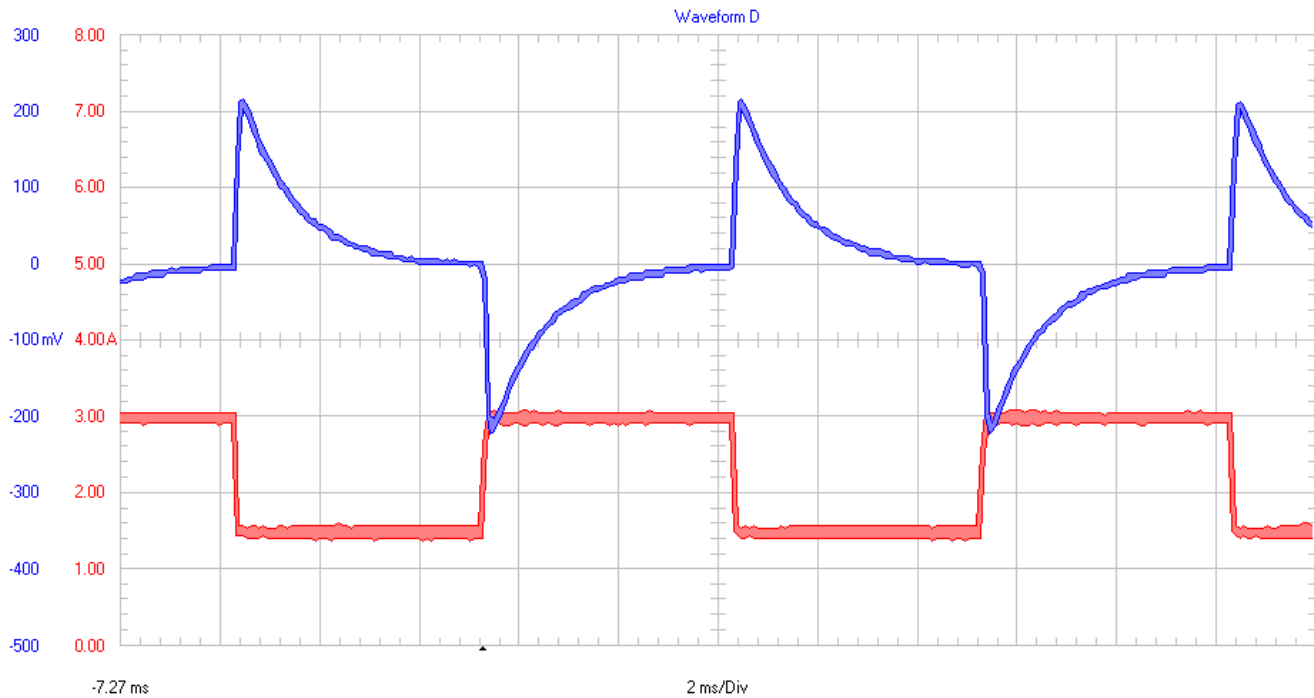
Figure 54. Load Step From 1.5 A to 3 A With 100-Hz Load Switching



- channel 1 (blue) : output voltage => 50 mV/div
- channel 2 (red) : output current => 1 A/div
- 2 ms/div

4.5.2 12-V Input Voltage and 12-V Output Voltage

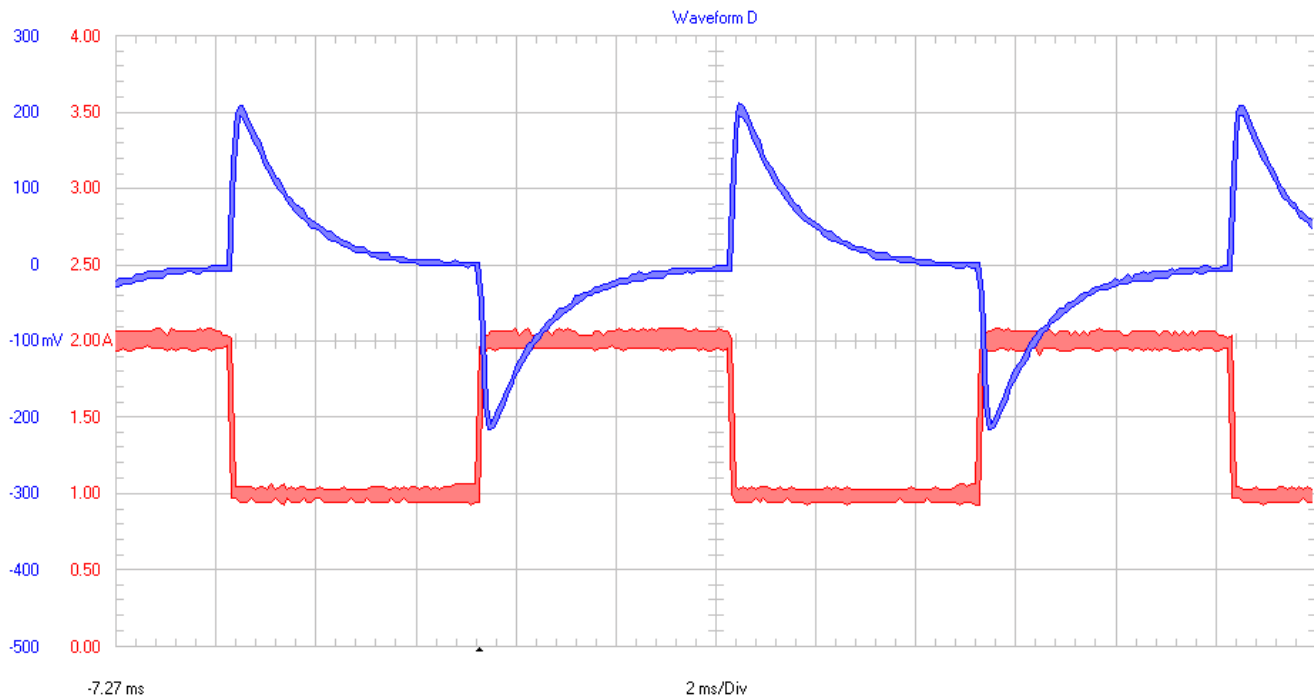
Figure 55. Load Step From 1.5 A to 3 A With 100-Hz Load Switching



- channel 1 (blue) : output voltage => 100 mV/div
- channel 2 (red) : output current => 1 A/div
- 2 ms/div

4.5.3 9-V Input Voltage, 18-V Output Voltage

Figure 56. Load Step From 1 A to 2 A With 100-Hz Load Switching



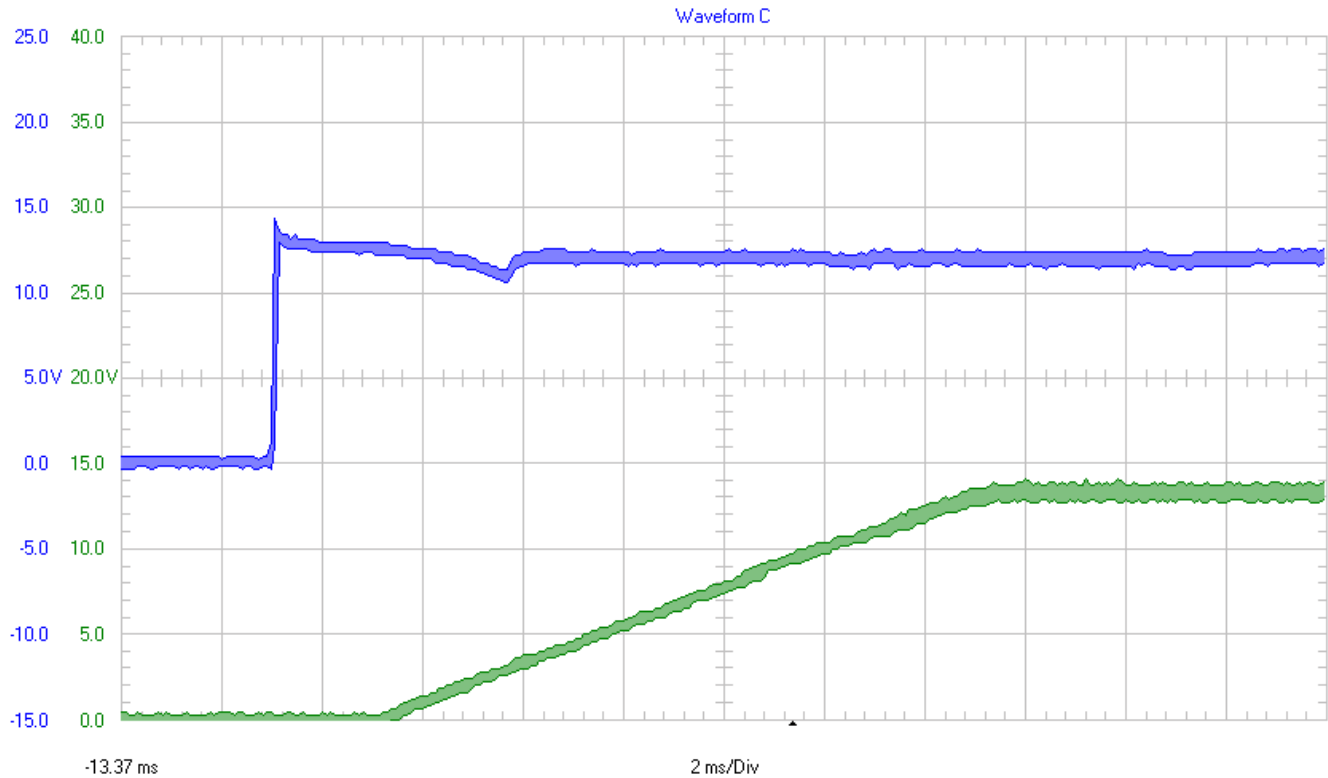
- channel 1 (blue) : output voltage => 100 mV/div
- channel 2 (red) : output current => 0.5 A/div
- 2 ms/div

4.6 Start-up Sequence

All waveforms are done with 20-MHz bandwidth filter

4.6.1 12-V Input Voltage, 13.3-V Output Voltage at 3 A

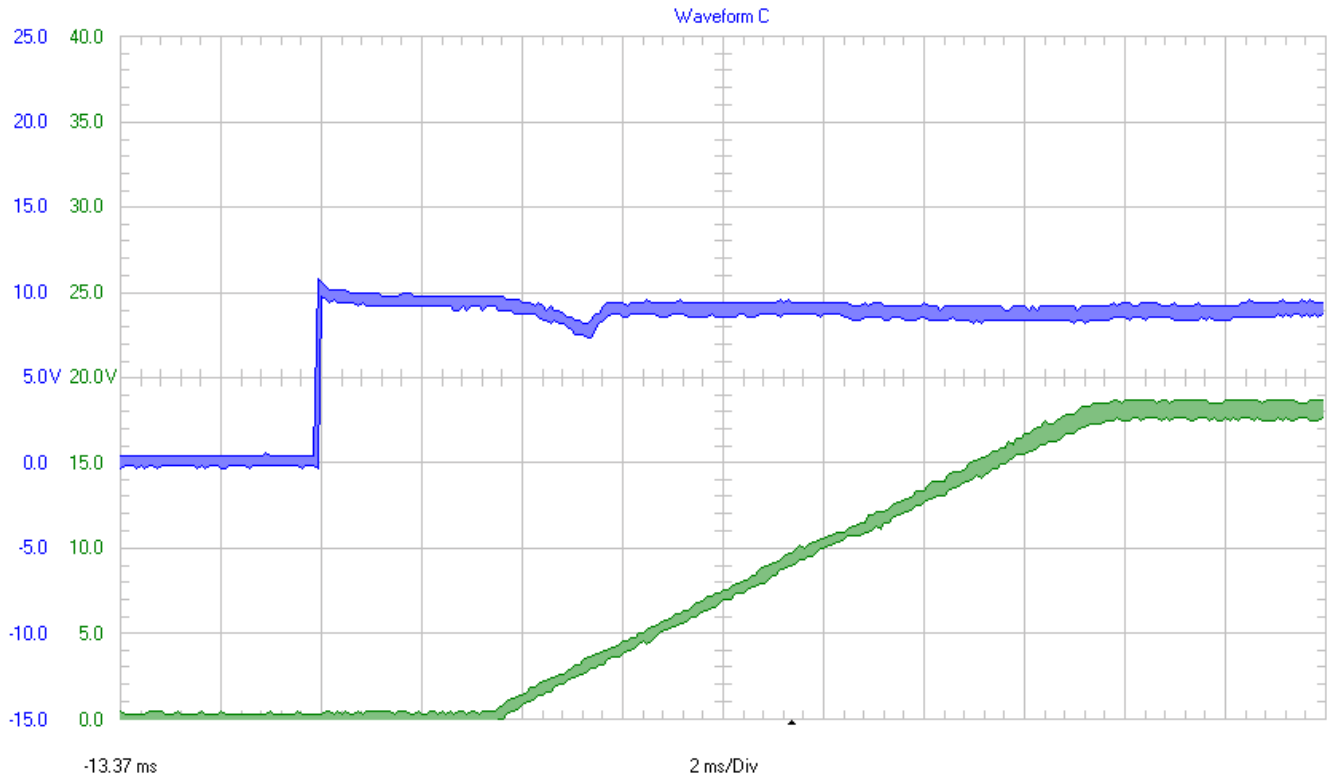
Figure 57. Start-up ($V_{OUT}=13.3V$)



- channel 1 (blue) : input voltage => 5 V/div
- channel 2 (green) : output voltage => 5 V/div
- 2 ms/div

4.6.2 9-V Input Voltage, 18-V Output Voltage at 2 A

Figure 58. Start-up ($V_{OUT}=18V$)

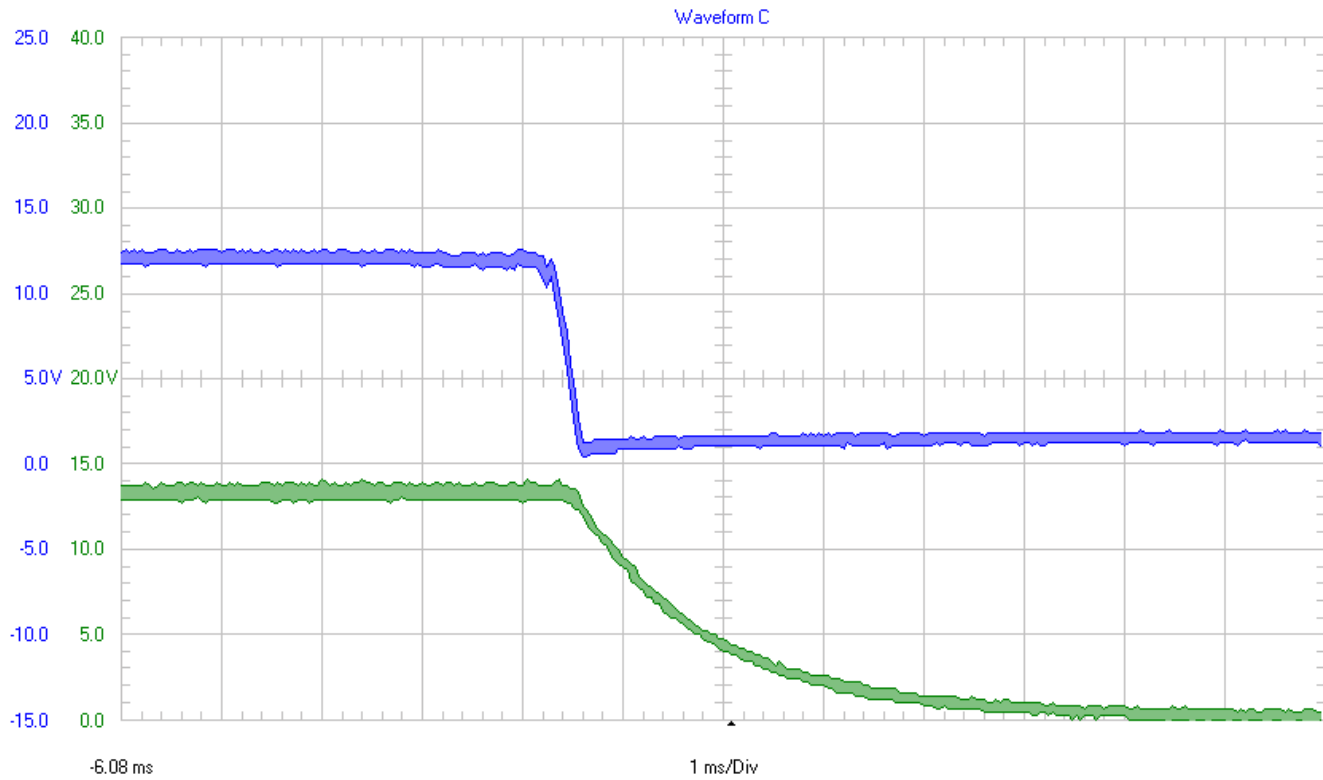


- channel 1 (blue) : input voltage => 5 V/div
- channel 2 (green) : output voltage => 5 V/div
- 2 ms/div

4.7 Shutdown Sequence

4.7.1 12-V Input Voltage, 13.3-V Output Voltage at 3 A

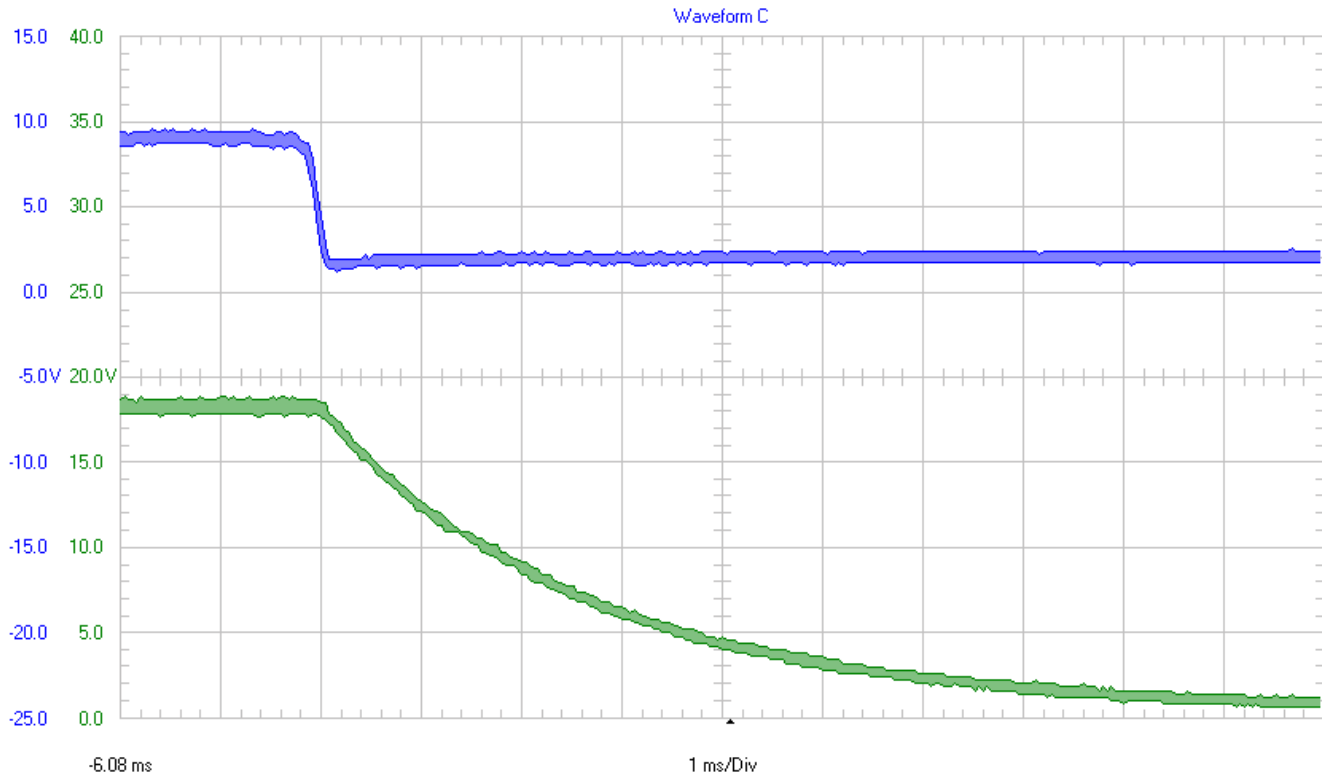
Figure 59. Shutdown ($V_{OUT}=13.3V$)



- channel 1 (blue) : input voltage => 5 V/div
- channel 2 (green) : output voltage => 5 V/div
- 2 ms/div

4.7.2 9-V Input Voltage, 18-V Output Voltage at 2 A

Figure 60. Shutdown ($V_{OUT}=18V$)



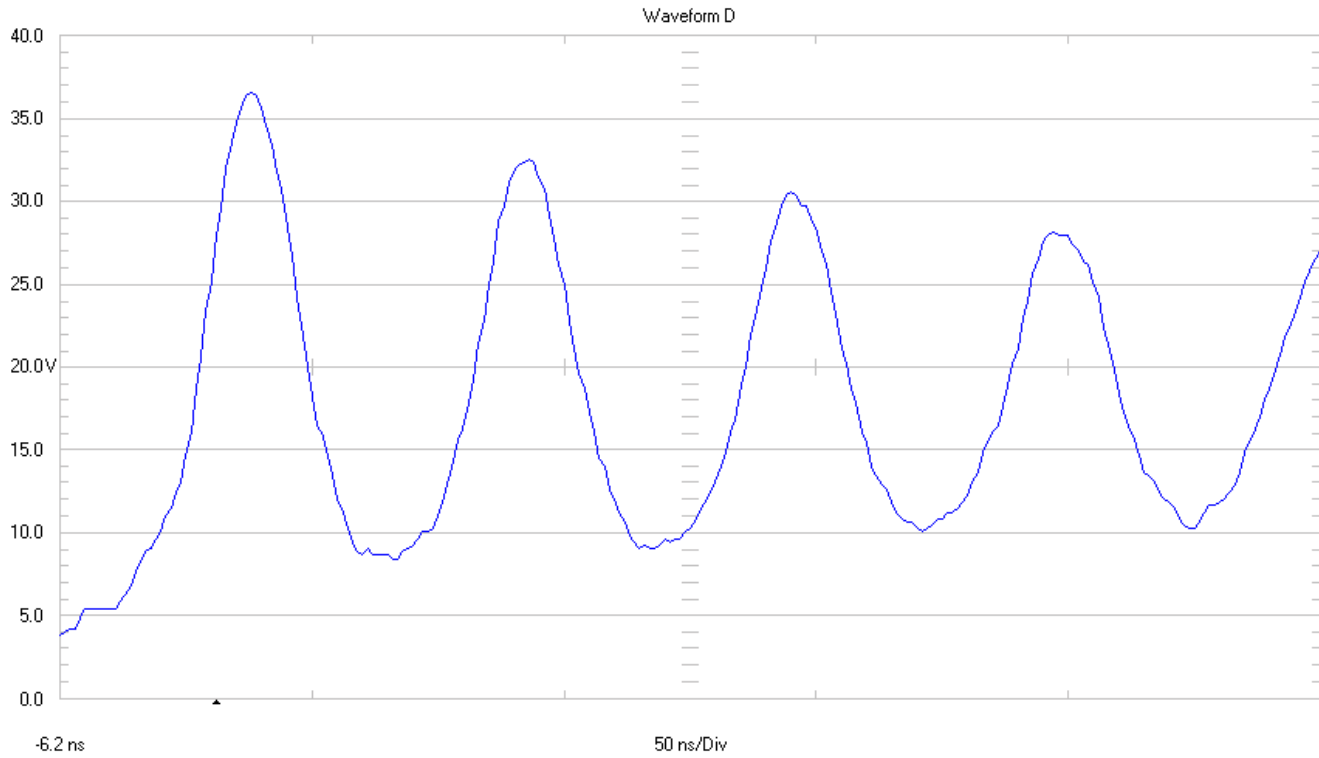
- channel 1 (blue) : input voltage => 5 V/div
- channel 2 (green) : output voltage => 5 V/div
- 2 ms/div

4.8 Snubber Evaluation (C4 +R1)

The measurements are done with 18-V input voltage and 3-A output current. All waveforms are done with full bandwidth.

4.8.1 No Snubber

Figure 61. Zoom of Switch Node Voltage with non added Snubber

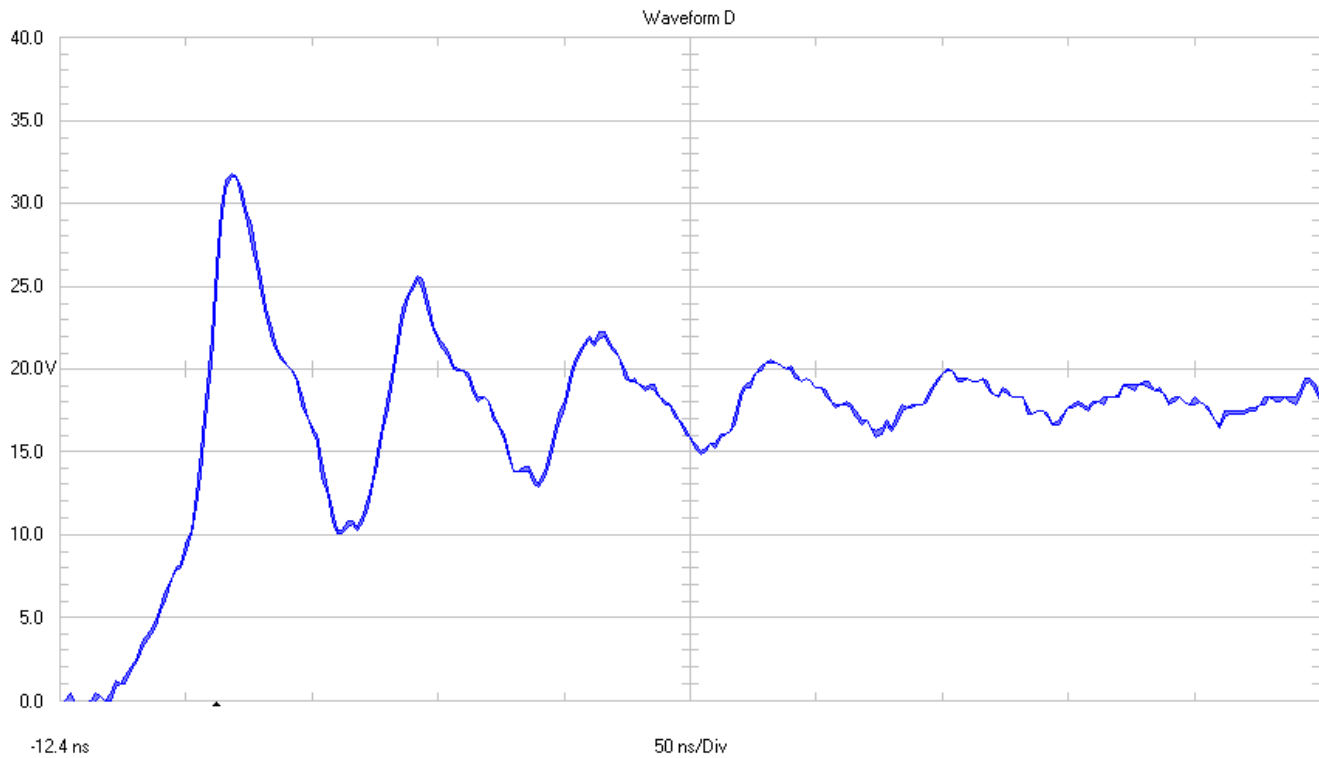


- 5 V/div
- 50 ns/major div

The ripple frequency is around 94 MHz with a maximum voltage of 37 V and 19.2-V overshoot.

4.8.2 470 pF + 0R

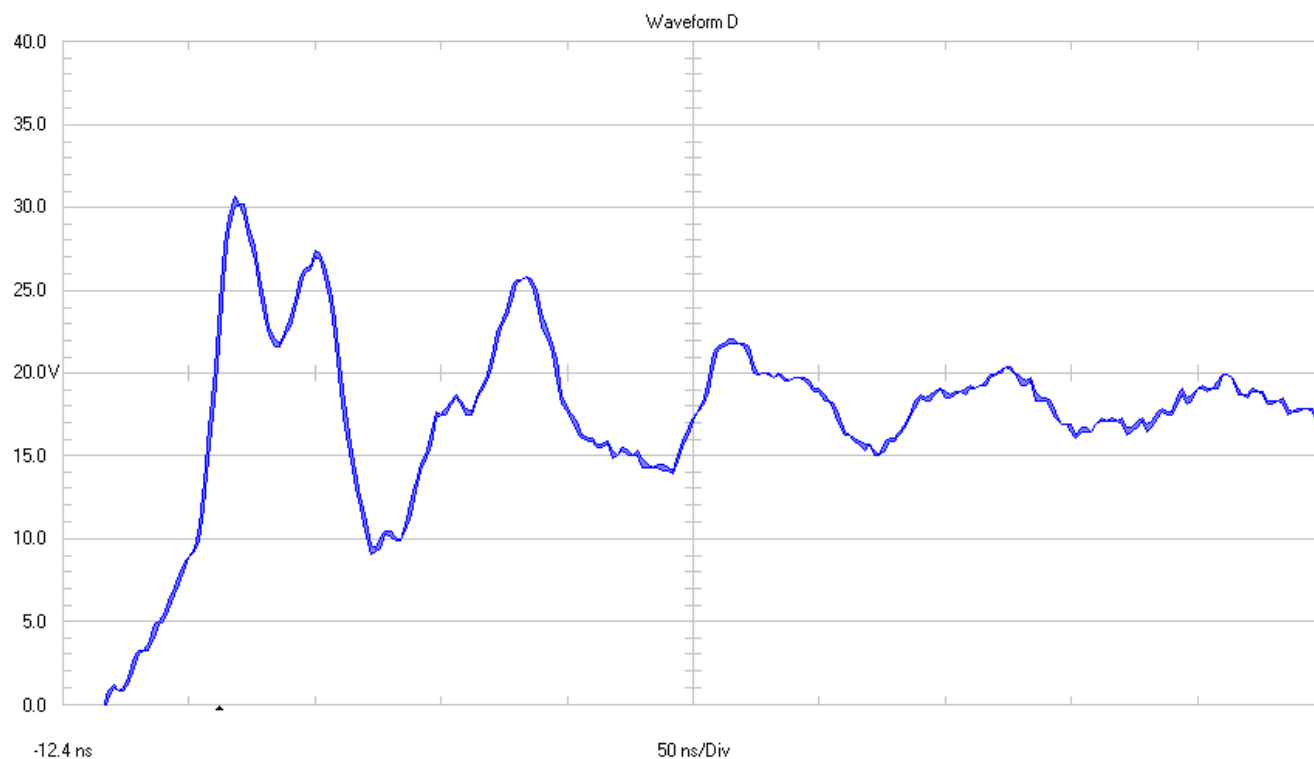
Figure 62. Zoom of Switch Node Voltage with 470pF



5 V/div

50 ns/major div

The ripple frequency is around 70.4 MHz with a maximum voltage of 31.6 V and 13.8-V overshoot.

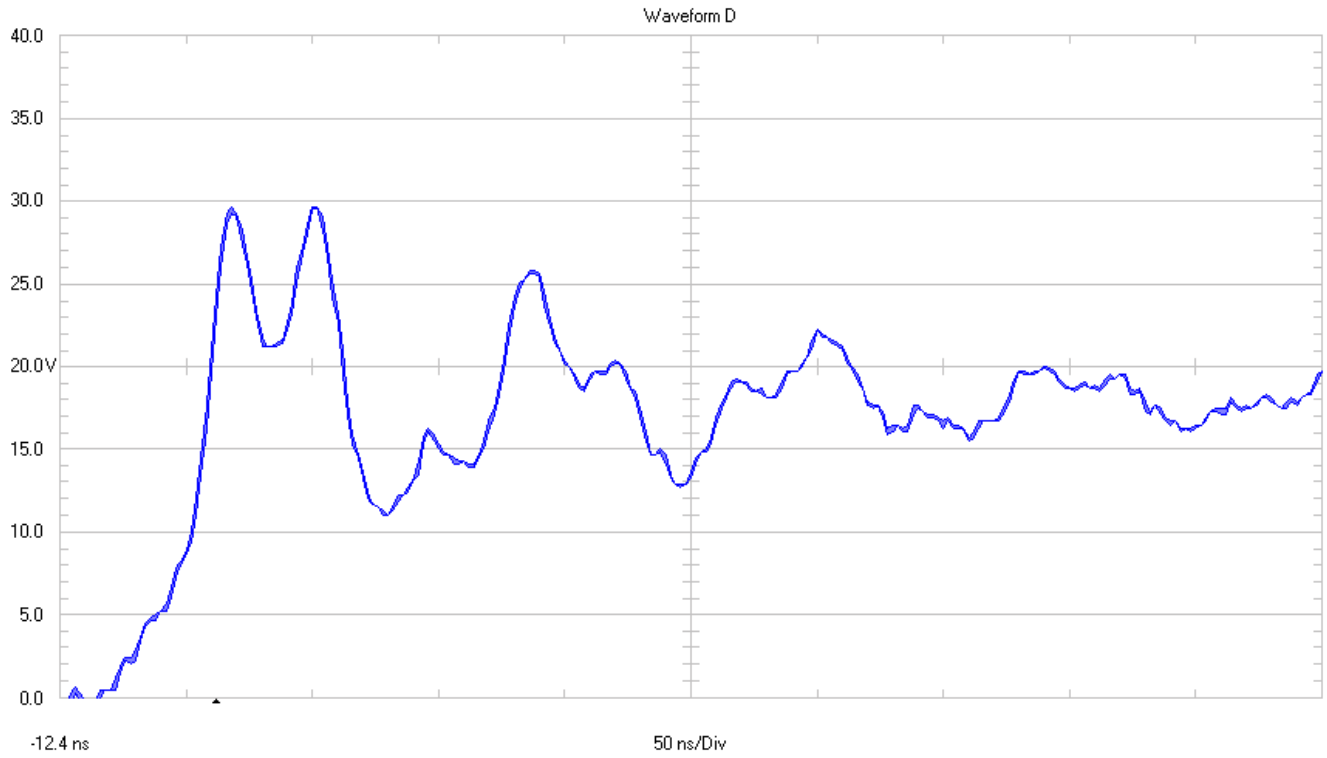
4.8.3 1 nF + 0R
Figure 63. Zoom of Switch Node Voltage with 1 nF


- 5 V/div
- 50 ns/major div

The ripple frequency is around 54 MHz with a maximum voltage of 30.4 V and 12.6-V overshoot.

4.8.4 1.2 nF + 0R

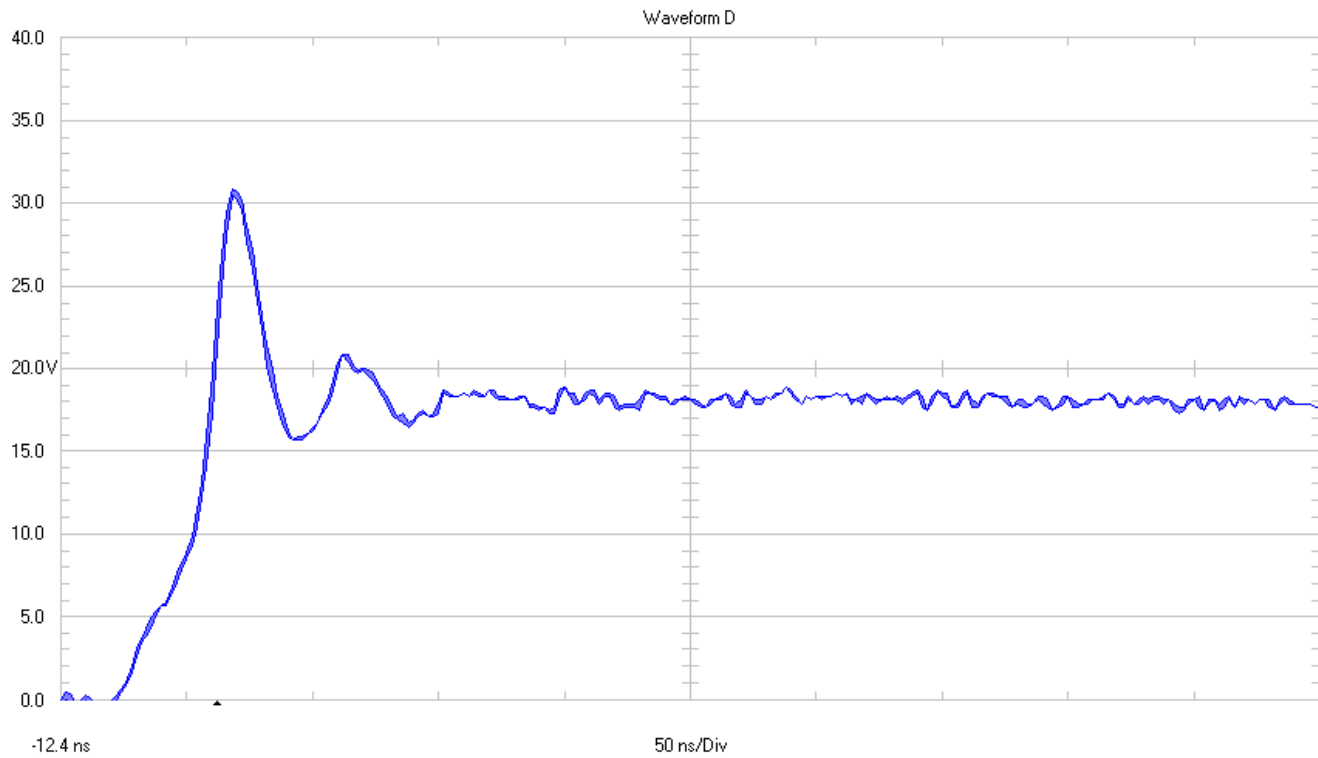
Figure 64. Zoom of Switch Node Voltage with 1.2 nF



5 V/div

50 ns/major div

The ripple frequency is around 48 MHz with a maximum voltage of 29.8 V and 12-V overshoot.

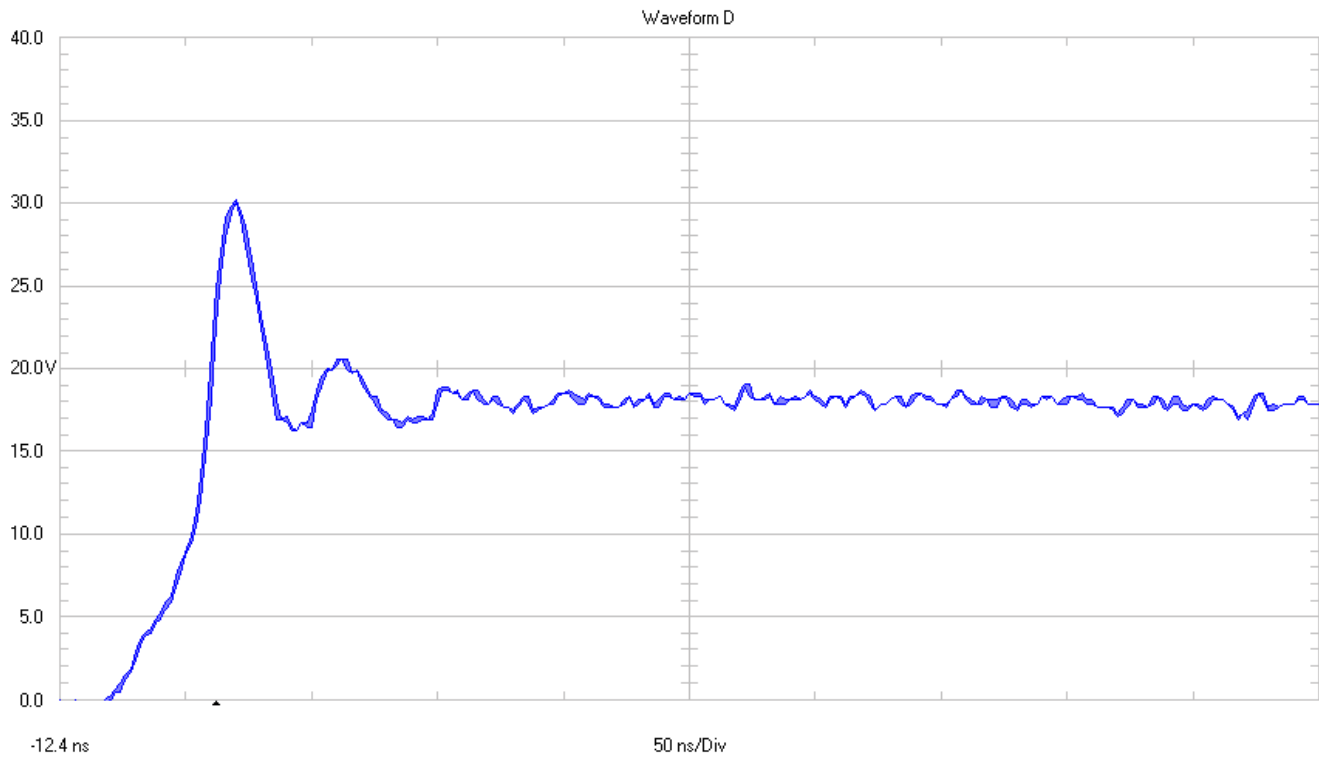
4.8.5 1.2 nF + 4.3 Ω
Figure 65. Zoom of Switch Node Voltage with 1.2nF and 4.3 Ω


- 5 V/div
- 50 ns/div

The maximum voltage is 30.6 V and the overshoot is 12.8 V.

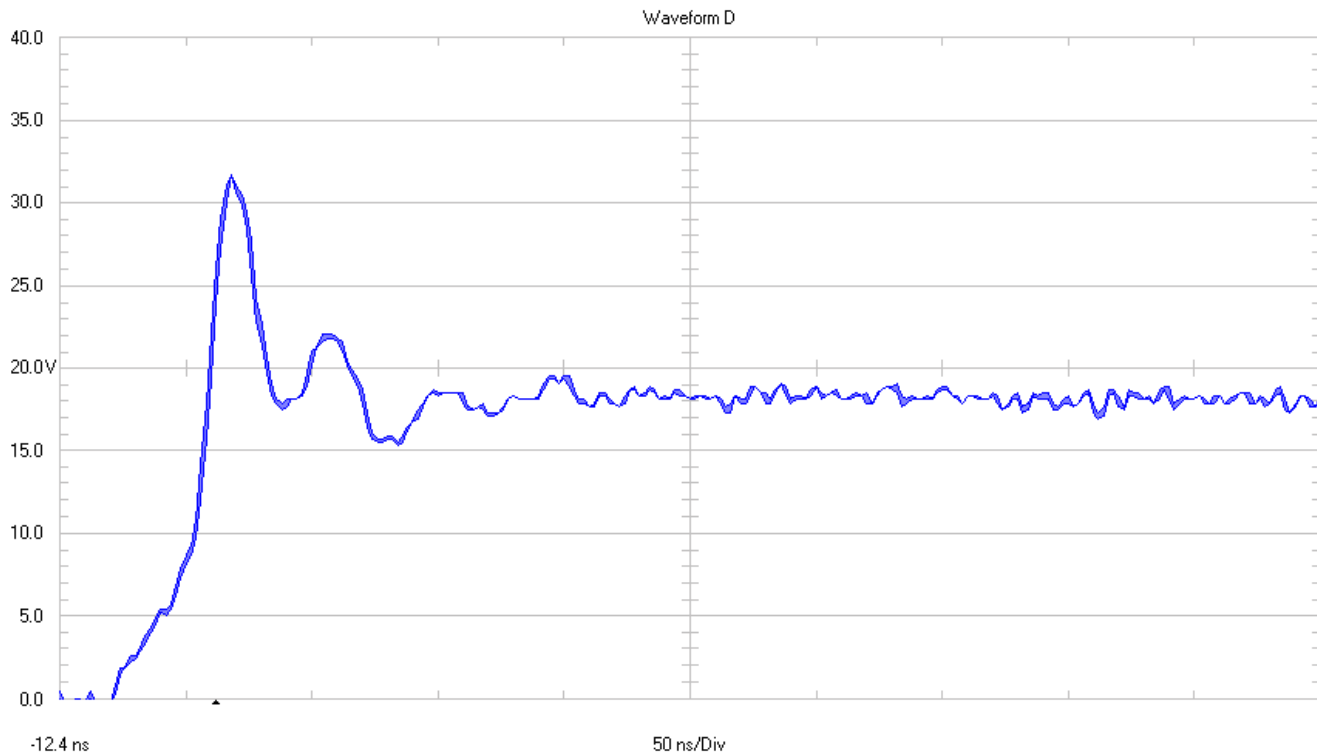
4.8.6 1.2 nF + 3.3 Ω

Figure 66. Zoom of Switch Node Voltage with 1.2 nF and 3.3 Ω



- 5 V/div
- 50 ns/div

The maximum voltage is 30.2 V and the overshoot is 12.4 V.

4.8.7 1.2 nF + 2.2 Ω
Figure 67. Zoom of Switch Node Voltage with 1.2nF and 2.2 Ω


- 5 V/div
- 50 ns/div

A further reduction of the resistor value yielded in an increase of the overshoot. The maximum voltage is now 31.4 V and the overshoot is 13.8 V. Therefore the decision for the snubber was made for 1.2 nF and 3.3 Ω .

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (<https://www.ti.com/legal/termsofsale.html>) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2021, Texas Instruments Incorporated