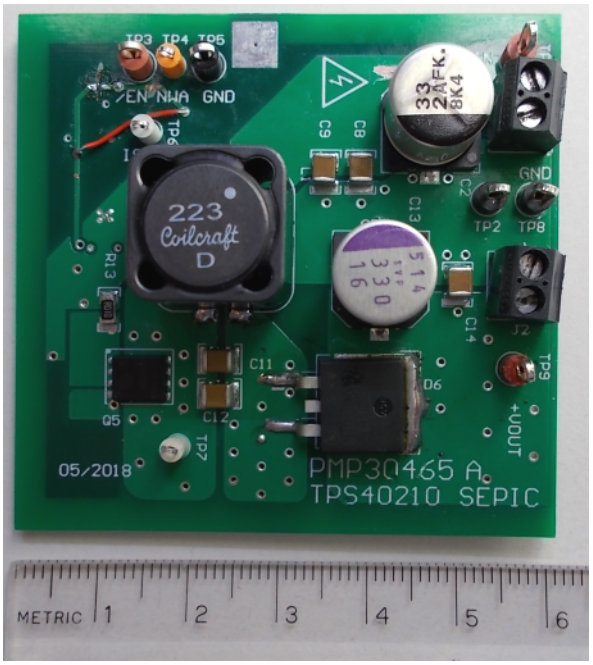
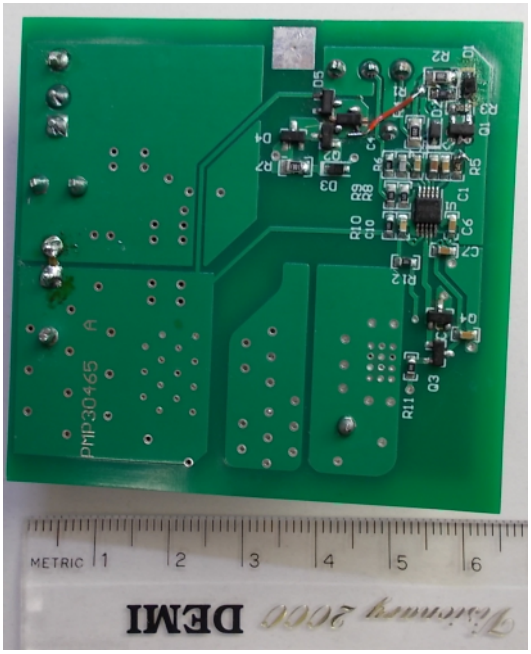
Test Report: PMP30465
30-W SEPIC reference design with extended input voltage range

Description

This reference design is a wide input voltage range SEPIC converter delivering up to 30 W continuous output power; using a cost effective discrete startup circuitry the design is able to be supplied up to 80 V input. Another discrete UVLO circuitry prevents from large input currents at low input voltage. So the power supply is able to handle an input range 1:8. The internal driver of the controller is boosted by a small external push pull stage using bipolar transistors. Using a coupled inductor from stock results in less amount and stress for the flying capacitors .Beside this no additional damping RC network needs to be added here.





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1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1. Voltage and Current Requirements

PARAMETER	SPECIFICATIONS
V_{IN}	10 V-80 V
V_{OUT}	12 V
Nominal switching frequency	200 kHz
Max Output Current	3 A

1.2 Considerations

The switching frequency is about 225 kHz. The circuit switches on at 9.2 V and off at 8.5 V. Unless otherwise mentioned a resistor was used as load. The output current was adjusted to 3A.

2 Testing and Results

2.1 Efficiency Graphs

Figure 1. Efficiency cs Load Current

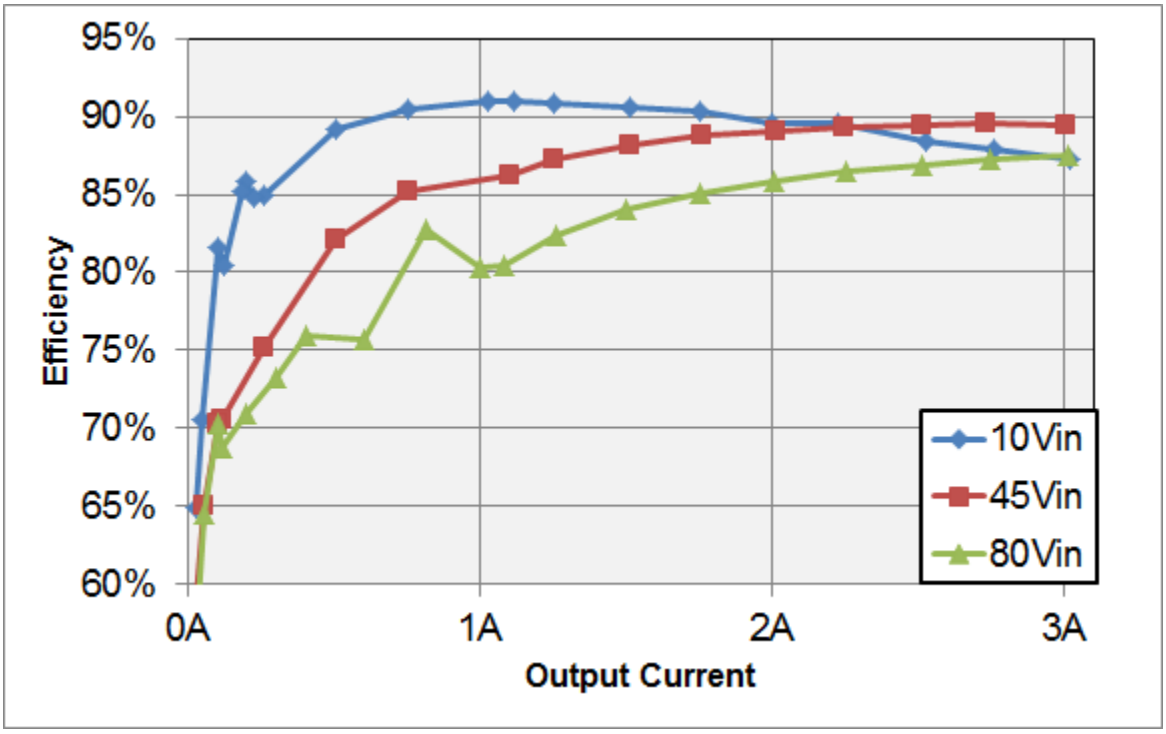
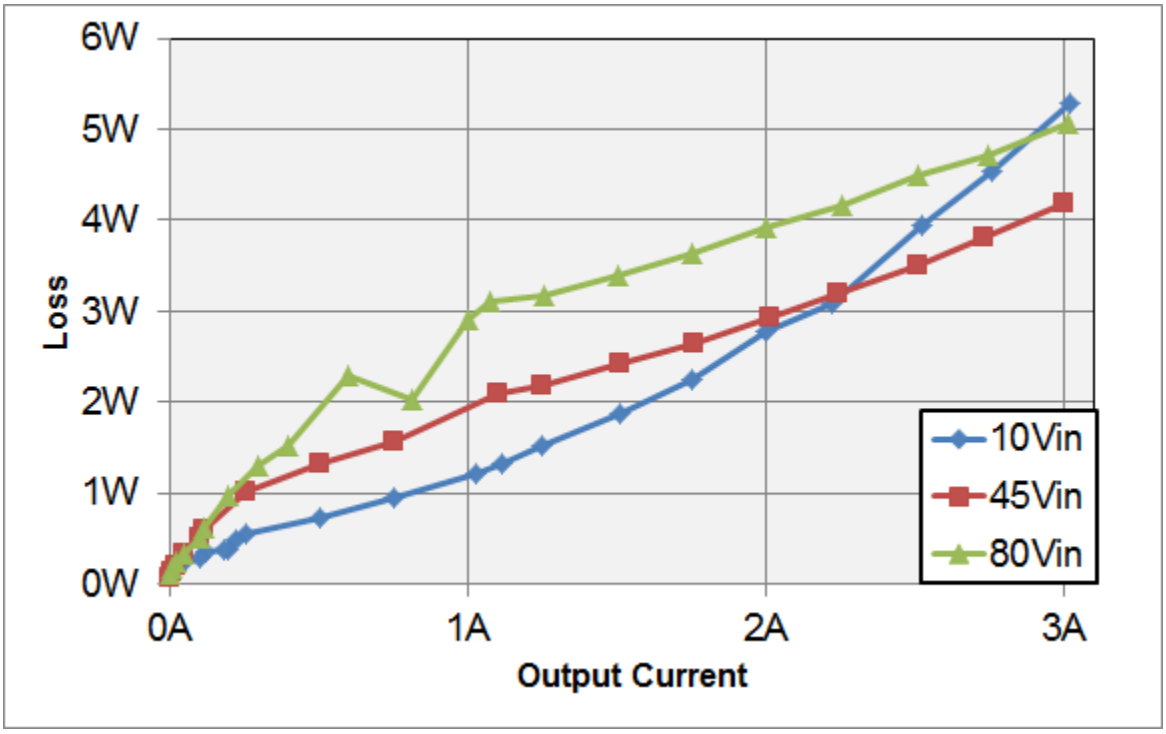
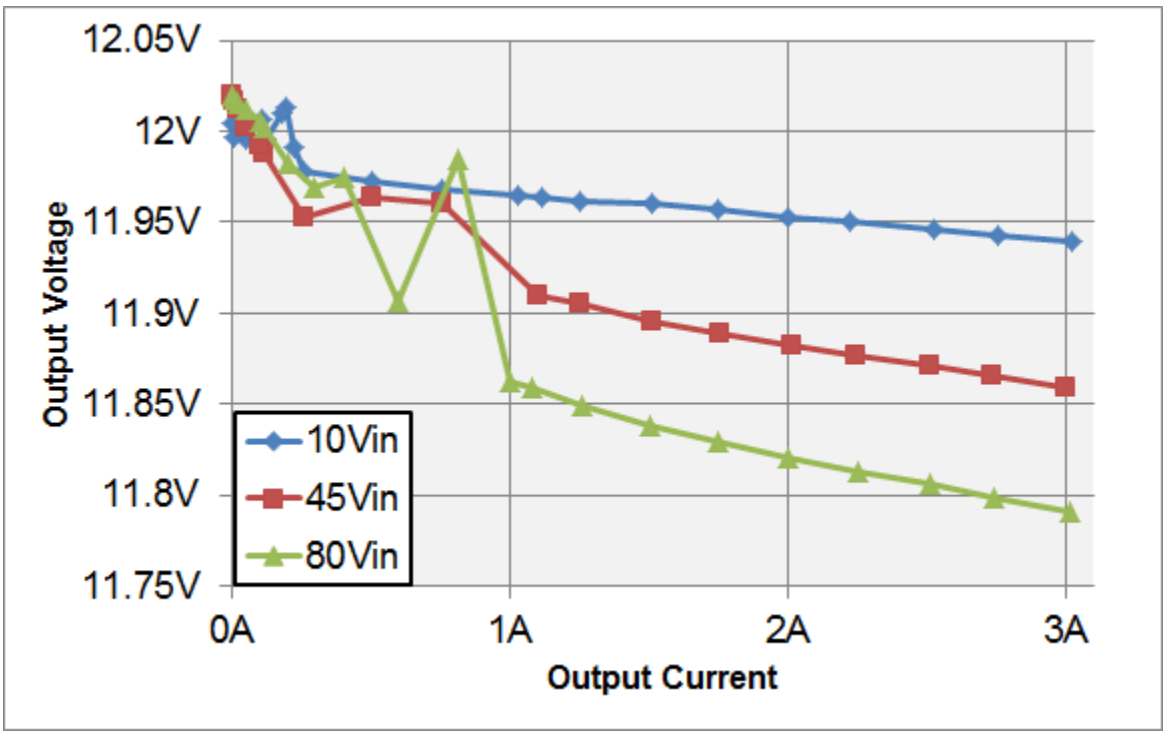


Figure 2. Loss vs Output Current



2.2 Load Regulation

Figure 3. Output Voltage vs Output Current



2.3 Line Regulation

Figure 4. Output Voltage vs Input Voltage

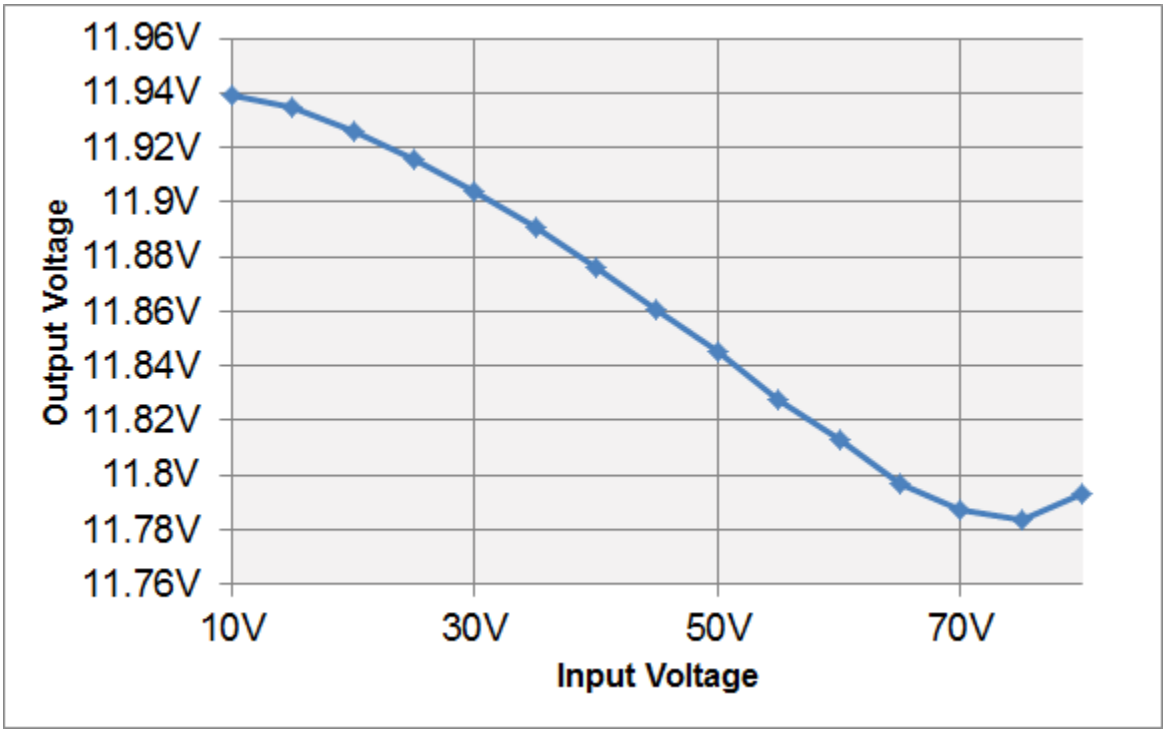
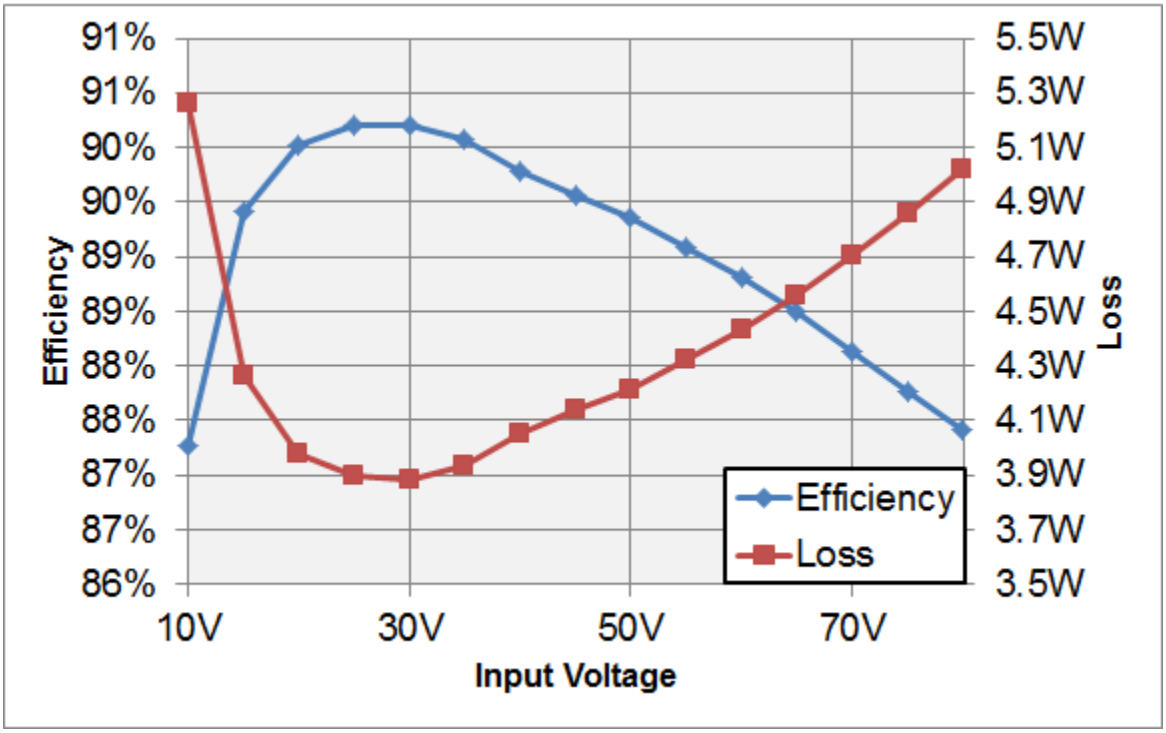
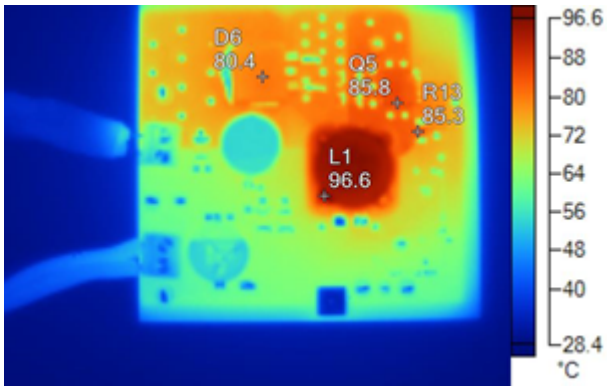


Figure 5. Efficiency and Loss vs Input Voltage



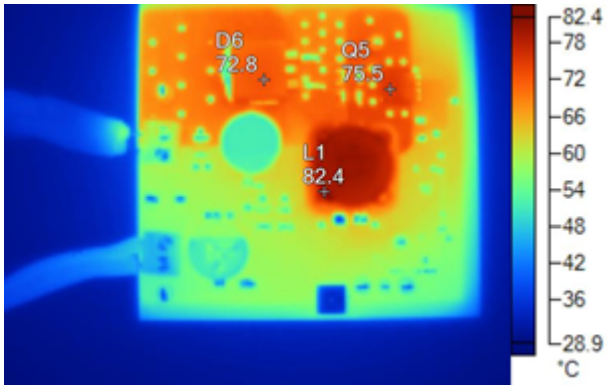
2.4 Thermal Images

Figure 6. Thermal Image of 10 V Input Voltage and 3 A Output Voltage



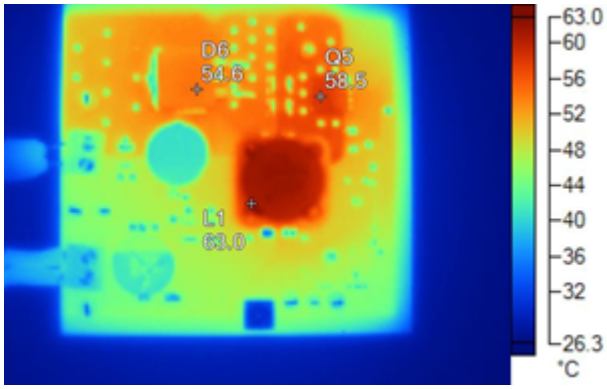
Name	Temperature
D6	80.4° C
L1	96.6° C
Q5	85.8° C
R13	85.3° C

Figure 7. Thermal Image of 45 V Input Voltage and 3 A Output Voltage



Name	Temperature
D6	72.8° C
L1	82.4° C
Q5	75.5° C

Figure 8. Thermal Image of 45 V Input Voltage and 2 A Output Voltage



Name	Temperature
D6	54.6° C
L1	63.0 °C
Q5	58.5° C

Figure 9. Thermal Image of 45 V Input Voltage and 1 A Output Voltage

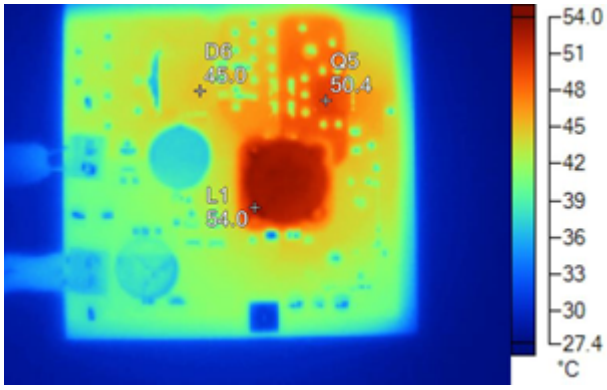
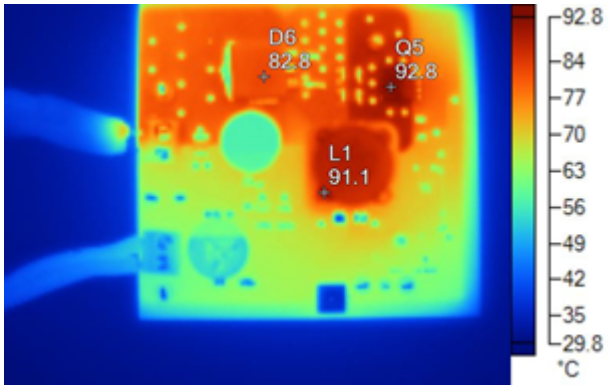


Figure 10. Thermal Image of 80 V Input Voltage and 3 A Output Voltage



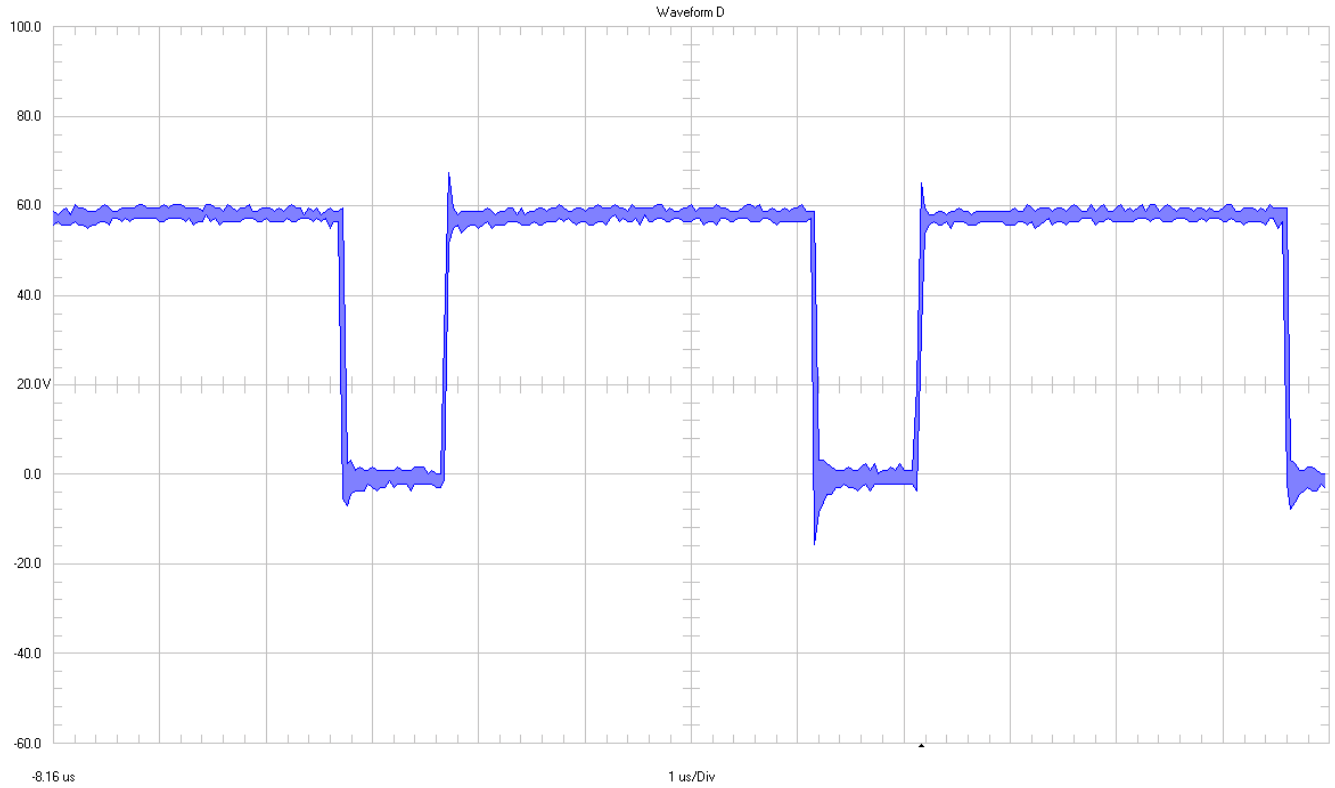
Name	Temperature
D6	82.8° C
L1	91.1° C
Q5	92.8° C

3 Waveforms

3.1 Switch Node Q5

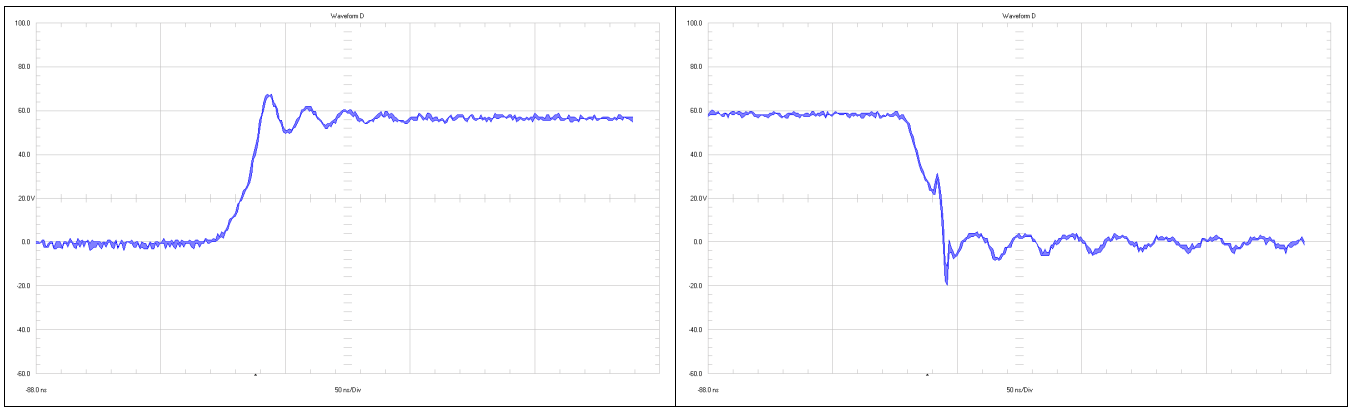
Waveform below shows the switch node voltage measured at 45 V input voltage from Q5 drain to GND

Figure 11. Switchnode at 45 V Input Voltage



20 V/div (full bandwidth)

1 µs/div

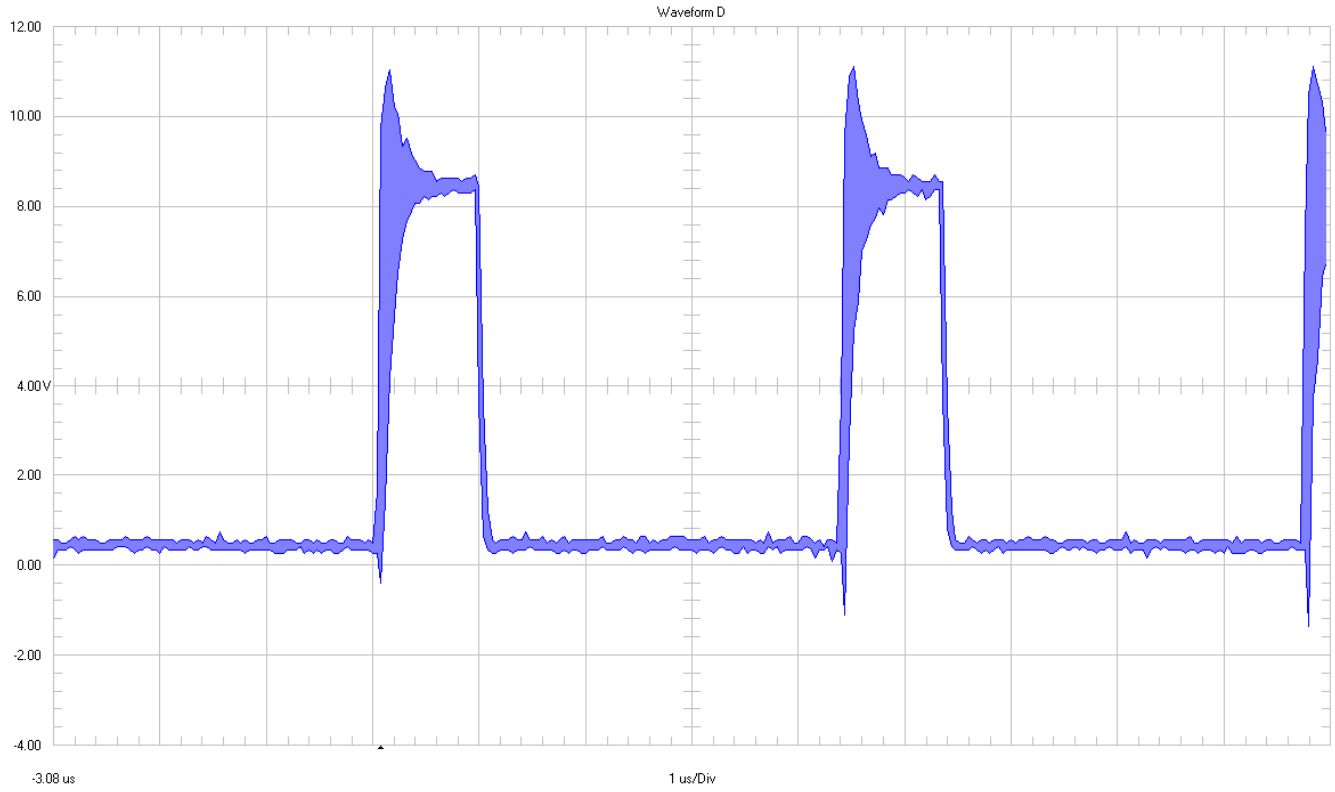


20V/div; 50ns/ major div

3.2 Q5 Gate

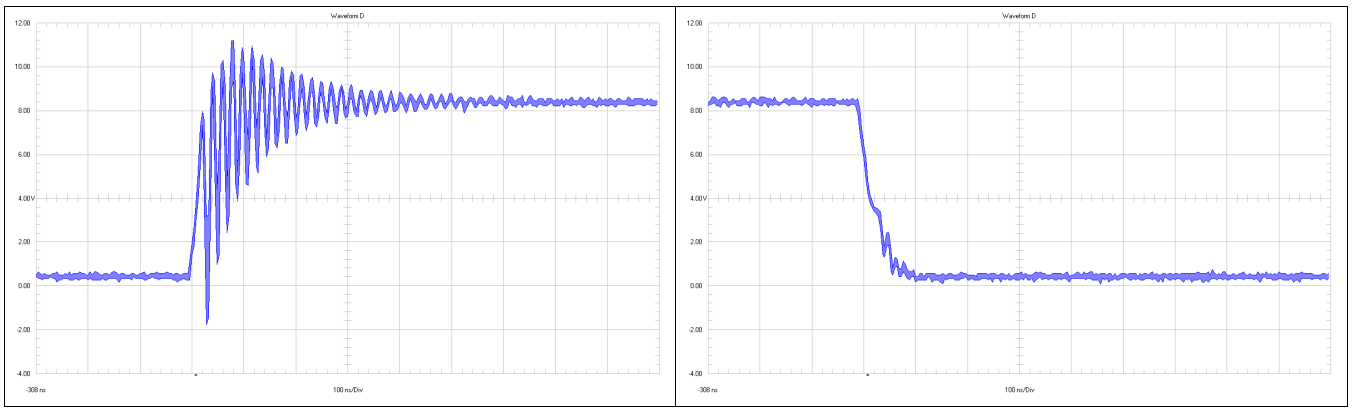
The waveform below shows the voltage measured from Q5 gate to GND

Figure 12. Gate at 45 V Input Voltage



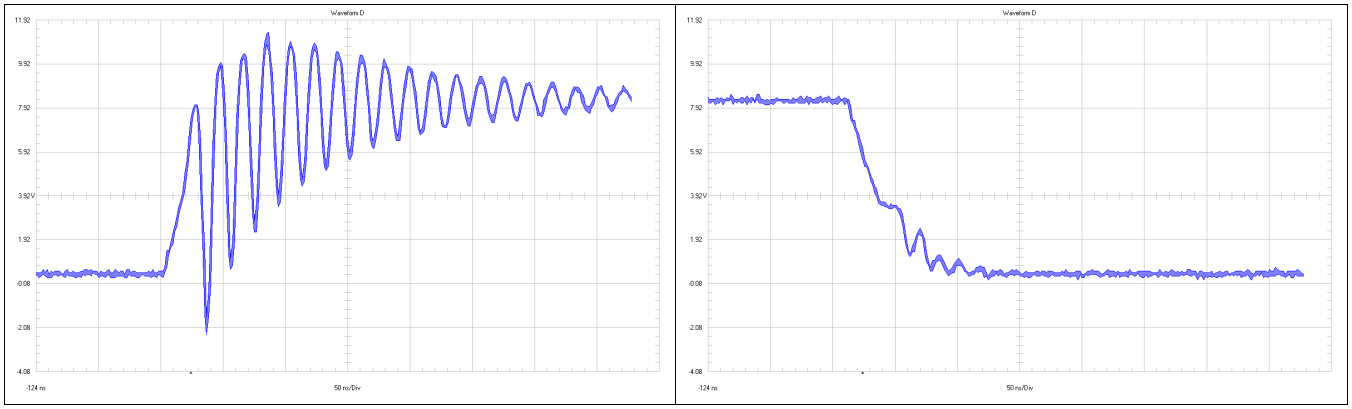
2 V/div (full bandwidth); 1µs/Div

Below is the same waveform with a different time axis.



100 ns/div

Below is the same waveform with a different time axis.

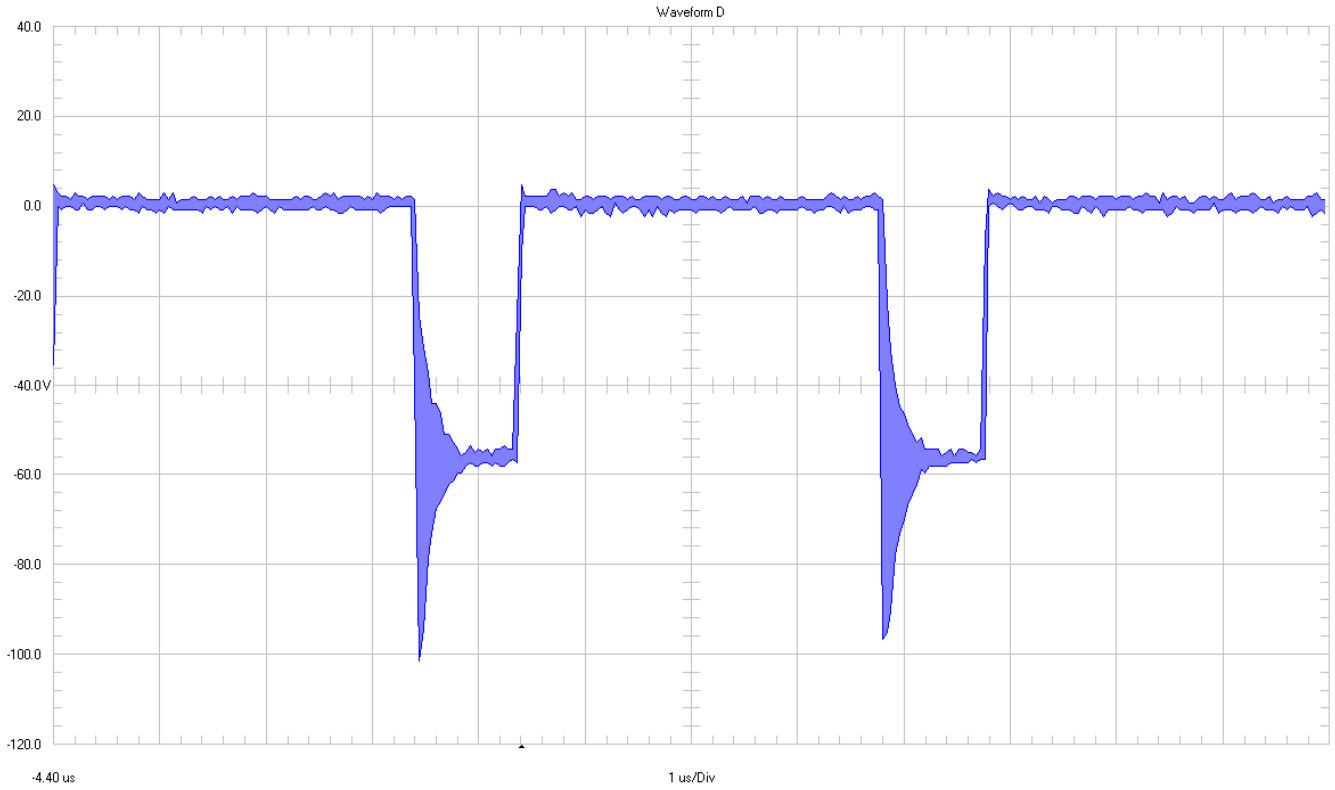


50 ns/div

3.3 Diode D6

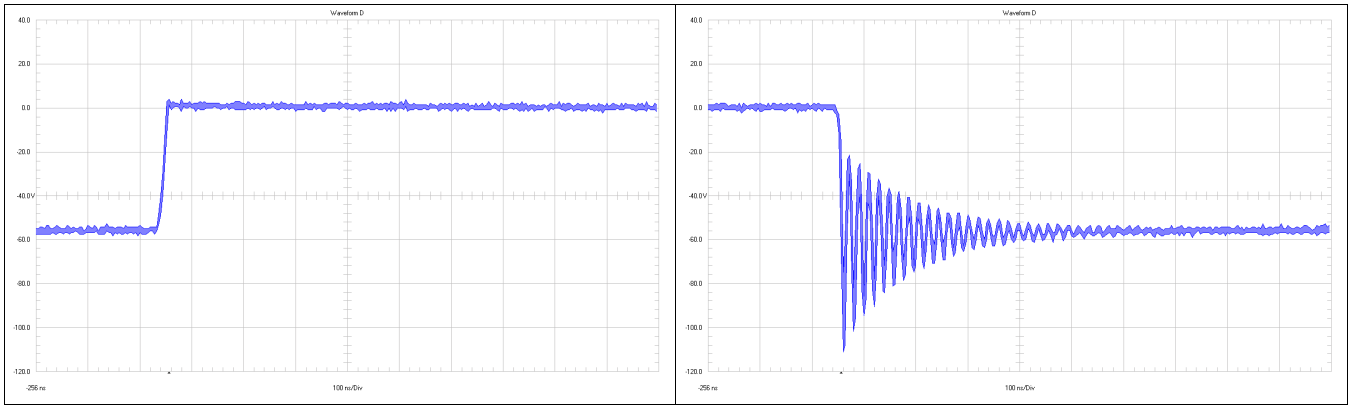
The waveform below are showing the voltage at the diode D6 referenced to VOUT.

Figure 13. Diode D6 with 45 V Input Voltage



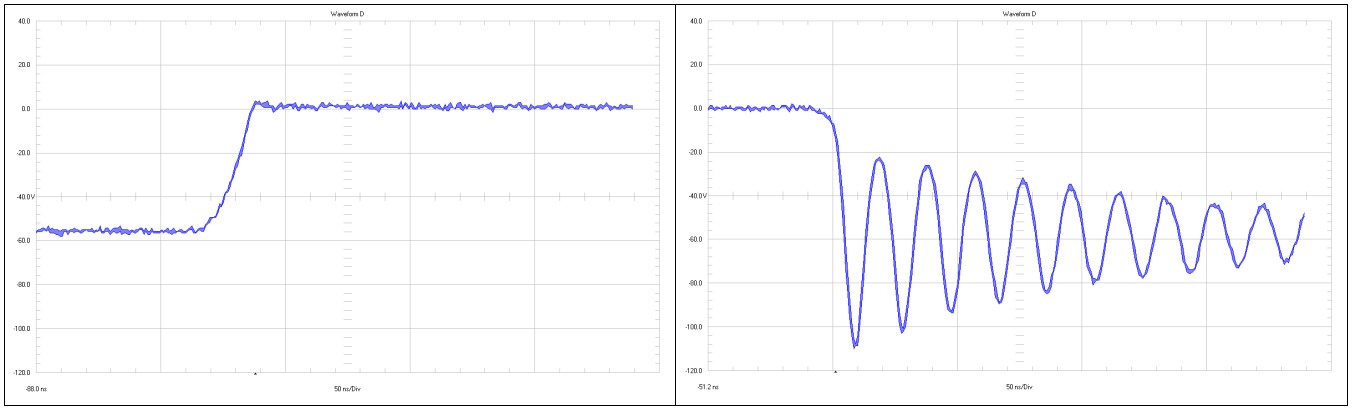
20 V/div (full bandwidth); 1 µs/div

Below there is the same waveform with a different time axis.



100 ns/div

Below there is the same waveform with different time axis.



50ns/di

3.4 Output Voltage Ripple

Below are the waveforms at VOUT at different input voltages. Also the effect of an added 100nF capacitor is shown.

All measurements were done with 20 MHz bandwidth.

3.4.1 10 V Input Voltage

Figure 14. VOUT at 10 V Input Voltage

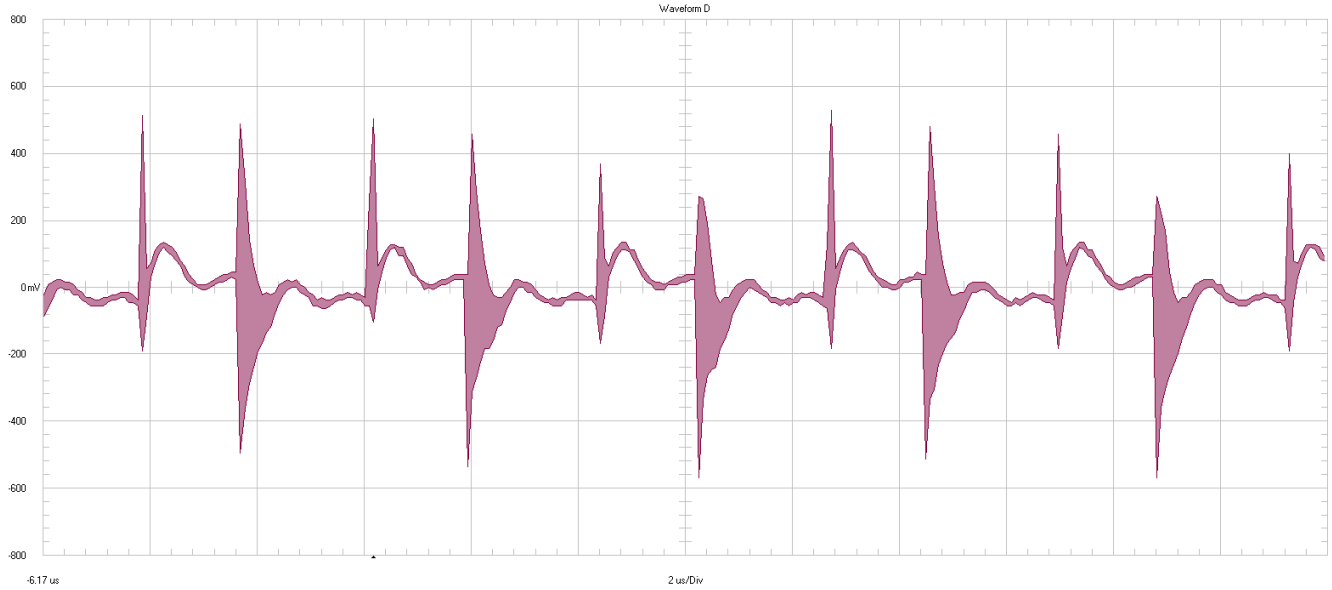
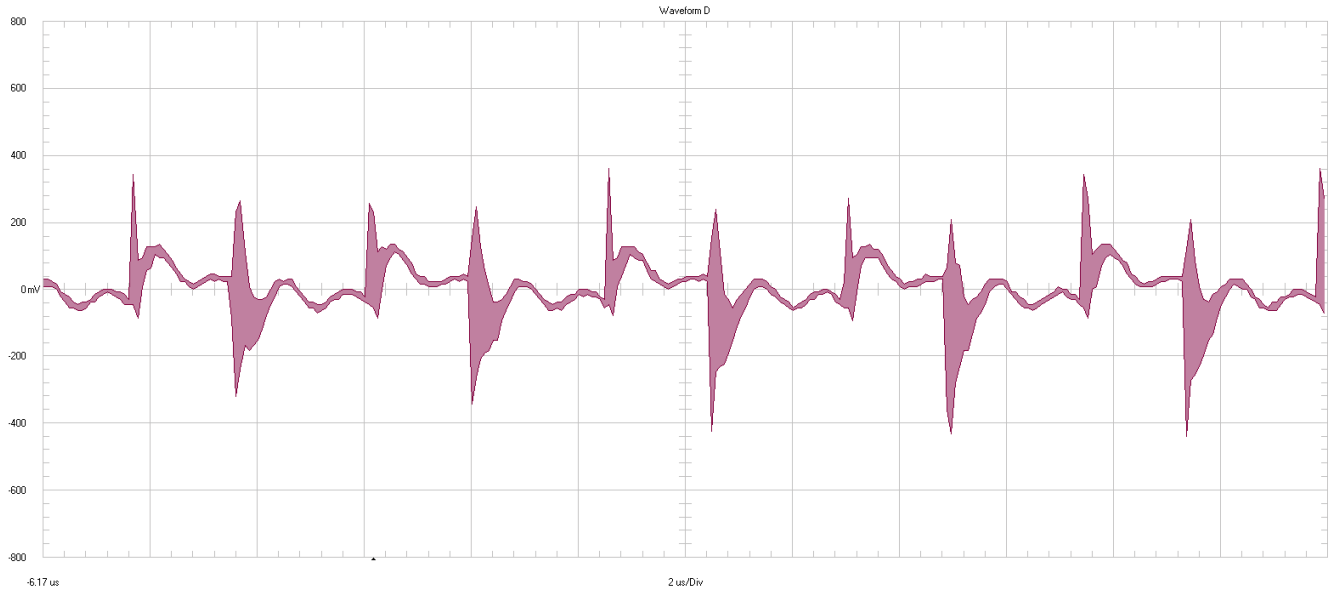


Figure 15. VOUT at 10 V Input Voltage and a Added 100nF Capacitor at VOUT



200mV/div (AC, 20MHz bandwidth setting)

2µs/div

3.4.2 45V Input Voltage

Figure 16. VOUT at 45 V Input Voltage

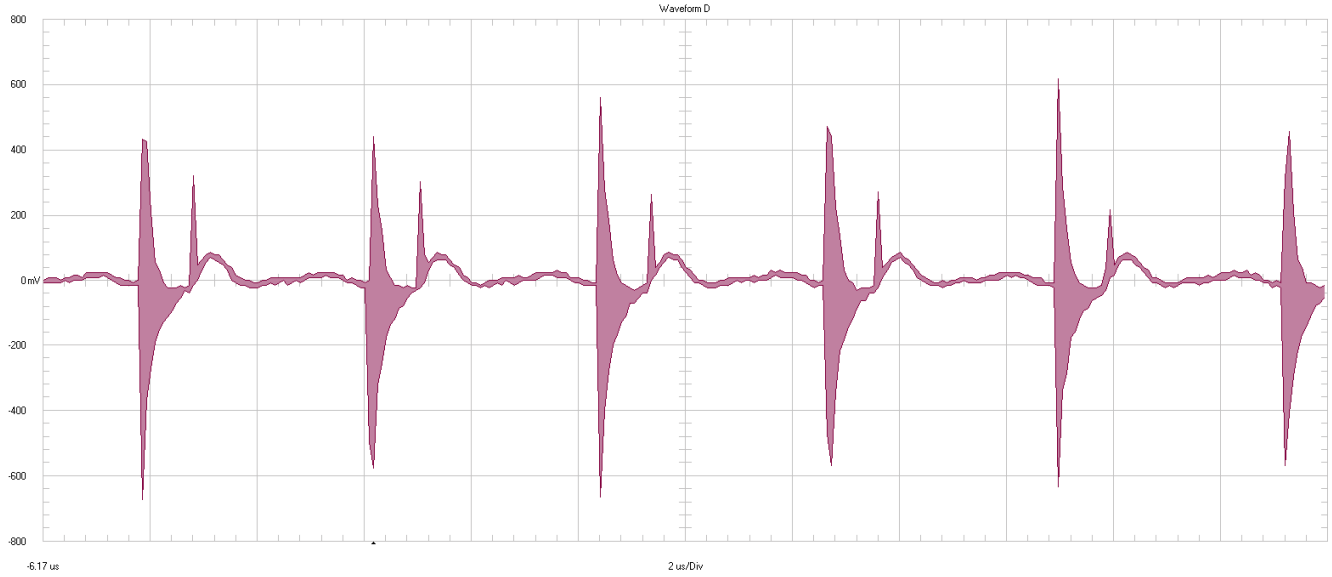
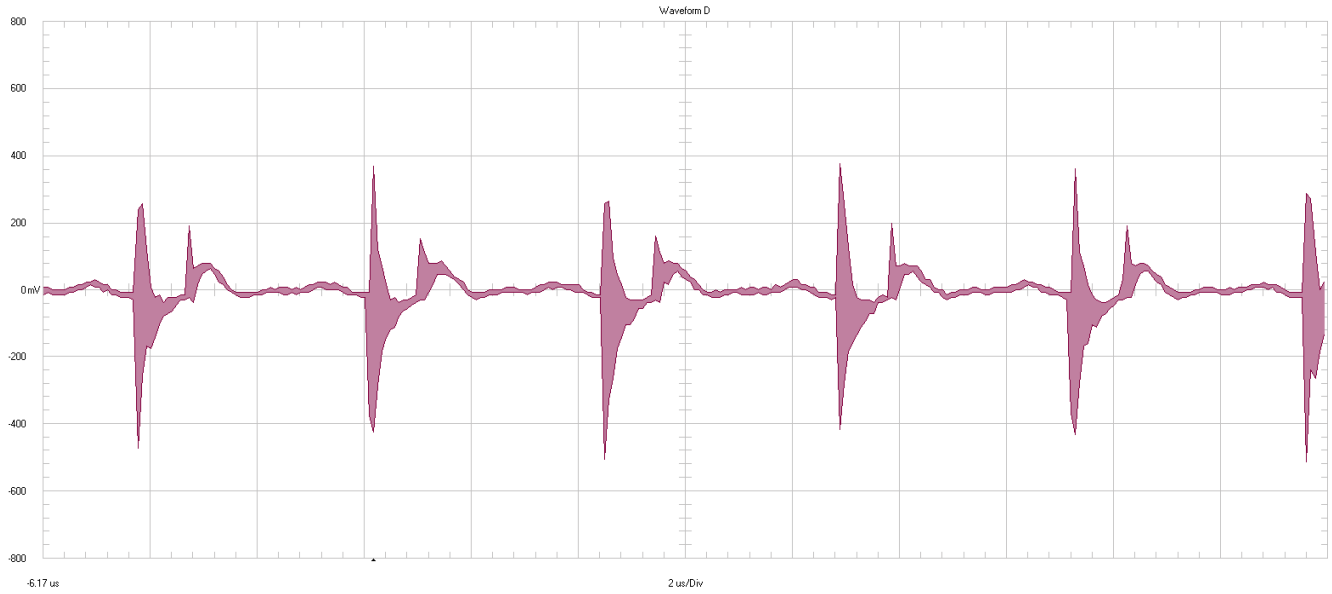


Figure 17. VOUT at 45 V Input Voltage and a Added 100nF Capacitor at VOUT



3.4.3 80 V Input Voltage

Figure 18. VOUT at 80 V Input Voltage

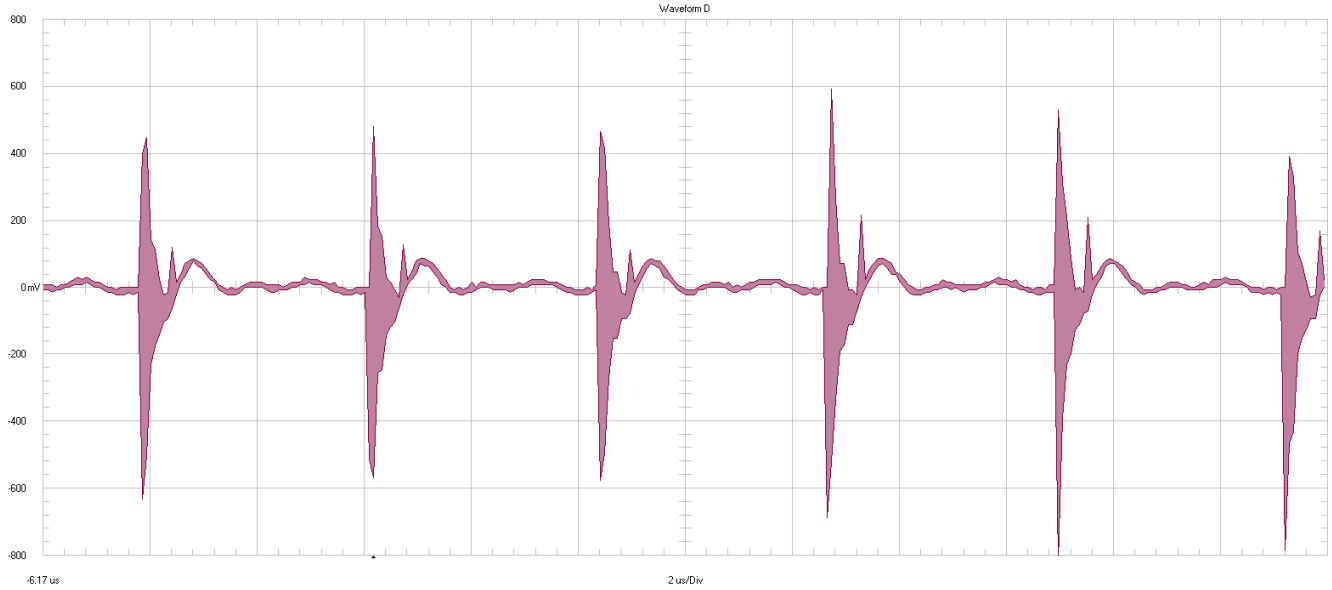
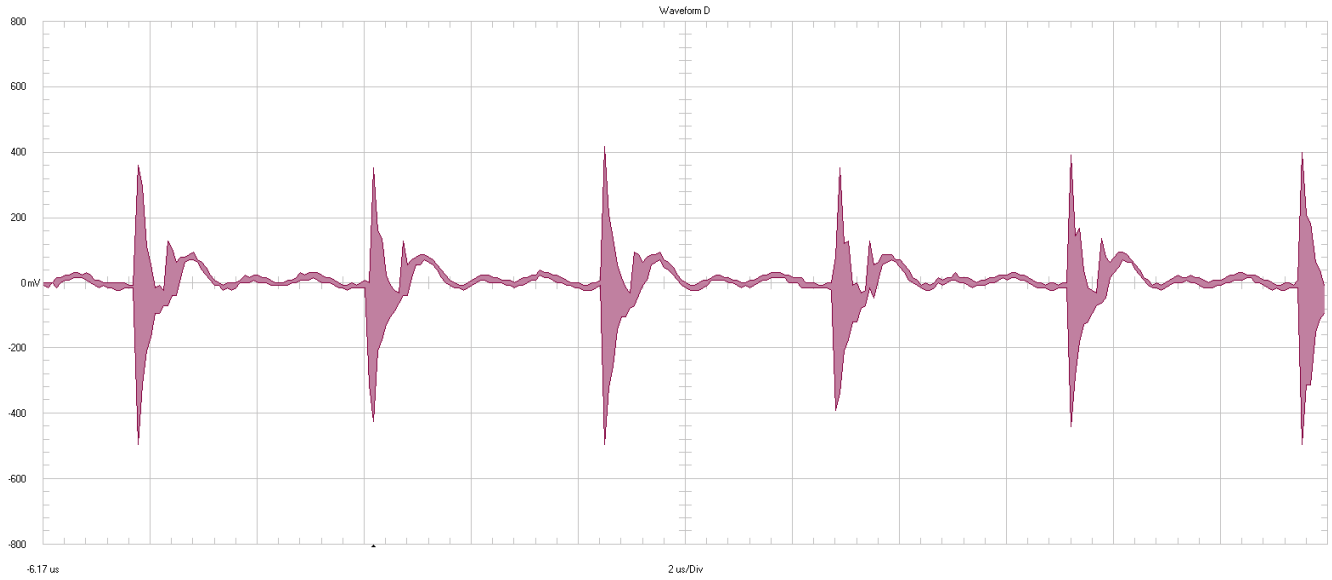


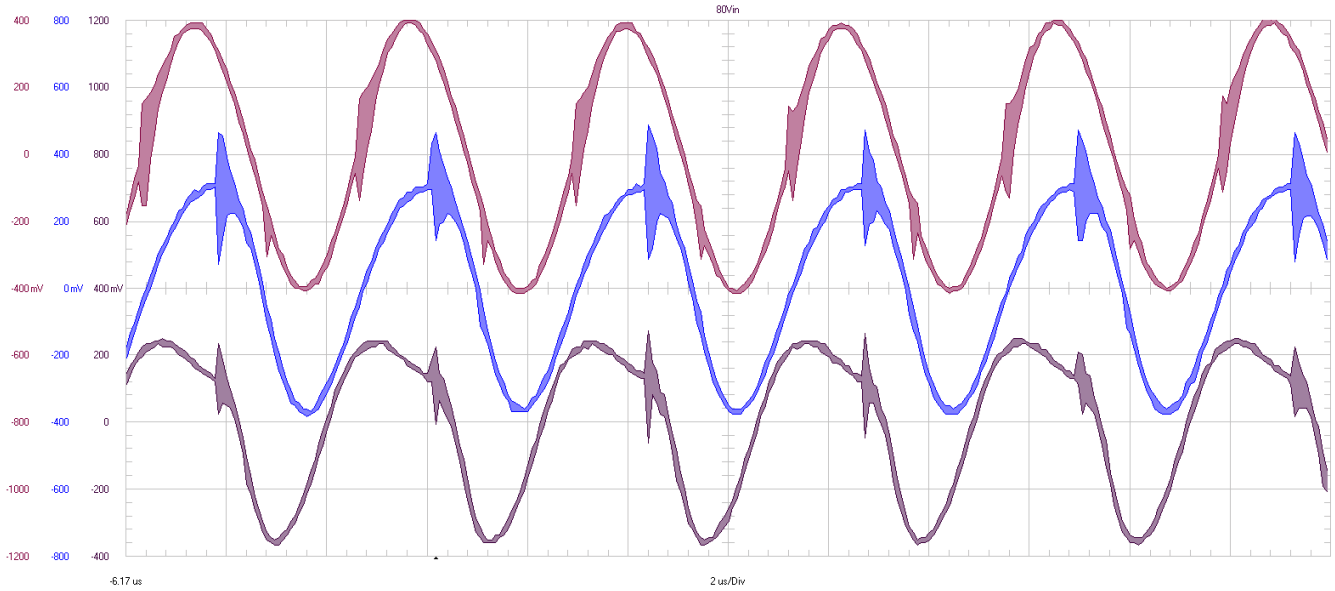
Figure 19. VOUT at 80 V Input Voltage and a Added 100 nF Capacitor at VOUT



3.5 Input Voltage

Measured with 20MHz bandwidth (AC)

Figure 20. VIN at 10 V, 45 V and 80 V Input Voltage



channel 1 (red) 10 V input voltage -> 200mV/div; 2µs/div

channel 2 (blue) 45 V input voltage -> 200mV/div; 2µs/div

channel 3 (dark red) 80 V input voltage -> 200mV/div; 2µs/div

3.6 Bode Plot

Figure 21. Loop Response @ 10 V Input Voltage

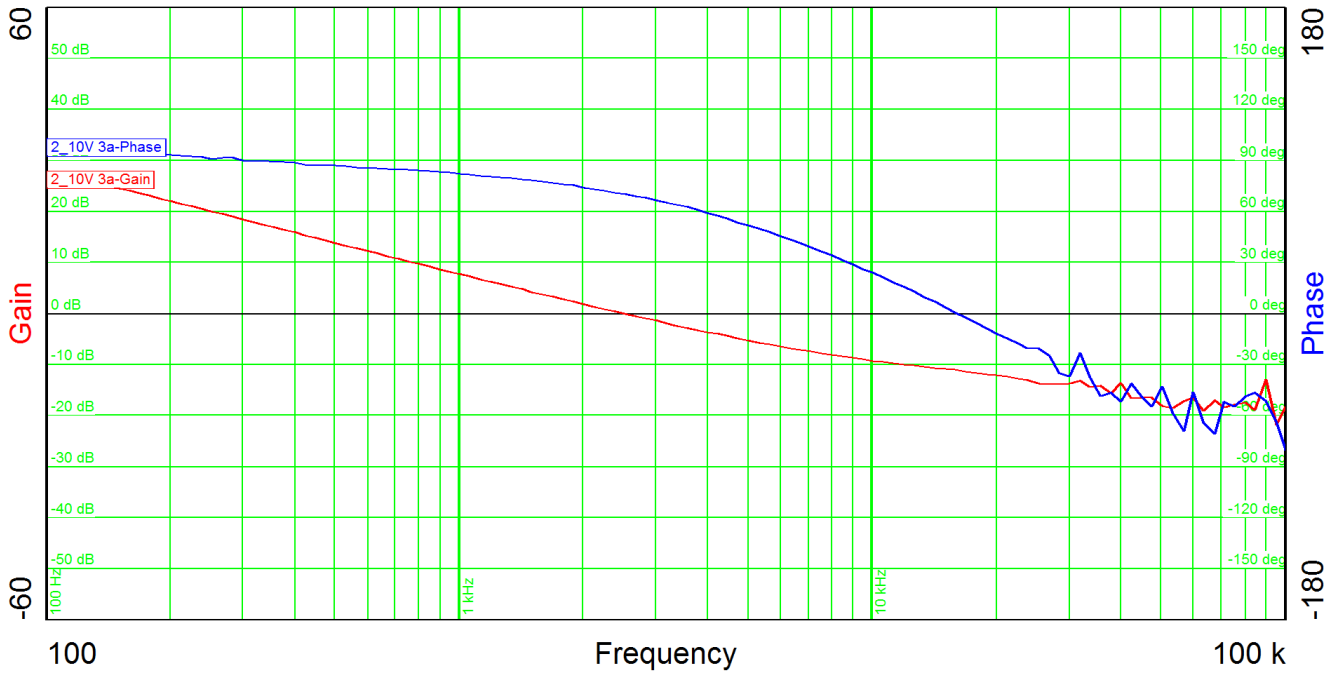
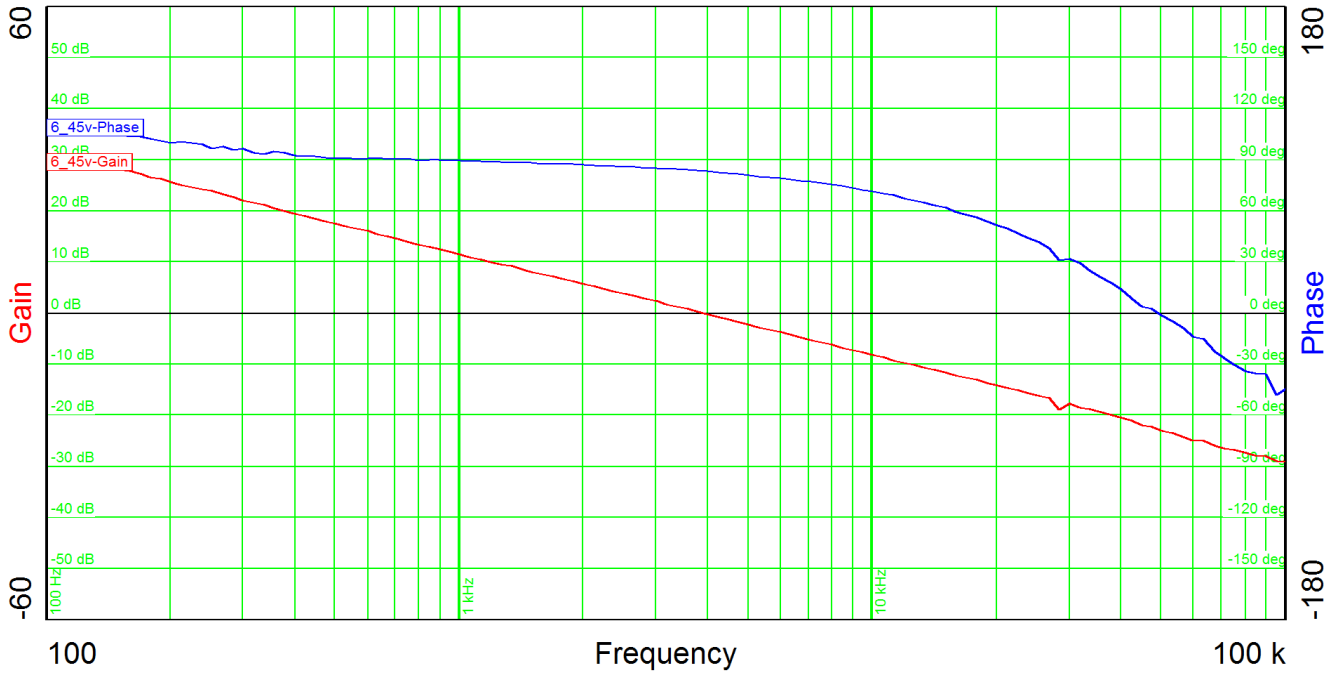


Figure 22. Loop Response @ 45 V Input Voltage

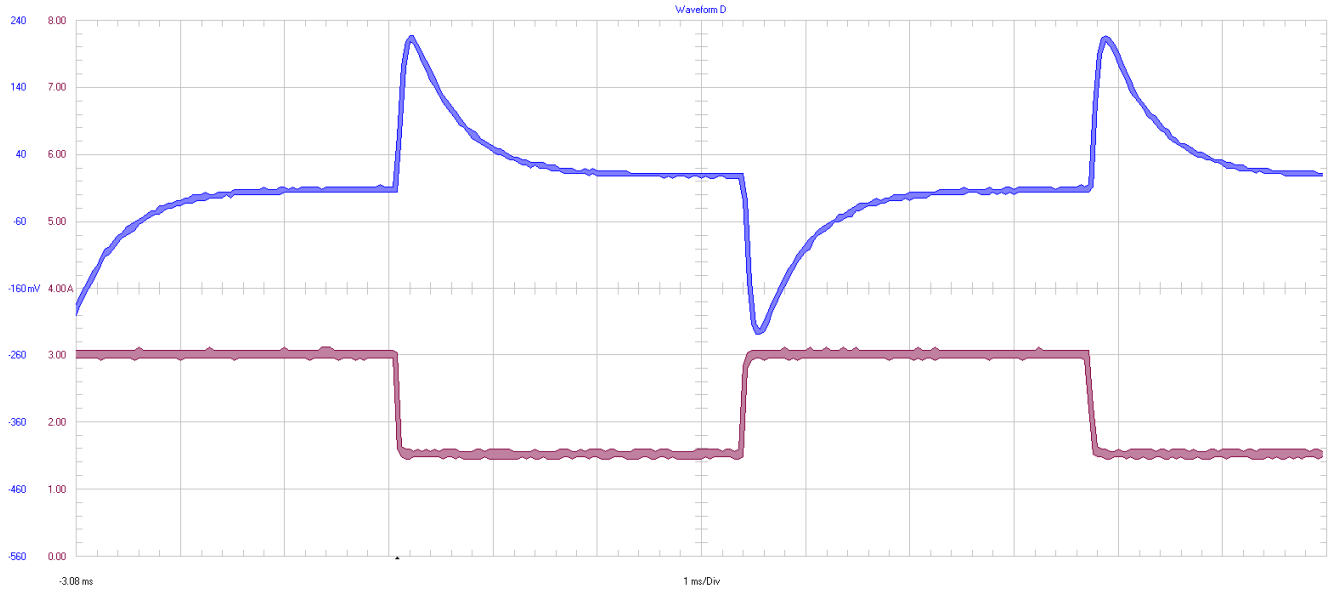


Vin	10 V	45 V
Bandwidth (kHz)	2.5	3.9
Phase Margin	70	83
slope (20dB/decade)	0.95	0.99
gain margin (dB)	-11.1	-22.7
slope (20 dB/decade)	-0.58	-1.2
freq (kHz)	16	49

3.7 Load Transients

The electronic load was switching from 1.5 A to 3 A with a frequency of 150 Hz.

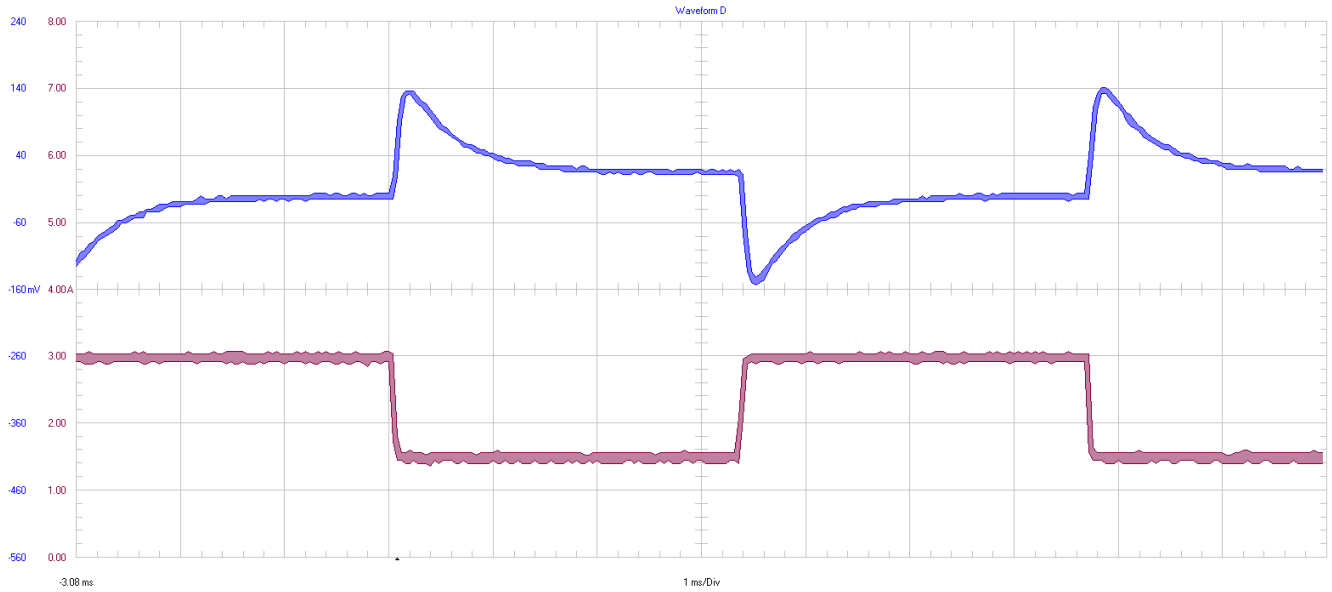
Figure 23. Transient @ 10V Input Voltage



channel 1: Output Voltage (10 kHz bandwidth) -> 100mV/div; 1ms/div

channel 2: Output Current (20 MHz bandwidth) -> 1A/div; 1ms/div

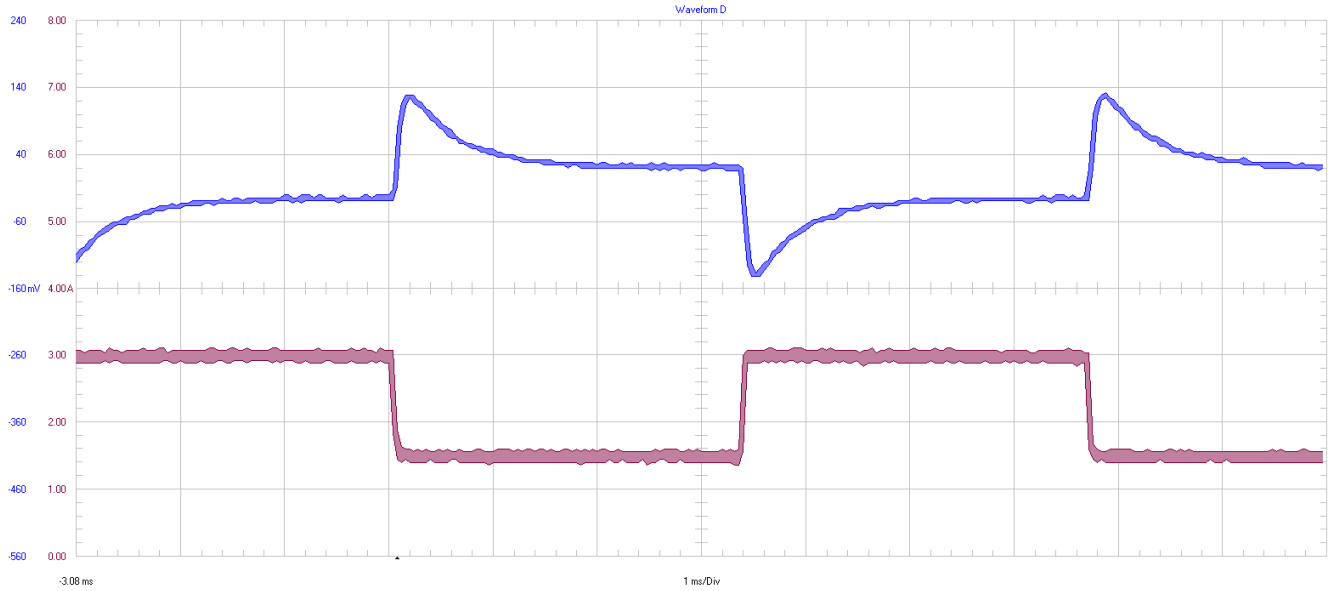
Figure 24. Transient @ 45 V Input Voltage



channel 1: Output Voltage (10kHz bandwidth) -> 100mV/div; 1ms/div

channel 2: Output Current (20MHz bandwidth) -> 1A/div; 1ms/div

Figure 25. Transient @ 80 V Input Voltage



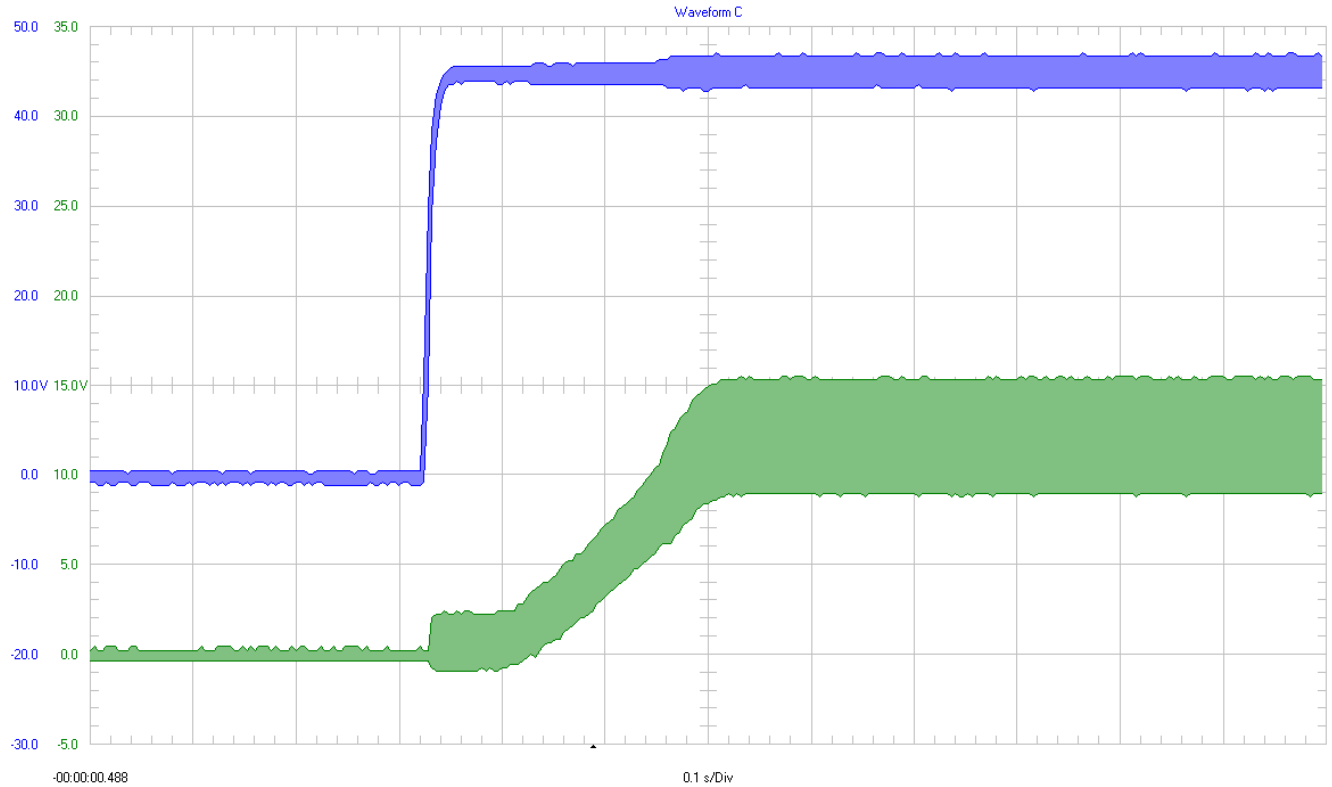
channel 1: Output Voltage (10 kHz bandwidth) -> 100mV/div; 1ms/div

channel 2: Output Current (20 MHz bandwidth) -> 1A/div; 1ms/div

3.8 Start-up Sequence

The power supply was switched on.

Figure 26. Start-up @ 45V Input Voltage



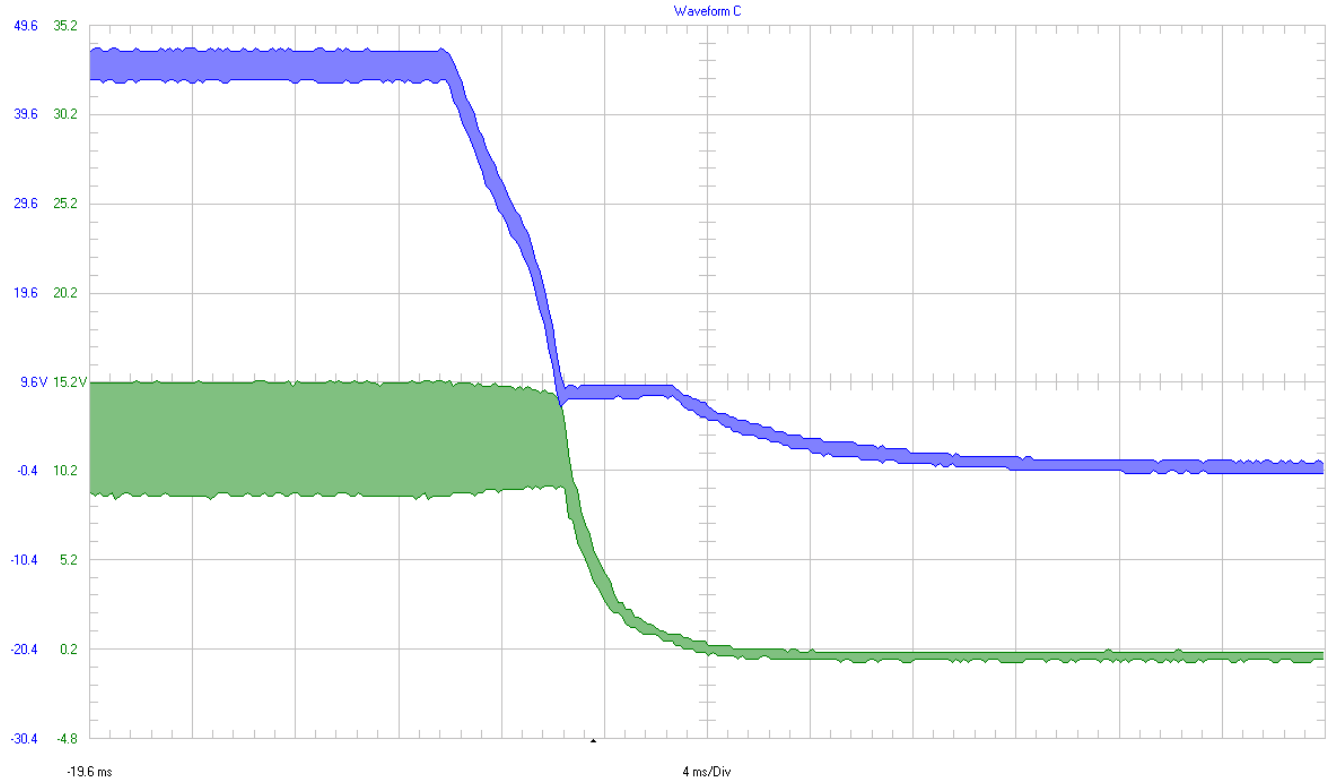
channel 1: input voltage -> 10 V/div; 0.1s

channel 2: output voltage -> 5 V/div;0.1s

3.9 Shut-down

The power supply was switched off.

Figure 27. Shut-down @ 45 V Input Voltage

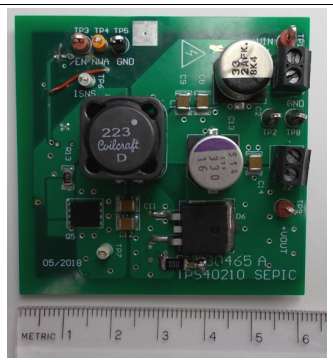


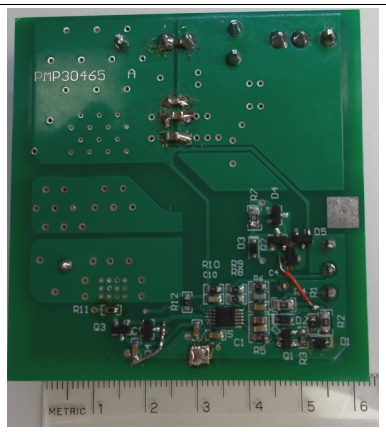
channel 1: input voltage -> 10V/div; 4ms/div
channel 2: output voltage -> 5V/div ; 4ms/div

4 Addendum

For improving the EMI behaviour did following modifications

- improved GND-connection of the gate-driver circuit
- changed gate resistor from 10R to 33.2R (R11)
- added snubber to rectifier (D6)
- added MLCCs to VOUT





The following subsections are some details.

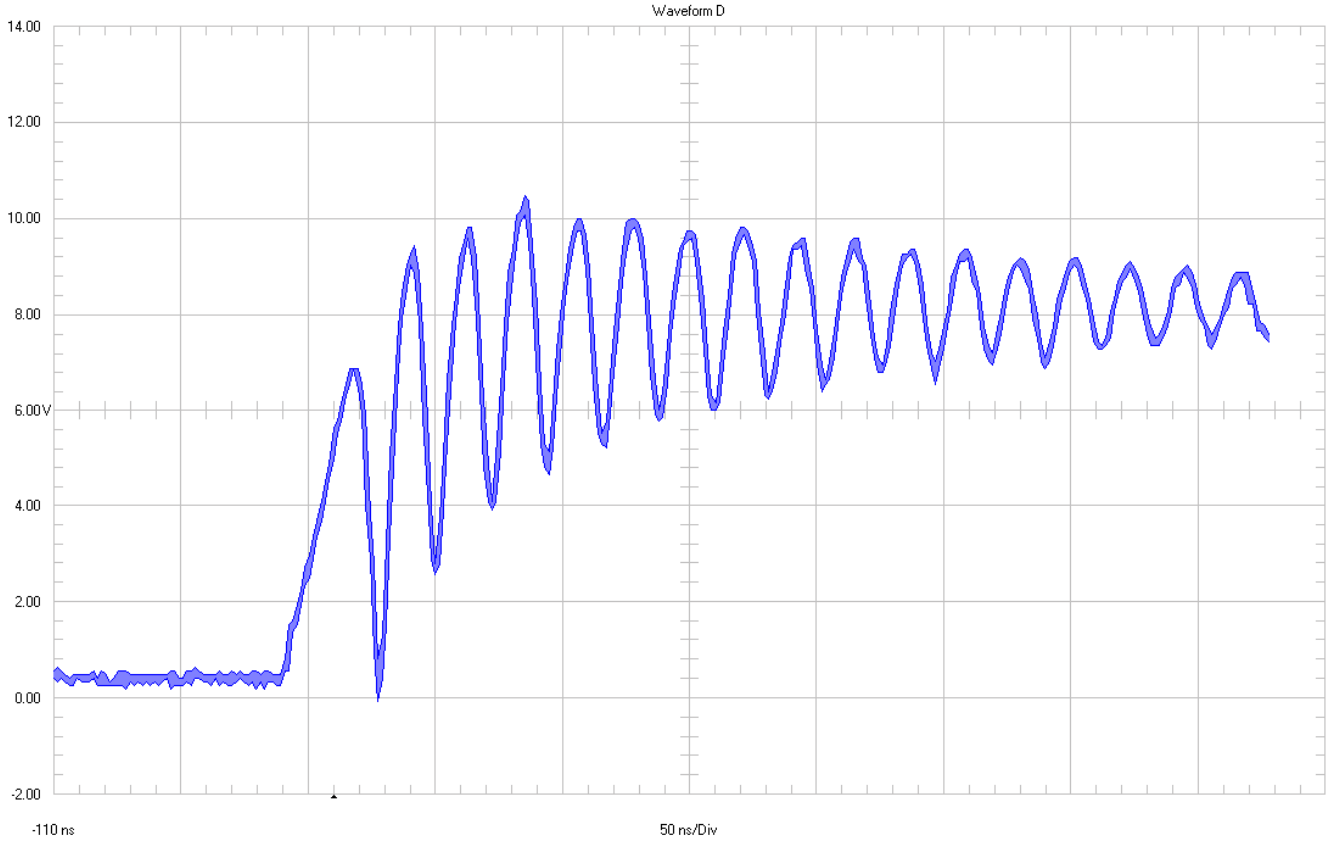
4.1 Gate Resistor

The following measurements were done with 20 V input voltage

4.1.1 Gate Resistor = 10R

The following picture shows the waveform before any modification

Figure 28. Gate to GND with R11=10R



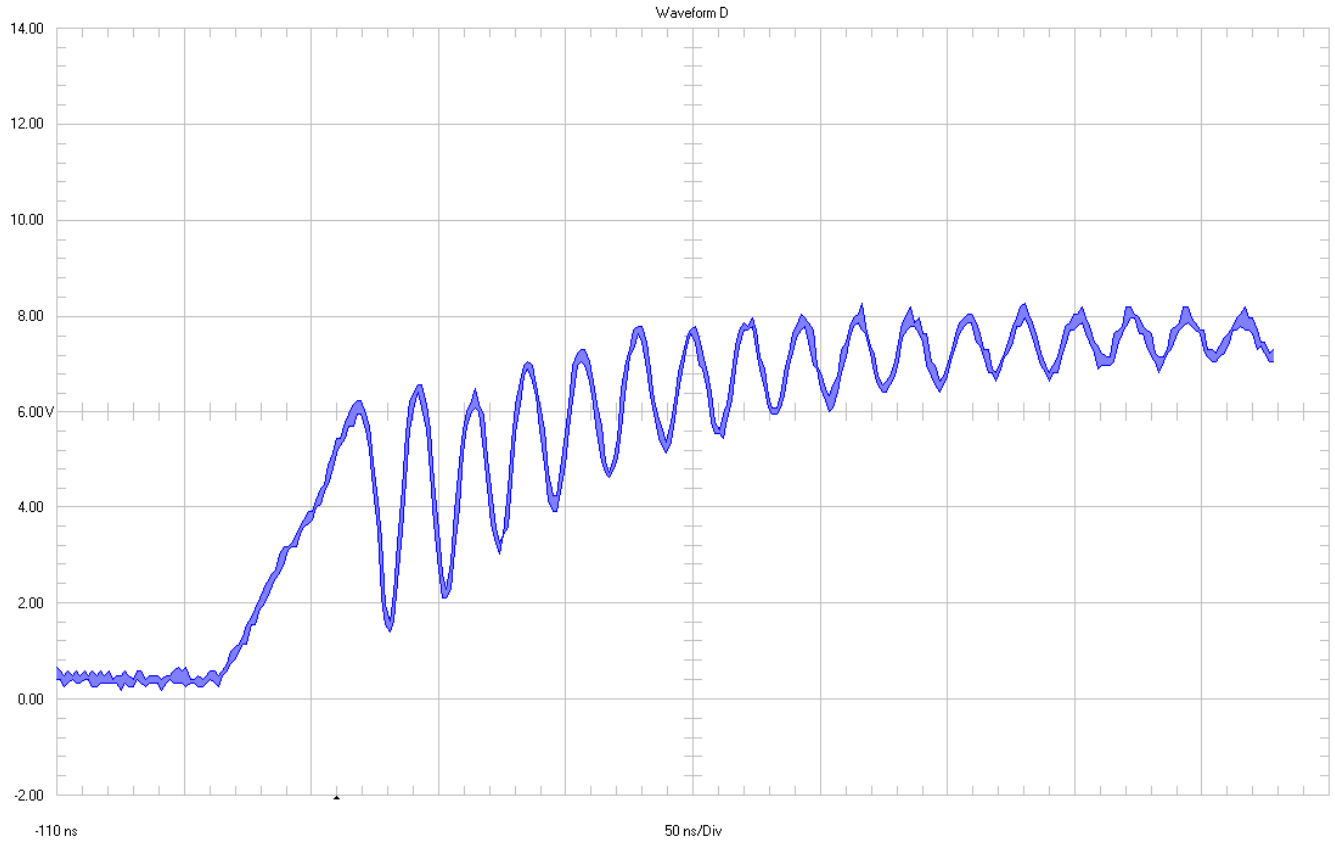
2V /div (full bandwidth)

50ns/div

4.1.2 Gate Resistor = 33.2R

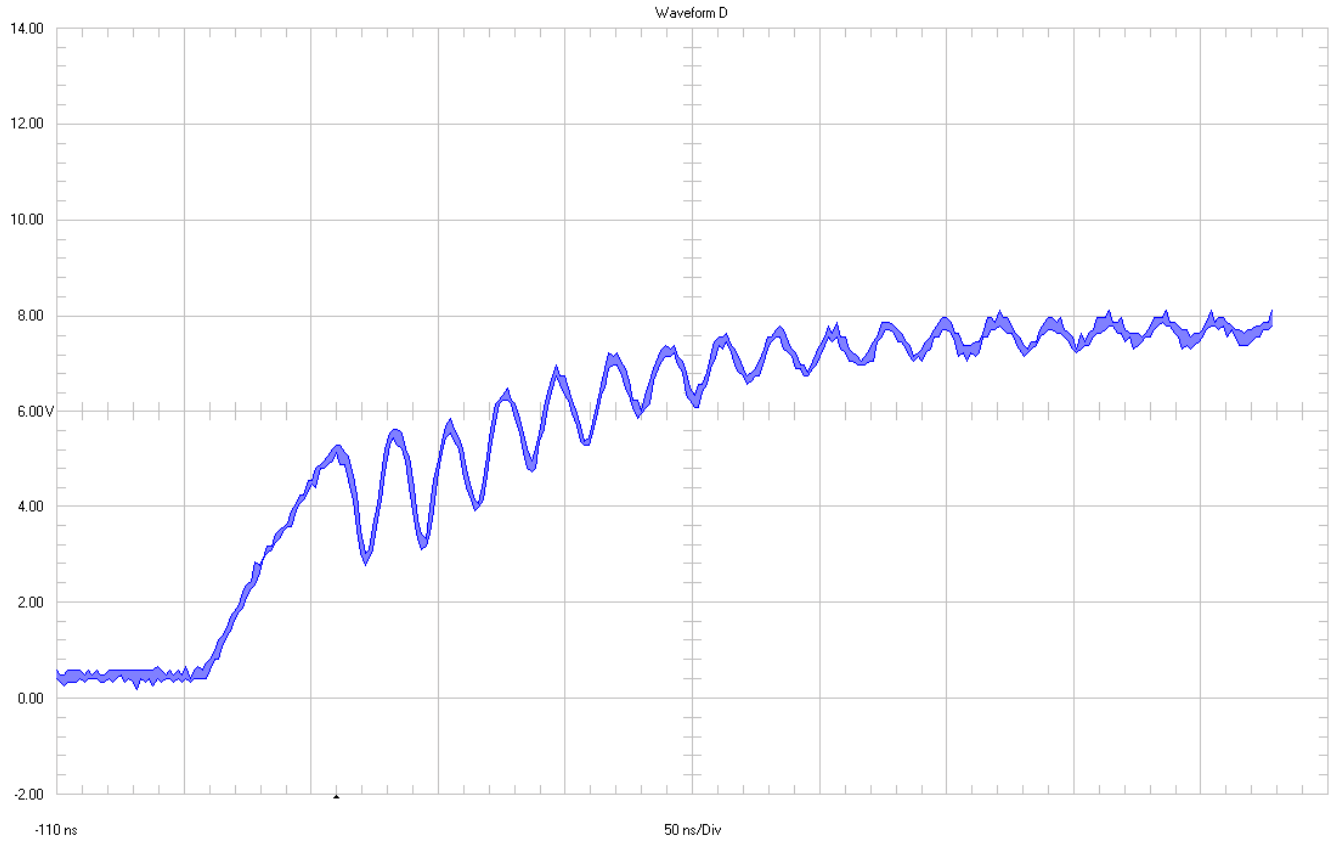
Below there is the waveform with 33.2R gate resistor with the ame settings as above.

Figure 29. Gate to GND with R11=33.2R



Measured from Gate to source is shown in folowing picture (same settings as above).

Figure 30. Gate to Source with R11=33.2R



4.2 Rectifier

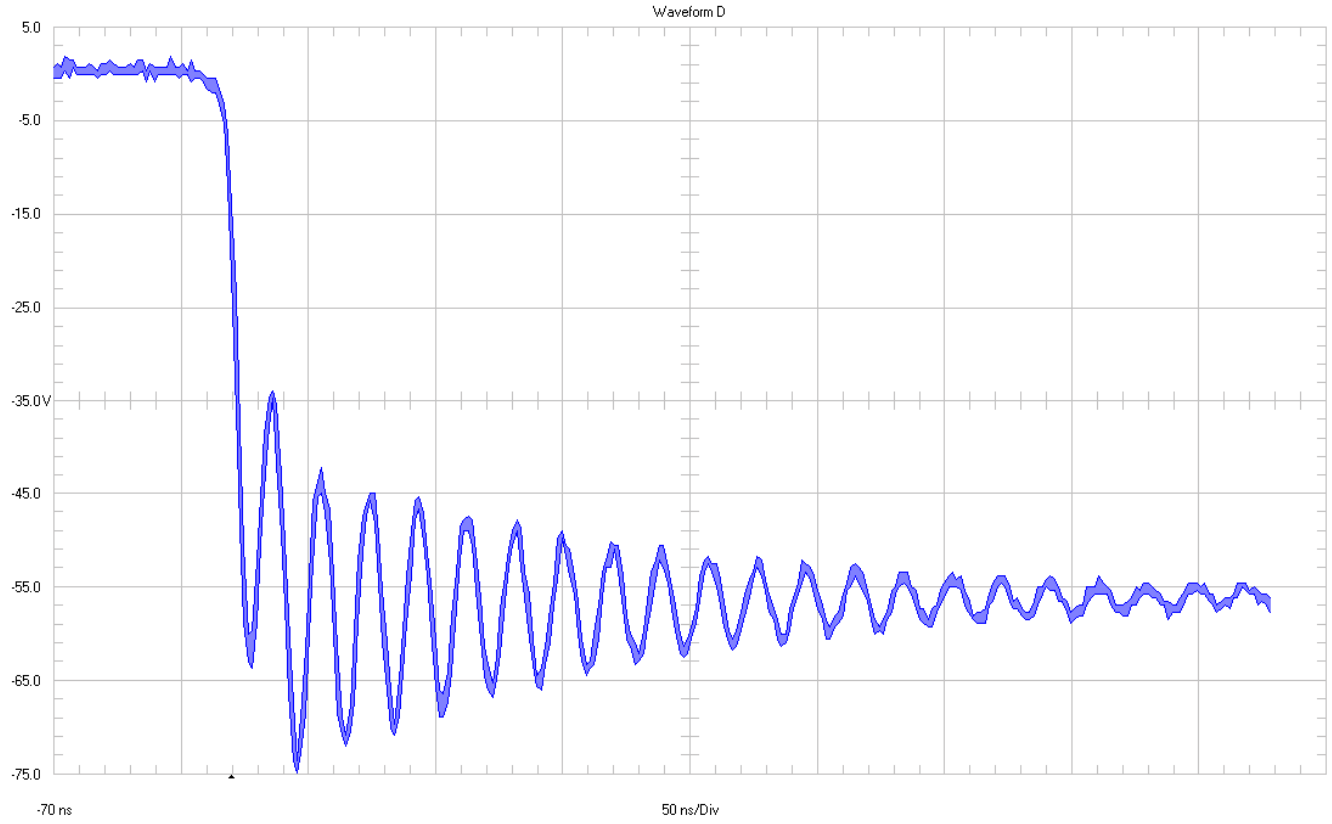
After changing the gate resistor a snubber 10R + 470 pF was added.

The following picture are measured at the rectifier D6 (referenced to VOUT) with following settings.

- 10V/div (full bandwidth)
- 50ns/div

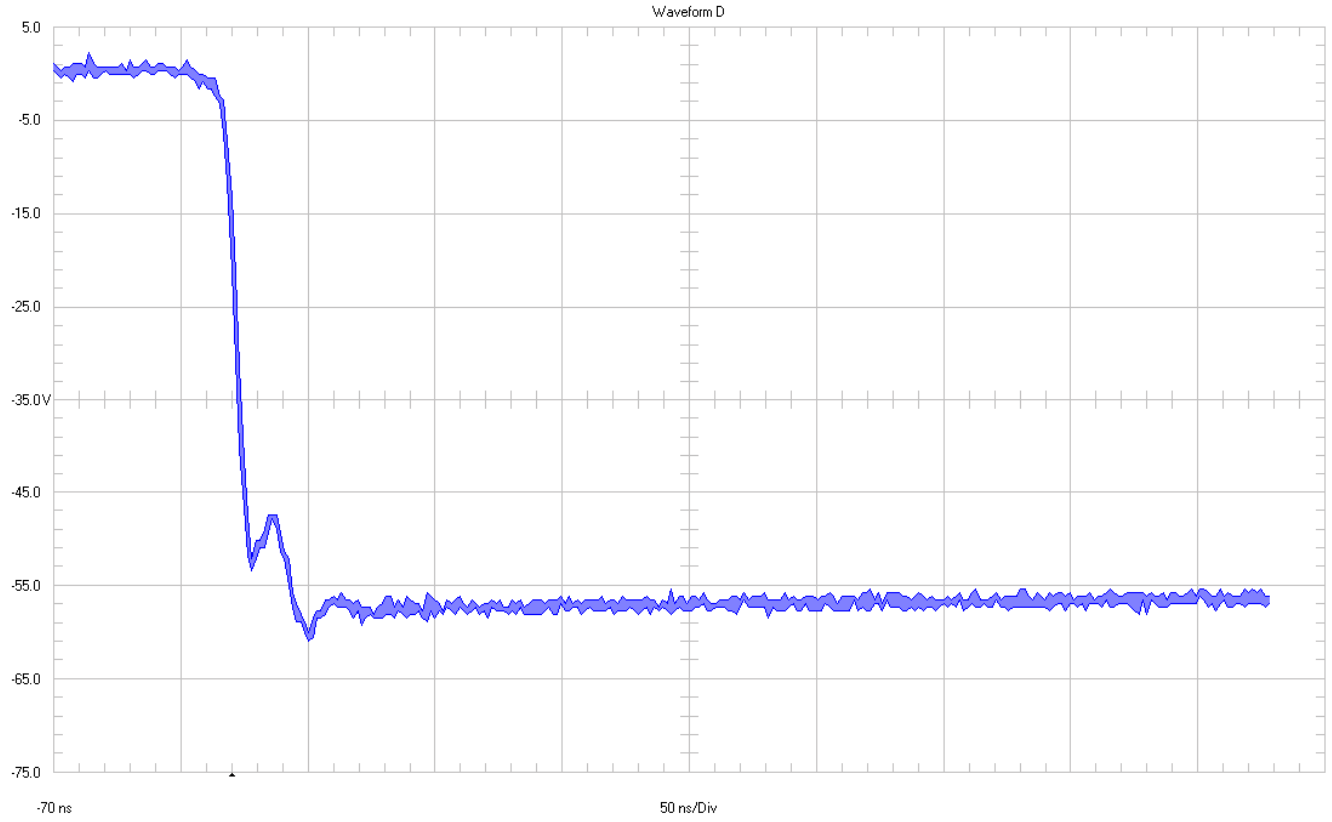
4.2.1 No Snubber

Figure 31. Diode D6 without Snubber @ 45 V Input Voltage



4.2.2 With Snubber 10R + 470 pF

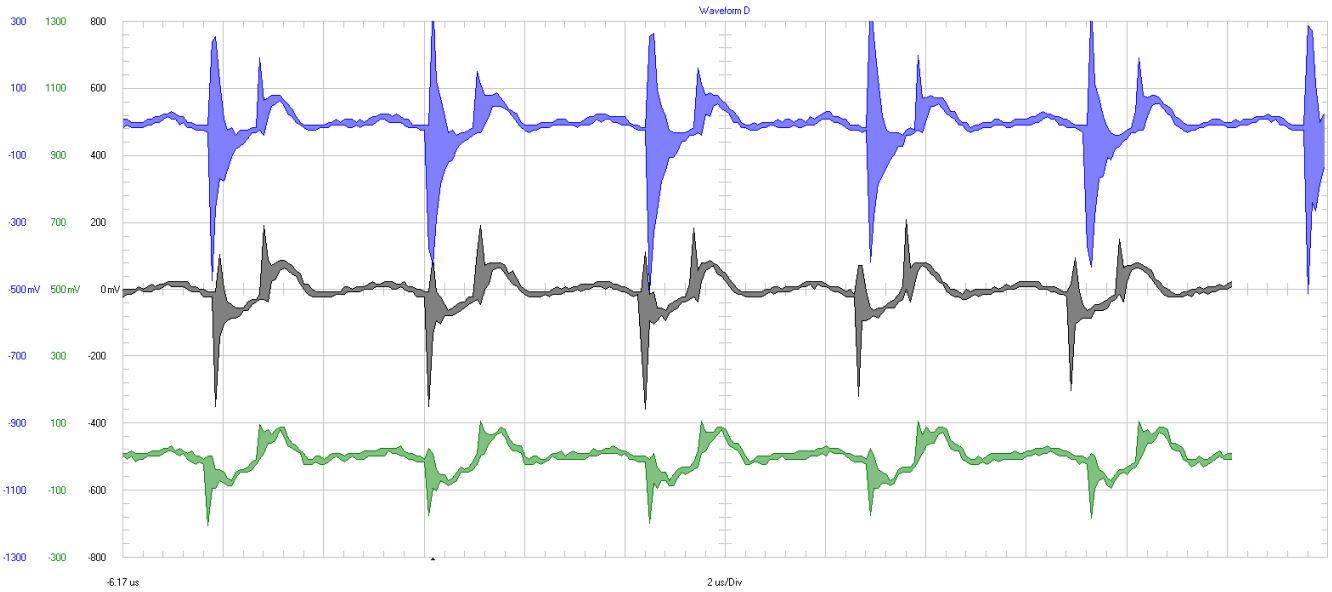
Figure 32. Diode D6 with Snubber @ 45 V Input Voltage



4.3 Output Voltage

For further improvements of the VOUT-ripple additional MLCC capacitors were added to VOUT . The following waveforms are showing VOUT without and with rectifier snubber and with additional MLCC capacitors (1 µF, 100 nF and 10 nF soldered on bottom side of the pcb).

Figure 33. VOUT at 45 V Input Voltage



channel 1: without snubber -> 200 mV/div (20MHz bandwidth); 2 µs/div

channel 2: with snubber -> 200 mV/div (20MHz bandwidth); 2 µs/div

channel3: with snubber and added caps -> 200 mV/div (20 MHz bandwidth); 2 µs/div

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