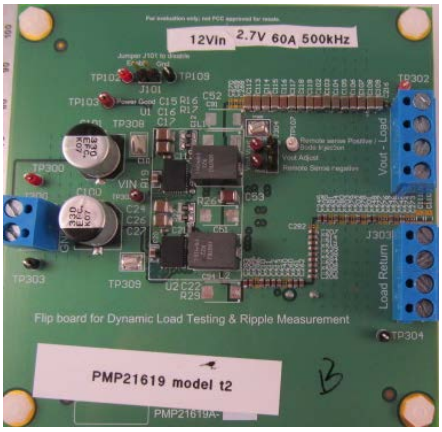
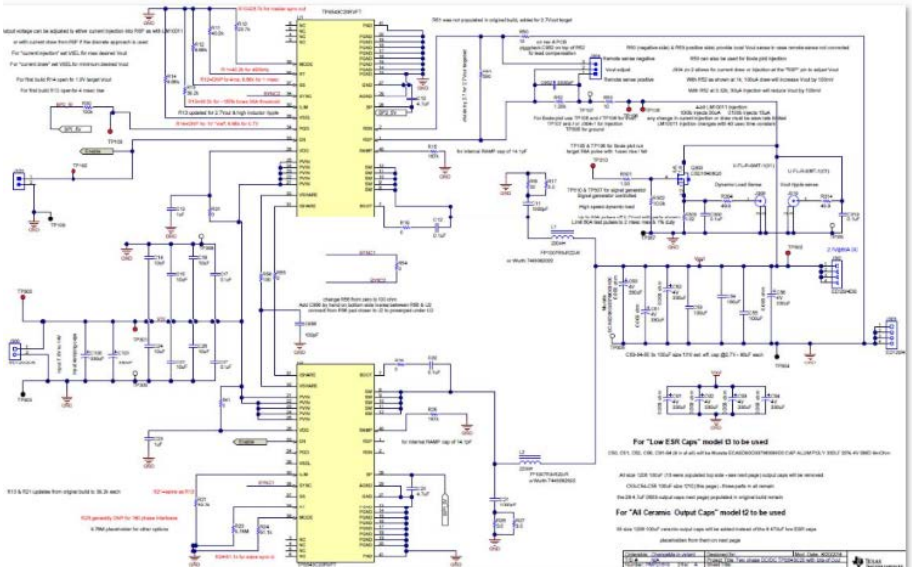
Test Report: PMP21619

Dual-phase compact reference design for 2.7 V 60 A for telecommunications

Description

This reference design uses only 2 ICs in a stacked configuration to provide 2.7 V at 60 A in a compact form factor. Both an all ceramics output capacitors version and a low ESR polymer output capacitors version were demonstrated to meet requirement of less than 3% undershoot for a step load from 2 A to 60 A in less than 1 microsecond. Internal compensation simplifies the design process. Design includes on-board high speed dynamic load tester, output ripple probe interface and test points for a stability analyzer.





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1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1. Voltage and Current Requirements

PARAMETER	SPECIFICATIONS
Vin	12V
Vout	2.7V
Iout	60A
Step load response: 2A to 60A in 1usec	Less than 3% or 81mV undershoot

Summary of differences between the two versions tested:

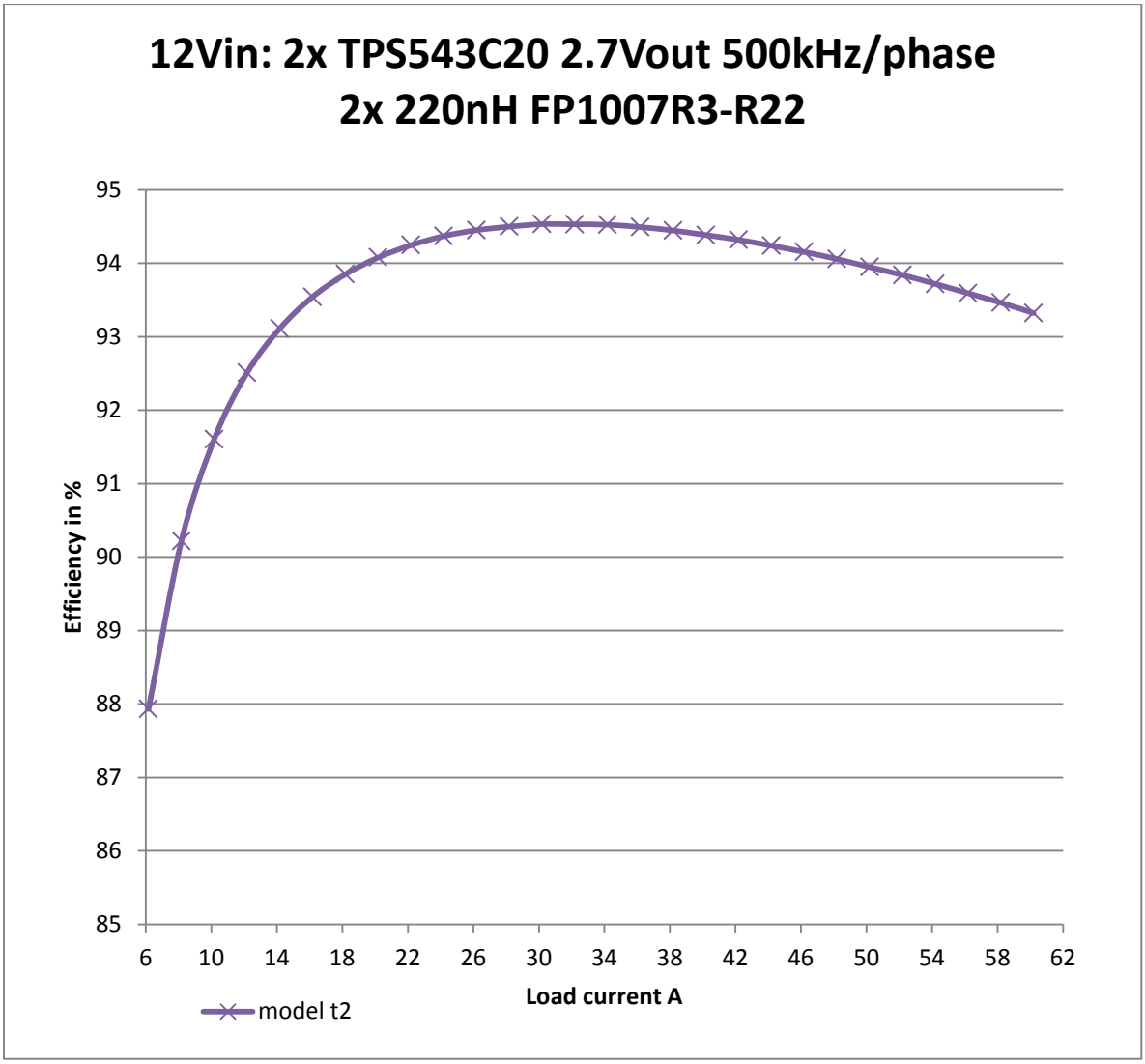
Both versions had same input capacitors; switching frequency (target 500kHz/phase) and output inductors of 220nH Eaton FP1007R3-R22. Also both had 3x 100uF size 1210 capacitors near converters to handle high frequency ripple in inductors close by plus 28x 4.7uF size 0603 ceramic caps to represent the filter caps near target load (such as an ASIC).

Both versions had RAMP resistors of 187k to target an internal RAMP capacitance of 14pF and voltage dividers of 1.00k high side and 590 ohms low side for a 2.7 to 1 division of Vout against a 1.0V internal Vref. Both versions had 3300pF across this high side 1.00k for a leading zero at 48kHz and pole at 130kHz to boost gain near crossover and speed up dynamic response.

Only difference between the two versions was the bulk of output capacitance: Model t2 was all ceramic with 33 of 100uF 6.3V size 1206 caps added, and model t3 had instead 8 of Murata ECASD90G337M008K00 CAP ALUM POLY 330UF 20% 4V SMD 8mOhm. Here, one 330uF low ESR cap replaced about 4 (4 & $1/8^{th}$ to be exact) 100uF size 1206 ceramic caps.

2 Testing and Results

2.1 Efficiency Graph; model t2 (all ceramic caps) used



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Efficiency & Loss Data

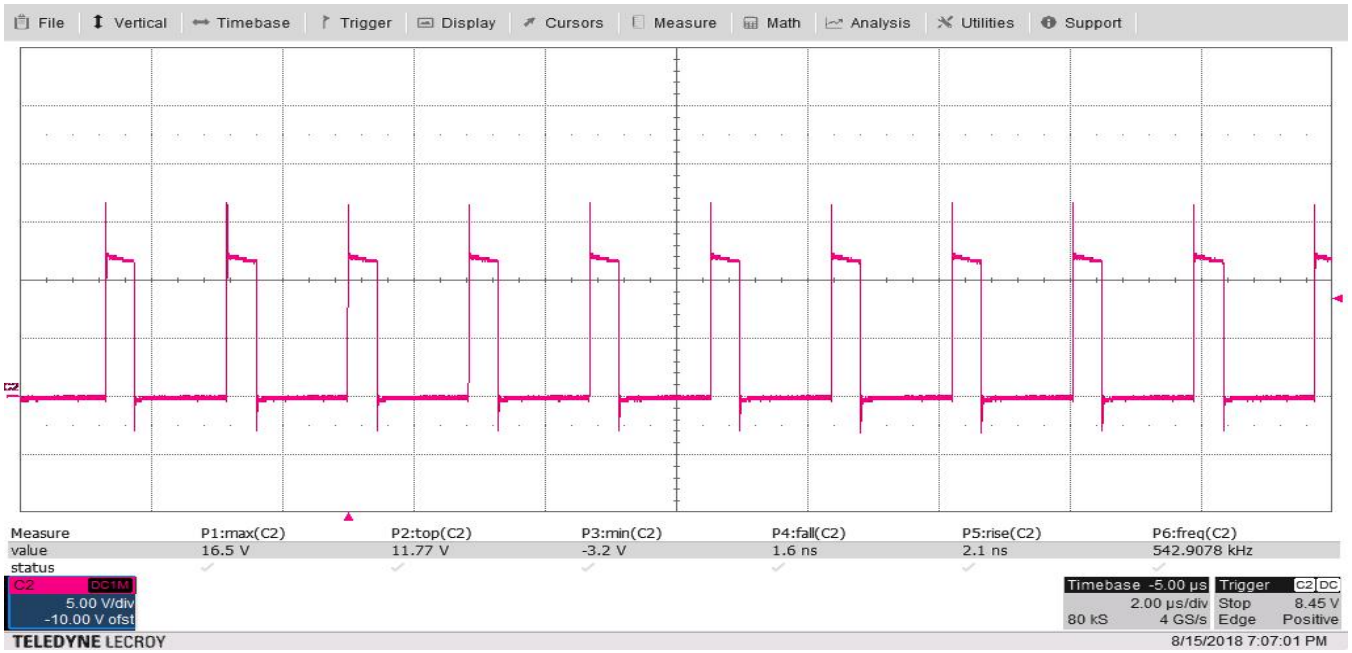
PMP21619 model t2: 12Vin to 2.7V 60A max 500kHz / phase

2x TPS543C20 FP1007R3-R22 inductors with fan

Vin V	Iin A	Vout	Iout A	eff %	loss W
11.999	0.176	2.728	0.00	0.00	2.11
11.999	0.670	2.728	2.15	73.15	2.16
11.999	1.131	2.728	4.16	83.62	2.22
11.999	1.593	2.728	6.16	87.93	2.31
11.999	2.058	2.728	8.17	90.22	2.42
11.999	2.524	2.728	10.17	91.60	2.54
11.999	2.991	2.728	12.17	92.51	2.69
11.999	3.461	2.728	14.17	93.11	2.86
11.998	3.931	2.728	16.17	93.54	3.05
11.998	4.403	2.728	18.18	93.85	3.25
11.998	4.876	2.728	20.18	94.08	3.46
11.998	5.350	2.727	22.18	94.25	3.69
11.998	5.825	2.727	24.18	94.37	3.94
11.998	6.303	2.727	26.19	94.45	4.20
11.998	6.781	2.727	28.19	94.50	4.48
11.998	7.260	2.727	30.19	94.53	4.76
11.998	7.741	2.727	32.19	94.53	5.08
11.998	8.223	2.727	34.19	94.52	5.40
11.998	8.707	2.727	36.20	94.49	5.75
11.997	9.194	2.727	38.20	94.45	6.13
11.997	9.682	2.727	40.20	94.38	6.52
11.997	10.172	2.727	42.20	94.32	6.93
11.997	10.664	2.728	44.20	94.24	7.37
11.997	11.157	2.728	46.20	94.15	7.83
11.997	11.652	2.728	48.20	94.06	8.31
11.997	12.150	2.728	50.20	93.95	8.82
11.997	12.649	2.728	52.20	93.84	9.35
11.997	13.151	2.728	54.20	93.72	9.91
11.997	13.655	2.728	56.20	93.59	10.50
11.996	14.161	2.728	58.20	93.46	11.10
11.996	14.669	2.728	60.20	93.32	11.75

Switching waveforms:

The photo below shows the switch node voltage of the master TPS53C20. The input voltage is 12V and the 2.7V output is loaded to 60A or 30A/phase. (5V/DIV, 1uS/DIV) (model t2 used)
Waveforms of master & slave very similar will show 11 pulses of master & 1 pulse of slave
Master SW node



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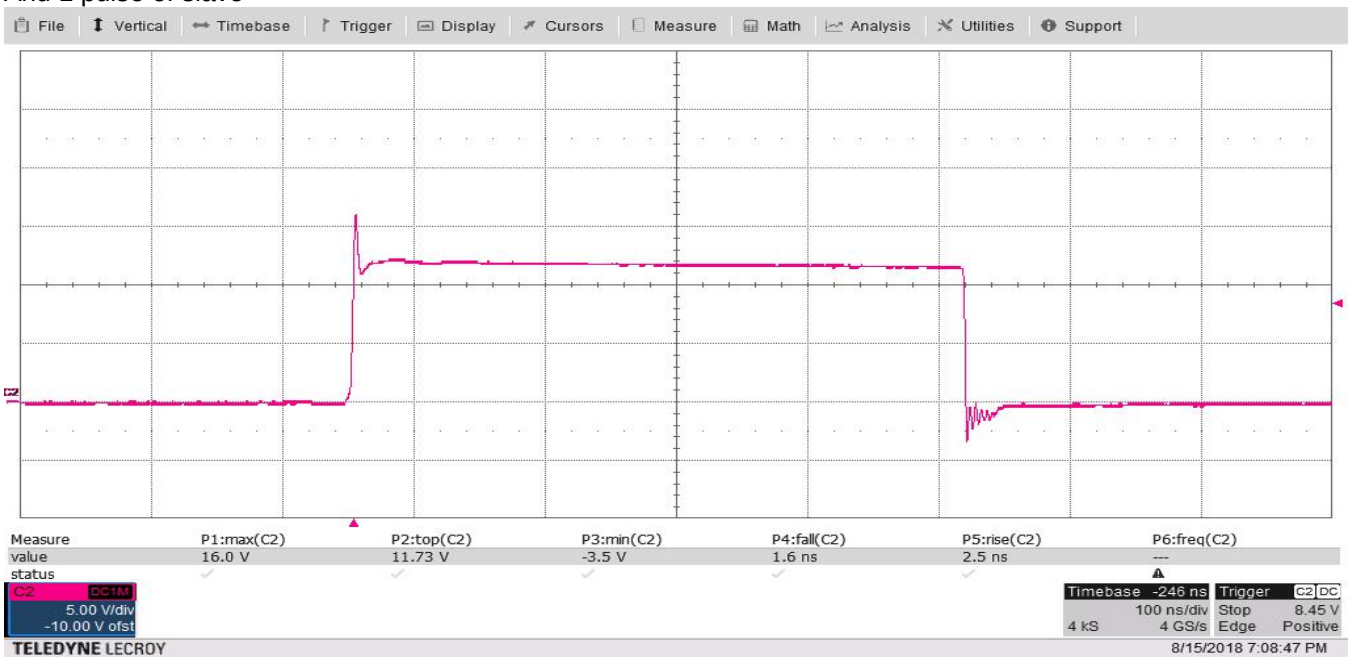
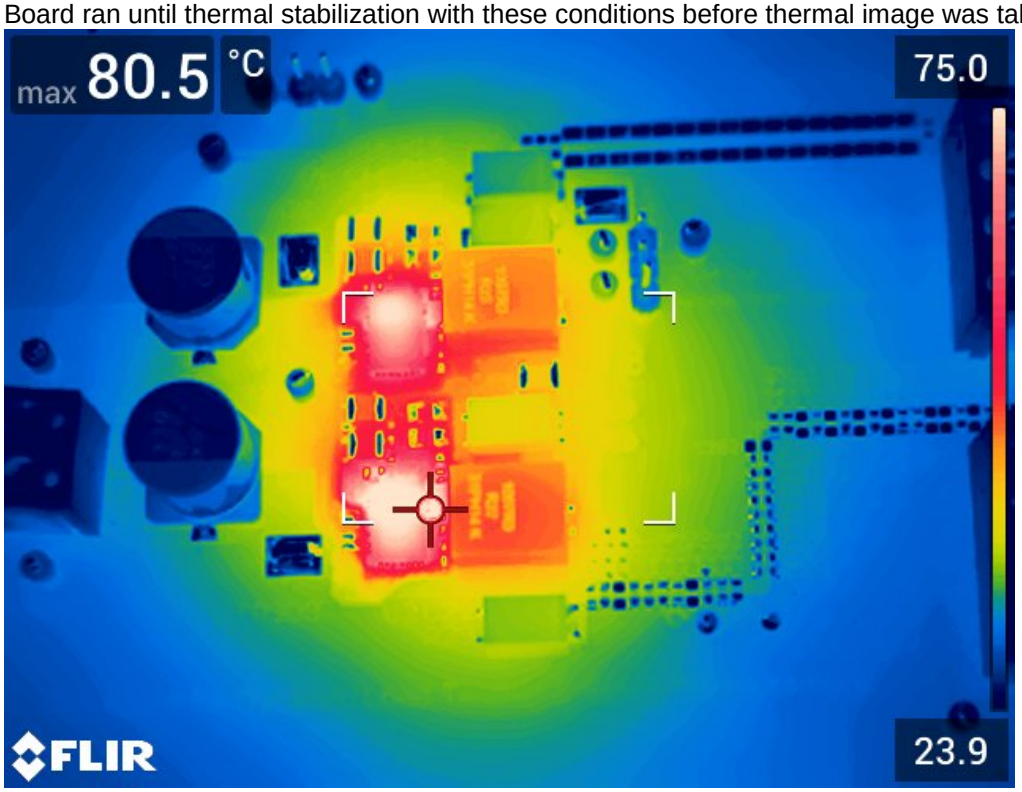
And 1 pulse of slave

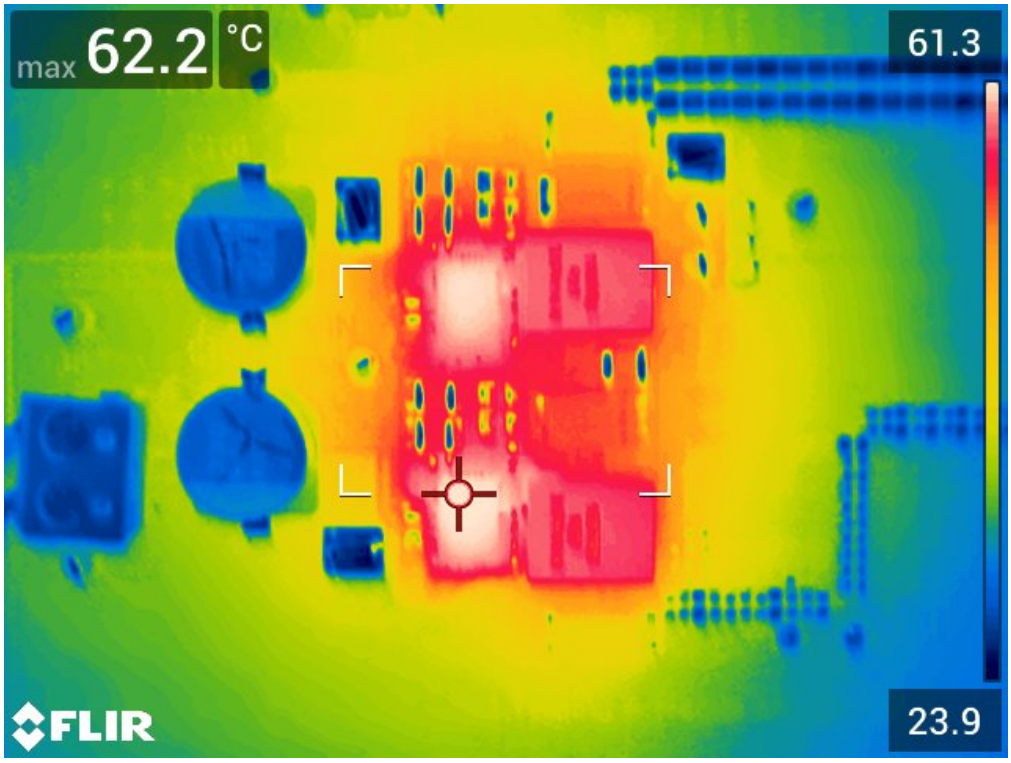


Thermal Images

The thermal image below shows operation at 12V input and 2.7V at 60A with fan, and 2.7V at 30A without fan. Board ran until thermal stabilization with these conditions before thermal image was taken. (model t3 used)



And now 30A without fan



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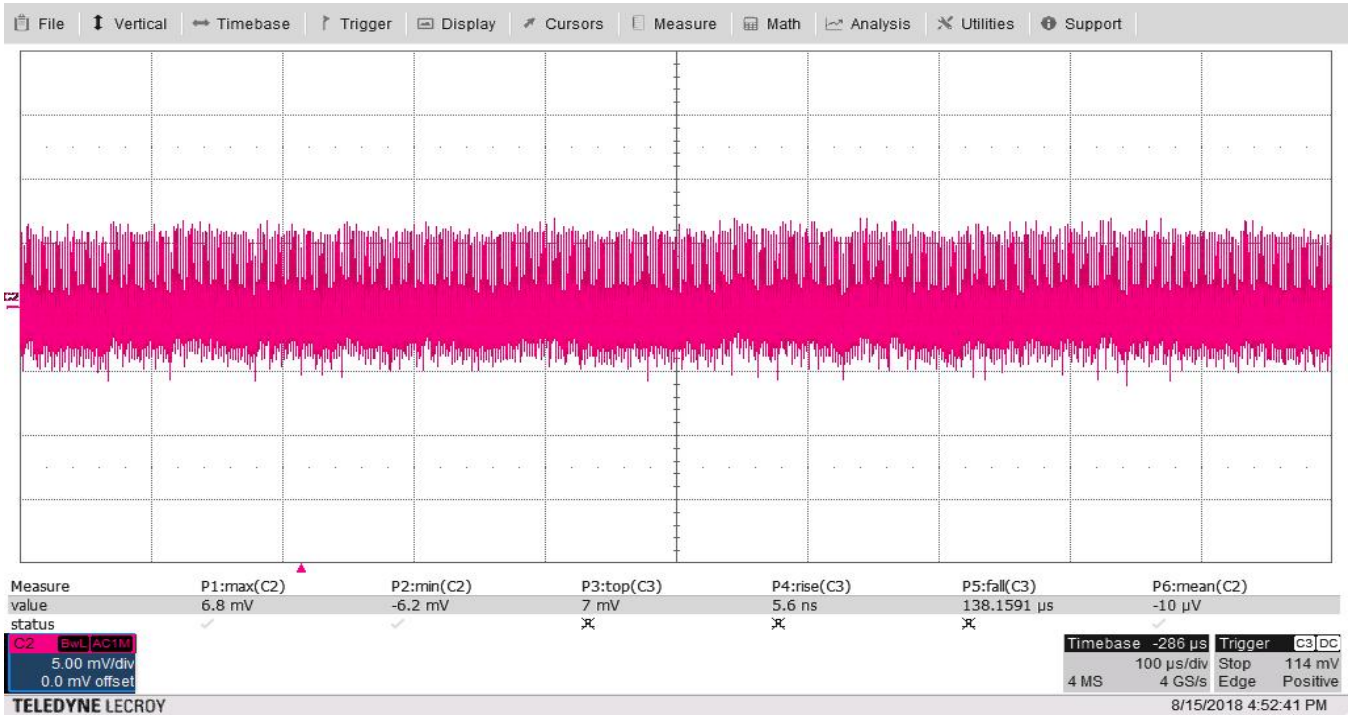
Testing on model t2: All ceramics version

Output Voltage Ripple

The output ripple voltage is shown in the figure below. The image was taken with the 2.7V output loaded to 60A and the input voltage set to 12V.
(5mV/DIV, 100uS/DIV) Ripple measurement was taken using connections on the bottom side of the board. Peak to peak ripple is 13.0mV. At no load (not shown) p-p ripple was 12.7mV.



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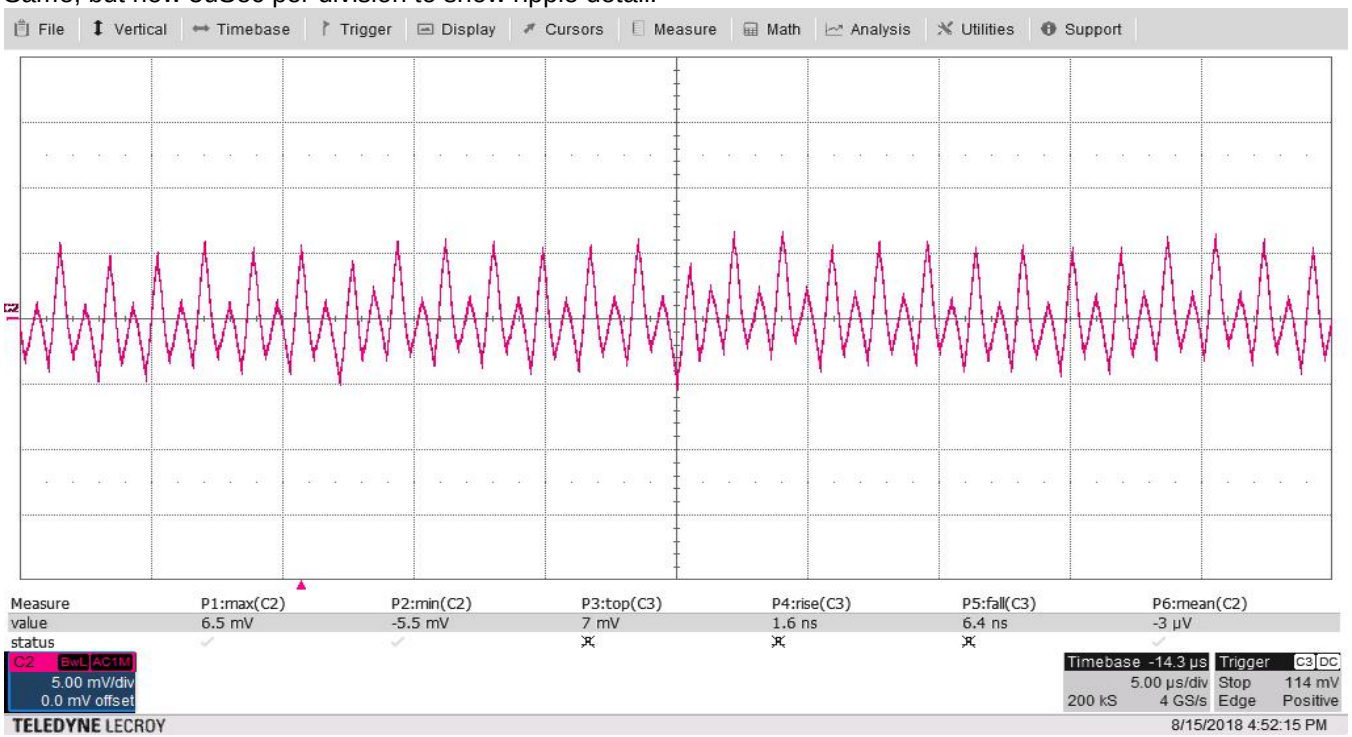
Same, but now 5uSec per division to show ripple detail:

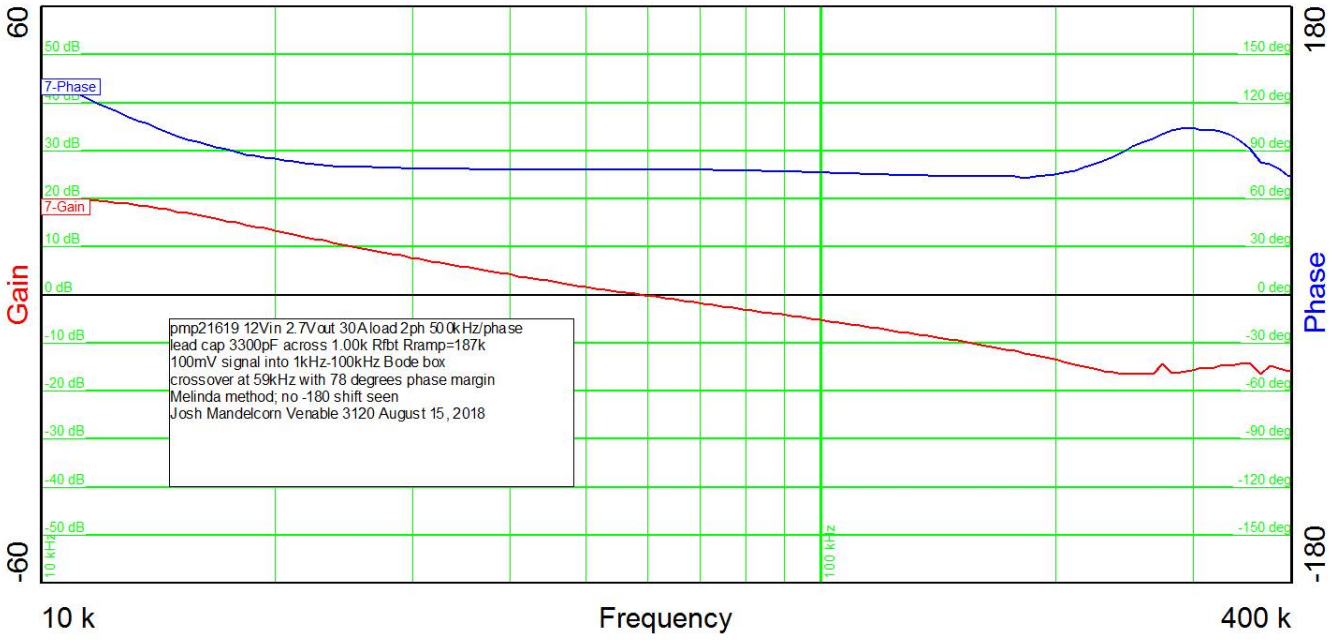


Testing on all ceramics output caps version model t2 continued:

Bode Plot

The plot below shows the converter's loop gain and phase margin when loaded to 2.7V @ 30A. All ceramics output caps version with 3700uF nominal capacitance and ~2000uF estimated at 2.7V bias; Cff at 3300pF for a zero at 48kHz & a pole at 130kHz; Rramp at 187k for both phases; inductors 220nH; 500kHz/phase setting

Vin = 12V Band Width = 59KHz Phase Margin = 78 degrees



Testing on all ceramics output caps version model t2 continued:

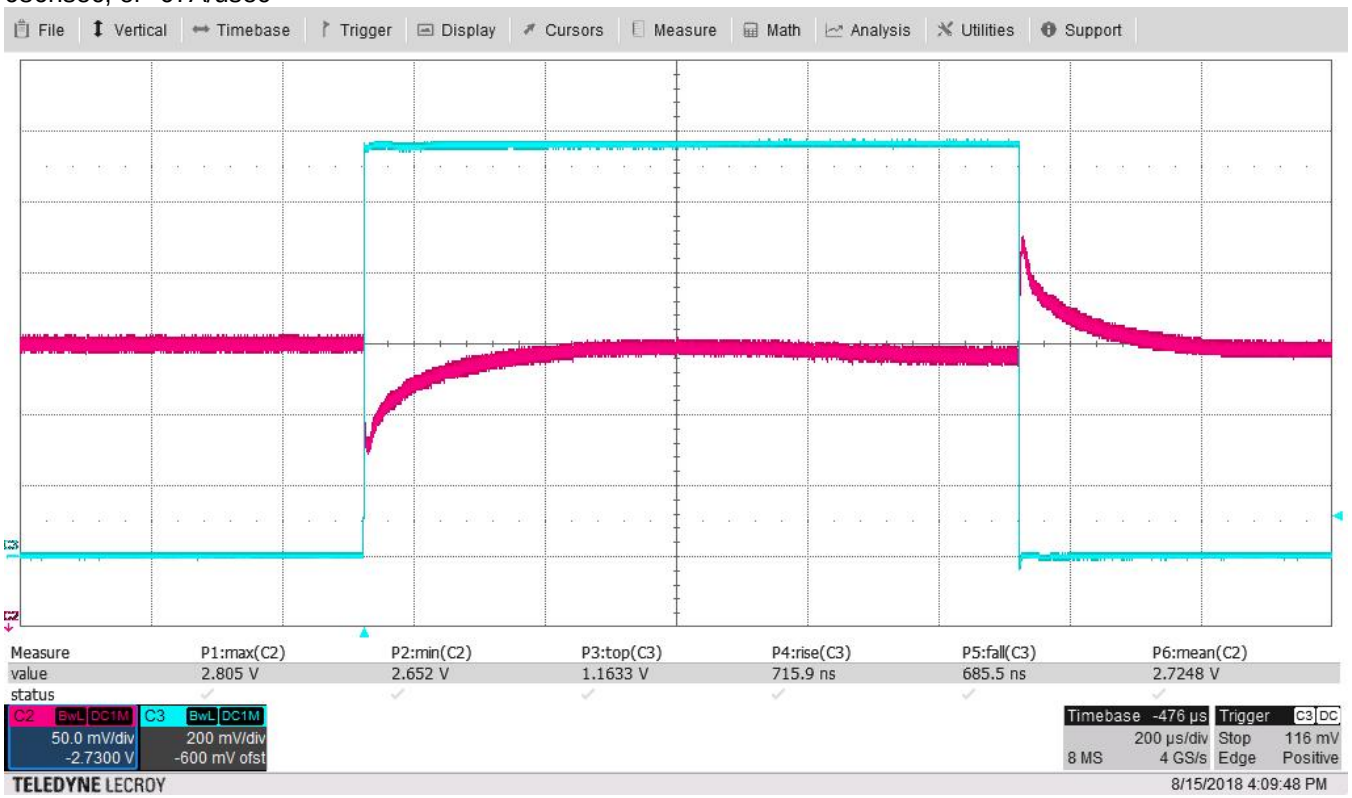
Load Transients

The photo below shows the 2.7V output voltage when the load current is stepped between 2A and 60A. Application request was 2→ 60A in 1us.

External static load of 2A was used along with on board dynamic load for 58A pulses. All ceramics output caps version with 3700uF nominal capacitance and ~2000uF estimated at 2.7V bias; Cff at 3300pF for a zero at 48kHz & a pole at 130kHz; Rramp at 187k for both phases; inductors 220nH; 500kHz/phase setting. Vin = 12V.

Vout is scope channel 2 red measured on bottom side of the board using coax connection:
Max overshoot to 2.805V is 80mV above static Vout of 2.725V, or 2.9% above static level.
Max undershoot to 2.652V is 73mV below static Vout of 2.725V, or 2.7% below static level.

Scope channel 3 blue Waveform below is across 20mOhm resistor to ground on the dynamic load.
Hence, the "top" of this pulse of 1.16mV divided by 20mOhms corresponds to 58A pulse.
Rise slew rate 65A/uS, Fall slew rate 67A/us
dI/dT of rise is 80% of this 58A (as rise time is defined for "10% to 90%" or 80%") divided by the rise time of 716nsec; or 65A/usec
dI/dT of fall is 80% of this 58A (as fall time is defined for "90% to 10%" or 80%") divided by the fall time of 686nsec; or -67A/usec



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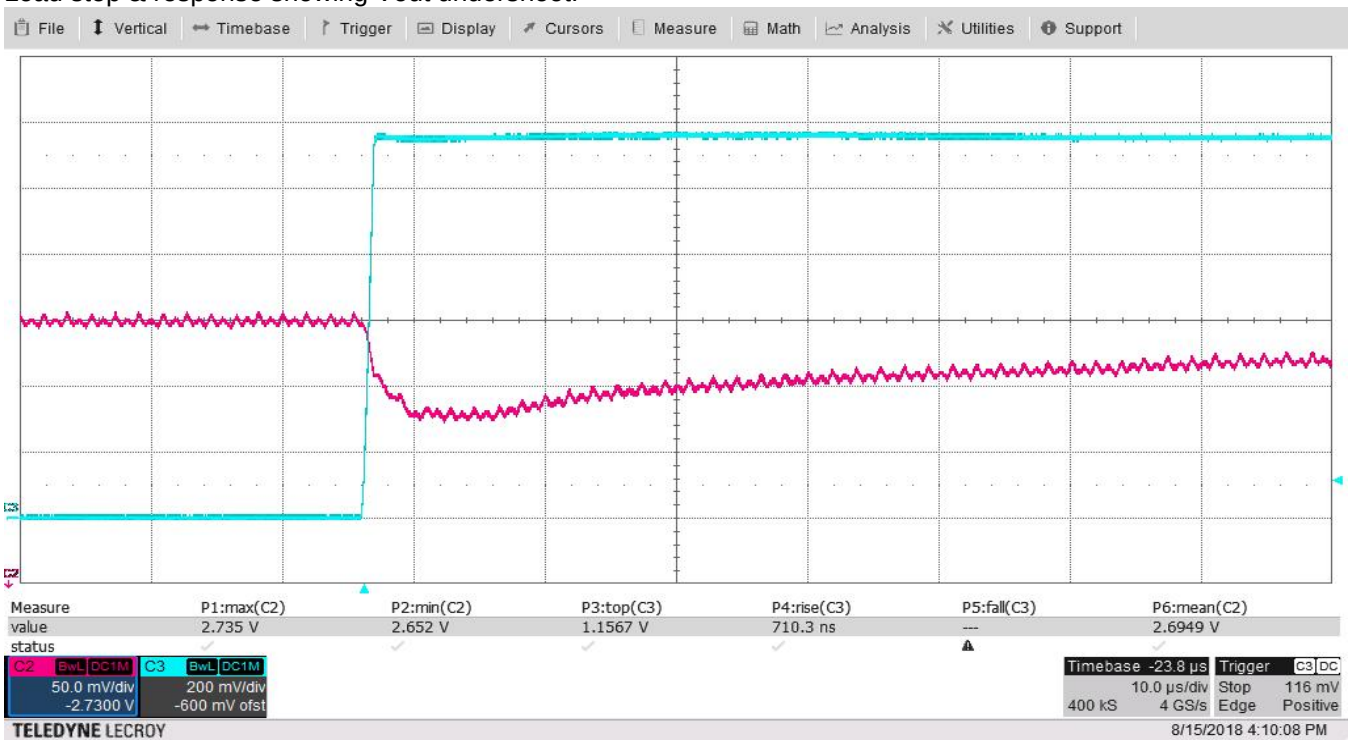
Testing on all ceramics output caps version model t2 continued:

Load transients – continued – showing expansion detail of load step and load dump from previous page:
Load step & response showing Vout undershoot:



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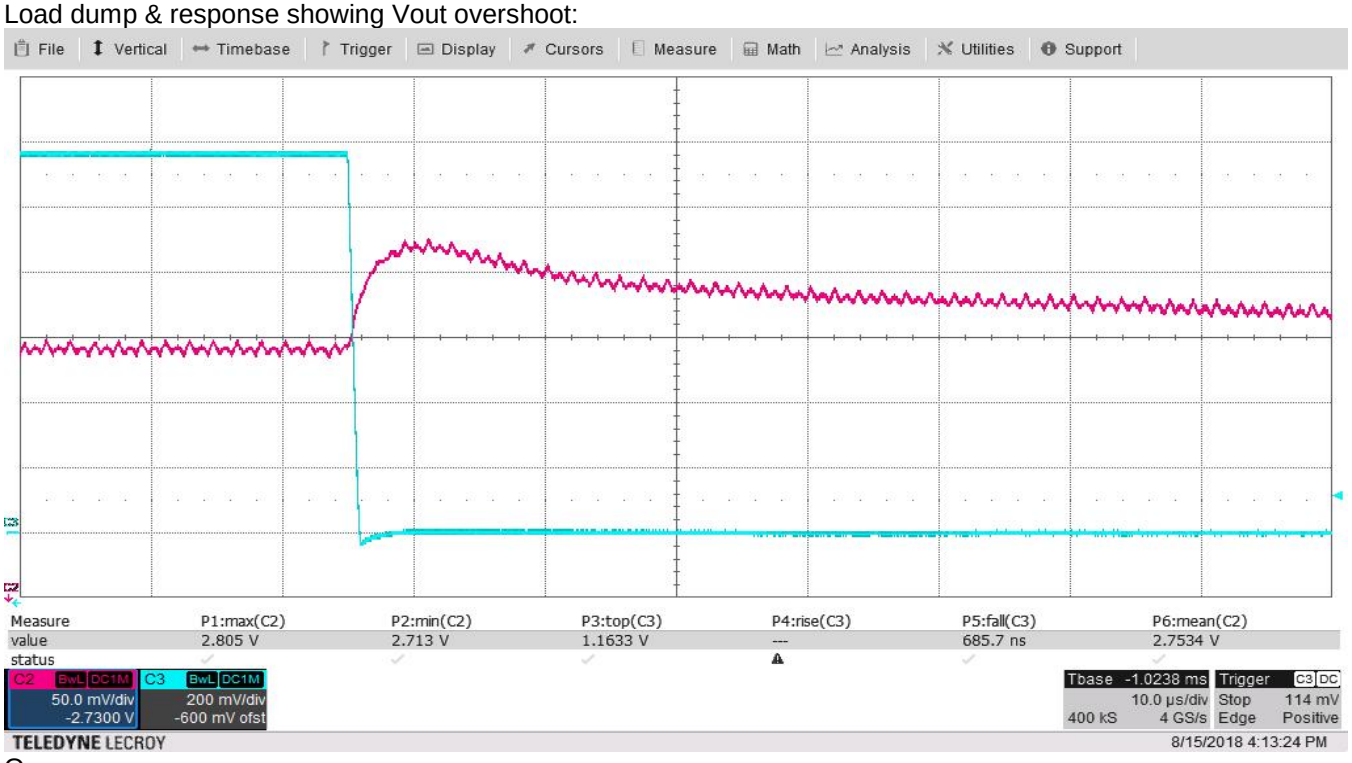
Load dump & response showing Vout overshoot:



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Testing on all ceramics output caps version model t2 continued:

Output start up vs. Vin when Vin plugged in – hot plug

No load: red is Vout and blue is Vin

Monotonic rise; ~15mV overshoot; and 4 msec rise time 0-100%

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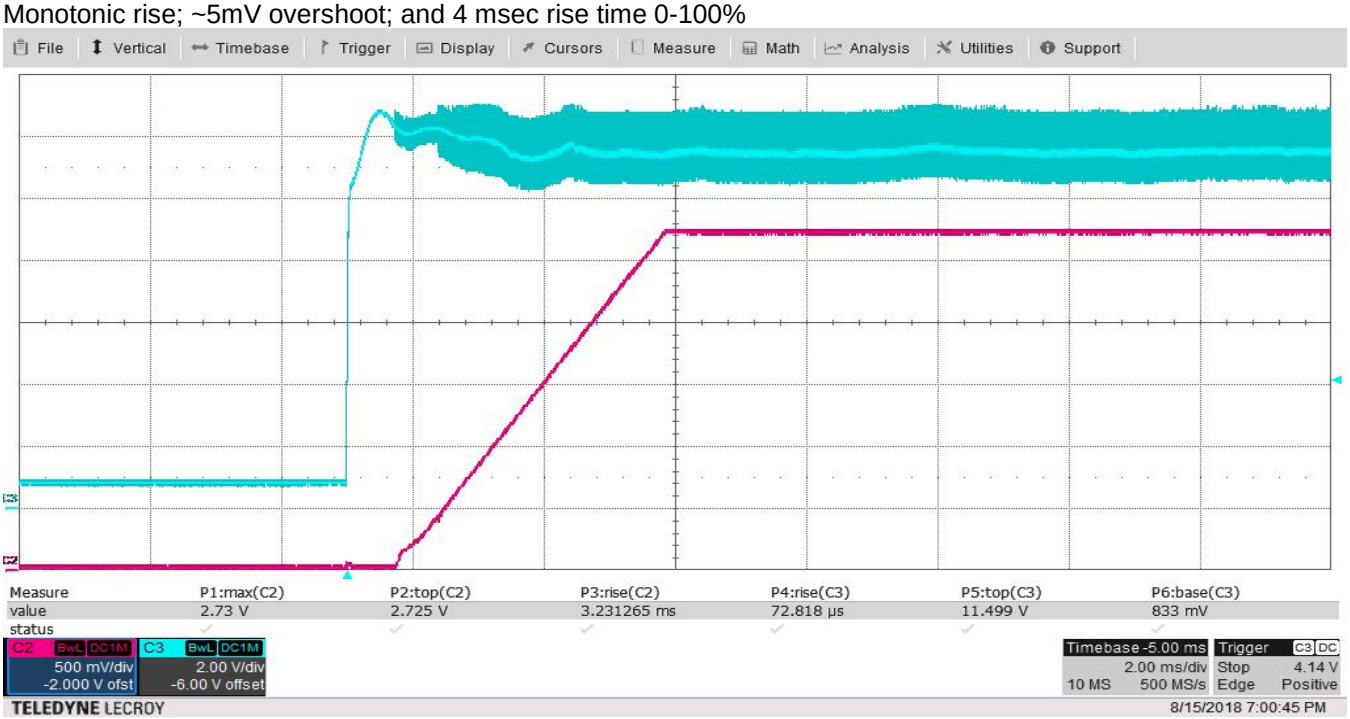
Same, but 60A on load: red is Vout and blue is Vin

Monotonic rise; ~5mV overshoot; and 4 msec rise time 0-100%



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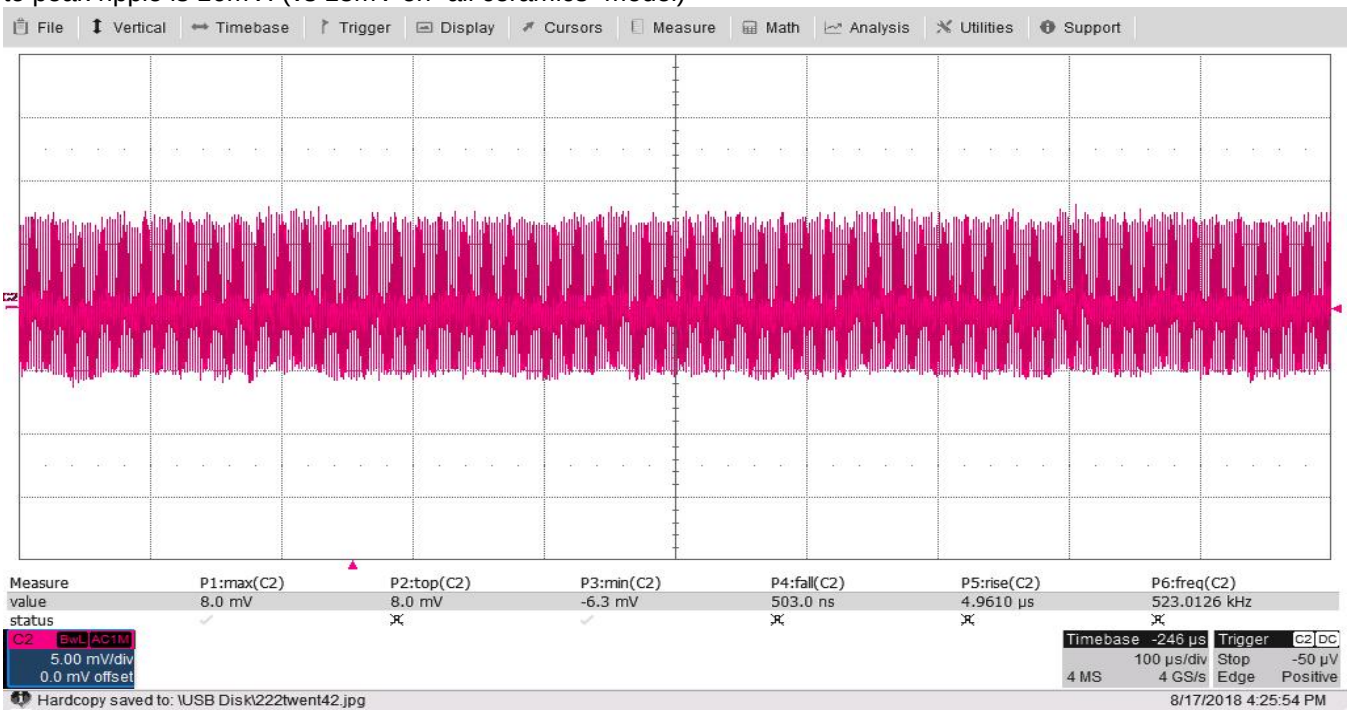
Testing on model t3: Low ESR output caps version

Output Voltage Ripple

The output ripple voltage is shown in the figure below. The image was taken with the 2.7V output loaded to 60A and the input voltage set to 12V.
(5mV/DIV, 100uS/DIV) Ripple measurement was taken using connections on the bottom side of the board. Peak to peak ripple is 16mV. (vs 13mV on “all ceramics” model)



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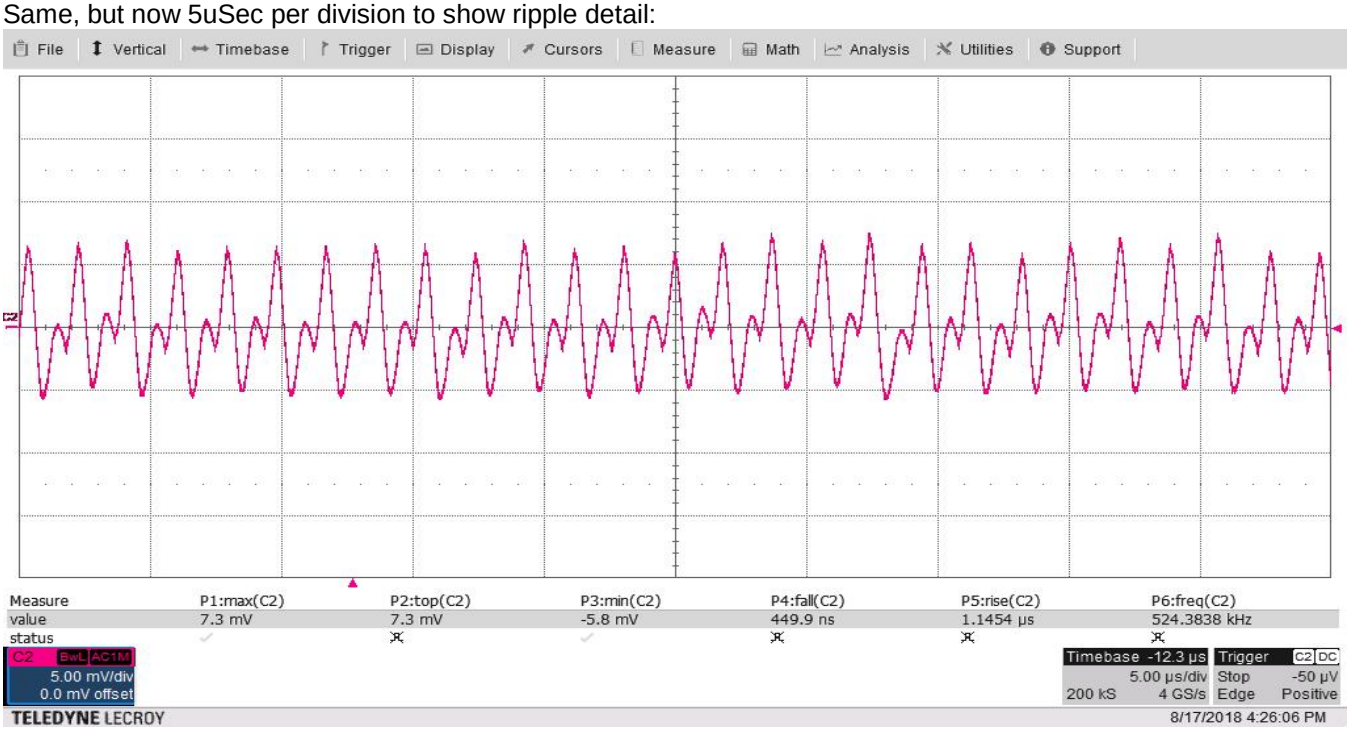
Same, but now 5uSec per division to show ripple detail:

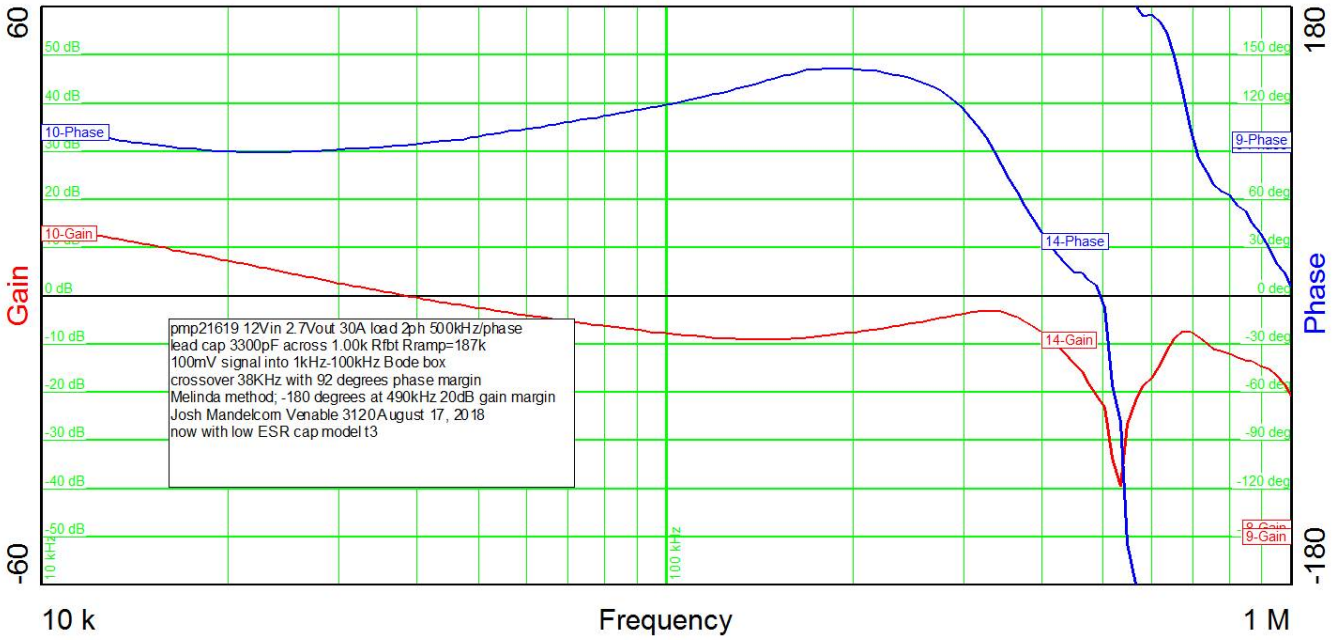


Testing on model t3: Low ESR output caps version continued:

Bode Plot

The plot below shows the converter's loop gain and phase margin when loaded to 2.7V @ 30A. Low ESR output caps version with 2640uF (8x 330uF) nominal capacitance in series with 1mOhm max (8mOhm/8); Cff at 3300pF for a zero at 48kHz & a pole at 130kHz; Rramp at 187k for both phases; inductors 220nH; 500kHz/phase setting

Vin = 12V Band Width = 38KHz Phase Margin = 92 degrees



Crossover here 38kHz vs 59kHz for all ceramics version. However, gain above 100kHz here was higher. Hence, the Bode plot was extended to 1 MHz to show actual frequency at which phase crosses -180 degrees which was about 500kHz with a gain margin of about 20dB.

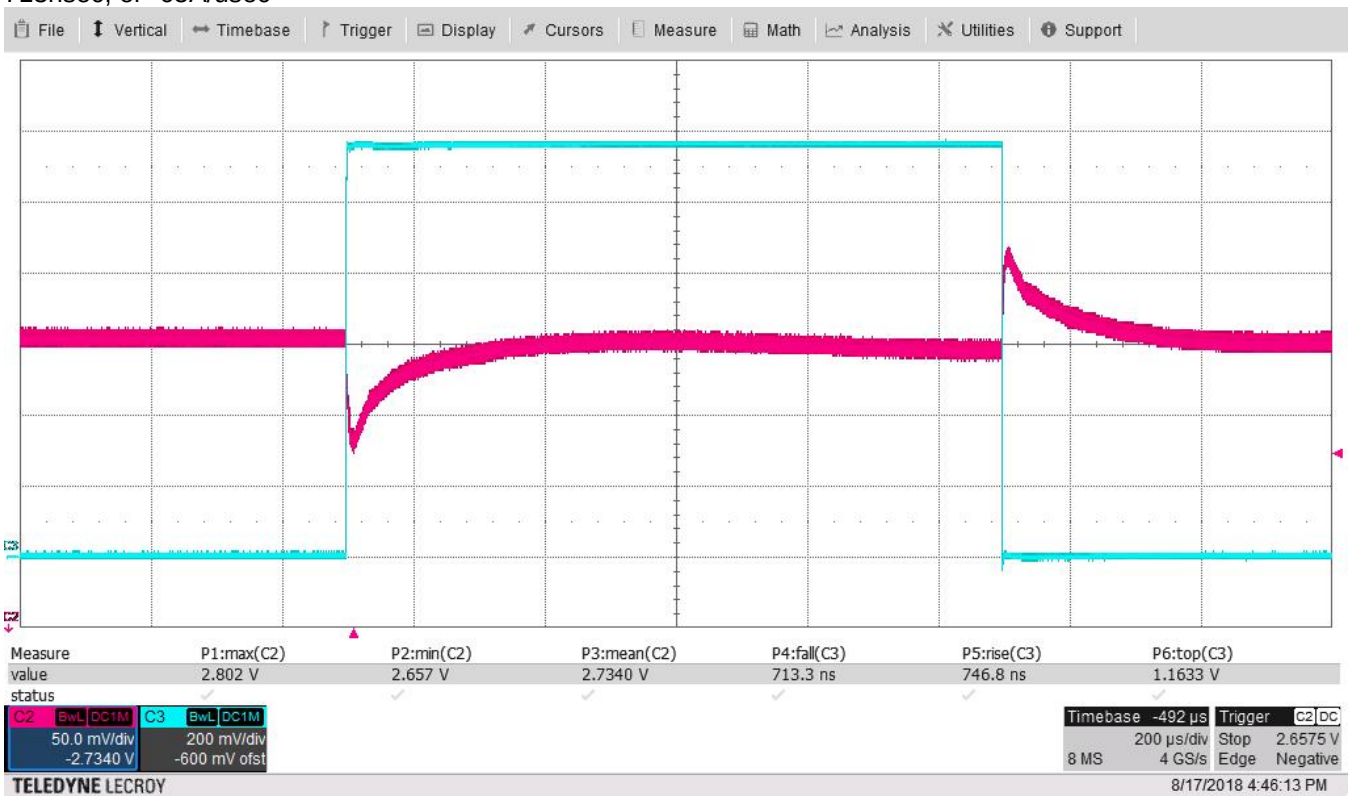
Testing on model t3: Low ESR output caps version *continued:*

Load Transients

The photo below shows the 2.7V output voltage when the load current is stepped between 2A and 60A. Application request was 2→ 60A in 1us.

External static load of 2A was used along with on board dynamic load for 58A pulses. Low ESR output caps version with 2640uF (8x 330uF) nominal capacitance in series with 1mOhm max (8mOhm/8); Cff at 3300pF for a zero at 48kHz & a pole at 130kHz; Rramp at 187k for both phases; inductors 220nH; 500kHz/phase setting. Vin = 12V.

Vout is scope channel 2 red measured on bottom side of the board using coax connection:
Max overshoot to 2.802V is 68mV above static Vout of 2.734V, or 2.5% above static level (vs. 80mV in all ceramics version)
Max undershoot to 2.657V is 77mV below static Vout of 2.734V, or 2.8% below static level (vs. 73mV in all ceramics version)
Scope channel 3 blue Waveform below is across 20mOhm resistor to ground on the dynamic load.
Hence, the “top” of this pulse of 1.16mV divided by 20mOhms corresponds to 58A pulse.
Rise slew rate 62A/uS, Fall slew rate 65A/us
dI/dT of rise is 80% of this 58A (as rise time is defined for “10% to 90%” or 80%”) divided by the rise time of 747nsec; or 62A/usec
dI/dT of fall is 80% of this 58A (as fall time is defined for “90% to 10%” or 80%”) divided by the fall time of 713nsec; or -65A/usec



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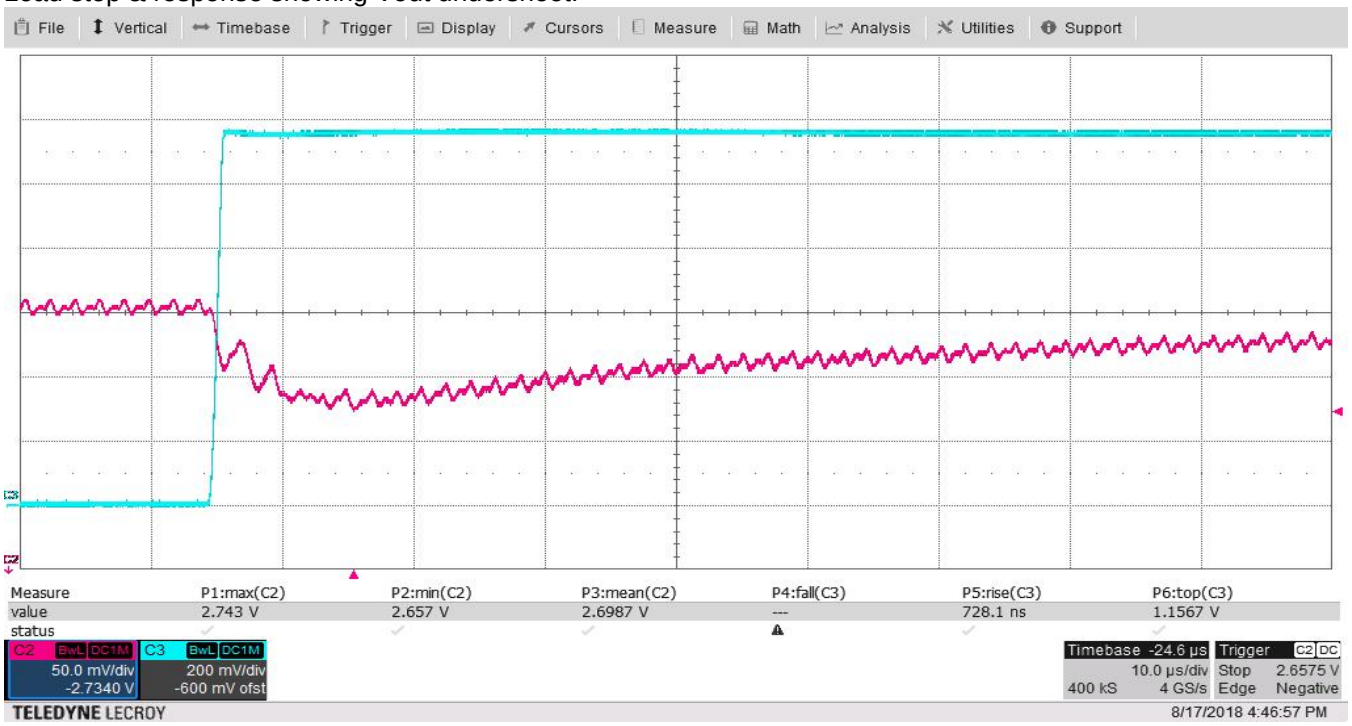
***Testing on model t3: Low ESR output caps version* continued:**

Load transients – continued – showing expansion detail of load step and load dump from previous page:
Load step & response showing Vout undershoot:



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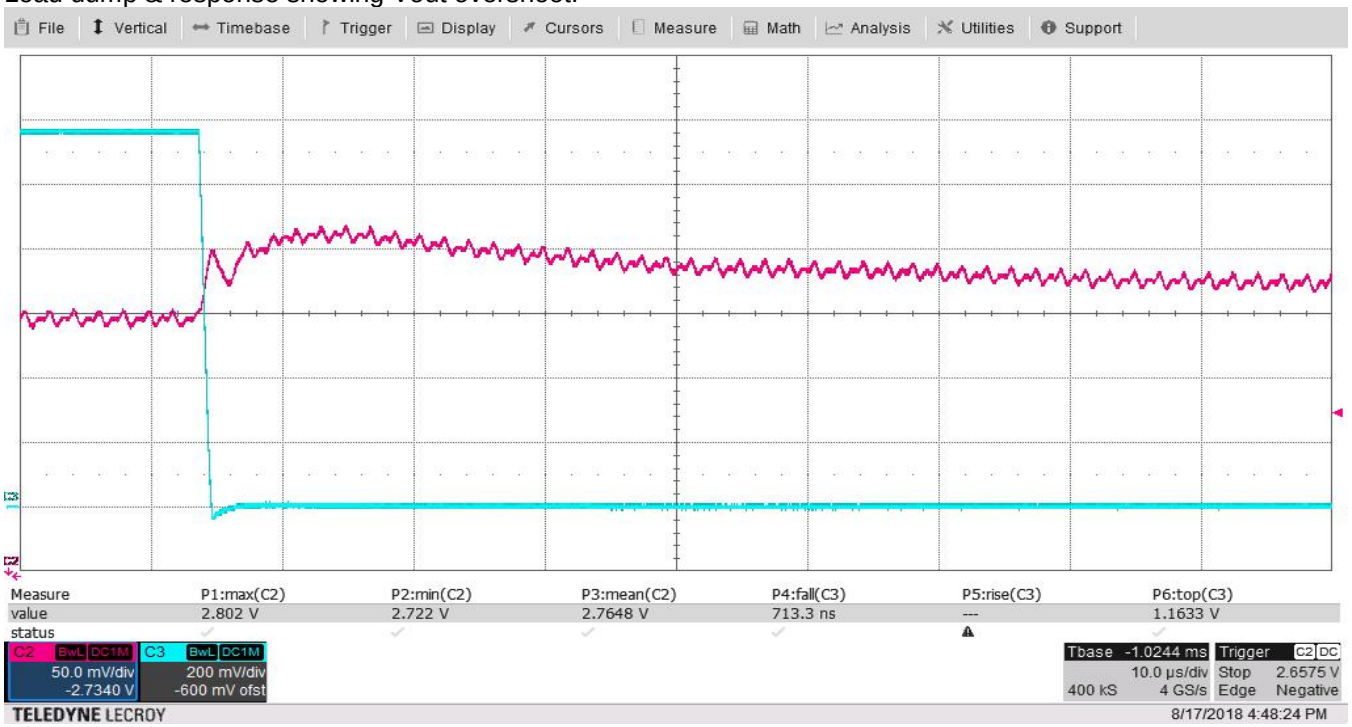
Load dump & response showing Vout overshoot:



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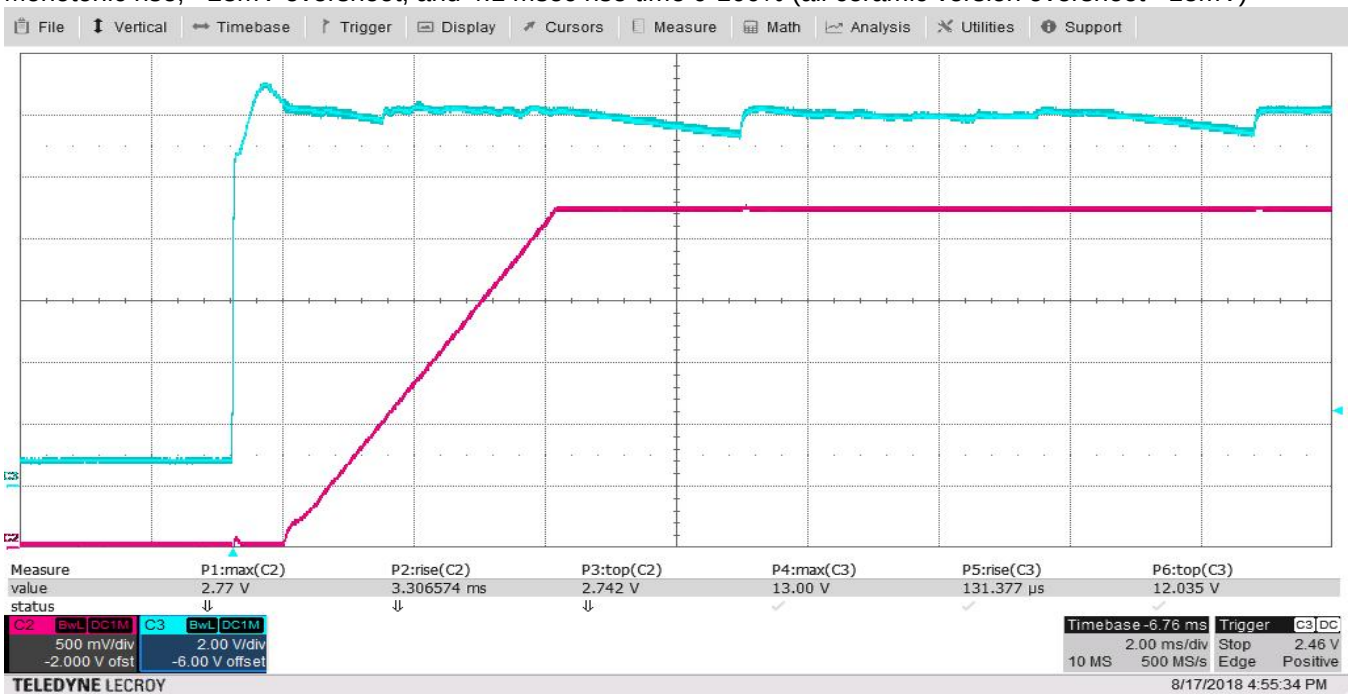
***Testing on model t3: Low ESR output caps version* continued:**

Output start up vs. Vin when Vin plugged in – hot plug

No load: red is Vout and blue is Vin

Monotonic rise; ~28mV overshoot; and 4.1 msec rise time 0-100% (all ceramic version overshoot ~15mV)



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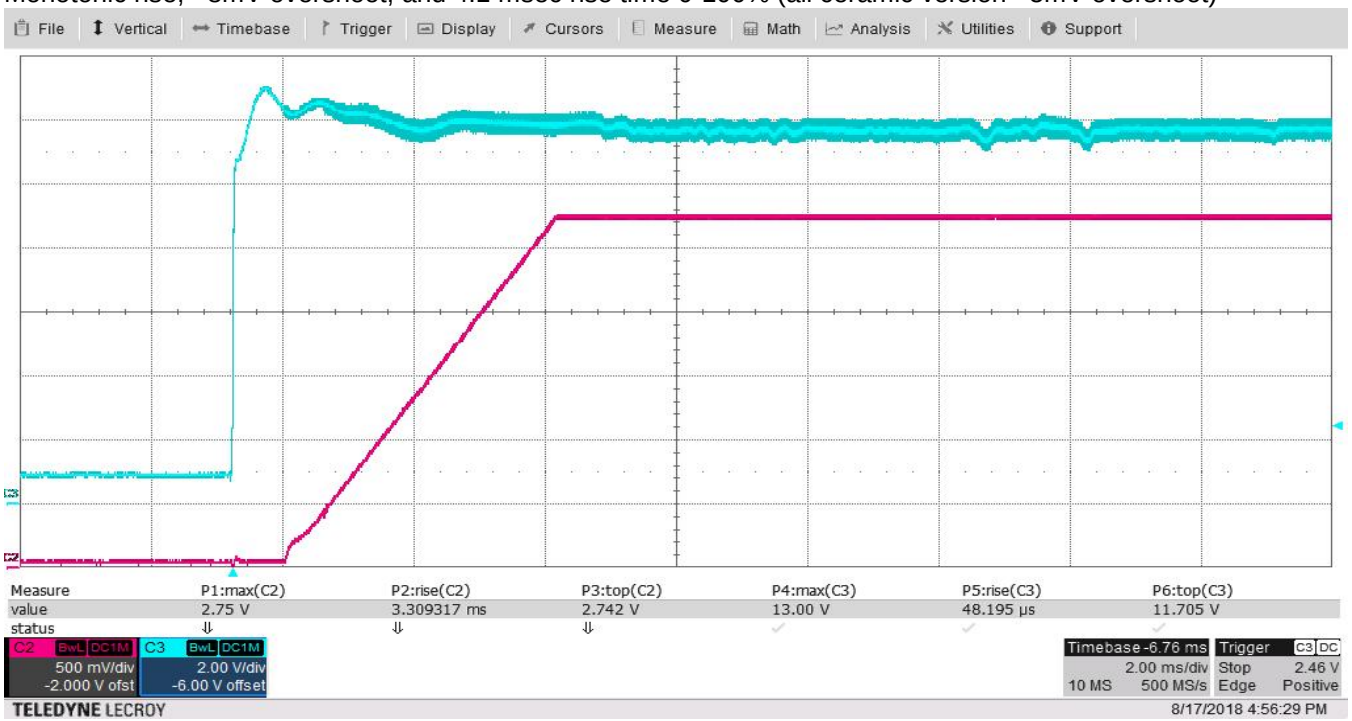
Same, but 60A on load: red is Vout and blue is Vin

Monotonic rise; ~8mV overshoot; and 4.1 msec rise time 0-100% (all ceramic version ~5mV overshoot)



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