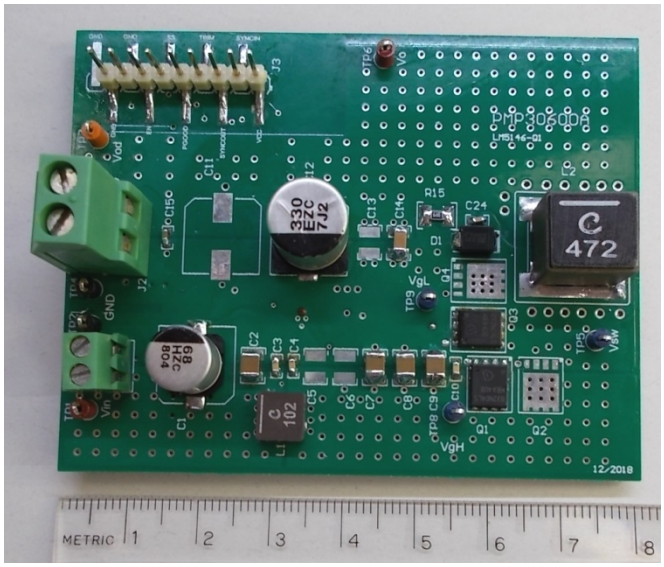
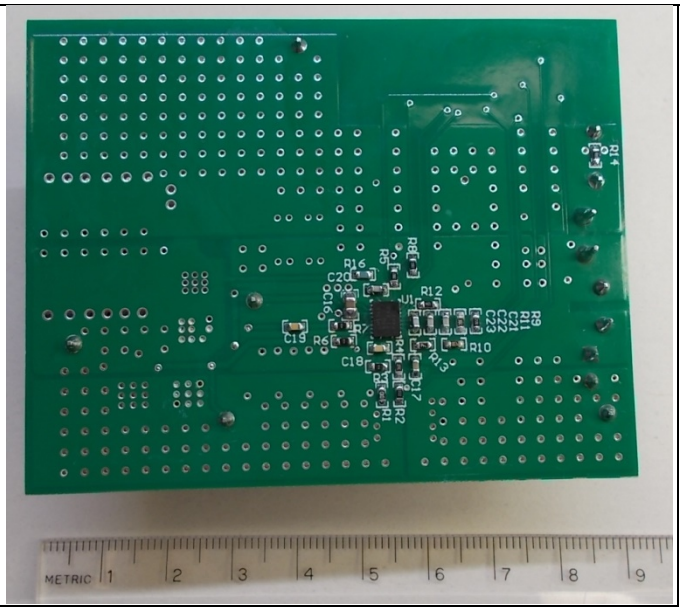
Test Report: PMP30600-AL
10-A Automotive Pre-Regulator Reference Design

Description

This reference design is a synchronous buck converter primarily to supply automotive loads. The IC is LM5146-Q1 in fixed frequency operation at 400 kHz to ensure low noise operation. To minimize conducted emissions an input filter prevents from reflected ripple. Furthermore a RC snubber attenuates noise in the RF band to reduce radiated emissions. To reduce system EMI the design is prepared either to synchronize other converters (output) or just to be externally synchronized (input). The power stage itself withstands surge voltages up to 36Vpk.





1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1. Voltage and Current Requirements

PARAMETER	SPECIFICATIONS
Input Voltage Range	6 V to 18 V
Output Voltage	5 V
Maximum Output Current	10 A
Calculated Switching Frequency	400 kHz

1.2 Considerations

The circuit is built on board PMP30600RevA.

2 Testing and Results

2.1 Efficiency Graphs

The efficiency is shown in the Figure 1 below. The input voltage was set to 14V.

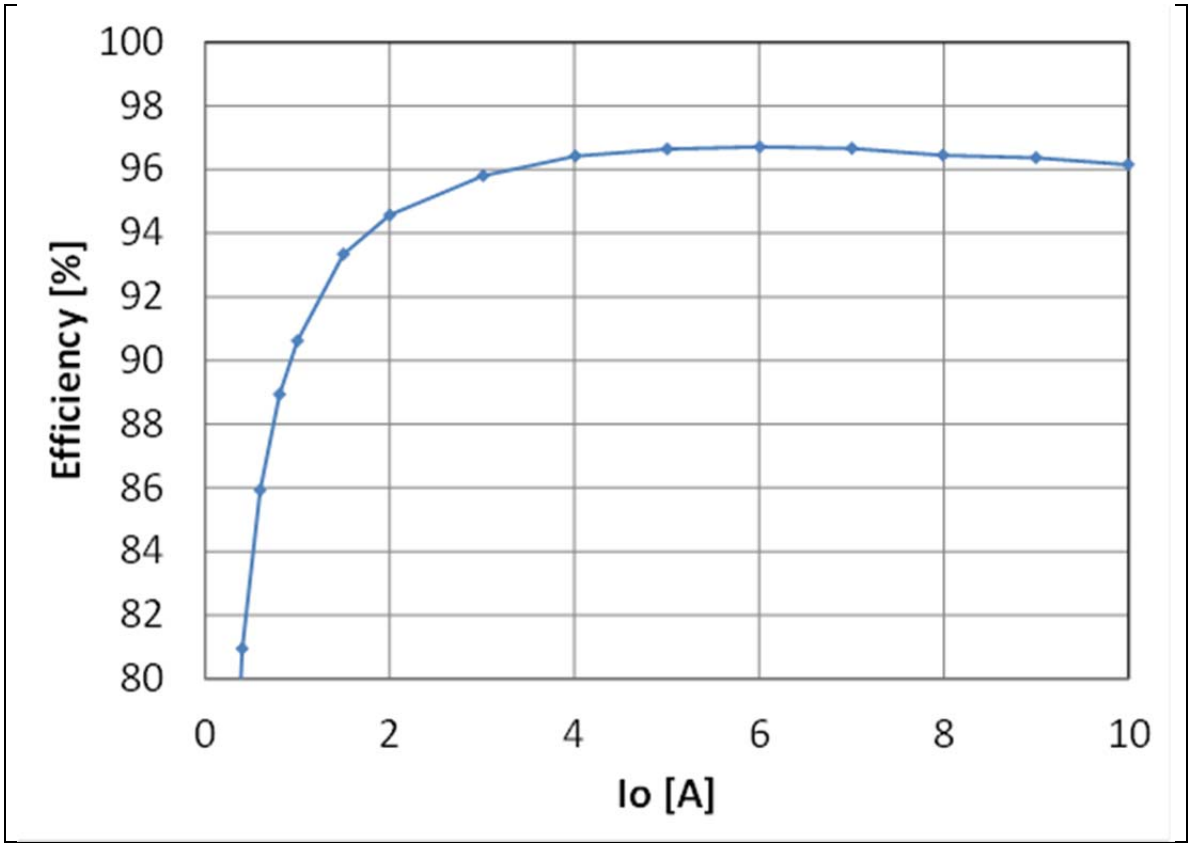


Figure 1

Full load efficiency 96.2%

Maximum efficiency 96.7% at 6A.

Effcy ≥95% in a range 2.5A to 10A, It is 25% load to 100% load.

2.2 Load Regulation

The load regulation of the output is shown in the Figure 2 below. The input voltage was set to 14V.

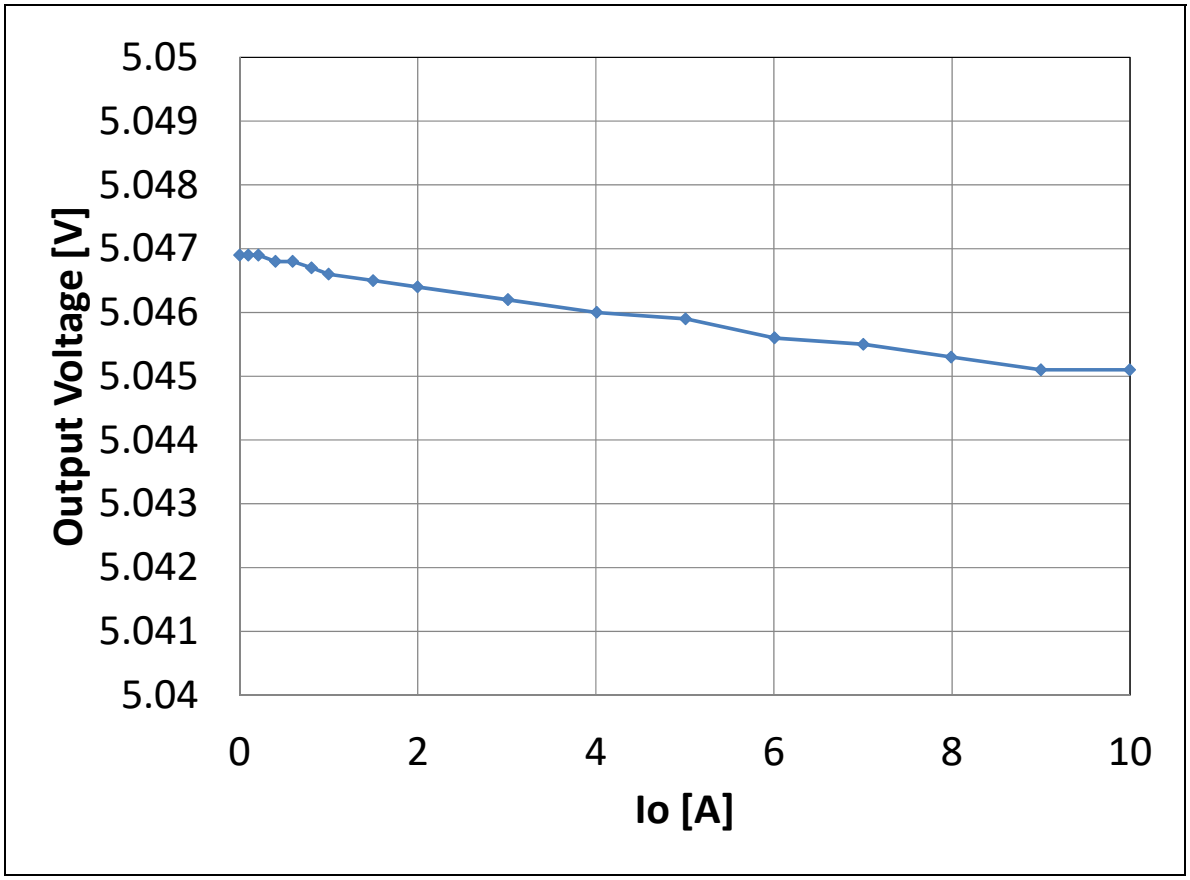


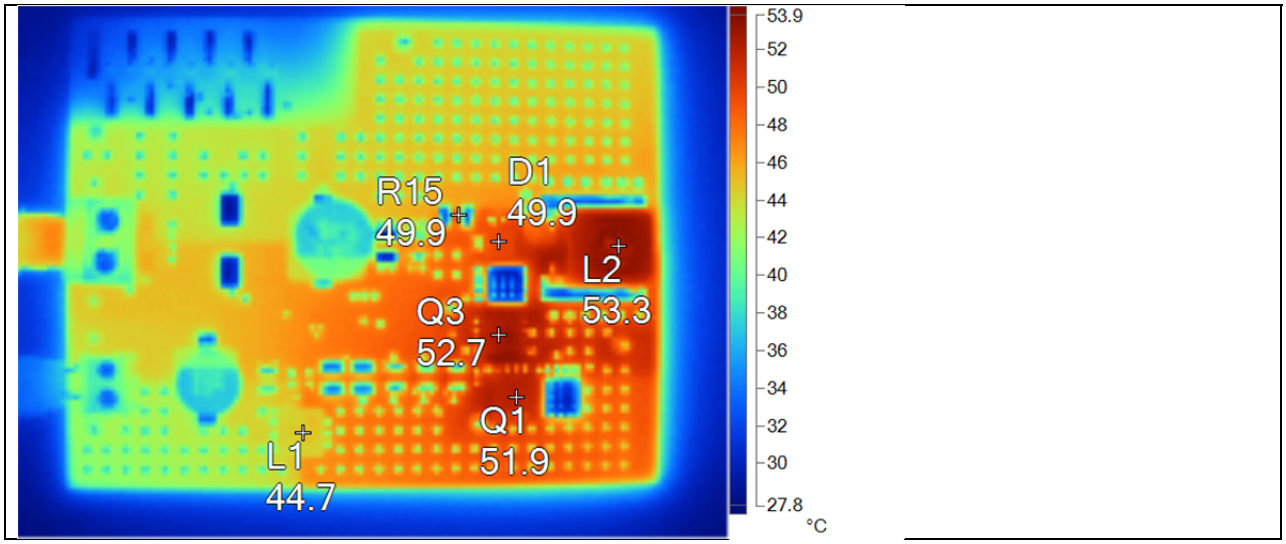
Figure 2

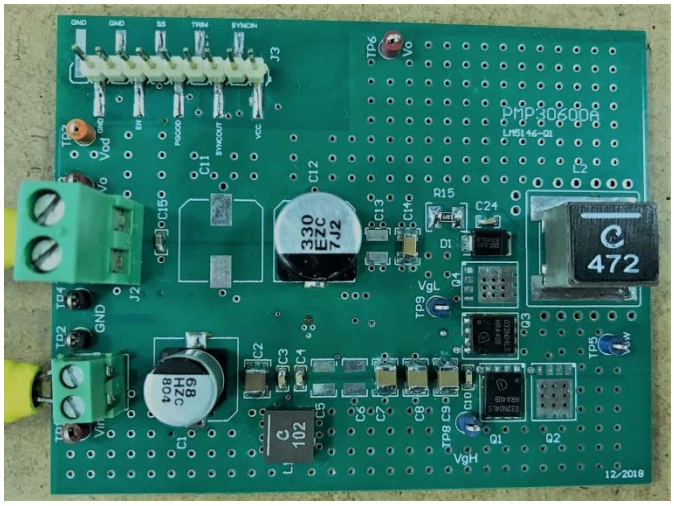
Min. Vout 5.045V (10A), max Vout 5.047V (No Load),

Output voltage variation 2.0mV, so 0.04%, negligible.

2.3 Thermal Images

Thermal image at 14V input and full load 10A after 20mins continuous operation [Rt = 23c]:





Name	Temperature
L1	44.7C
Q1	51.9C
Q3	52.7C
L2	53.3C
D1	49.9C
R15	49.9C

Temperature rise is below +25K, a proper design of the power stage with maximum efficiency results in relaxed thermal stress; this means higher reliability, best MTBF.

2.4 Dimensions

The extension of the board are 79 mm x 62 mm.

3 Waveforms

3.1 Switching

3.1.1 Switchnode D1

With input voltage set to 14V and 10A Iout results in the waveform shown in Figure 3.

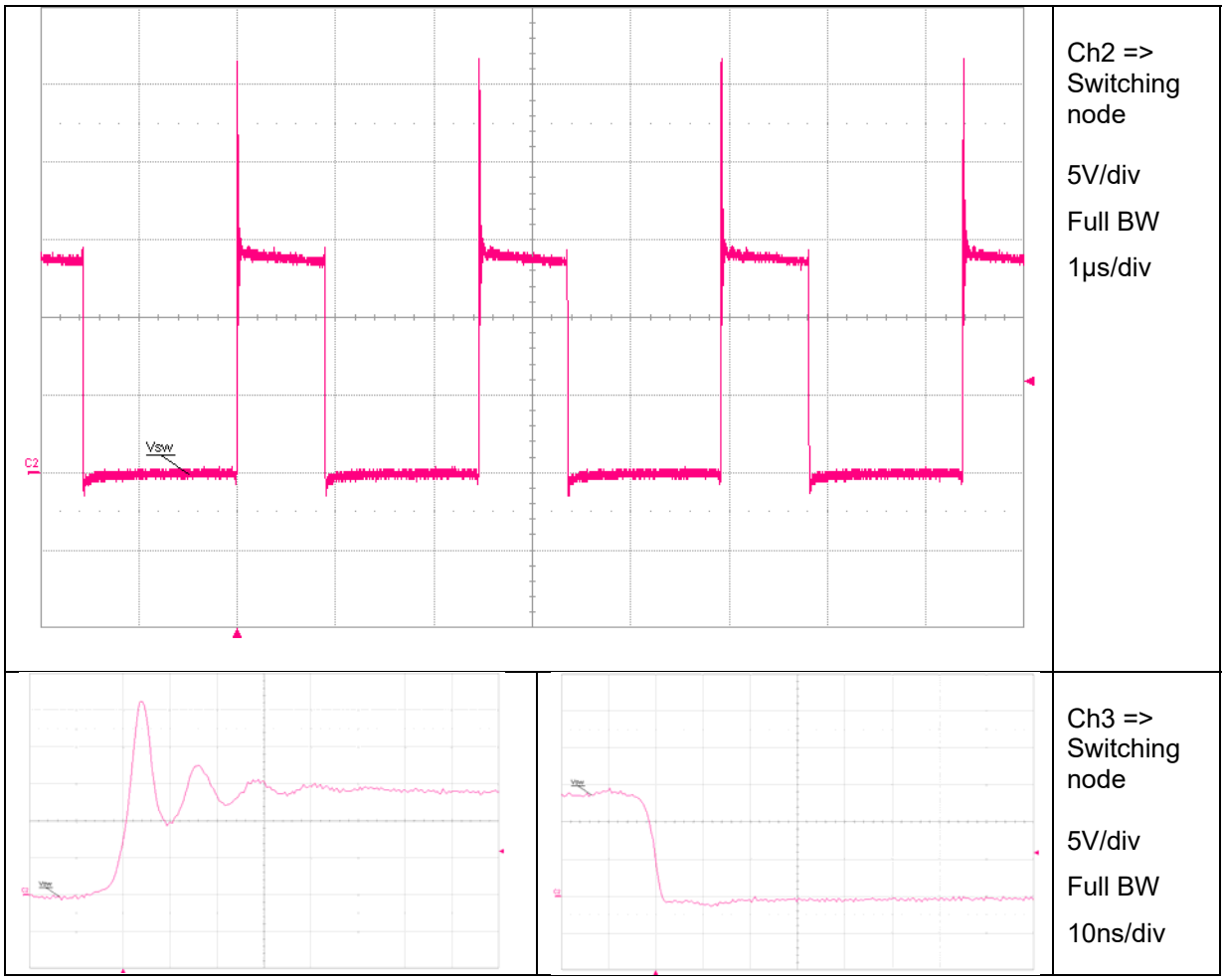
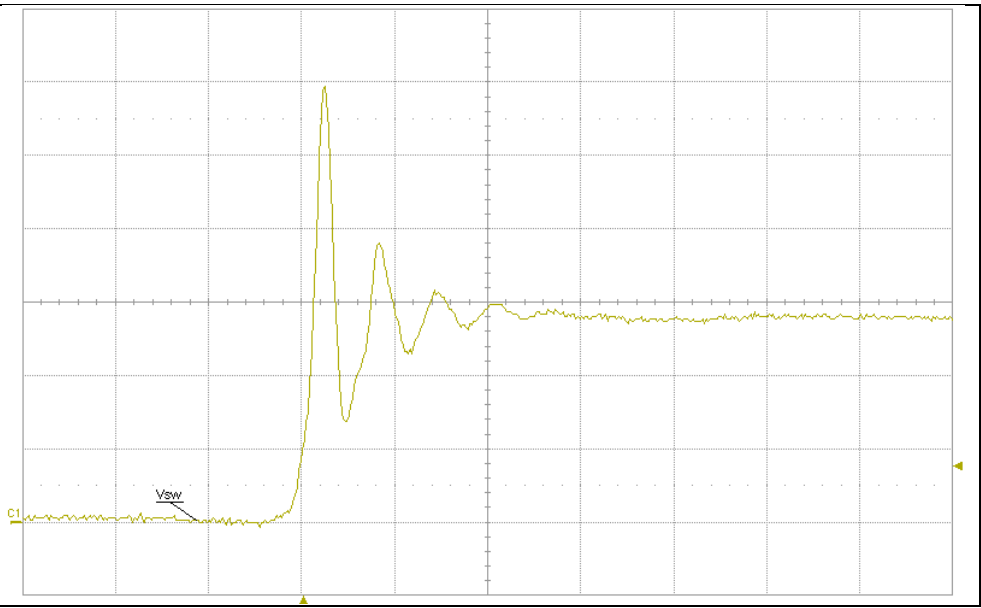


Figure 3

Nominal input voltage is 14V and the overshoot is less than 16V. Vds rating of BSC032N04LS is 40V – enough margin. To fight the 83MHz ringing further a RC snubber circuit was implemented to demonstrate RF suppression:

Measure ringing frequency at switch node w/ RF probe (no GND leads, use GND clip), here 83MHz – could cause trouble , radiated emissions:



Ch1 => Switching node

no snubber

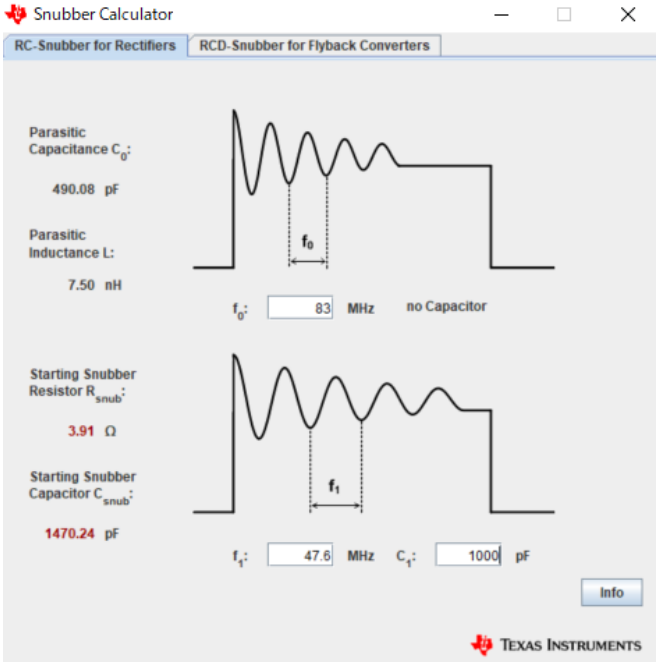
5V/div

full BW

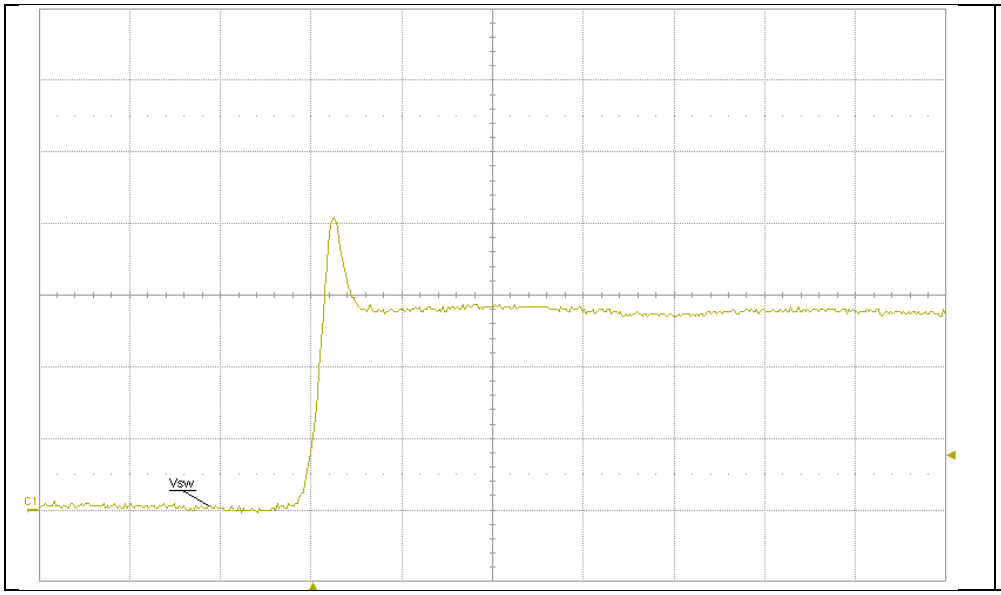
20ns/div

1) **Add capacitor from switch node to GND and the measure the shifted oscillation frequency.** here 1000pF resulted in 47.6MHz

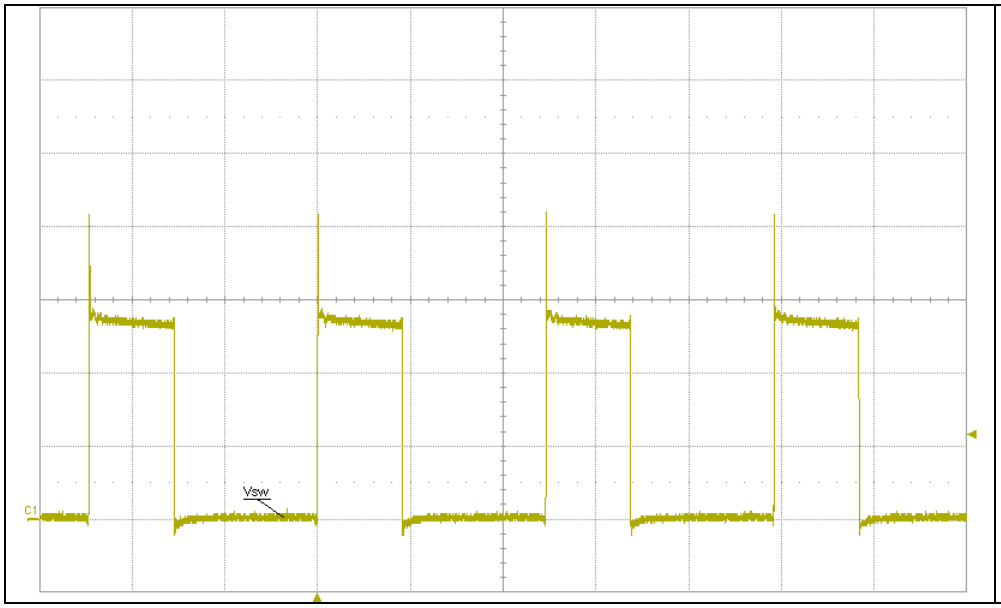
2) **Calculate the snubber register and capacitor by utilizing the Power stage designer**, Enter the ringing frequency w/o capacitor and shifted oscillation frequency w/ capacitor.



3) **add resistor in series and adjust capacitor value**,
here RC-snubber of 1500pF / 3.9 Ohm reduced overshoot from 16V to 6V:



Clamping network 1500pF / 3.9 Ohm reduces RF content at the switch node, less EMI !



It has to be stated that this hard clamping of the switch node causes a drop in efficiency of 0.24%, so roughly 120mW losses at the snubber resistor.

By experience could be said that a drop in efficiency from 0.2% to 0.5% is typically caused by adding the RC snubber circuit. For a middle power design like PMP30600B geometry 0805 or 1206 might fit, but for high power designs be aware of losses up to 500mW:

- 0603 <100mW
- 0805 <150mW
- 1206 <200mW
- 1210 <250mW
- 1812 <500mW
- 2010 <750mW
- 2512 <1W

3.1.2 Gate-Source of Low Side FET

With input voltage set to 14V and 10A Iout results in the waveform of low-side gate voltage shown in Figure 4.

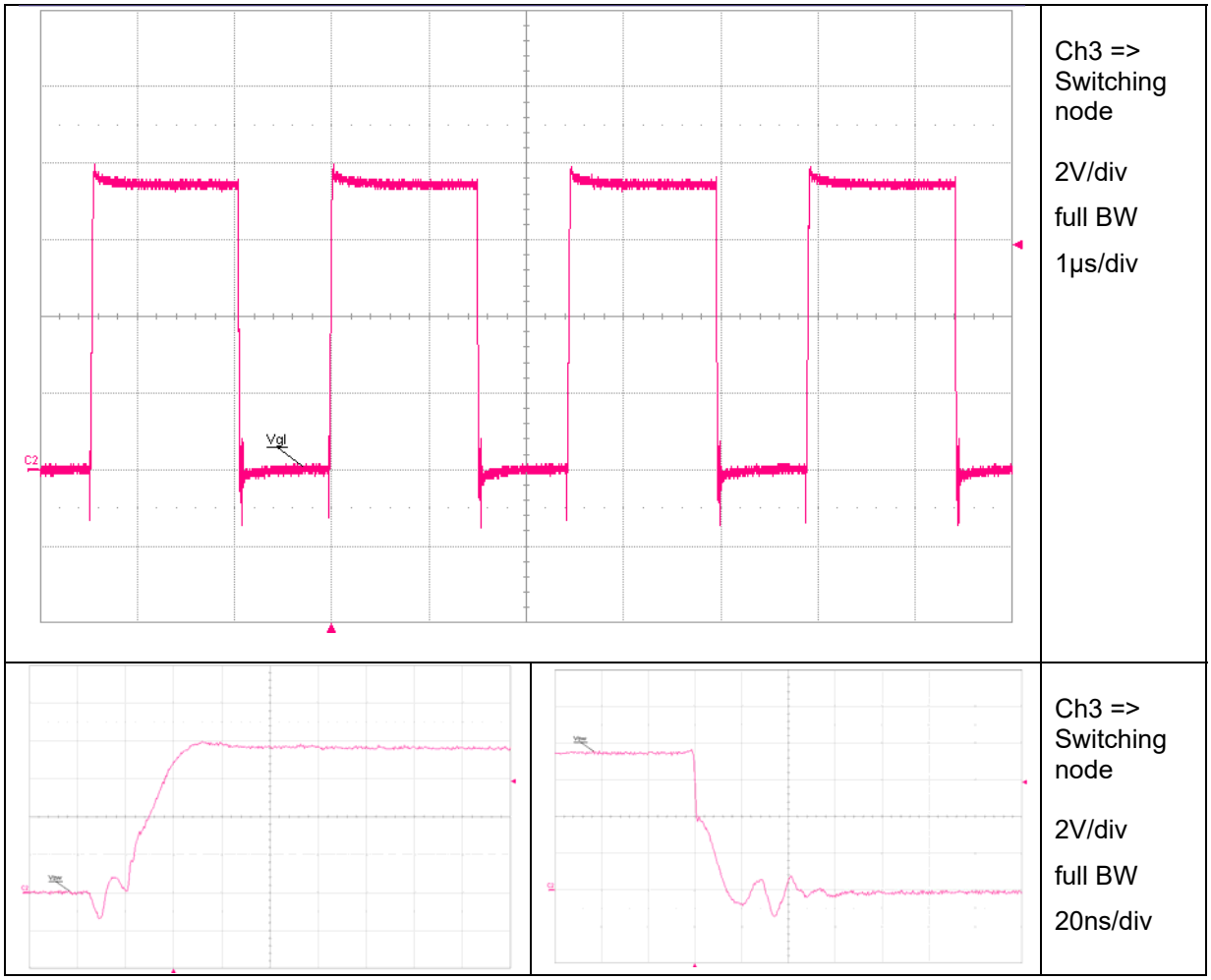


Figure 4 Low-side Gate voltage

3.1.3 Gate-Source of High Side FET

With input voltage set to 14V and 10A Iout results in the waveform of Hi-side gate to switch voltage shown in Figure 5.

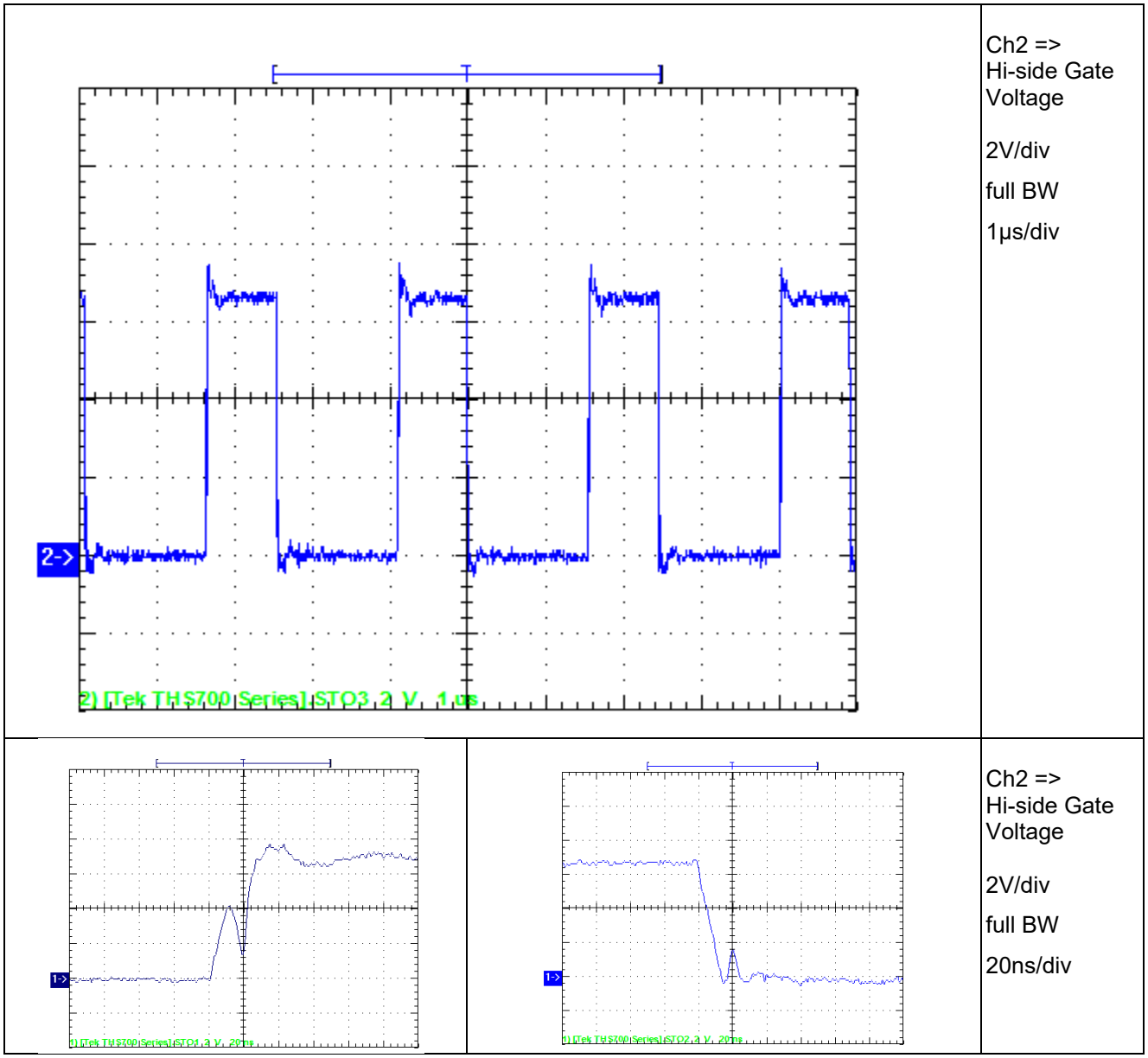
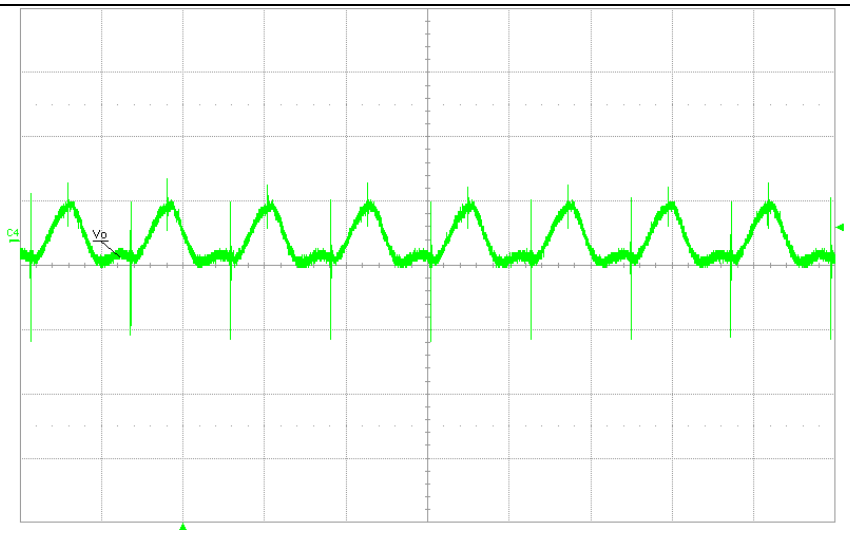


Figure 5 Hi-side Gate to switch voltage

To reach the Miller plateau around 3V and both sides are fast switching. Thanks to fast switching, switching losses would be small.

3.2 Output Voltage Ripple

The output ripple voltage is shown in Figure 6. The image was taken with 10A load 14V input at the output. The output ripple voltage is less than 50mV except noise.



Ch4 => output voltage 50mV/div

AC coupled

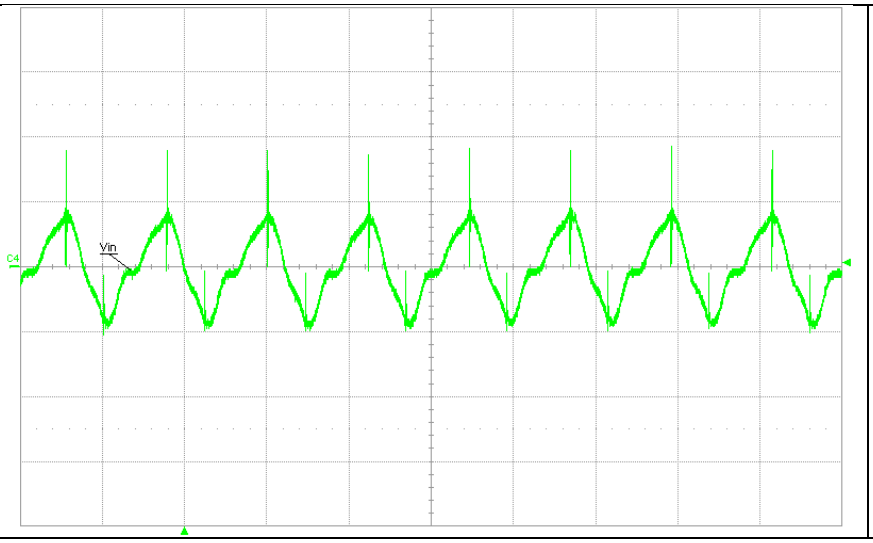
Full BW

2µs/div

Figure 6

3.3 Input Ripple Voltage

The input ripple voltage is shown in Figure 7. The image was taken with 10A load 14V input at the input.



Before passing through the PI filter

Ch4 => input voltage 200mV/div

AC coupled

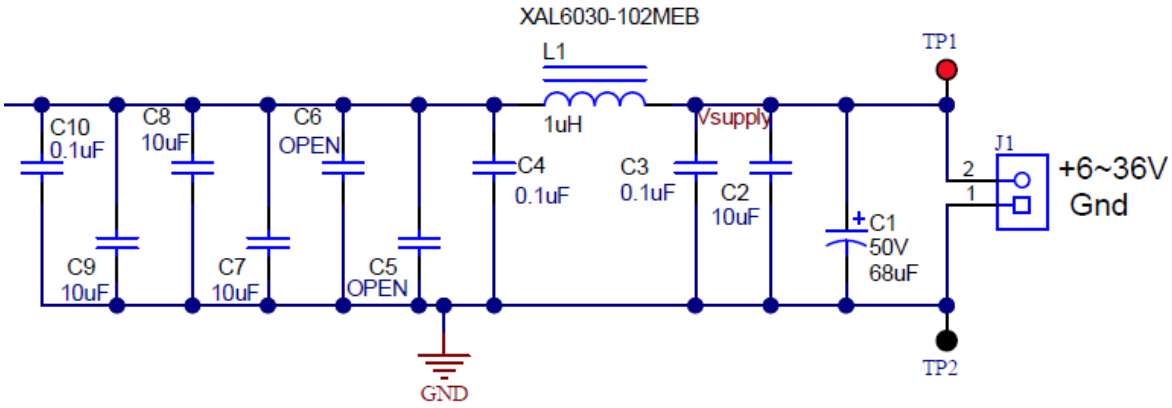
Full BW

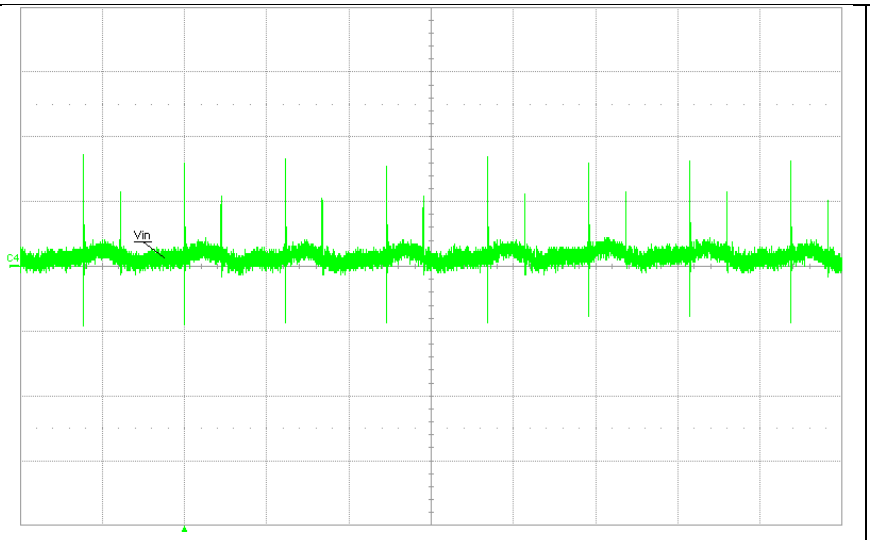
2µs/div

Figure 7

Input voltage ripple is around 360mV.

Finally the input voltage by using PI filter 3x10uF – 1.0uH – 10uF+68uF;
A small ceramic capacitor 100nF was added to suppress glitches:





After passing through the PI filter

Ch4 => input voltage 20mV/div

AC coupled

Full BW

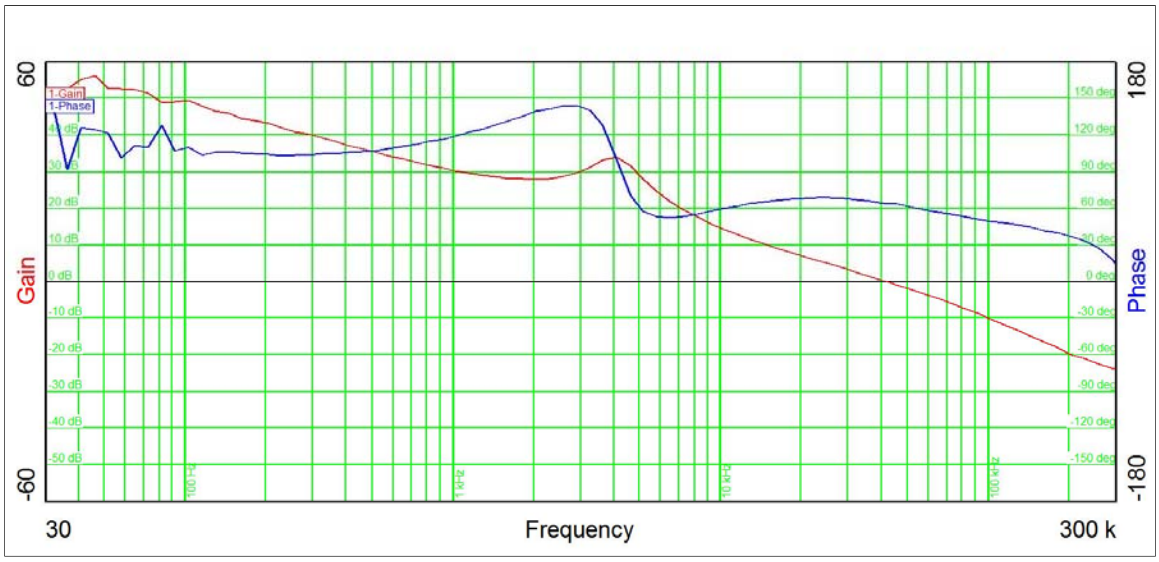
2µs/div

Input voltage ripple is reduced to 11mV; reduction rate is 1/33.

A tremendous reduction of reflected ripple resulted in better EMI behavior !
The inductor prevents the source from seeing the pulse currents – less conducted emissions.

3.4 Bode Plot

Figure below shows the loop response with 10A load and 14V input.



The bandwidth is measured with NWA Venable #3120. The crossover frequency is 42kHz, the phase margin more than 60 degrees. Slope at crossover is close to -1, here -1.18.

REMEMBER:

This analysis is a small signal analysis, shows the small signal behavior of the power supply.

The only true analysis is a large signal analysis, the system response on a load transient!

3.5 Load Transients

The Figure 8 shows the response to load transients. The load is switching from 5A to 10A. The input voltage was set to 14V.

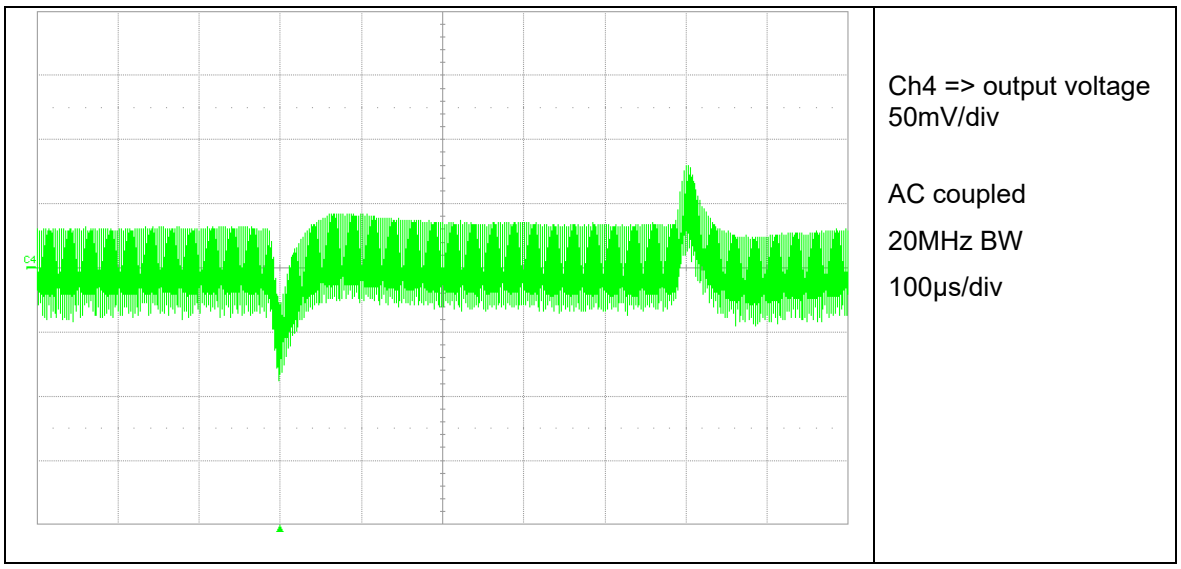


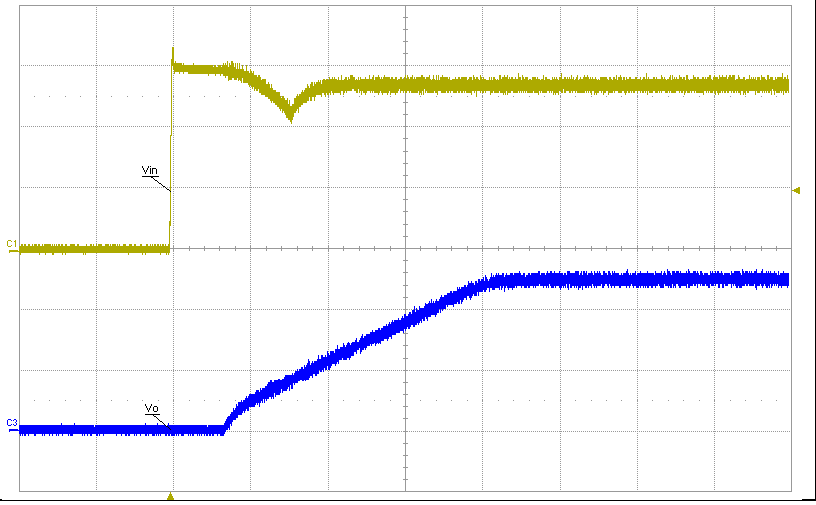
Figure 8

The voltage drop caused by 5A is around 85mV, so less than 2% of the output voltage 5V;
The combination output capacitor to loop bandwidth matches.

A proper calculation of the error amplifier compensation results in a stable design. For series production a phase margin >60 degrees and a gain margin <-15dB is recommended.

3.6 Start-up Sequence

The startup waveform is shown in the Figure 9. The input voltage was set at 14V, with 10A load at the output. Startup w/in 3.6ms, calculated 4ms:



Ch1=> input voltage
5V/div

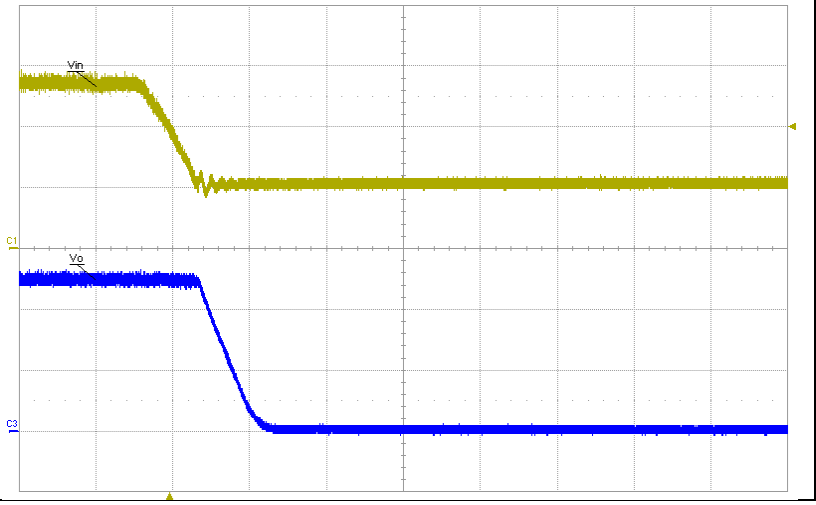
Ch2=> output voltage
2V/div

20MHz BW
1ms/div

Figure 9

3.7 Shutdown

The shutdown waveform is shown in the Figure 10. The input voltage was set at 14V, with 10A load on the output.



Ch1=> input voltage
5V/div

Ch2=> output voltage
2V/div

20MHz BW
2ms/div

Figure 10

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