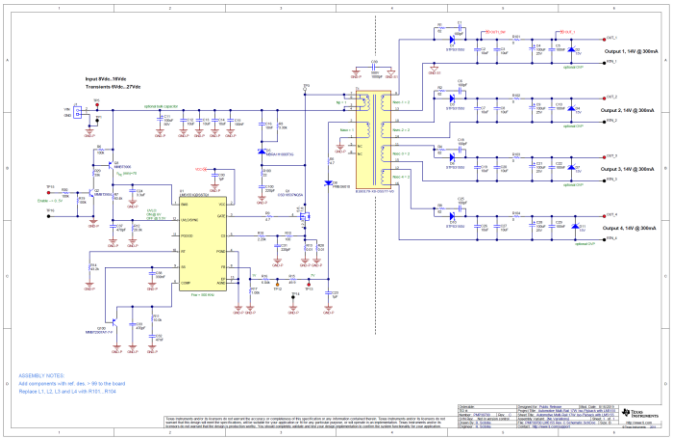
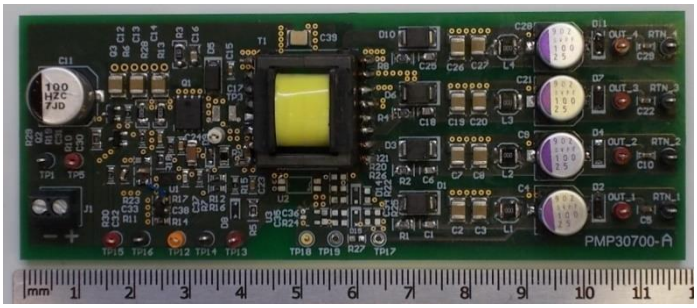
Test Report: PMP30700
Automotive Four-Rails 17-W Isolated Flyback Reference Design

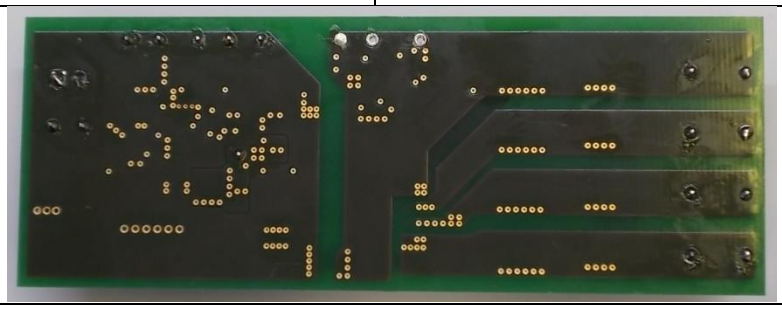
Description

The reference design PMP30700 Revision C is an isolated Flyback that supplies 4 independent rails; each of them delivers 14V @ 300mA. The voltage feedback loop is closed to primary side, therefore avoiding the optocoupler and increasing the reliability of the converter. The high switching frequency (500KHz) allows the use of a small transformer and filter components. A digital enable input removes the bias voltage to the controller, therefore reducing the current consumption practically to zero.

The reference design PMP30700 Rev_C has been built on PMP30700 Rev_A PCB.







1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1. Voltage and Current Requirements

PARAMETER	SPECIFICATIONS
Input Voltage (nominal)	8 VDC – 16 VDC
Input Voltage (transients)	6 VDC – 27 VDC
Output Voltages # 1,2,3,4:	14 V
Output Currents # 1,2,3,4:	300 mA

1.2 Required Equipment

- 0…30 VDC, (minimum current limit 5 Arms), DC constant voltage source (VS1)
- 4 x Electronic loads, (constant current range 0…1 A)
- Oscilloscope (min. 100 MHz bandwidth)
- Optional: infrared camera

1.3 Testing Conditions

The power supply has four outputs and the feedback loop is closed on the primary side by means of an auxiliary winding. On the revision B2 of the schematic it is shown the possibility to close the feedback loop to the output # 1. If this variant is used, all components inside the shaded area, marked as “PSR” should not be populated. The converter is enabled by supplying 5V on TP15, referred to TP16.

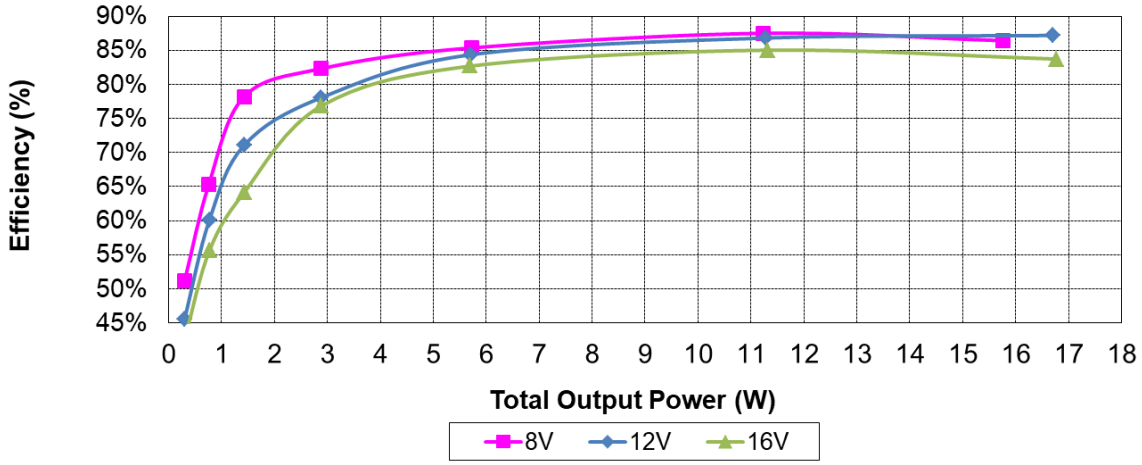
a) Connect the source VS1 to J1-2 and J1-1.
b) Connect the loads to test the points “OUT_#1…4” with the grounds to “RTN_#1…4”.
c) Turn on Vs1 (6 VDC…27 VDC).
d) Supply TP15, ground to TP16, with 3. 5V.

2 Testing and Results

2.1 Efficiency Graph and Data

2.1.1 Efficiency Graph:

The efficiency graph versus total output power, is shown below.
The input voltage has been set to 8, 12 and 16 VDC.



2.1.2 Efficiency Data:

The efficiency graph reports the data from the table shown below.

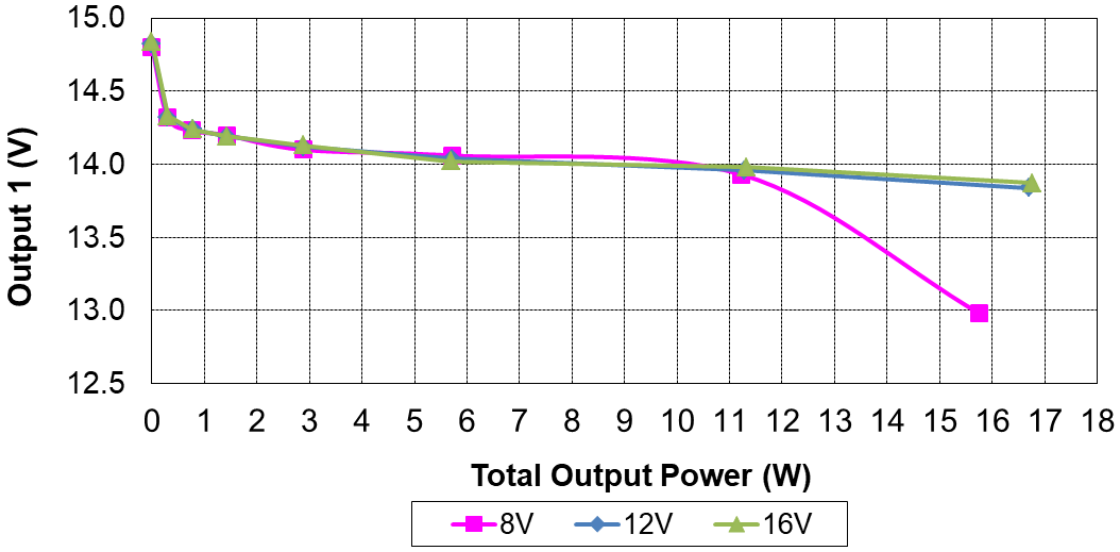
Vin(V)	Iin(mA)	Pin (W)	Vout_1 (V)	Iout_1 (mA)	Vout_2 (V)	Iout_2 (mA)	Vout_3 (V)	Iout_3 (mA)	Vout_4 (V)	Iout_4 (mA)	Pout (W)	Efficiency (%)
8.055	16.62	0.134	14.80	0	14.81	0	14.82	0	14.81	0	0	0%
8.034	73.09	0.587	14.32	5.23	14.34	5.23	14.36	5.24	14.36	5.24	0.300	51.16%
8.023	144.57	1.160	14.23	13.9	14.25	13.8	14.28	12.8	14.28	12.6	0.757	65.28%
8.038	226.6	1.821	14.20	24.5	14.20	25.0	14.23	25.2	14.22	25.5	1.424	78.19%
8.018	436.1	3.497	14.10	51.3	14.11	51.3	14.14	51.3	14.14	49.9	2.878	82.31%
8.014	836	6.700	14.06	102.2	14.07	101.7	14.09	101.2	14.09	101.2	5.720	85.37%
8.010	1602	12.83	13.93	200.9	13.92	200.8	13.95	206.1	13.96	197.7	11.23	87.51%
8.016	2274	18.23	12.98	302.5	12.95	306.0	12.97	304.5	12.97	302.0	15.76	86.43%

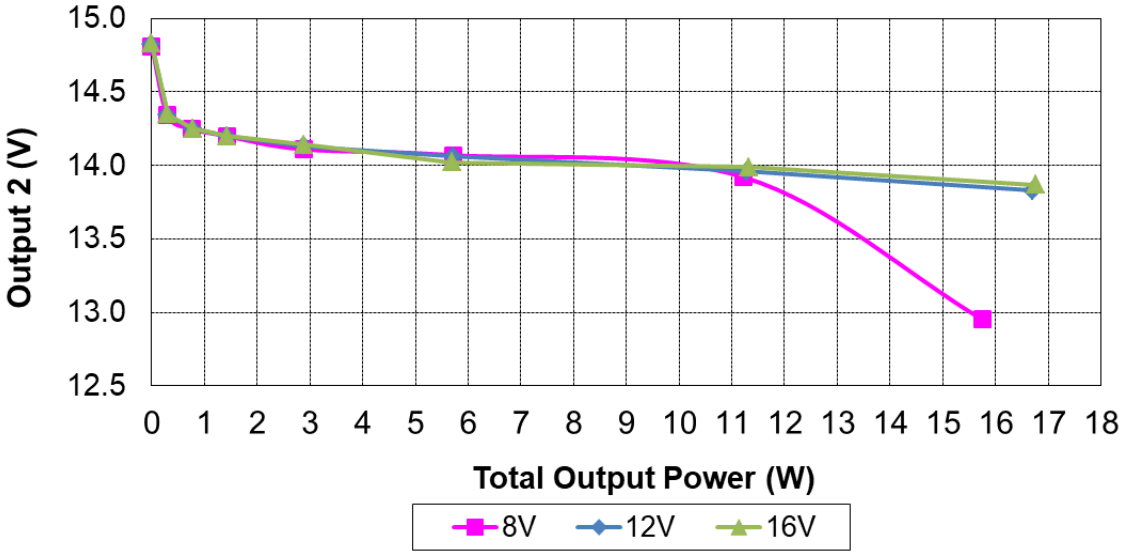
Vin(V)	Iin(mA)	Pin (W)	Vout_1 (V)	Iout_1 (mA)	Vout_2 (V)	Iout_2 (mA)	Vout_3 (V)	Iout_3 (mA)	Vout_4 (V)	Iout_4 (mA)	Pout (W)	Efficiency (%)
12.00	11.78	0.141	14.82	0	14.82	0	14.84	0	14.83	0	0	0%
12.03	54.81	0.659	14.32	5.23	14.34	5.23	14.36	5.24	14.36	5.24	0.300	45.56%
12.02	106.60	1.281	14.24	13.8	14.25	13.8	14.28	13.8	14.28	12.6	0.770	60.11%
12.04	166.4	2.004	14.19	24.5	14.20	25.0	14.23	25.2	14.22	25.5	1.424	71.05%
12.00	307.9	3.695	14.12	51.3	14.13	51.4	14.15	51.4	14.16	49.9	2.885	78.06%
12.03	563	6.769	14.04	102.2	14.06	101.6	14.09	101.1	14.08	101.1	5.711	84.37%
12.02	1081	12.99	13.96	200.9	13.96	201.4	13.99	206.6	14.00	198.2	11.28	86.82%
12.04	1592	19.17	13.84	302.5	13.83	303.0	13.85	300.8	13.86	300.7	16.71	87.18%

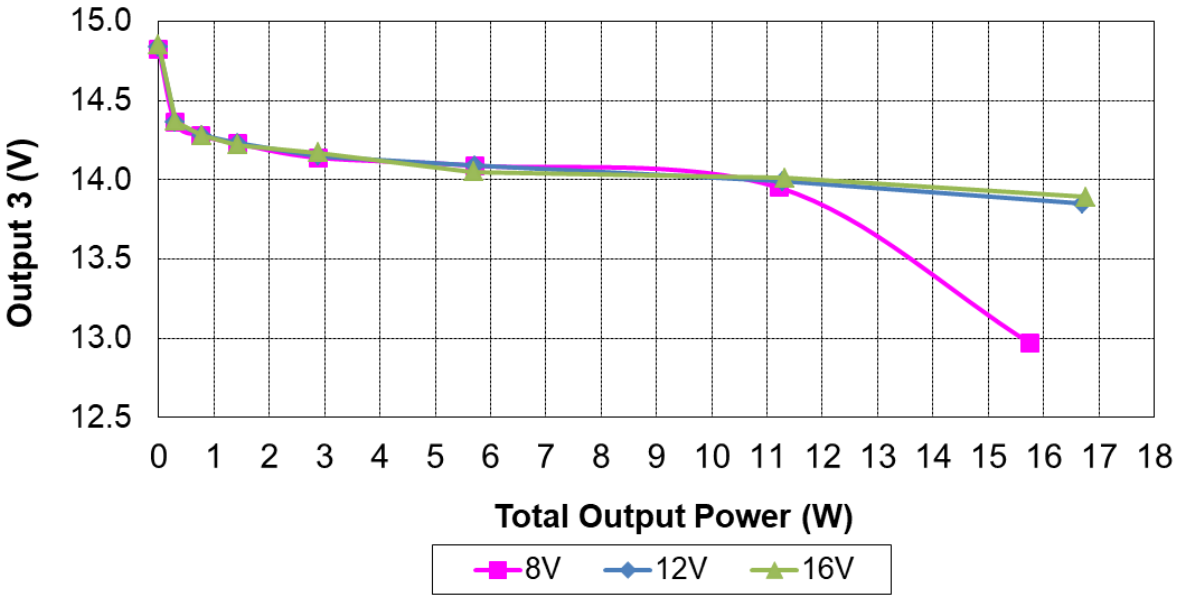
Vin(V)	Iin(mA)	Pin (W)	Vout_1 (V)	Iout_1 (mA)	Vout_2 (V)	Iout_2 (mA)	Vout_3 (V)	Iout_3 (mA)	Vout_4 (V)	Iout_4 (mA)	Pout (W)	Efficiency (%)
16.07	9.98	0.160	14.84	0	14.83	0	14.85	0	14.84	0	0	0%
16.00	44.12	0.706	14.33	5.23	14.35	5.24	14.37	5.24	14.37	5.24	0.301	42.61%
16.01	86.52	1.385	14.24	13.8	14.25	13.8	14.28	13.8	14.28	12.6	0.770	55.60%
16.08	138.1	2.221	14.19	24.5	14.20	25.0	14.22	25.2	14.22	25.5	1.424	64.11%
16.01	234.7	3.758	14.13	51.3	14.14	51.4	14.17	51.5	14.16	49.9	2.888	76.86%
16.05	429	6.887	14.02	102.2	14.02	101.6	14.05	100.9	14.06	101.0	5.695	82.69%
16.02	831	13.31	13.98	200.9	13.99	201.8	14.01	207.0	14.02	198.6	11.32	85.03%
16.00	1252	20.03	13.87	302.5	13.87	303.1	13.89	300.7	13.90	301.9	16.77	83.73%

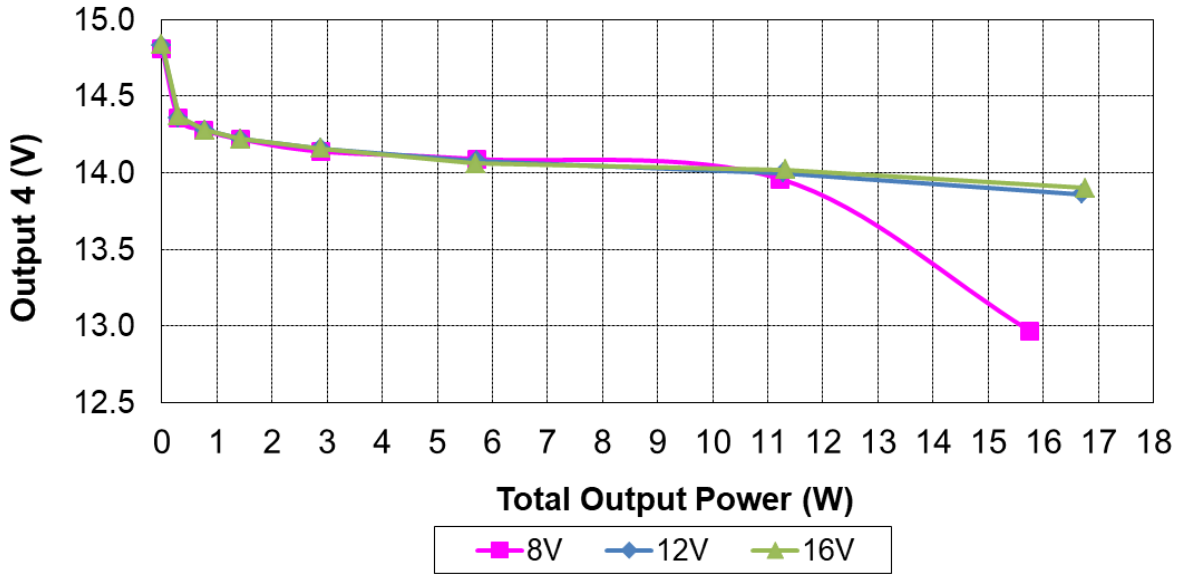
2.2 *Static Output Voltage Variation versus Load*

The output voltage regulation of each output, versus total output power, is shown in the graphs below. Each output has been loaded with the same current, up to full load.









The cross regulation of the converter has been tested by fully loading two outputs and keeping the remaining two unloaded. The input voltage Vin was set to 8V, 12V and 16V.

Vin(V)	Vout_1 (V)	Iout_1 (mA)	Vout_2 (V)	Iout_2 (mA)	Vout_3 (V)	Iout_3 (mA)	Vout_4 (V)	Iout_4 (mA)	Pout (W)
8.0	13.72	300	13.73	300	14.98	0	15.05	0	8.24
12.0	13.76	300	13.77	300	14.98	0	15.04	0	8.26
16.0	13.75	300	13.78	300	14.98	0	15.03	0	8.26

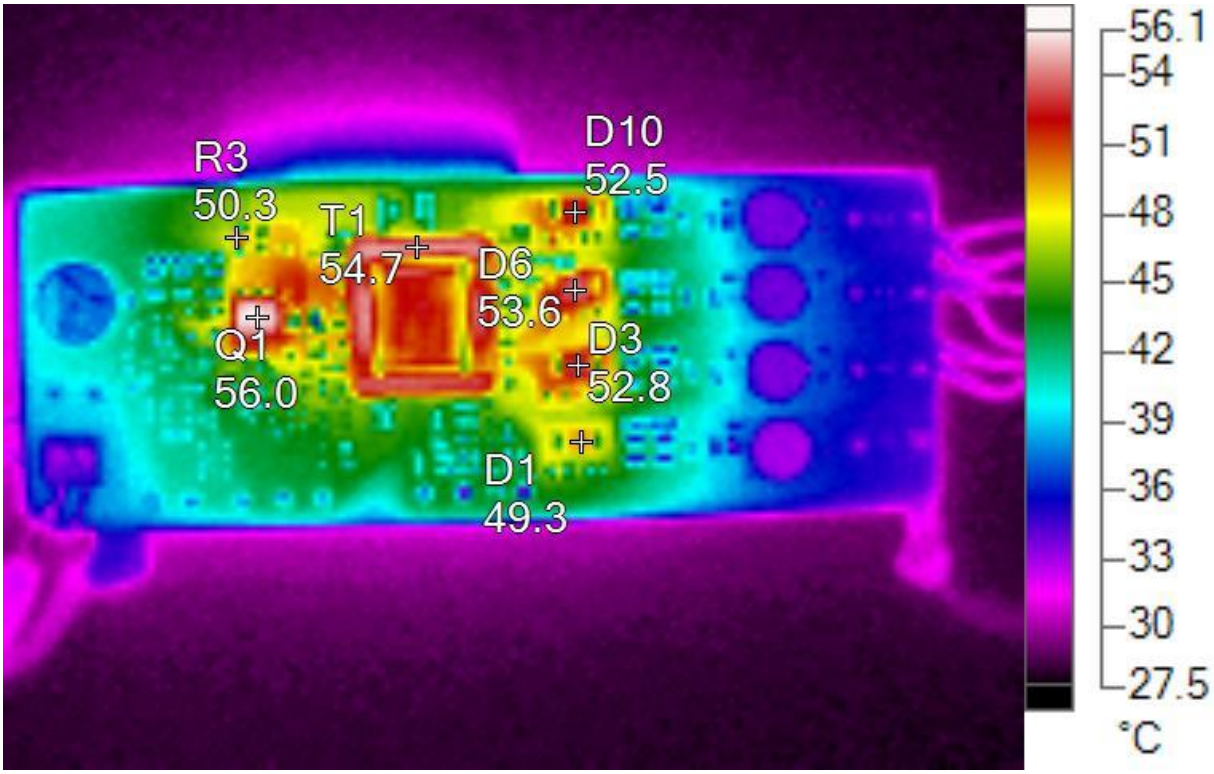
2.3 Board Dimensions

The board dimensions are 118.11 mm x 43.82 mm, height 15 mm.

2.4 Thermal Images

The graph and table below describe the thermal behavior of the converter placed horizontally on the bench, at full load, with ambient temperature of 25.5°C and in still air condition.

Conditions: Vin = 8 VDC, all outputs fully loaded; image taken after 30 minutes.



Main Image Markers

Name	Temperature	Emissivity	Background
Q1	56.0°C	0.96	25.5°C
R3	50.3°C	0.96	25.5°C
D10	52.5°C	0.96	25.5°C
D6	53.6°C	0.96	25.5°C
D3	52.8°C	0.96	25.5°C
D1	49.3°C	0.96	25.5°C
T1	54.7°C	0.96	25.5°C

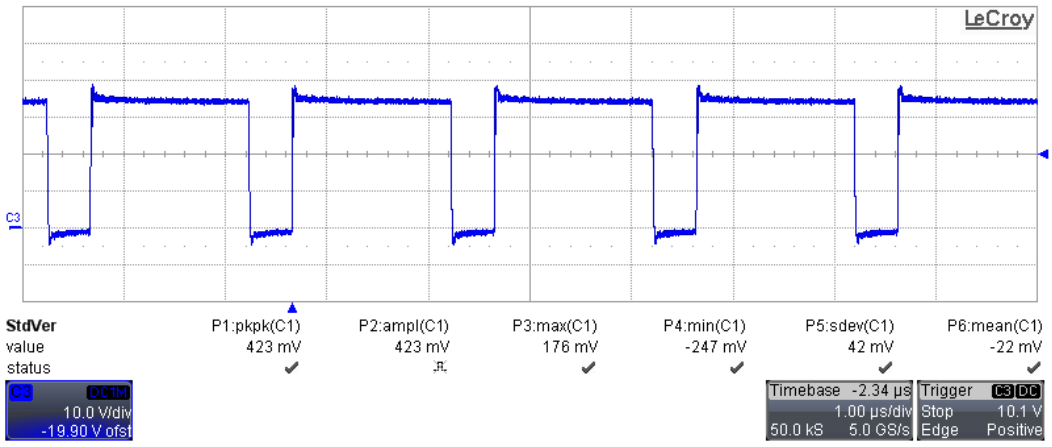
3 Waveforms

3.1.1 Switching Waveforms on Q1-Drain at Full Load

The switching waveforms have been measured by supplying the converter at 6V and 27V input voltage, with all outputs fully loaded.

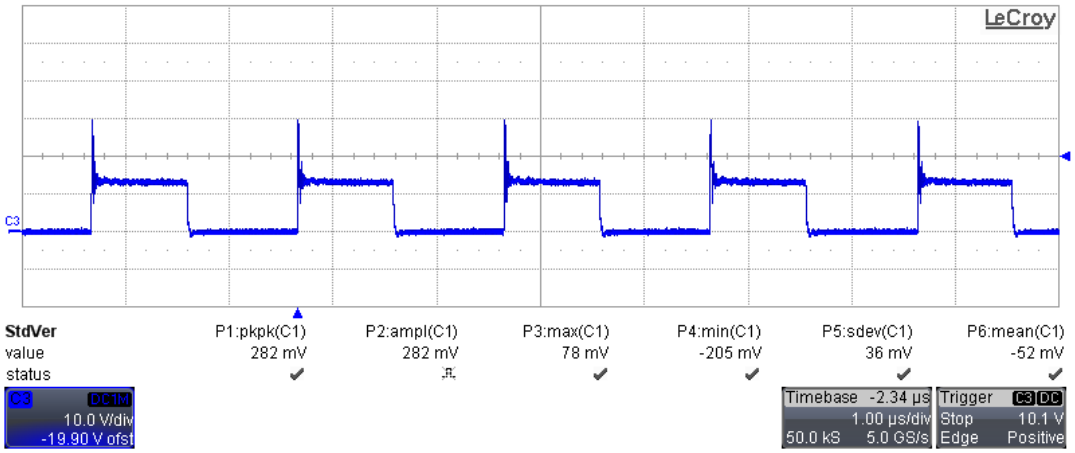
C3: Q1-Vds (10 V/div, 1 usec/div, no BWL)

Vin = 27 VDC



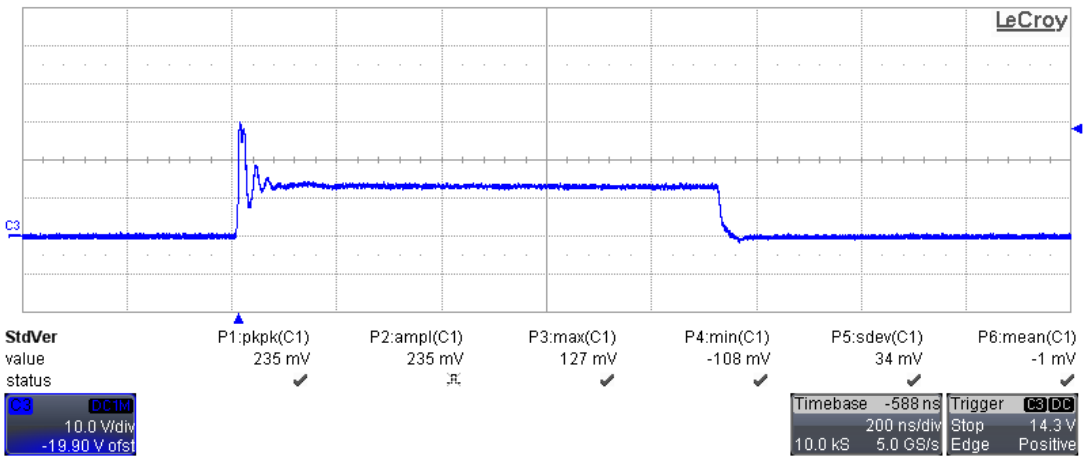
C3: Q1-Vds (10 V/div, 1 usec/div, no BWL)

Vin = 6 VDC



C3: Q1-Vds (10 V/div, 200 nsec/div, no BWL)

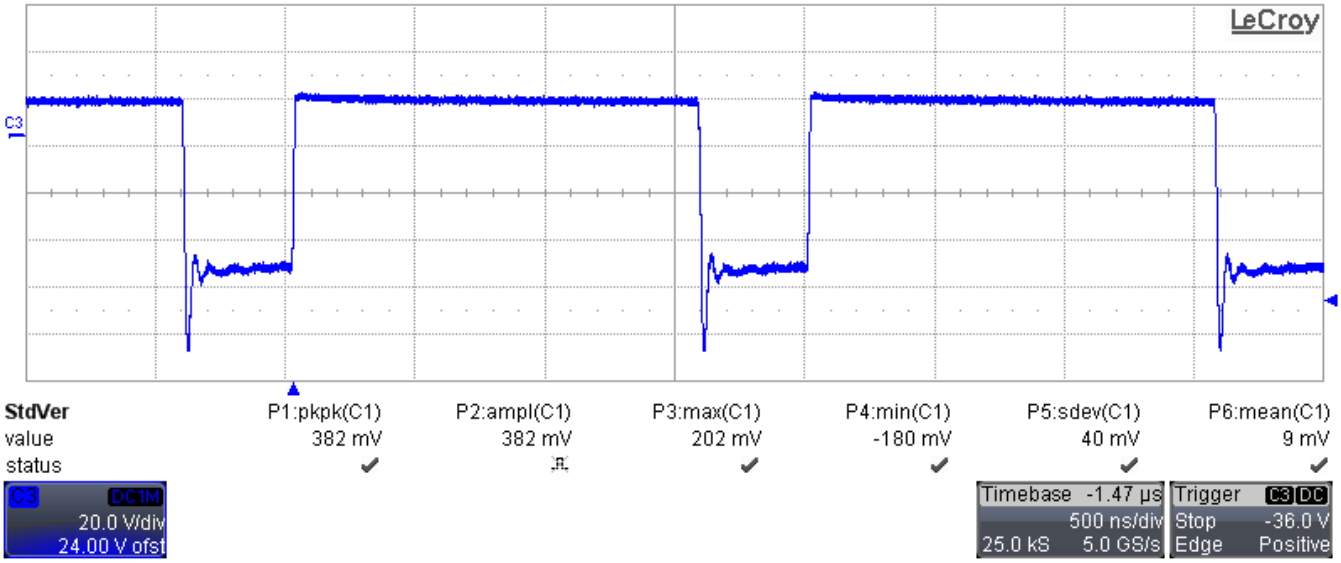
Zoomed waveform at same conditions of above:



3.1.2 Switching Waveform D10 Anode referred to RTN_4

The switching waveform on diode D10 has been measured by supplying the converter at 27V input voltage, with all outputs fully loaded.

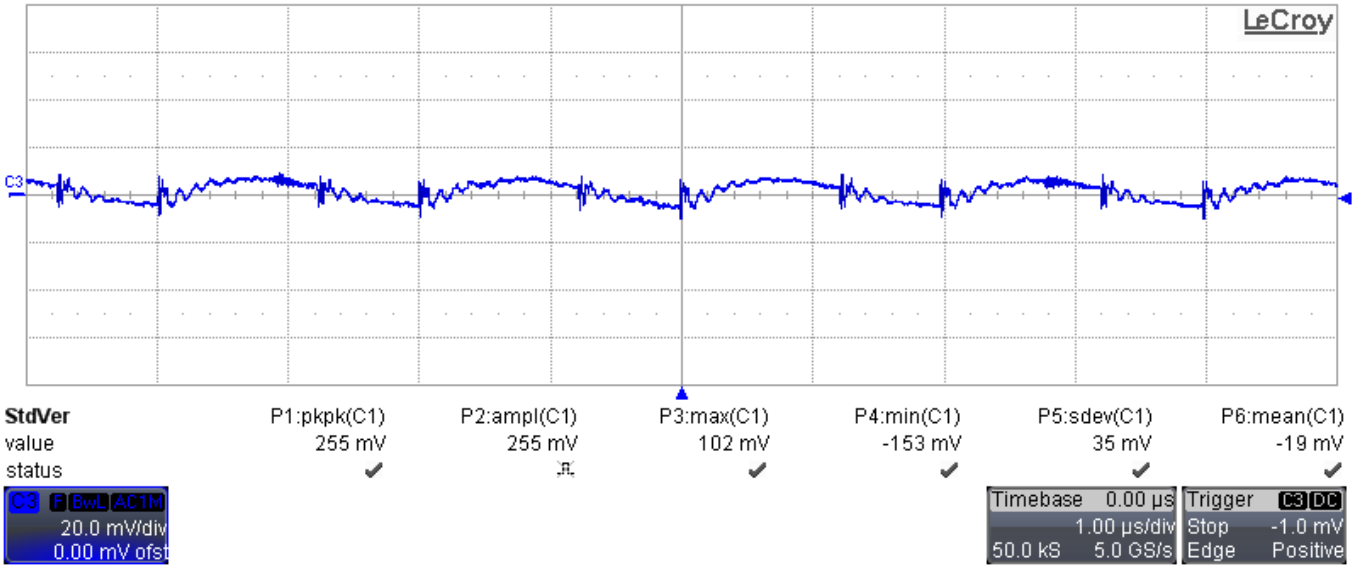
C3: D10-Anode to RTN_4 Voltage (20 V/div, 500 nsec/div, DC coupling, no BWL)



3.2 Output Voltage Ripple

All outputs deliver the same voltage and current, and have identical filters. Since we measured the same peak-peak ripple voltage on each output, we reported only the screenshot of the output # 4, taken at 12V input and with all outputs fully loaded.

C3: Ripple voltage on output # 4 (20 mV/div, 1 usec/div, AC coupling, 1 MHz BWL)



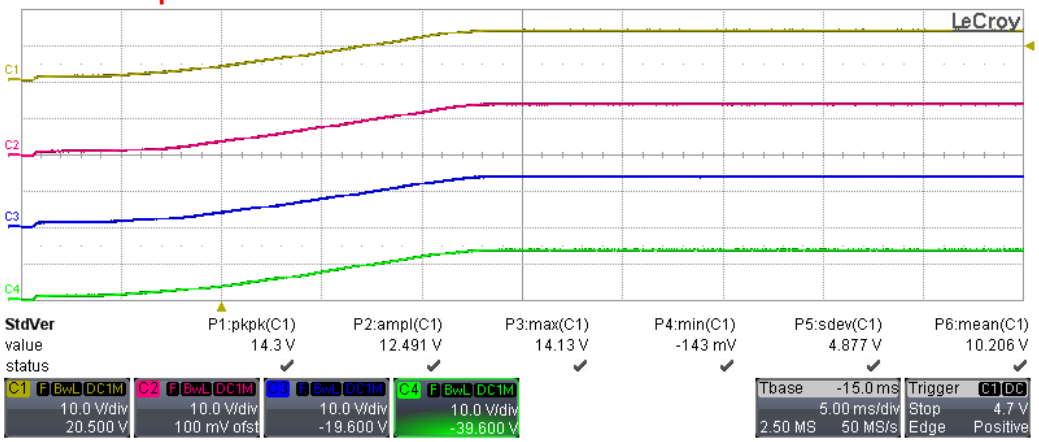
3.3 Start-up

Conditions: all outputs fully loaded (first screenshot) and unloaded (second screenshot), with Vin = 12V.

C1, C2, C3, C4 = Output # 1, 2, 3, 4

All waveforms @ 10 V/div, 5 msec/div, DC coupling, 20 MHz BWL

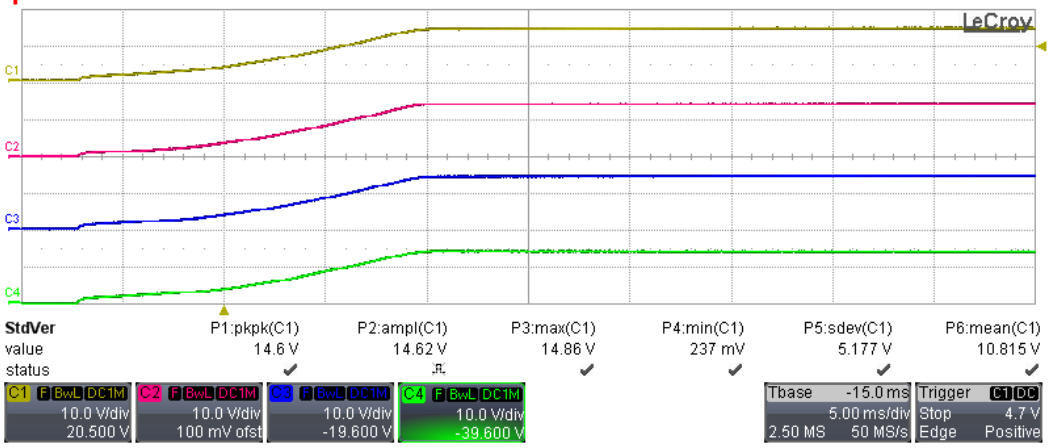
Full load on all outputs



C1, C2, C3, C4 = Output # 1, 2, 3, 4

All waveforms @ 10 V/div, 5 msec/div, DC coupling, 20 MHz BWL

All outputs unloaded

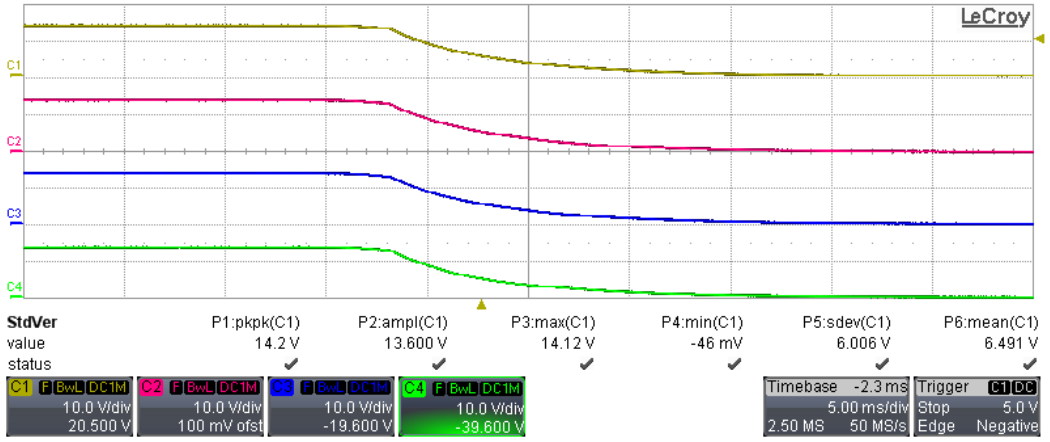


3.4 Shut Down

C1, C2, C3, C4 = Output # 1, 2, 3, 4

All waveforms @ 10 V/div, 5 msec/div, DC coupling, 20 MHz BWL

Full load on all outputs

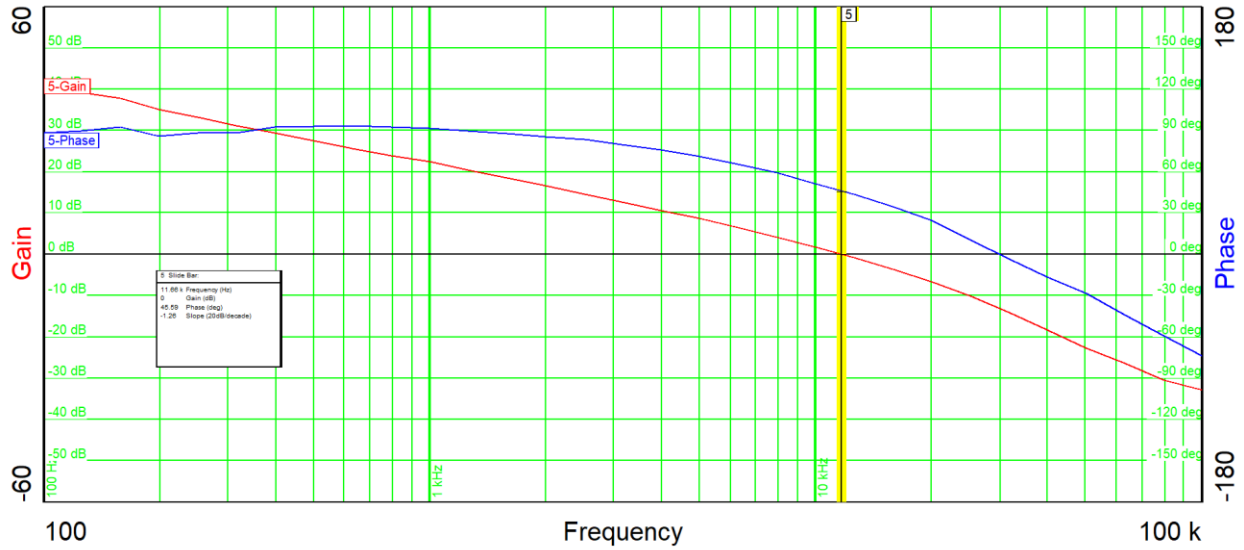


4 Bode Plot

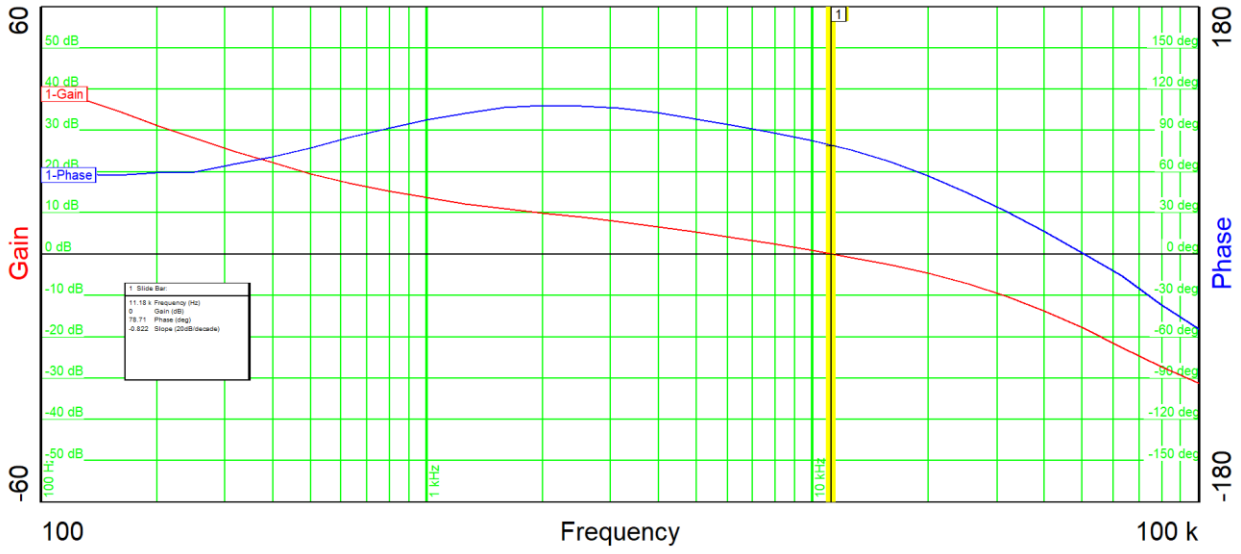
The following graph shows the bode plot of the converter, when supplied respectively at 6.7VDC, 12VDC and 27VDC with all outputs fully loaded.
Here are the results, in terms of crossover frequency, phase margin and gain margin:

Input Voltage:	6.7 V	12 V	27 V
Crossover frequency:	11.66 KHz	11.18 KHz	3.007 KHz
Phase margin:	45.59 deg.	78.71 deg.	61.13 deg.
Gain margin:	13.02 dB	18.07 dB	29.12 dB

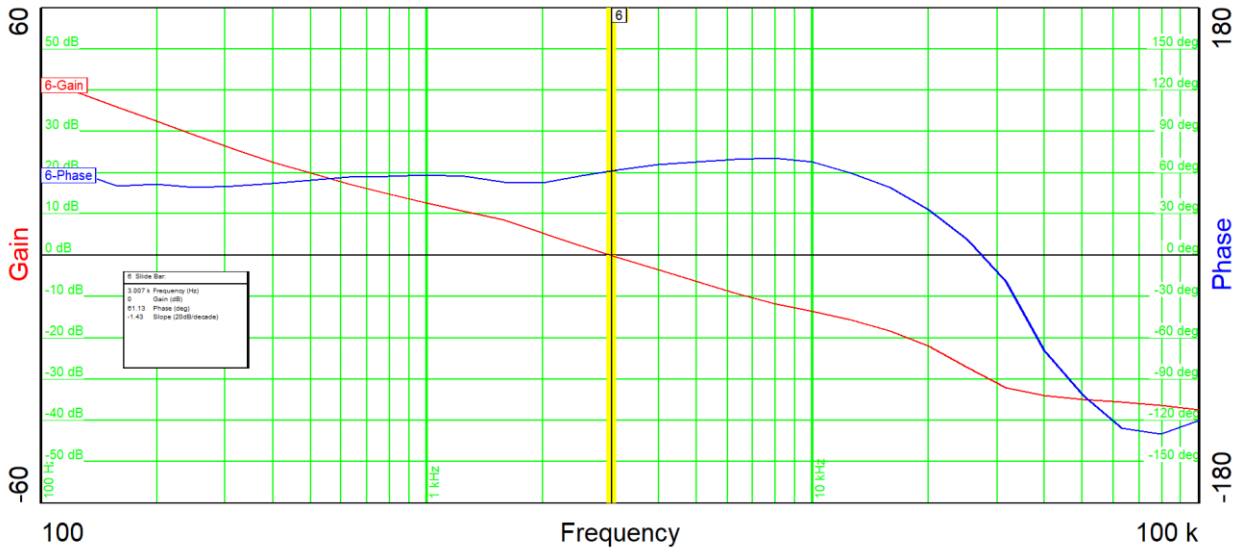
6.7Vin:



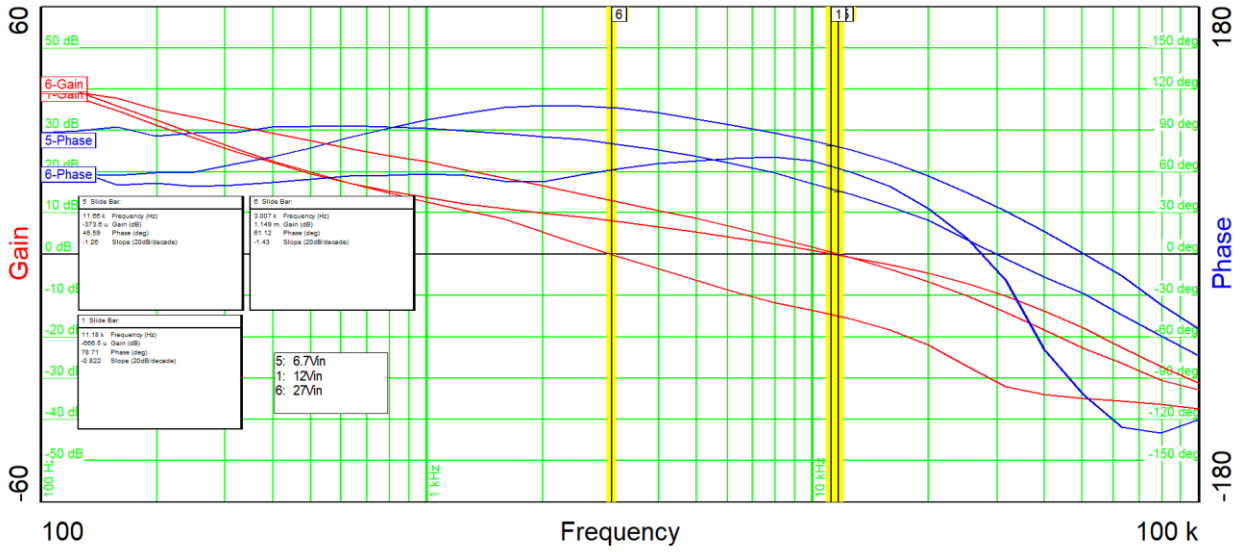
12Vin:



27Vin:



All curves together:



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