Test Report: PMP22835

Isolated IGBT and SiC Driver Bias Supply Reference Design for Traction-Inverter Applications

1 Description

This isolated open-loop LLC transformer driver converter provides dual 20-V and –4-V outputs up to 6 W for traction-inverter applications. The LLC topology allows the transformer to have significant leakage inductance, but a much smaller primary-secondary capacitance, which significantly reduces common-mode current injection through the bias transformer. It offers a high level of integration, low cost, and high efficiency in a compact form factor.

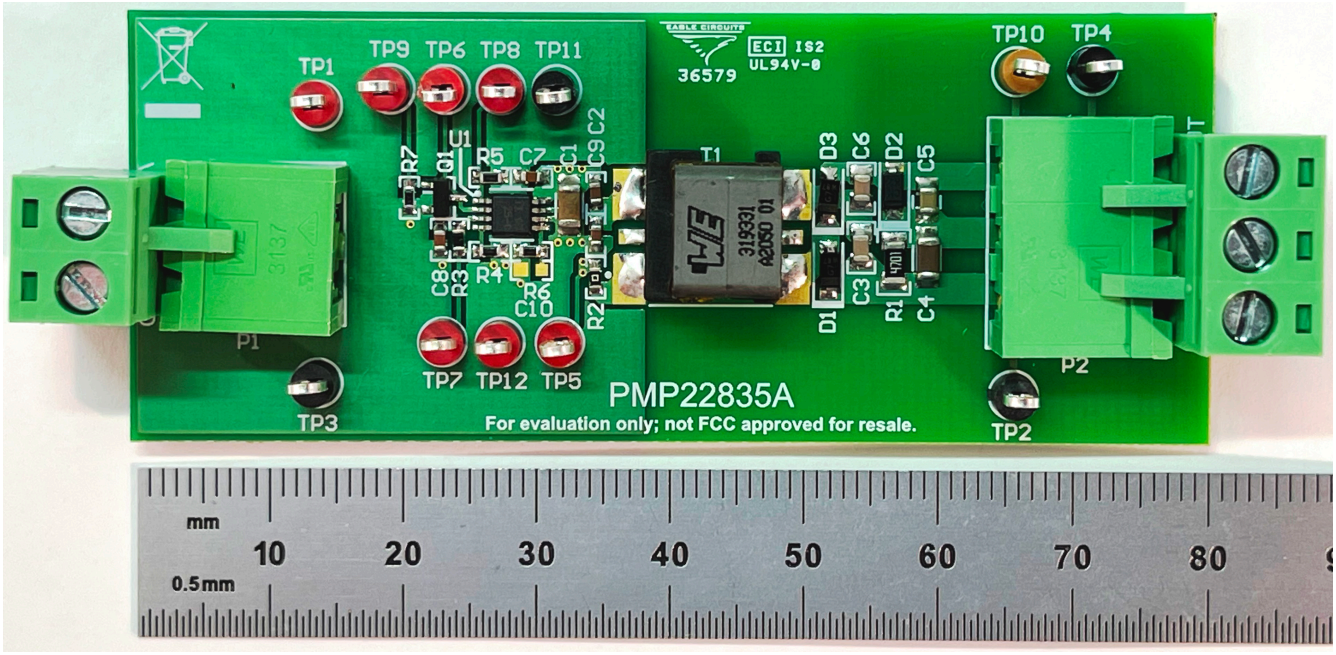


Figure 1-1. Top Side of PCB

2 Test Prerequisites

2.1 Voltage and Current Requirements

Table 2-1. Voltage and Current Requirements

Parameter	Specifications
Input voltage range	24 V, ±1 V (regulated)
Output voltage and current	20 V and –4 V, 300 mA (balanced), 6 W maximum
Switching frequency	1 MHz
Isolation	Yes, 2500 VAC (1 s)
Topology	Open-loop LLC transformer driver

2.2 Required Equipment

- Resistive loads (two resistor decade boxes), 6 W
- Power supply, regulated, 24 V and 0.5 A minimum
- Oscilloscope and probes
- Digital multimeters

3 Testing and Results

3.1 Thermal Images

This thermal image shows the operating temperature of the top side of the board with a 24-VDC input and the +20 V and –4 V at 200-mA output at room temperature and no air flow.

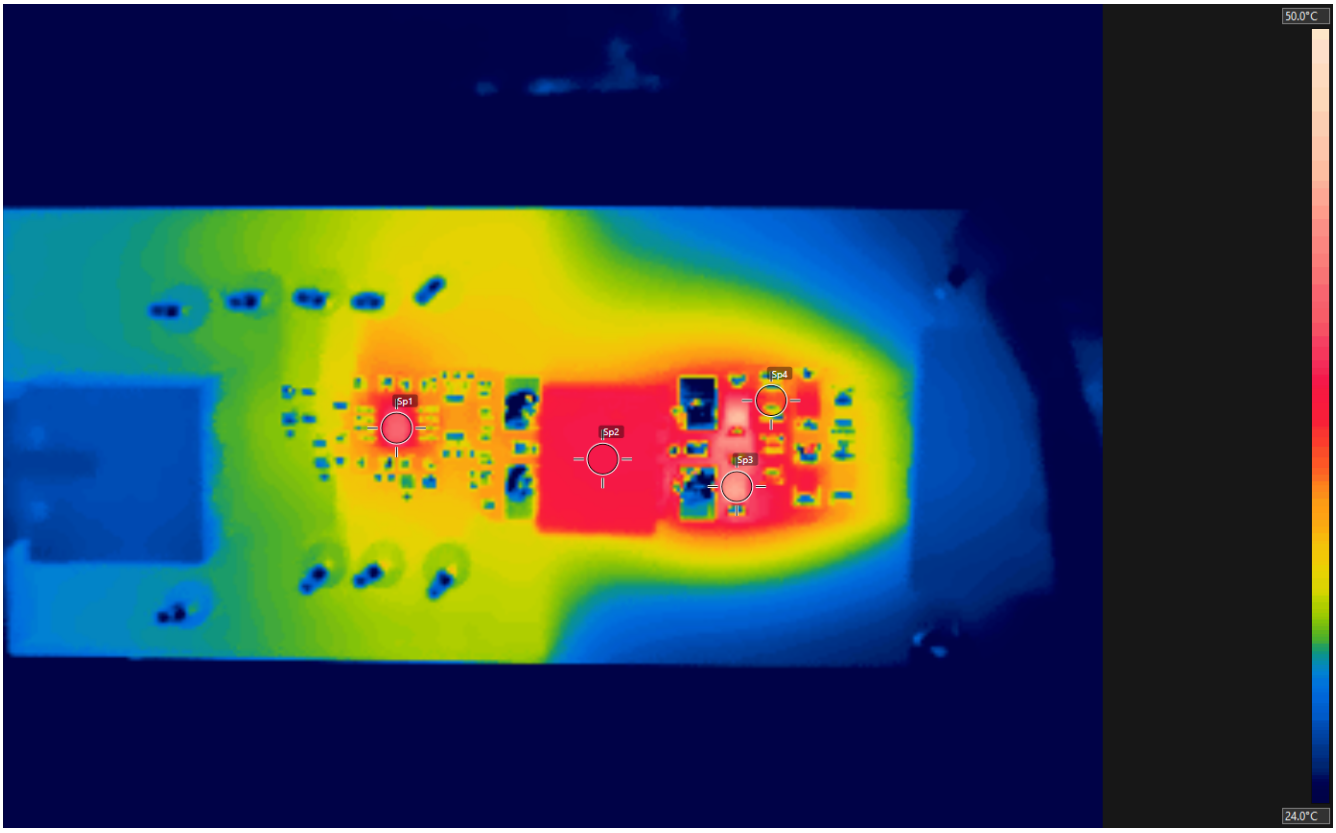


Figure 3-1. Top-Side Thermal Image With 200-mA Load

Measurement Location	Temperature (°C)
Sp1	41.7
Sp2	38.9
Sp3	44.6
Sp4	36.4

The following thermal image shows the operating temperature of the top side of the board with a 24-VDC input and the +20 V and –4 V at 100-mA output at room temperature and no air flow.

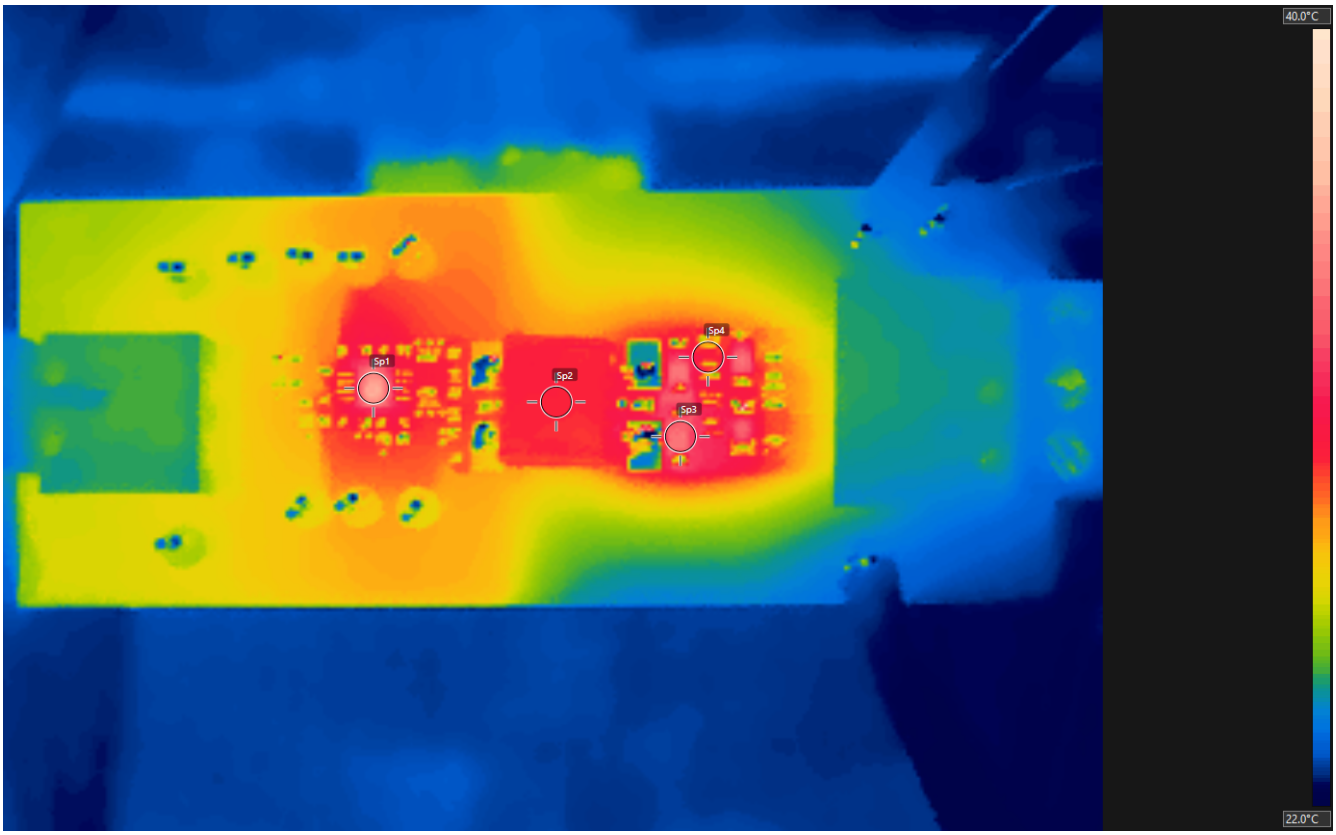


Figure 3-2. Top-Side Thermal Image With 100-mA Load

Measurement Location	Temperature (°C)
Sp1	36.3
Sp2	30.4
Sp3	34.4
Sp4	30.7

3.2 Efficiency and Power Dissipation Graph

This graph displays the efficiency and power dissipation of the converter with a 24-VDC input voltage.

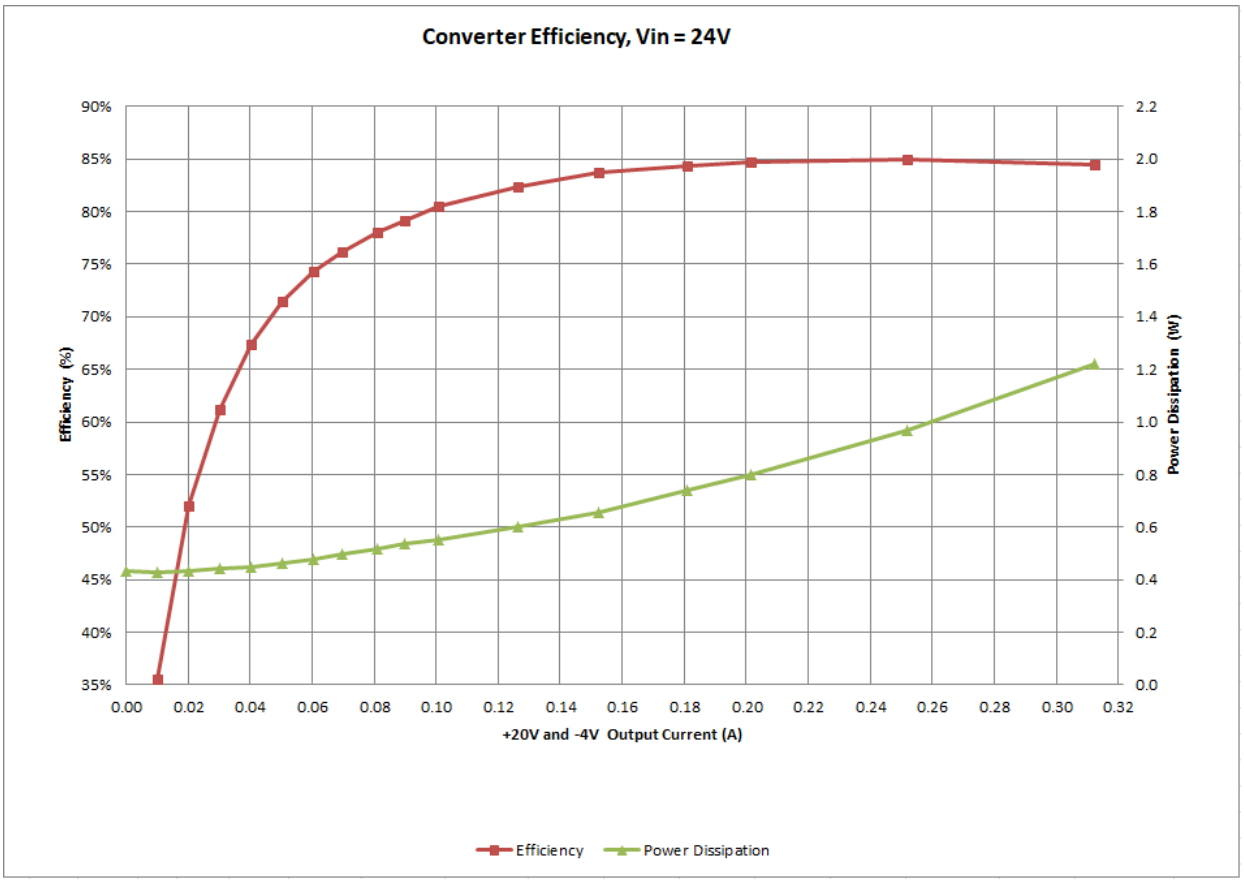


Figure 3-3. Efficiency Graph

3.3 Efficiency and Power Dissipation Data

Vin	Iin	Vsec total	Vout1	Iout1	Vout2	Iout2	Po	Pin	Efficiency	Pdiss (W)
24.012	0.0181	25.32	20.275	0.0000	-5.038	0.00000	0.000	0.435	0.0%	0.435
24.010	0.0278	23.69	18.655	0.0100	-5.033	0.01002	0.238	0.667	35.6%	0.430
24.008	0.0375	23.36	18.323	0.0201	-5.032	0.02006	0.469	0.900	52.1%	0.432
24.006	0.0475	23.21	18.174	0.0300	-5.031	0.03006	0.697	1.140	61.1%	0.443
24.004	0.0573	23.09	18.058	0.0402	-5.031	0.04019	0.927	1.375	67.4%	0.448
24.002	0.0673	22.96	17.925	0.0503	-5.032	0.05025	1.154	1.615	71.4%	0.461
24.000	0.0776	22.88	17.851	0.0605	-5.031	0.06052	1.384	1.862	74.3%	0.479
23.999	0.0869	22.82	17.783	0.0697	-5.032	0.06962	1.589	2.085	76.2%	0.497
24.007	0.0982	22.73	17.695	0.0809	-5.033	0.08086	1.838	2.357	78.0%	0.519
24.005	0.1070	22.65	17.615	0.0898	-5.033	0.08970	2.032	2.569	79.1%	0.536
24.003	0.1175	22.57	17.530	0.1006	-5.035	0.10043	2.269	2.820	80.4%	0.552
24.003	0.1430	22.39	17.357	0.1264	-5.035	0.12621	2.829	3.432	82.4%	0.604
24.001	0.1687	22.23	17.193	0.1526	-5.030	0.15275	3.391	4.049	83.8%	0.658
24.000	0.1970	22.02	17.008	0.1810	-5.037	0.18077	3.988	4.728	84.4%	0.740
24.003	0.2173	21.92	16.891	0.2015	-5.030	0.20140	4.417	5.216	84.7%	0.799
24.002	0.2668	21.61	16.562	0.2518	-5.041	0.25120	5.437	6.404	84.9%	0.967
24.001	0.3266	21.21	16.169	0.3123	-5.038	0.31170	6.620	7.839	84.5%	1.219

Figure 3-4. Efficiency and Power Dissipation Data

3.4 Cross-Load Voltage Regulation

VIN (V)	VOUT 20V (V)	IOUT 20V (A)	VOUT -4V (V)	IOUT -4V (A)	Vsec (V)
24	19.02	5mA	-5.081	0	24.10
24	18.60	10mA	-5.104	0	23.71
24	18.26	20mA	-5.103	10mA	23.36
24	18.11	30mA	-5.103	20mA	23.20
24	17.78	60mA	-5.103	50mA	22.88
24	17.62	80mA	-5.104	70mA	22.72
24	17.45	100mA	-5.105	90mA	22.55

Figure 3-5. Cross-Loading Regulation Values Up To 100 mA

3.5 Voltage Regulation Graph

This graph displays the total rectified secondary output voltage of the converter with a 24-VDC input voltage.

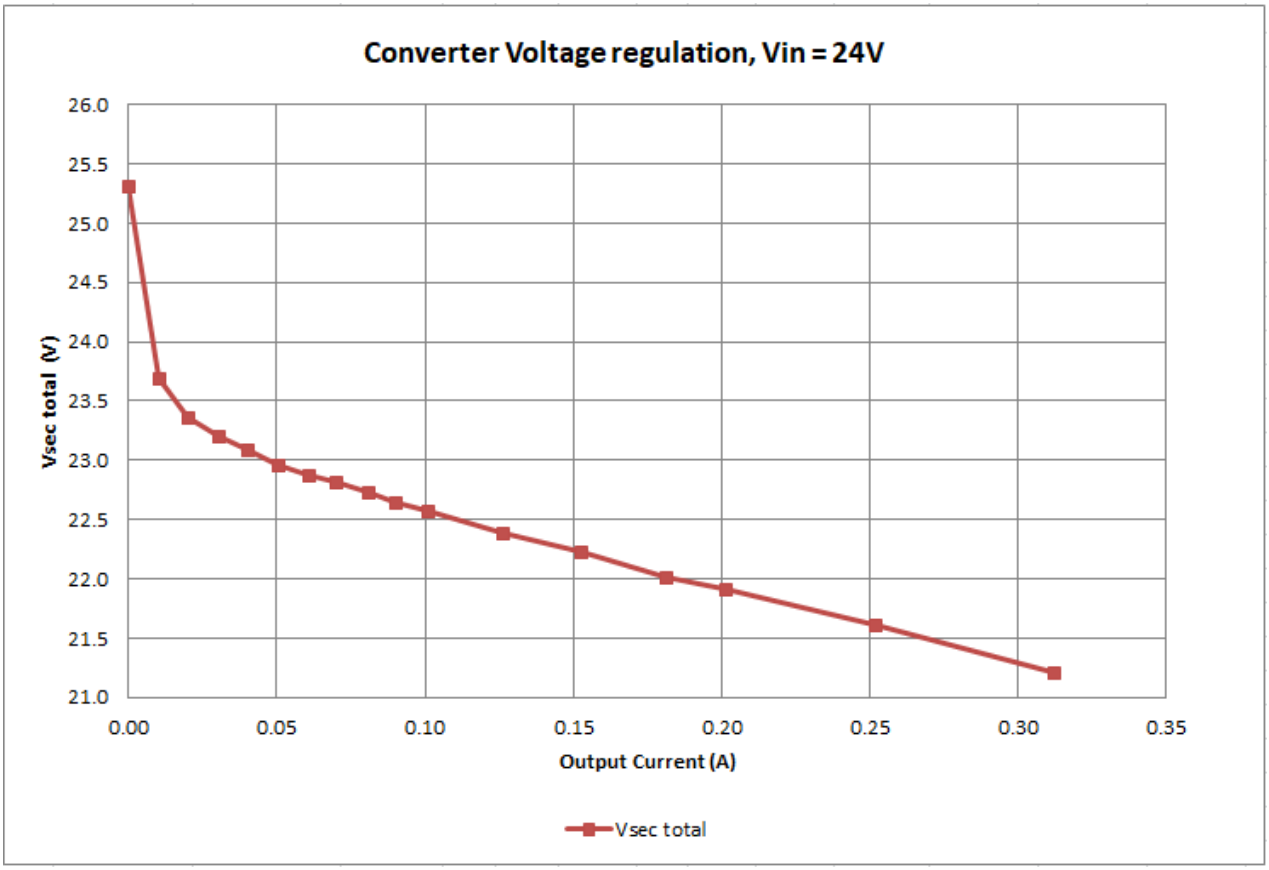
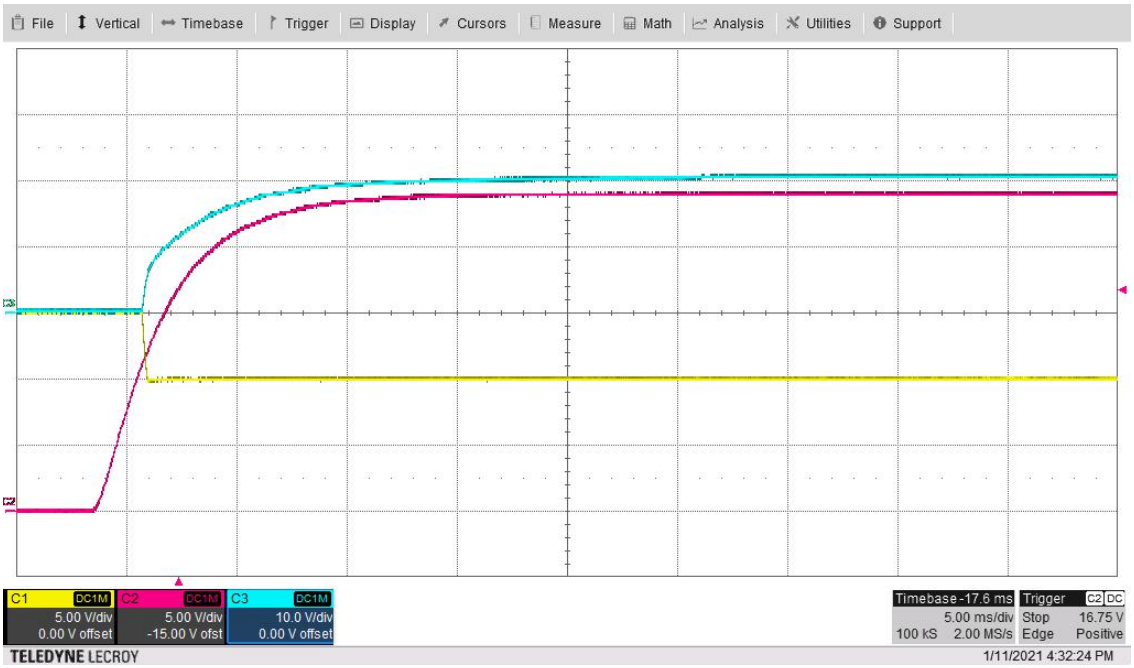


Figure 3-6. Converter Voltage Regulation for Vin of 24 V

4 Waveforms

4.1 Start-up Sequence

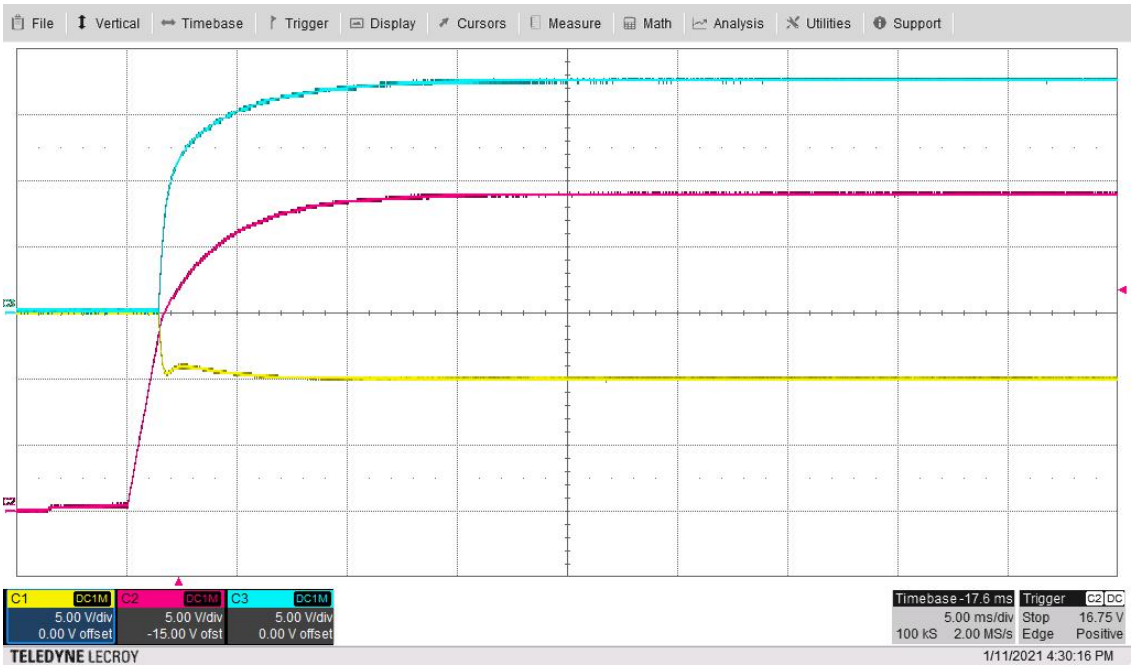
The following waveform shows the output voltage start-up waveform (20 V in Blue and –4 V in Yellow) after the application of 24-V input (Red) with each output *loaded to 0 mA*.



Vin and –4 V: 5 V/div, 20 V: 10 V/div, 5 ms/div, 750 MHz BWL

Figure 4-1. Output Voltage Start-up Waveform

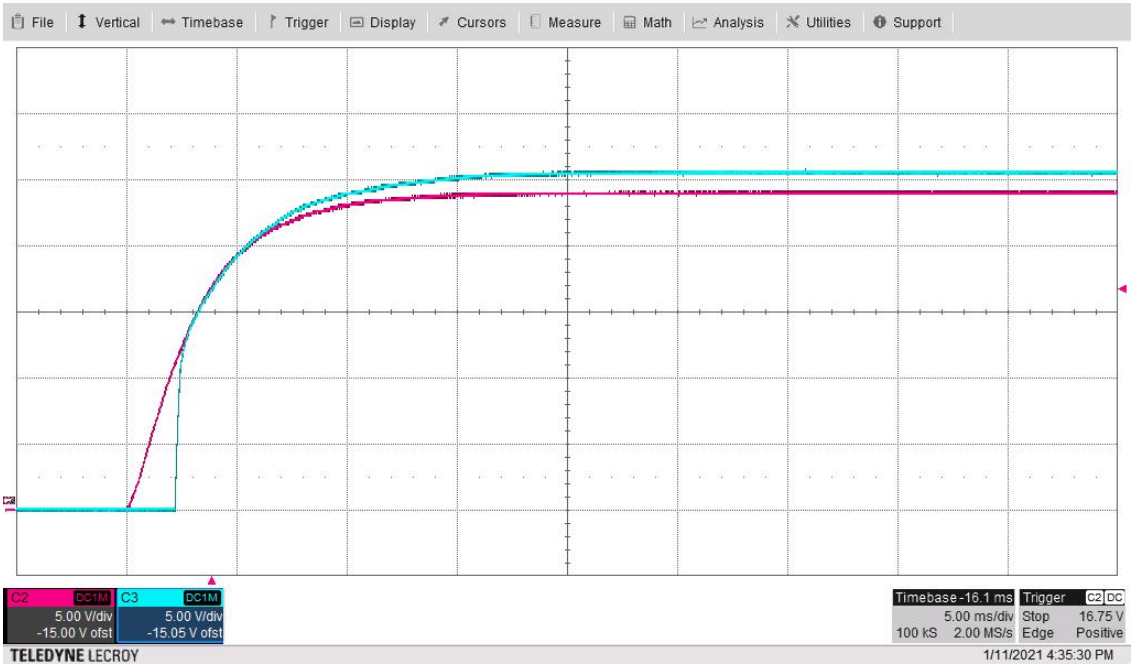
The following waveform shows the output voltage start-up waveform (+20 V in Blue and –4 V in Yellow) after the application of 24-V input (Red) with each output loaded to 100 mA.



5 V/div, 5 ms/div, 750 MHz BWL

Figure 4-2. Output Voltage Start-up Waveform

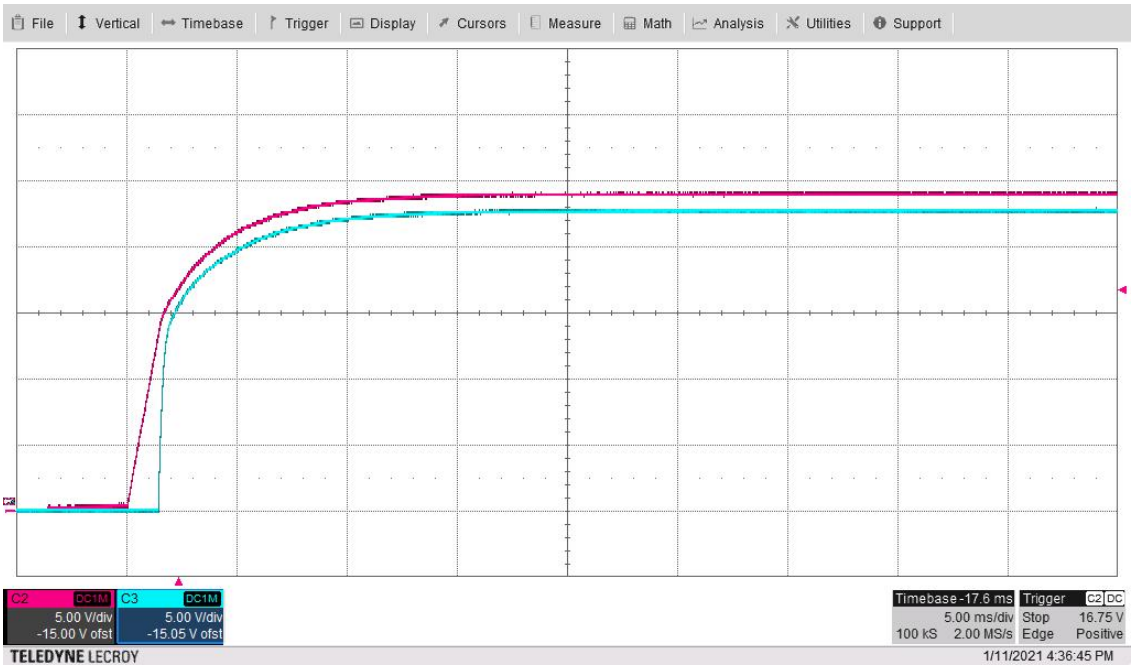
The following waveform shows the total rectified secondary output voltage start-up waveform (Blue) after the application of 24-V input (Red) with each output loaded to 0 mA.



5 V/div, 5 ms/div, 750 MHz BWL

Figure 4-3. Total Rectified Secondary Output Voltage Start-up Waveform

The following waveform shows the total rectified secondary output voltage start-up waveform (Blue) after the application of 24-V input (Red) with each output loaded to 100 mA.

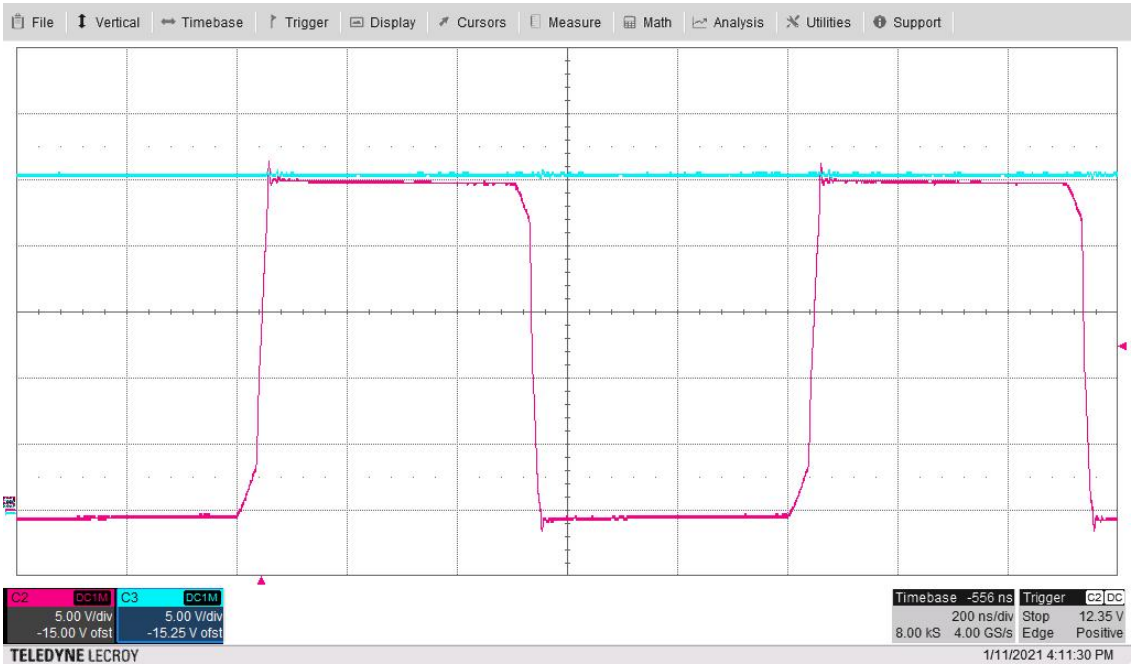


5 V/div, 5 ms/div, 750 MHz BWL

Figure 4-4. Total Rectified Secondary Output Voltage Start-up Waveform

4.2 Switch Node

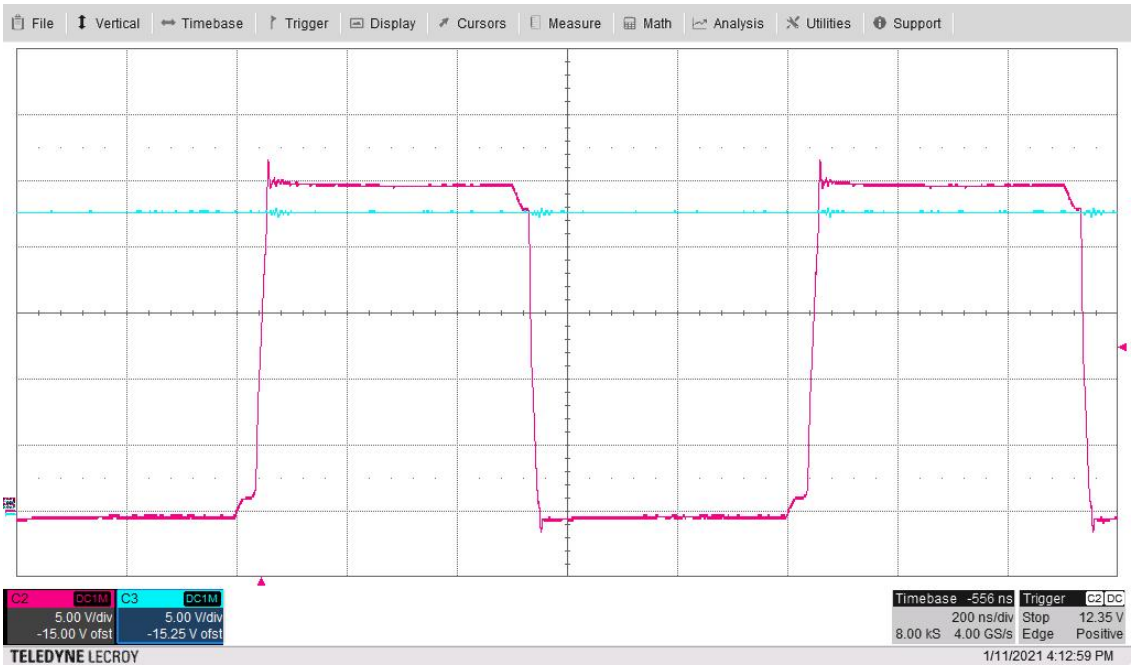
The following waveform shows the primary-side switch node voltage (Red) at TP5 and the total rectified secondary output voltage (Blue). The input voltage is 24 V and the 20-V and –4-V outputs are loaded to 0 mA each.



5 V/div, 200 ns/div, 750 MHz BWL

Figure 4-5. Primary-Side Switch Node Voltage and Total Rectified Secondary Output Voltage

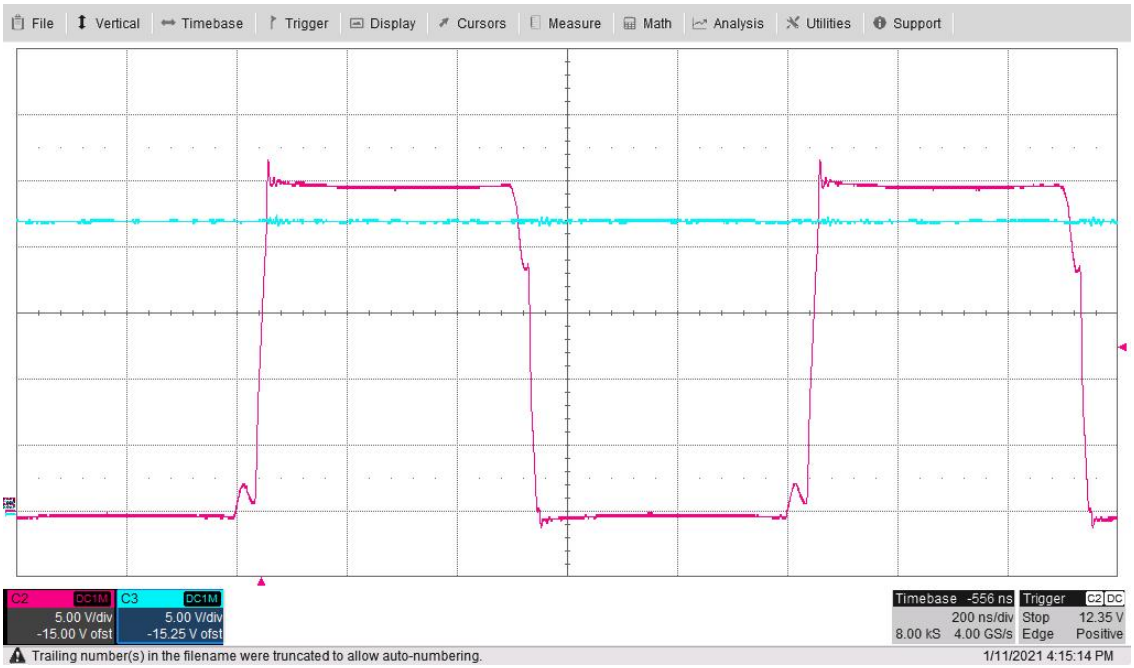
The following waveform shows the primary-side switch node voltage (Red) at TP5 and the total rectified secondary output voltage (Blue). The input voltage is 24 V and the 20-V and –4-V outputs are loaded to 100 mA each.



5 V/div, 200 ns/div, 750 MHz BWL

Figure 4-6. Primary-Side Switch Node Voltage and Total Rectified Secondary Output Voltage

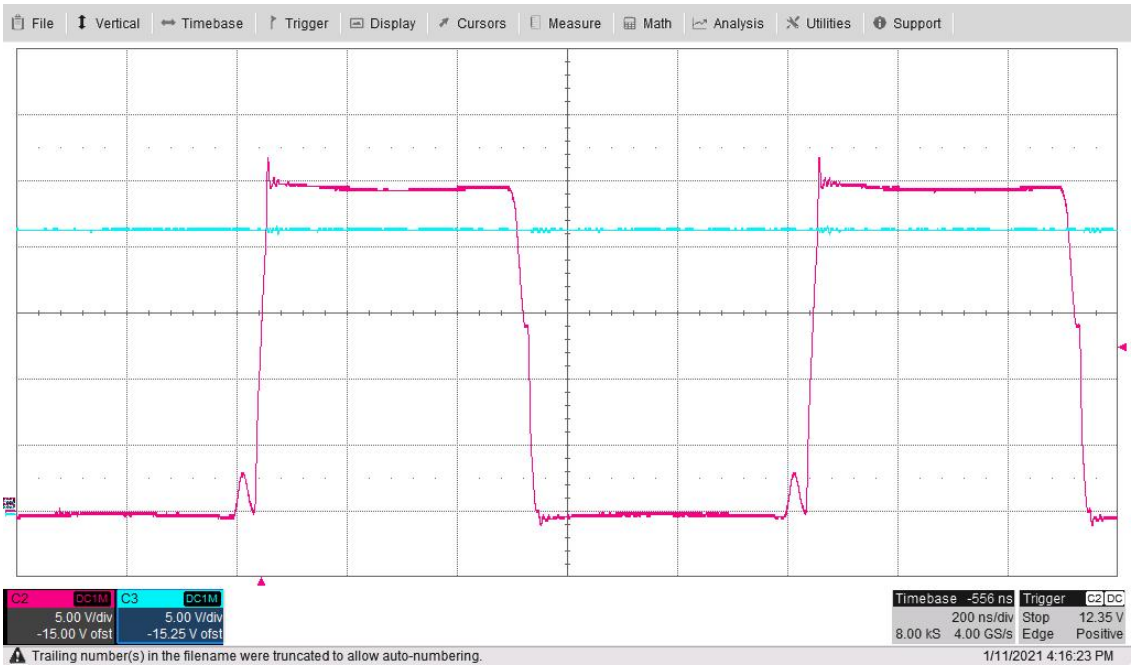
The following waveform shows the primary-side switch node voltage (Red) at TP5 and the total rectified secondary output voltage (Blue). The input voltage is 24 V and the 20-V and –4-V outputs are loaded to 200 mA each.



5 V/div, 200 ns/div, 750 MHz BWL

Figure 4-7. Primary-Side Switch Node Voltage and Total Rectified Secondary Output Voltage

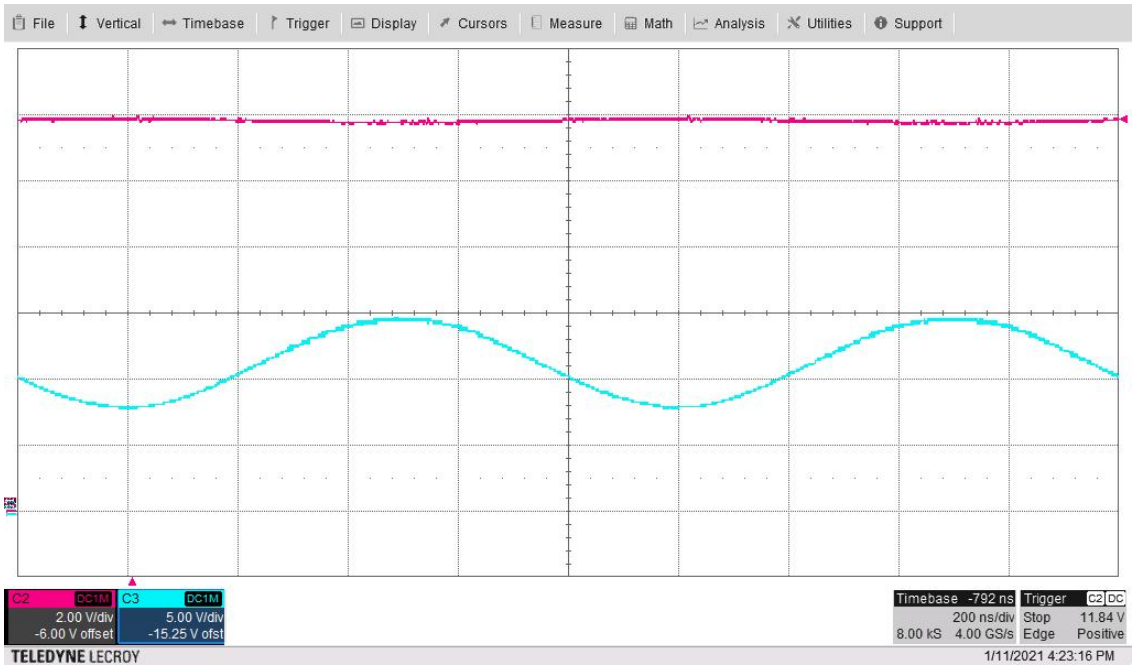
The following waveform shows the primary-side switch node voltage (Red) at TP5 and the total rectified secondary output voltage (Blue). The input voltage is 24 V and the 20-V and –4-V outputs are loaded to 300 mA each.



5 V/div, 200 ns/div, 750 MHz BWL

Figure 4-8. Primary-Side Switch Node Voltage and Total Rectified Secondary Output Voltage

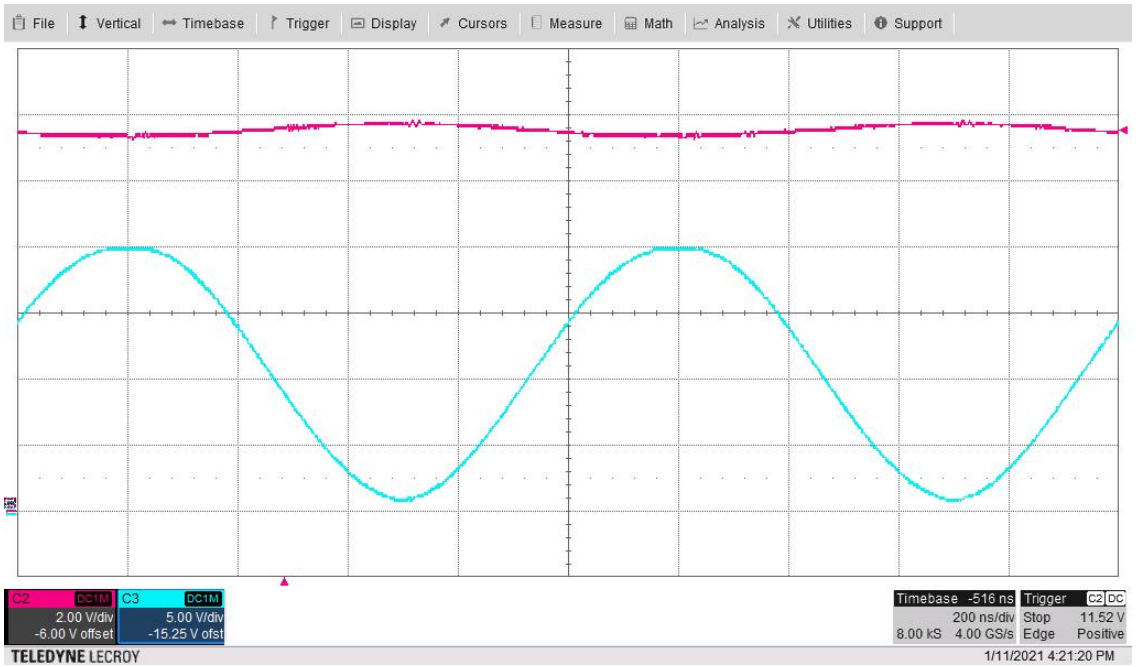
The following waveform shows the voltage at the middle of the input capacitor divider at C2 and C9 (Red) and the secondary rectified voltage across C3 (Blue). The input voltage is 24 V and the 20-V and –4-V outputs are loaded to 100 mA each.



C2/C9: 2 V/div, C3: 5 V/div, 200 ns/div, 750 MHz BWL

Figure 4-9. Input Capacitor Divider Voltage and Secondary Rectified Voltage

The following waveform shows the voltage at the middle of the input capacitor divider at C2 and C9 (Red) and the secondary rectified voltage across C3 (Blue). The input voltage is 24 V and the 20-V and –4-V outputs are loaded to 300 mA each.

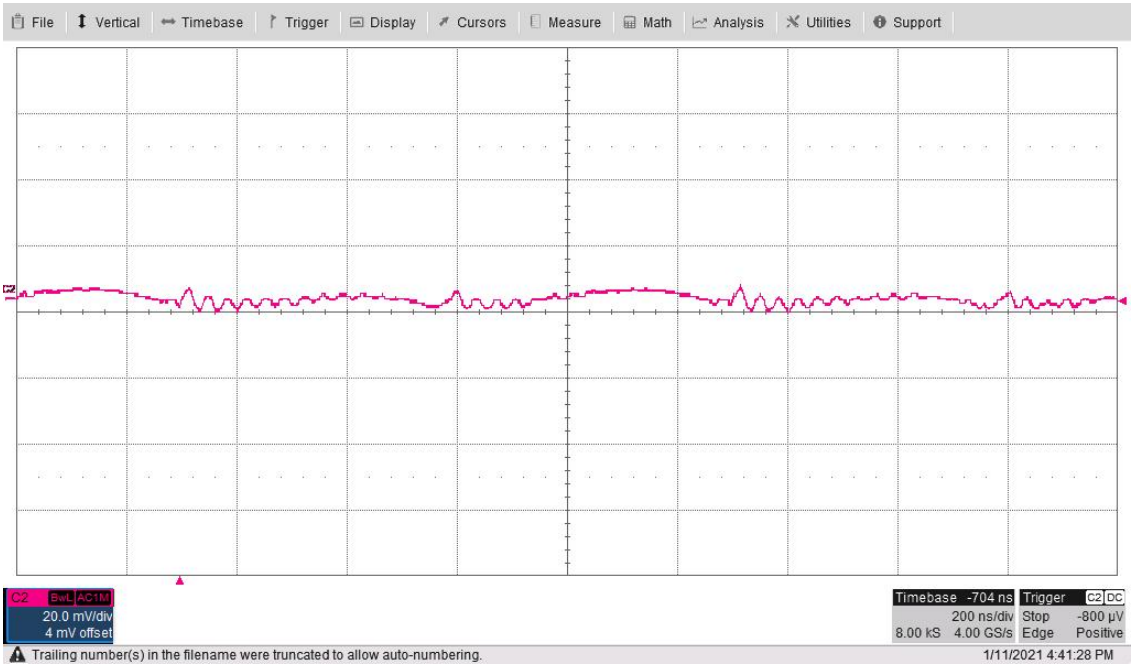


C2/C9: 2 V/div, C3: 5 V/div, 200 ns/div, 750 MHz BWL

Figure 4-10. Input Capacitor Divider Voltage and Secondary Rectified Voltage

4.3 Output Voltage Ripple

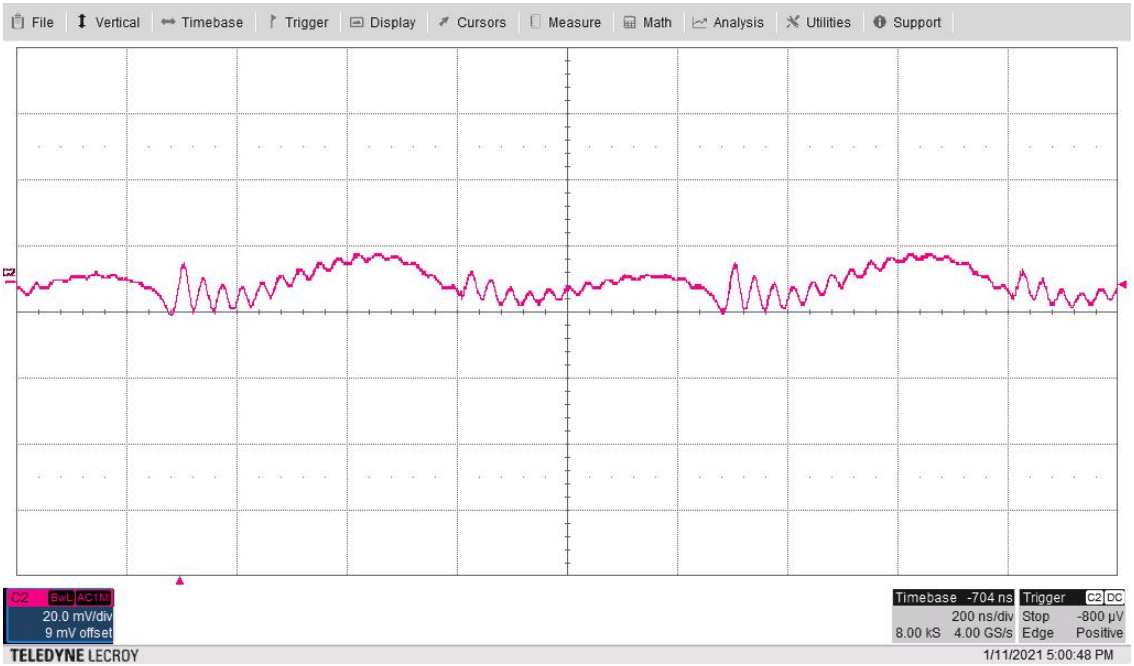
The following waveform shows the 20-V output ripple voltage (AC coupled) measured across C4. The input voltage is 24 V and the 20-V and –4-V outputs are loaded to 100 mA each.



20 mV/div, 200 ns/div, 20 MHz BWL

Figure 4-11. Output Ripple Voltage, 20 V (AC Coupled)

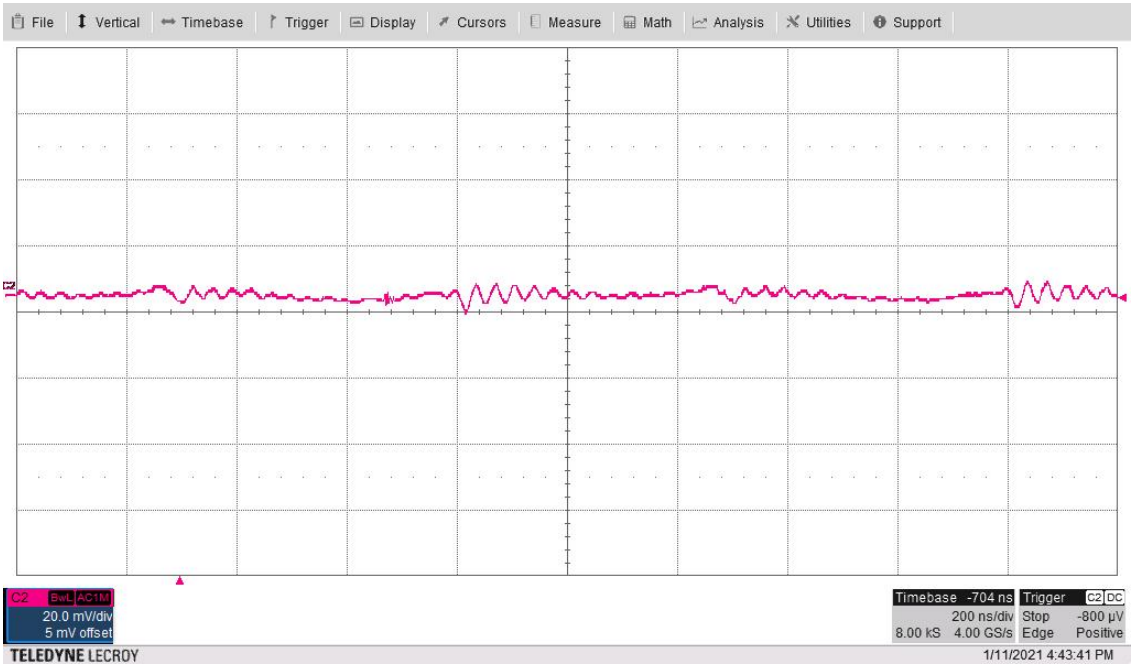
The following waveform shows the 20-V output ripple voltage (AC coupled) measured across C4. The input voltage is 24 V and the 20-V and –4-V outputs are loaded to 300 mA each.



20 mV/div, 200 ns/div, 20 MHz BWL

Figure 4-12. Output Ripple Voltage, 20 V (AC Coupled)

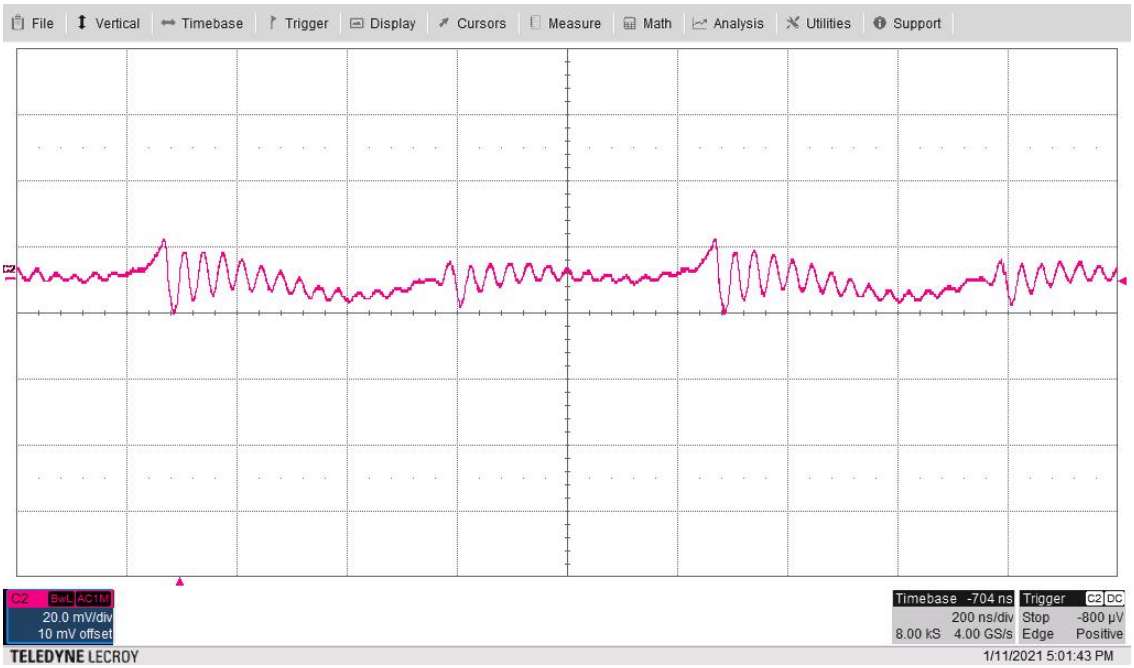
The following waveform shows the –4-V output ripple voltage (AC coupled) measured across C5. The input voltage is 24 V and the 20-V and –4-V outputs are loaded to 100 mA each.



20 mV/div, 200 ns/div, 20 MHz BWL

Figure 4-13. Output Ripple Voltage, –4 V (AC Coupled)

The following waveform shows the –4-V output ripple voltage (AC coupled) measured across C5. The input voltage is 24 V and the 20-V and –4-V outputs are loaded to 300 mA each.

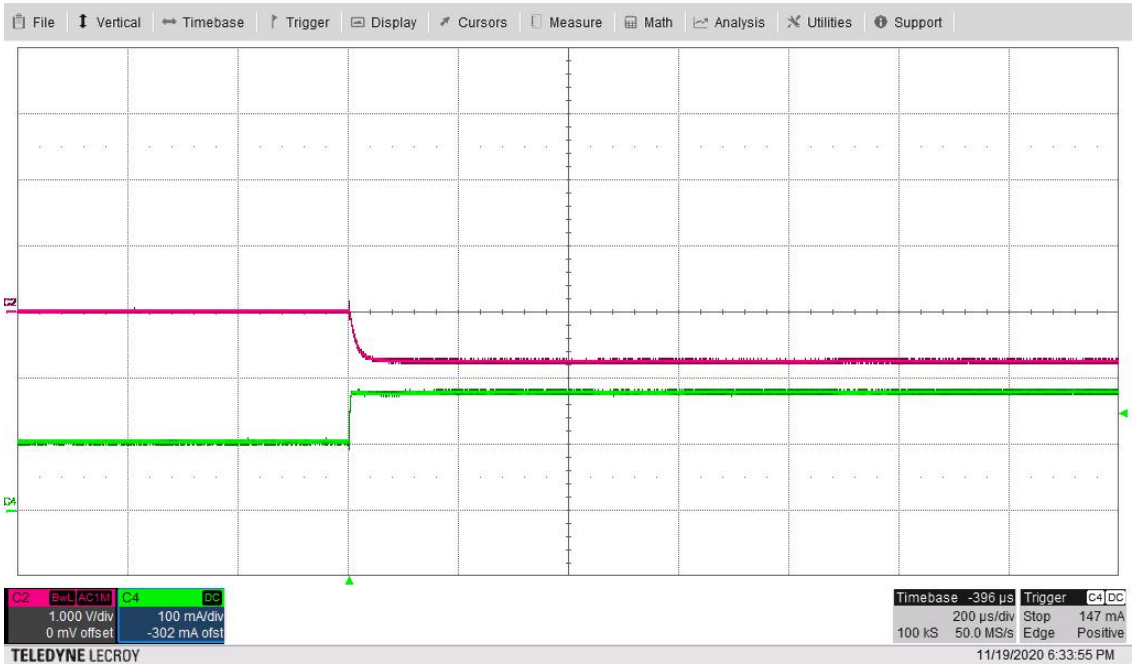


20 mV/div, 200 ns/div, 20 MHz BWL

Figure 4-14. Output Ripple Voltage, –4 V (AC Coupled)

4.4 Load Transients

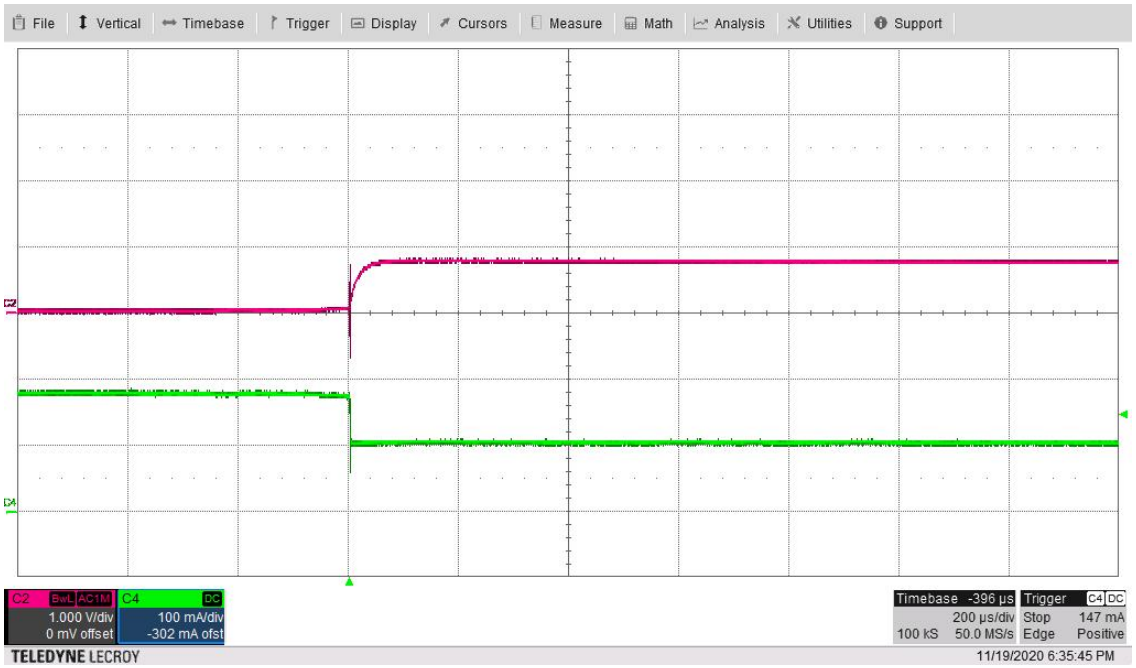
The total rectified secondary output voltage (AC coupled) is shown in Red in the following waveform for a load step (Green) from 100 mA to 175 mA with the input voltage at 24 V. The load current is sourced from the 20 V directly to the –4 V with no COM connection.



1 V/div, 100 mA/div, 200 µs/div

Figure 4-15. Total Rectified Secondary Output Voltage (AC Coupled)

The total rectified secondary output voltage (AC coupled) is shown in Red in the following waveform for a load step (Green) from 175 mA to 100 mA with the input voltage at 24 V. The load current is sourced from the 20 V directly to the –4 V with no COM connection.



1 V/div, 100 mA/div, 200 µs/div

Figure 4-16. Total Rectified Secondary Output Voltage (AC Coupled)

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