Test Report: PMP23124

Half-Bridge LLC Dual-Output Bias-Supply Pair Reference Design

Description

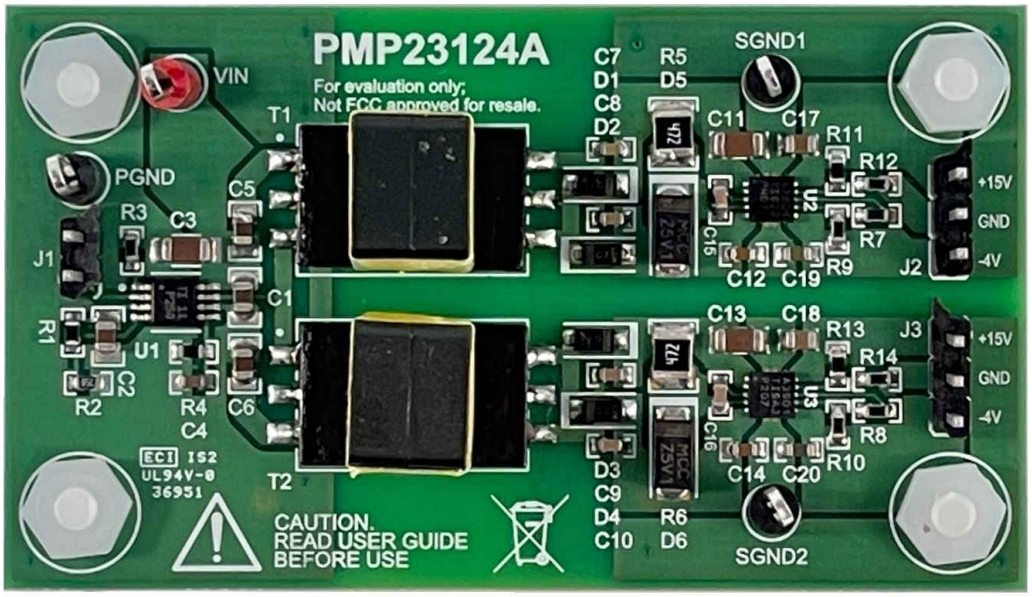
This reference design uses a single UCC25800-Q1 to drive two LLC transformers. Each isolated output feeds into a TPS7A39 dual-channel positive and negative output LDO. PMP23124 can be used to bias two wide band gap FETs that require a positive and negative voltage to drive. Each output can be loaded to 2.8 W.

Features

- Combined PD and PWM controller
- Primary side regulation (no optocoupler)
- Input power limiting
- Converters can be paralleled for increased power

Applications

- IP network camera
- WLAN, Wi-Fi® access point



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1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
Input Voltage	+15-V input, ±5%
Output Voltage	+15 V, –4-V split rail outputs
Max Current	150 mA

1.2 Required Equipment

- AC Power Supply
- Electronic Load
- AC Power Meter
- Digital Multimeter
- Oscilloscope

1.3 Considerations

- A resistive load connected between the positive and negative outputs was used for all tests
- Unless noted, all waveforms were captured at full load with a 12-V_{DC} input

1.4 Dimensions

The PCB is a two-layer, 1-oz per layer design. The dimensions are 1.5 in × 2.625 in with a maximum component height of 0.35 in.

1.5 Test Setup

- DC source capable of 25 V, 1 A
- Resistive loads rated for at least 1 W

2 Testing and Results

2.1 Load Regulation Graphs

Figure 2-1 and Figure 2-2 show the respective positive and negative voltage regulation graphs.

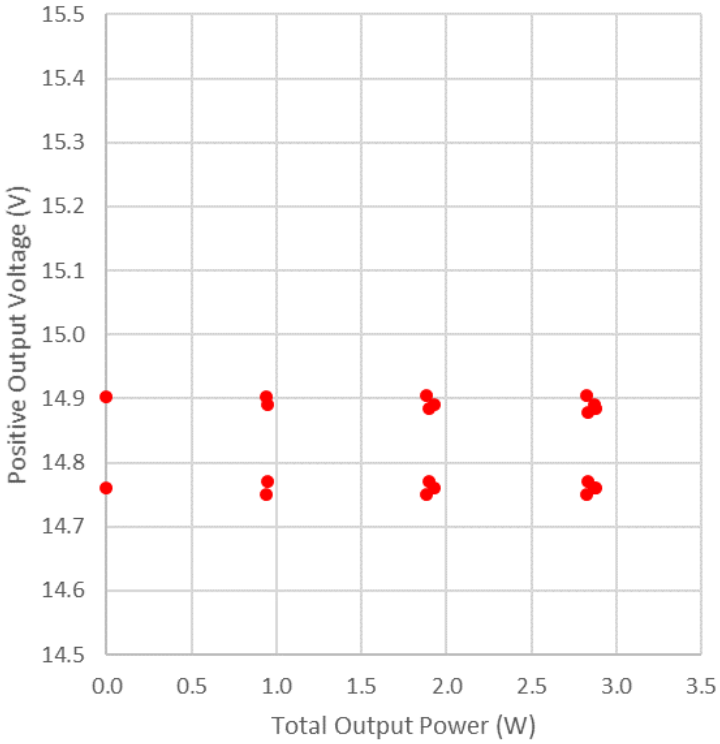


Figure 2-1. Positive Voltage Regulation

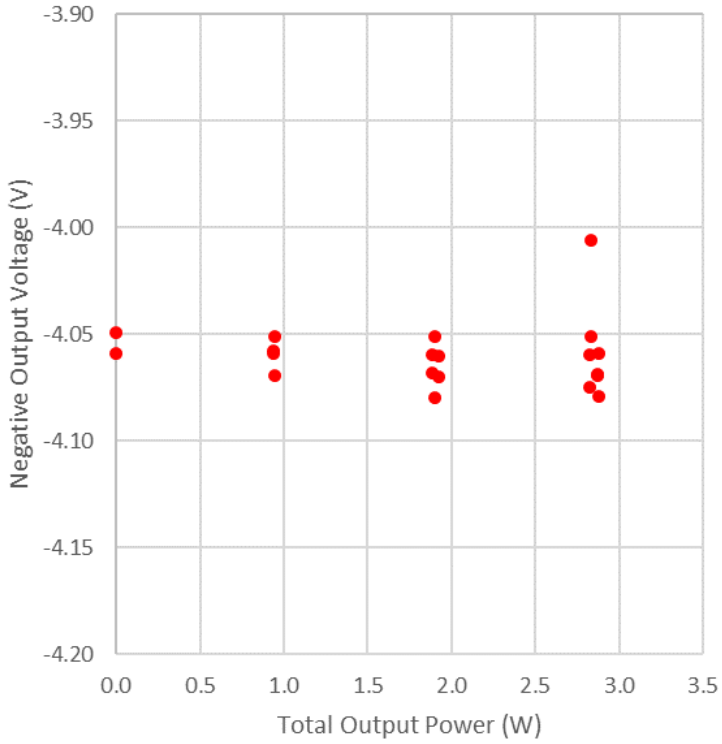


Figure 2-2. Negative Voltage Regulation

2.2 Efficiency Graphs

Figure 2-3 shows the efficiency graph.

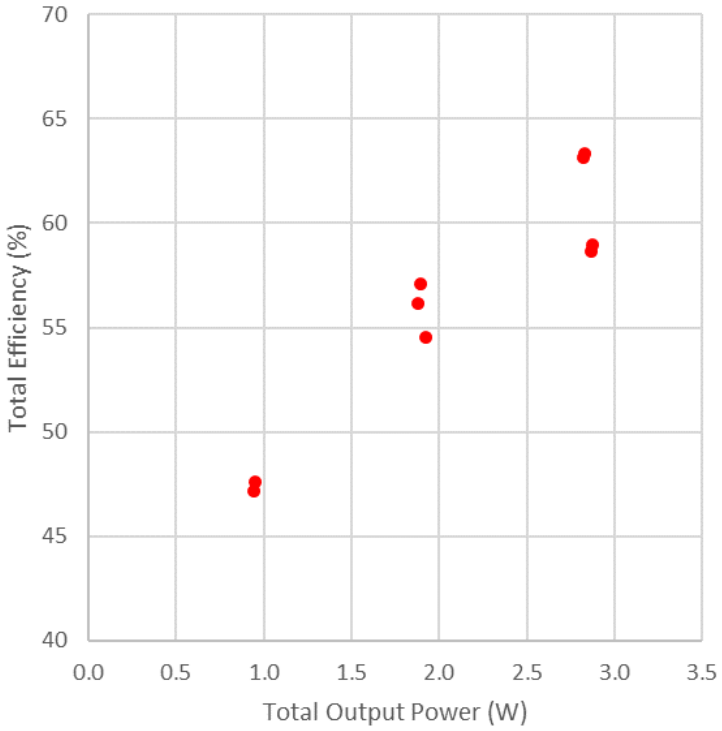


Figure 2-3. Efficiency Graph

2.3 Efficiency Data

Efficiency data is shown in the following table.

Table 2-1. Efficiency Data

Input Voltage Setting	Positive Output 1 Voltage (V)	Negative Output 1 Voltage (V)	Output 1 Current (mA)	Output 1 Power (W)	Positive Output 2 Voltage (V)	Negative Output 2 Voltage (V)	Output 2 Current (mA)	Total Output Power (W)	Input Power (W)	Efficiency (%)	Power Loss (W)
15 V_{DC}	14.76	–4.049	0	0	14.90	–4.059	0	0	0.525	0	0.525
	14.75	–4.058	50	0.94	14.90	–4.059	0	0	1.993	47.194	1.052
	14.75	–4.068	100	1.882	14.90	–4.059	0	0	3.353	56.129	1.471
	14.75	–4.075	150	2.824	14.90	–4.060	0	0	4.472	63.149	1.648
	14.77	–4.051	0	0	14.89	–4.069	50	0.948	1.993	47.577	1.045
	14.77	–4.051	0	0	14.89	–4.080	100	1.896	3.323	57.073	1.426
	14.77	–4.051	0	0	14.88	–4.006	150	2.833	4.472	63.342	1.639
	14.76	–4.060	50	0.941	14.89	–4.070	52	0.986	3.532	54.562	1.605
	14.76	–4.059	50	0.941	14.88	–4.079	102	1.934	4.874	58.993	1.999
	14.76	–4.069	100	1.883	14.89	–4.070	52	0.986	4.889	58.680	2.020

2.4 Thermal Images

Measurements		
Bx1	Max	75.9 °C
Bx2	Max	43.2 °C

Parameters	
Emissivity	0.94
Refl. temp.	20 °C

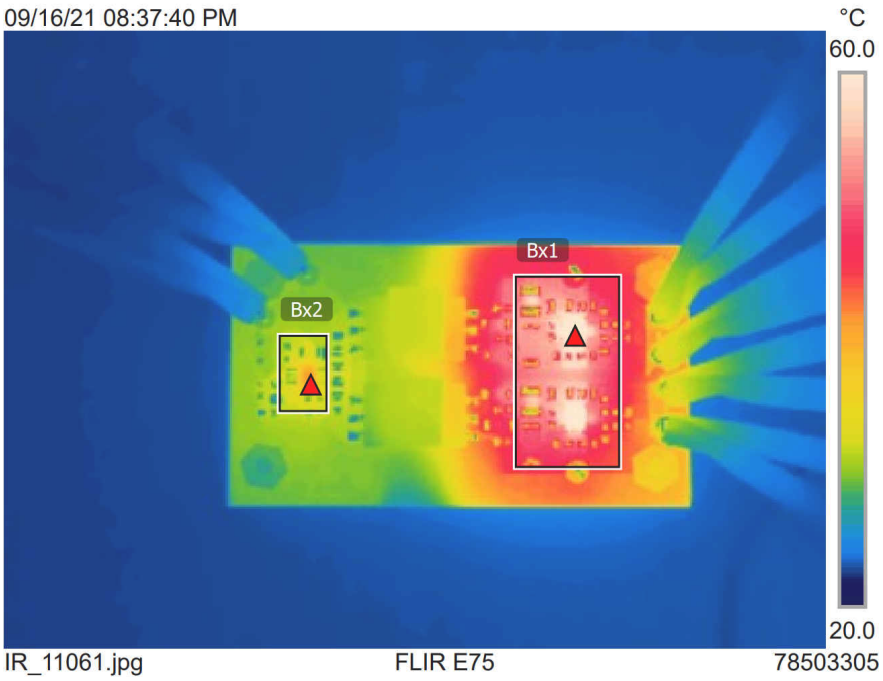


Figure 2-4. Thermal Image

Bx1: Dual LDO Output
Bx2: LLC Converter

3 Waveforms

3.1 Switching

The following waveform shows the primary switching at 2.6 W.

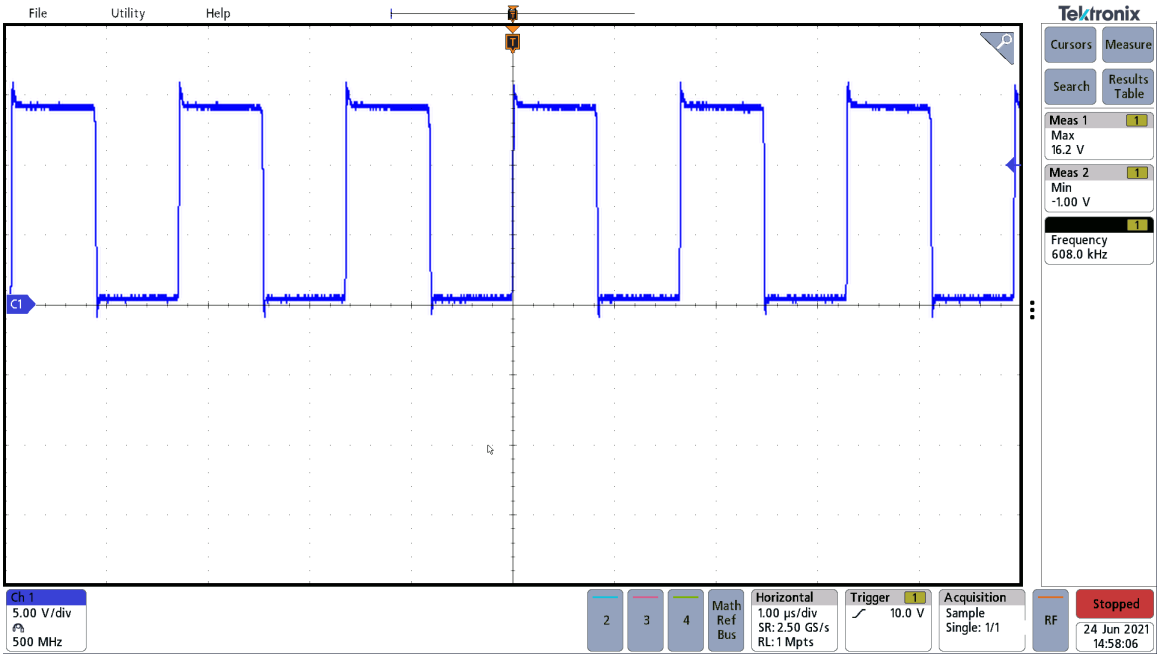


Figure 3-1. Primary Switching 2.6 W

3.2 Output Voltage Ripple

Figure 3-2 shows the PMP23124 output voltage ripple waveform.

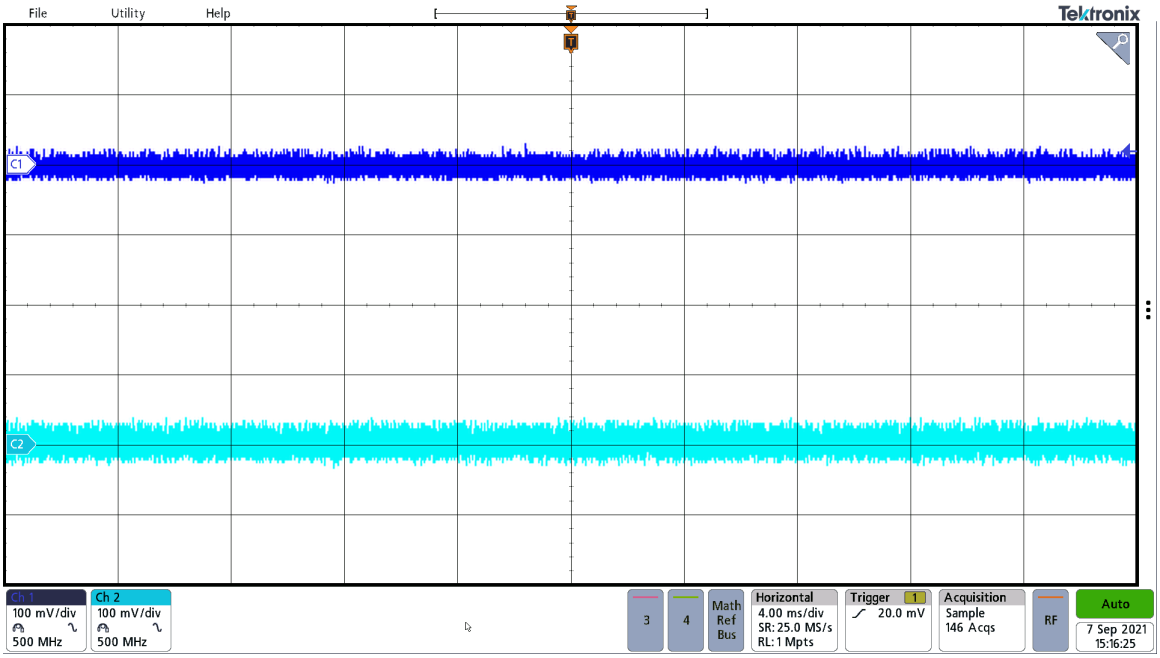


Figure 3-2. Output Voltage Ripple

Channel 1 (blue): +15-V output (AC coupled)
Channel 2 (cyan): –4-V output (AC coupled)

3.3 Load Transients

The following waveform illustrates the PMP23124 load transient.

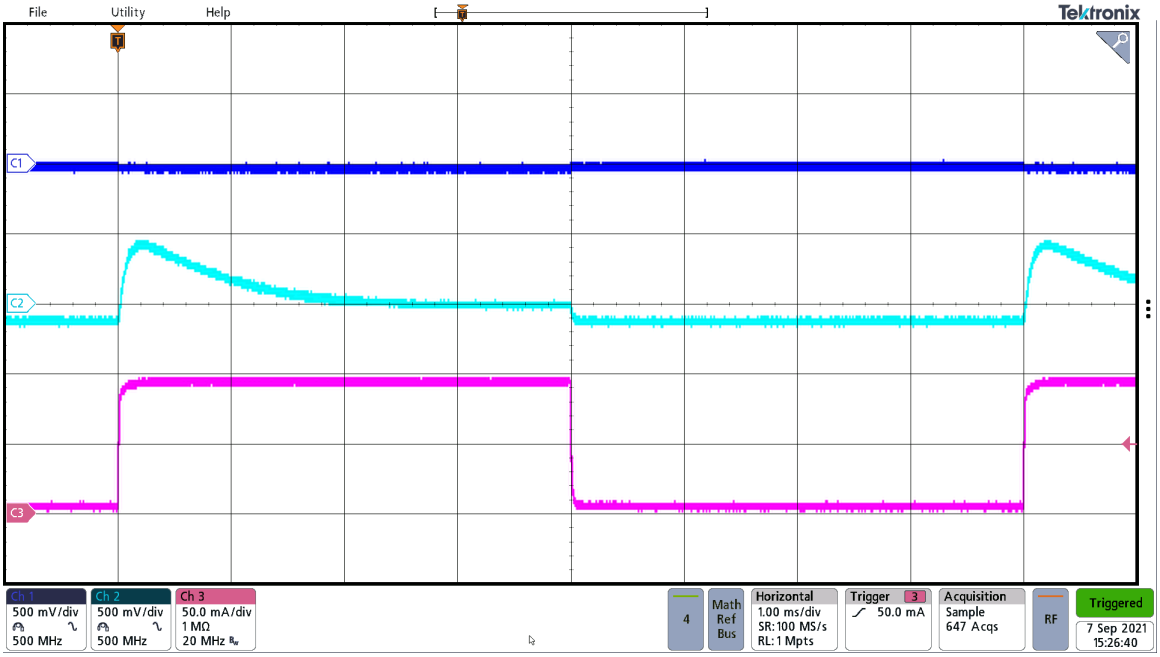
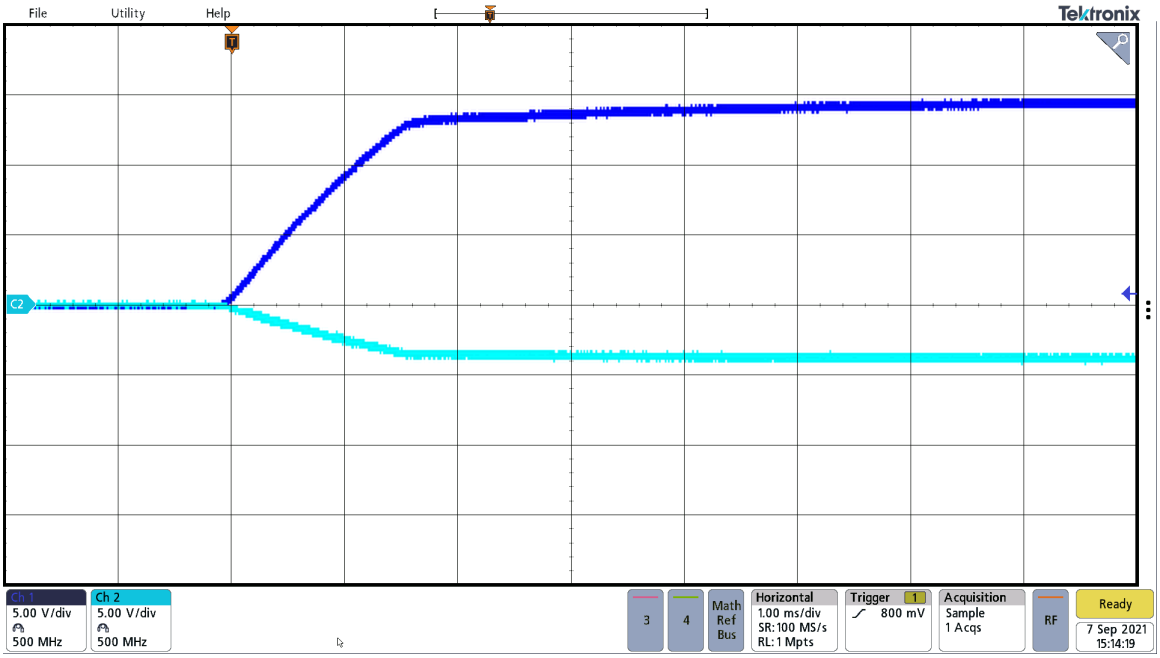


Figure 3-3. Load Transient

3.4 Start-up Sequence

Figure 3-4 shows the Start-up Rise Time waveform. Figure 3-5 shows the start-up with V_{IN} waveform



Channel 1 (blue): +15-V output
Channel 2 (cyan): –4-V output

Figure 3-4. Start-up Rise Time

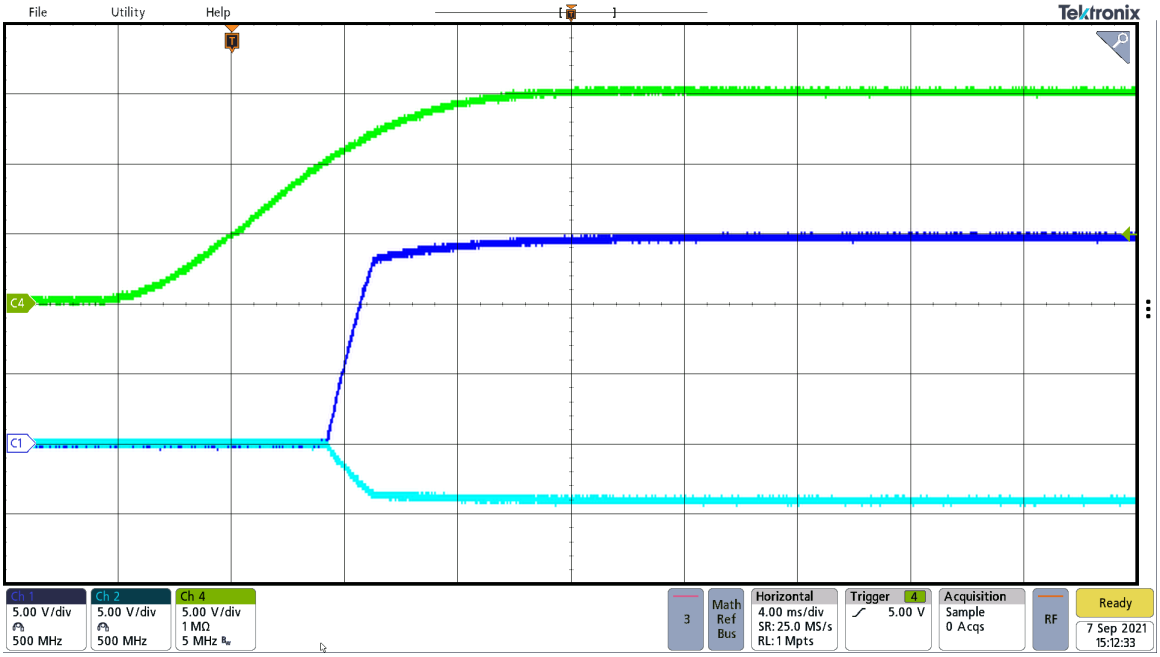


Figure 3-5. Start-Up With V_{IN}

Channel 1 (blue): +15-V output
Channel 2 (cyan): –4-V output

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