Test Report: PMP31052

Four-Switch Buck-Boost Reference Design > 300 W

Description

The circuit is an automotive four-switch buck-boost converter circuit using the LM5176-Q1 controller IC, so the power supply is able to step up and step down the input voltage.

The circuit accepts an input voltage of 4.5 V to 27 V and provides a regulated output of 12 V that can deliver up to 30 A, depending on cranking level, cranking time, thermal interface, and maximum ambient temperature.

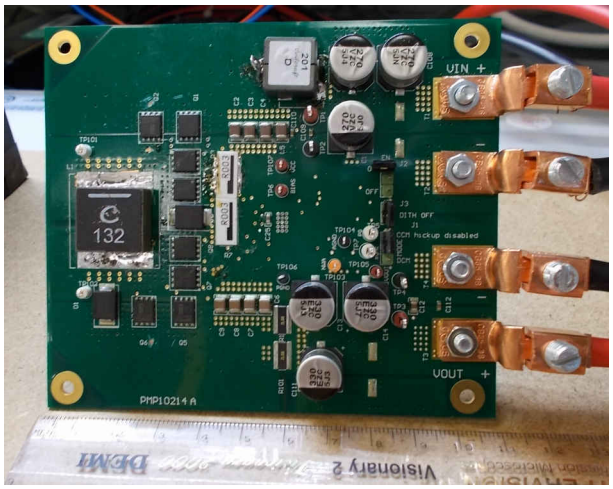
The purpose of this is design is to squeeze a single power stage to maximum output current.

Features

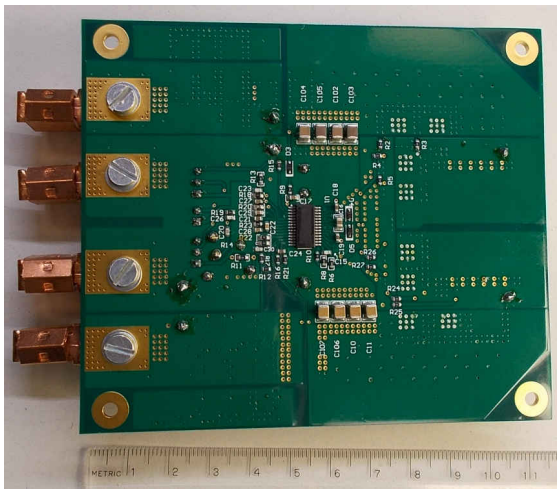
- Automotive 12-V bus converter is suitable for up to 30-A+ load current
- Cranking as low as 4.5-V input voltage is possible
- Efficiency remains flat and high between 4-A load to 30-A load 98%+
- Input filter to attenuate reflected ripple less than 20 mVpp
- Extended thermal information regarding various operating points

Applications

- ADAS domain controller



Board Photo (Top)



Board Photo (Bottom)

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
Input Voltage Range	4.5 V to 27 V
Output Voltage	12 V
Maximum Output Current	20 A to 30 A
Switching Frequency	200 kHz (100 kHz during buck-boost transition)

1.2 Considerations

WARNING

At cranking level 4.5 V and output current 20 A, the input current will be 60 A. Use a high current source and high current wiring, refer to Board Photo (Top).

This board is built on PMP10214RevA PCB.

Place current-sense resistor R71 beside R7, no backpack is possible; scratch PCB and do not short the via below R71.

Unless otherwise mentioned, the output current was set to 30 A with an electronic load (N3305A).

- UVLO thresholds
  - ON at 7.7 V
  - Off at 4.1 V
- Measured switching frequency
  - 193 kHz at buck or boost, 97 kHz at transition (V_{IN} is 11 V to 13 V)
- Measured output voltage
  - 12.14 V

Table 1-2. Trip Levels Current Sense

Input Voltage	Output Current (Maximum)
4.5 V	22 A
5.5 V	27 A
7 V	35 A
9 V	45 A

1.3 Dimensions

The dimensions of the PMP10214RevA board are 108 mm × 93 mm.

2 Testing and Results

2.1 Efficiency Graphs

Efficiency and load are shown in the following figures.

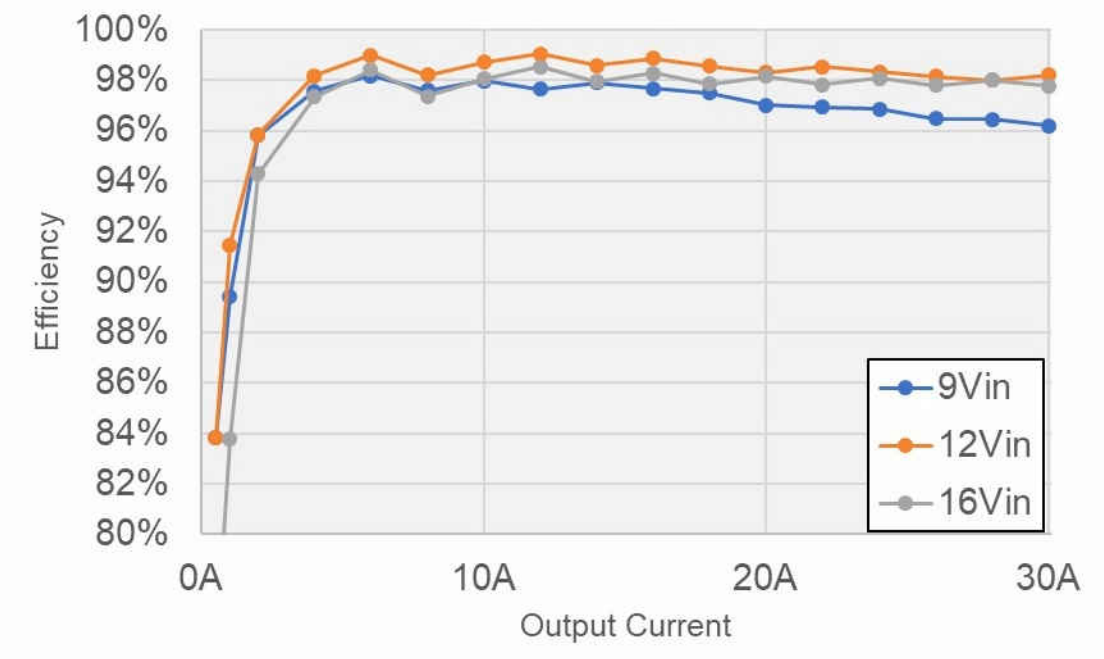


Figure 2-1. Efficiency vs Output Current

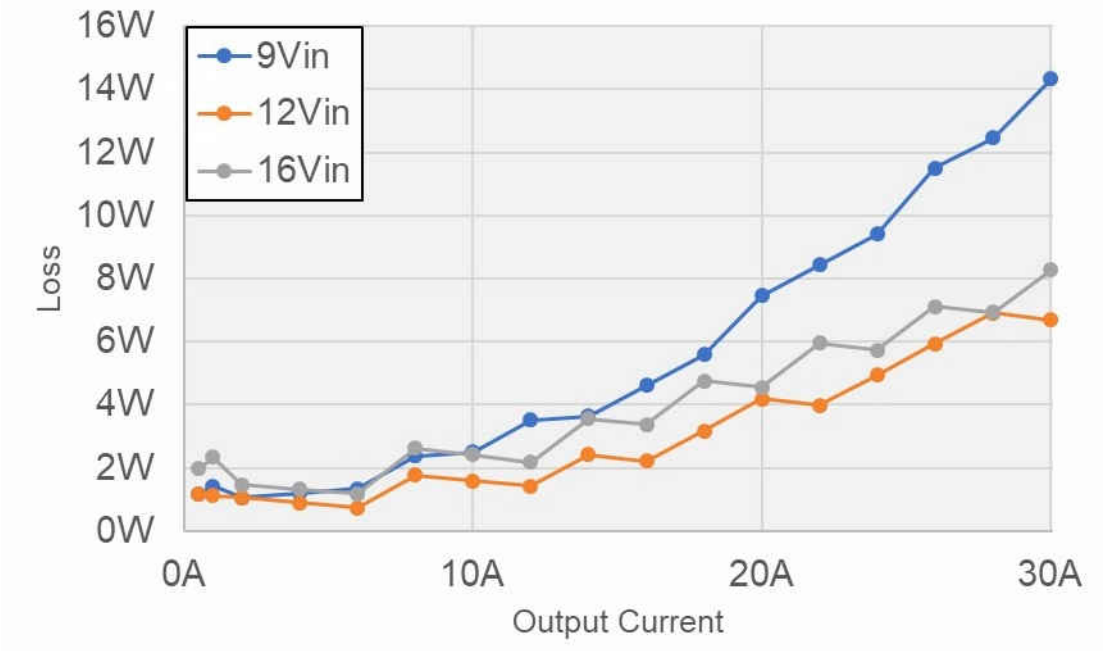


Figure 2-2. Loss vs Output Current

2.2 Load Regulation

The load regulation graph is shown in the following image.

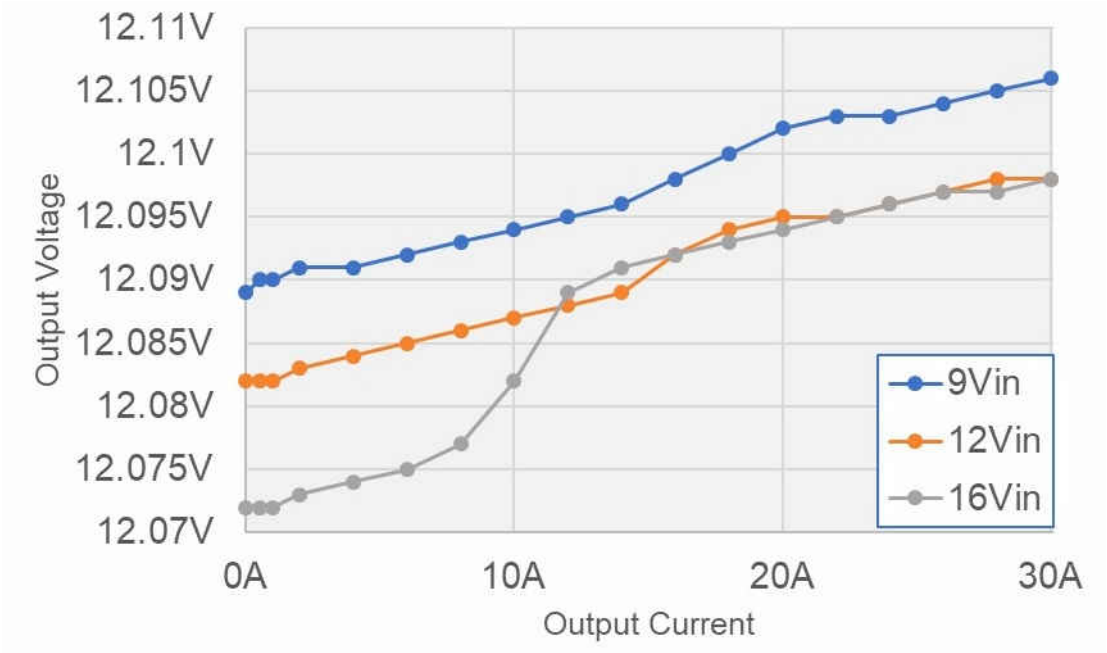


Figure 2-3. Output Voltage vs Output Current

2.3 Line Regulation

Figure 2-4 shows the line regulation graph for output voltage versus input voltage.

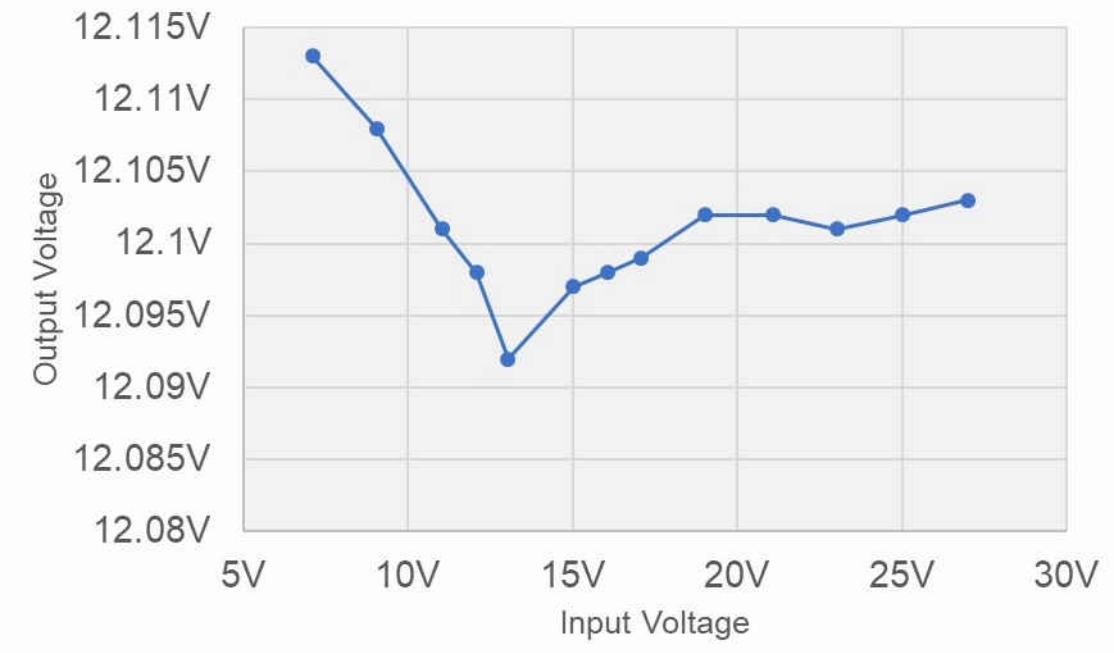


Figure 2-4. Output Voltage vs Input Voltage

At 5-V input voltage the output voltage was down regulated to 10.1 V due to current limit.

Figure 2-5 shows the efficiency and loss versus input voltage graph.

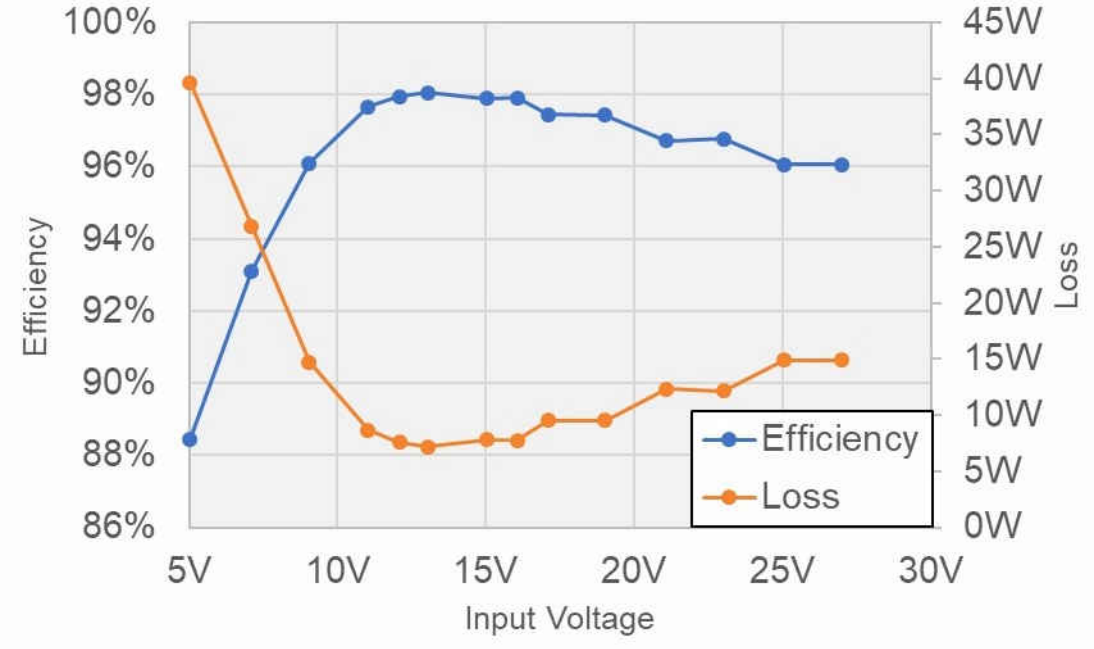


Figure 2-5. Efficiency and Loss vs Input Voltage

2.4 Thermal Images

The following photos show the thermal images for this reference design.

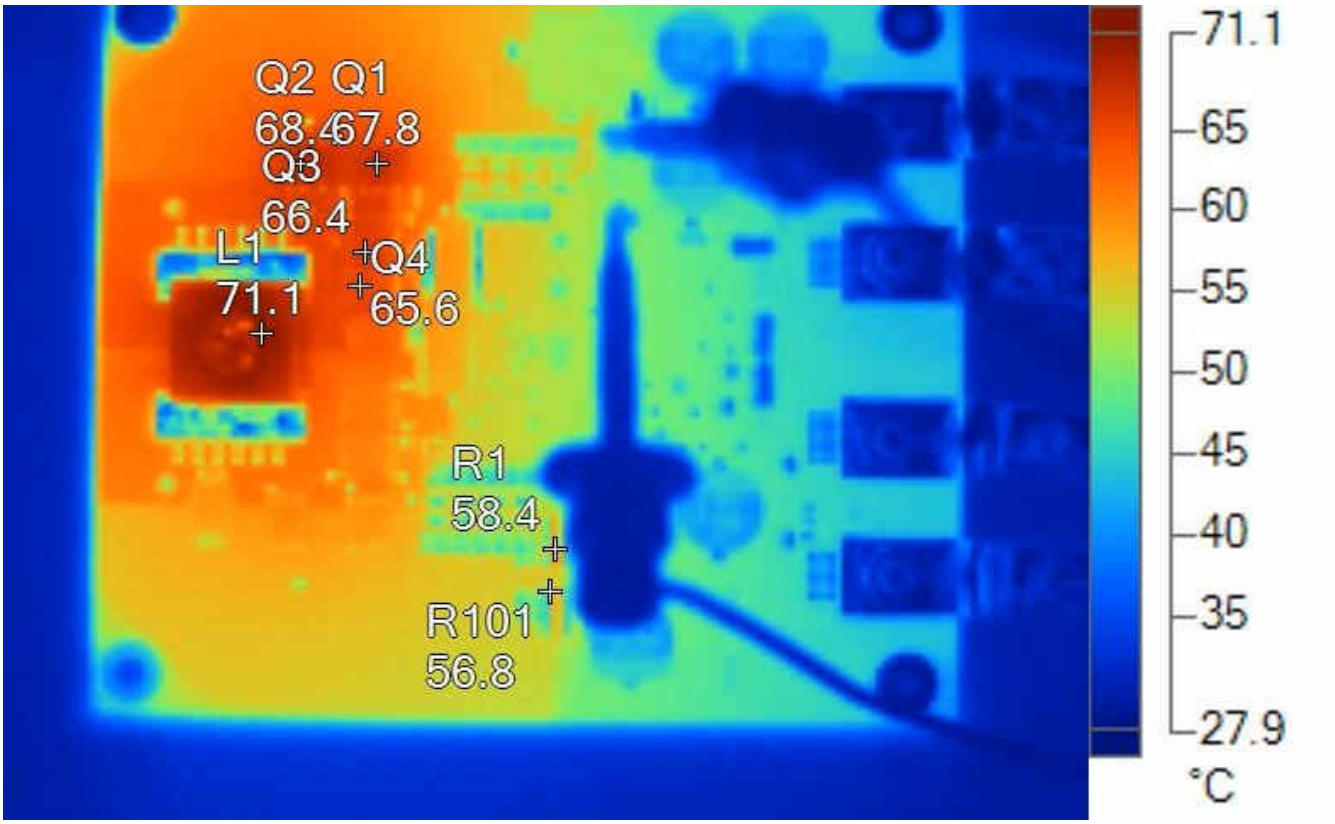


Figure 2-6. 16-V Input Voltage and 30-A Output Current

Name	Temperature
L1	**71.1°C**
Q1	67.8°C
Q2	68.4°C
Q3	66.4°C
Q4	65.6°C
R1	58.4°C
R101	56.8°C

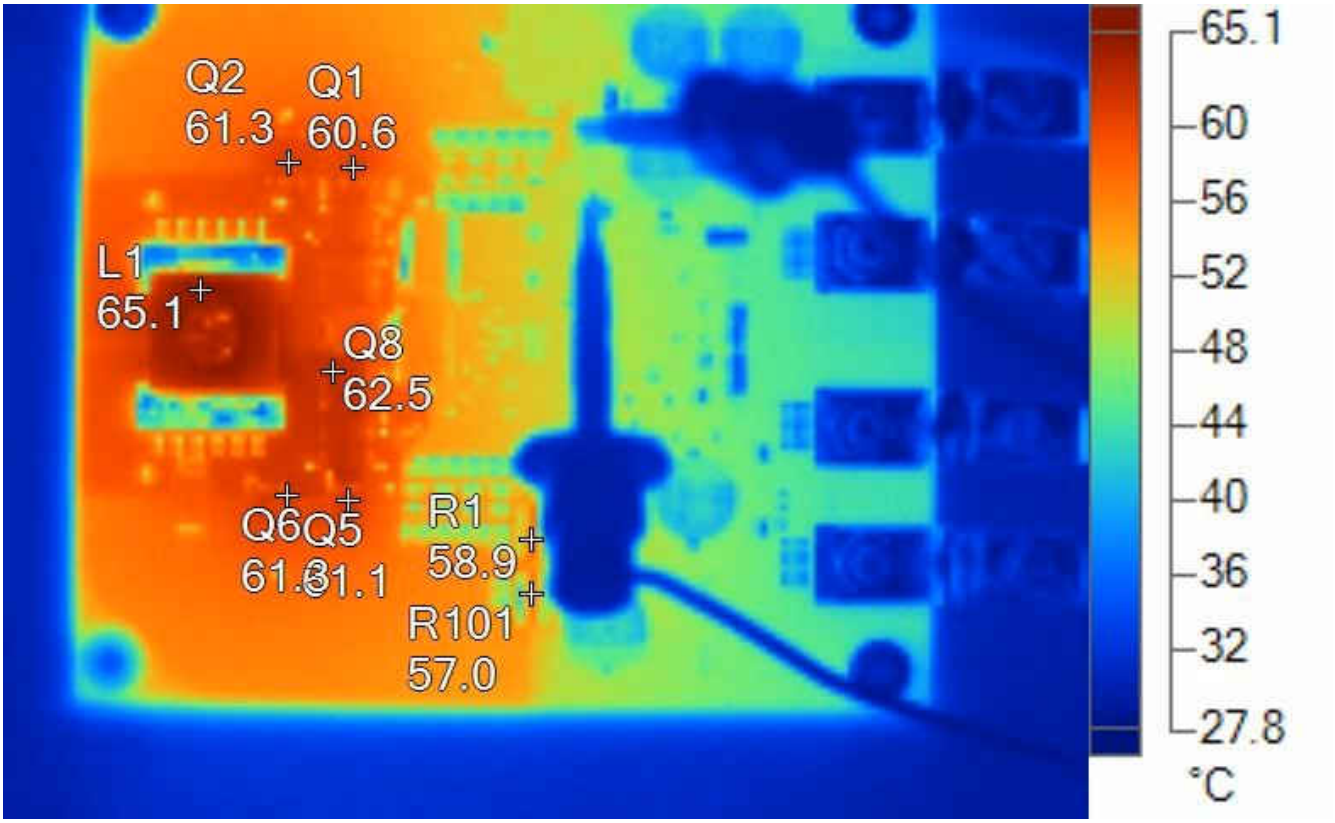


Figure 2-7. 12-V Input Voltage and 30-A Output Current

Name	Temperature
L1	**65.1°C**
Q1	60.6°C
Q2	61.3°C
Q5	61.1°C
Q6	61.3°C
Q8	62.5°C
R1	58.9°C
R101	57.0°C

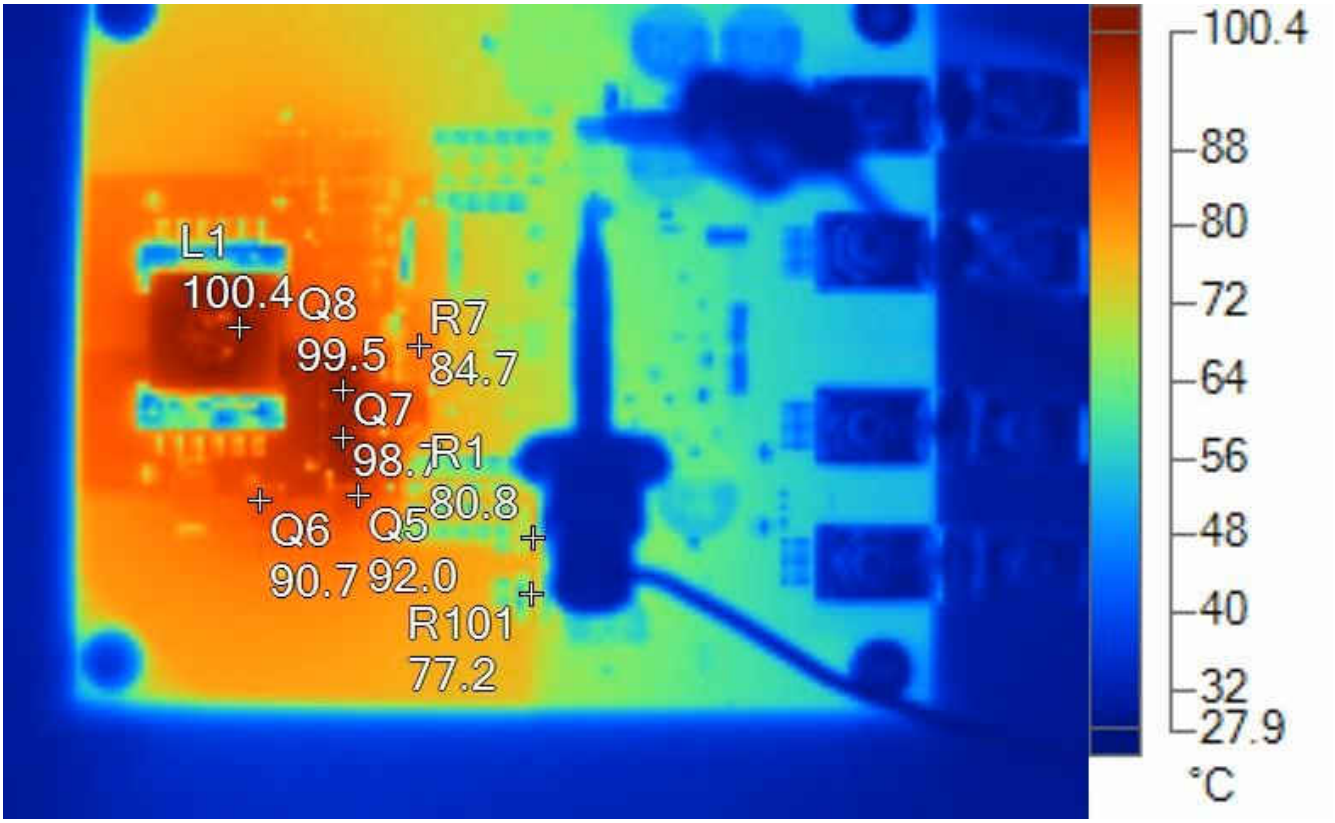


Figure 2-8. 9-V Input Voltage and 30-A Output Current

Name	Temperature
L1	**100.4°C**
Q5	92.0°C
Q6	90.7°C
Q7	98.7°C
Q8	99.5°C
R1	80.8°C
R101	77.2°C
R7	84.7°C

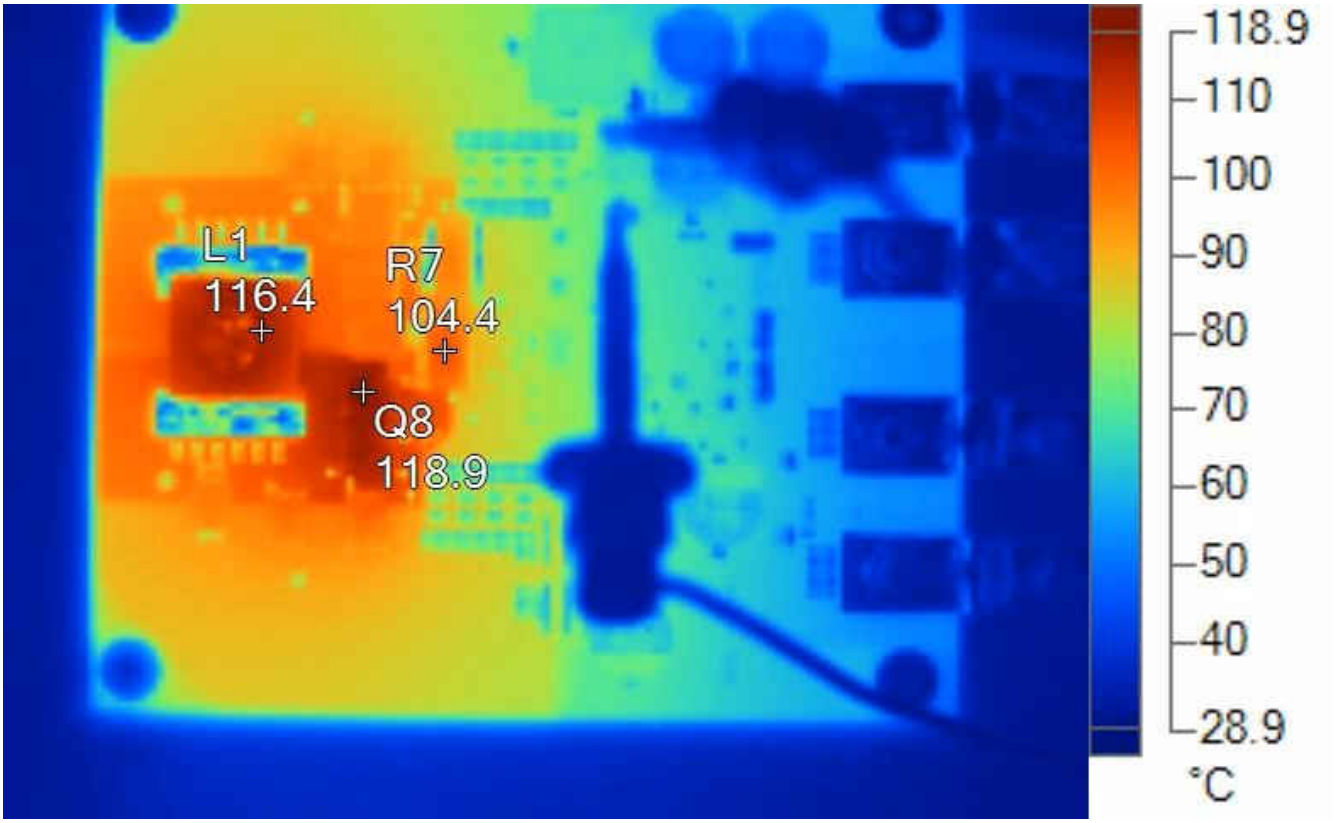


Figure 2-9. 5.5-V Input Voltage and 20-A Output Current (After Around 3 minutes)

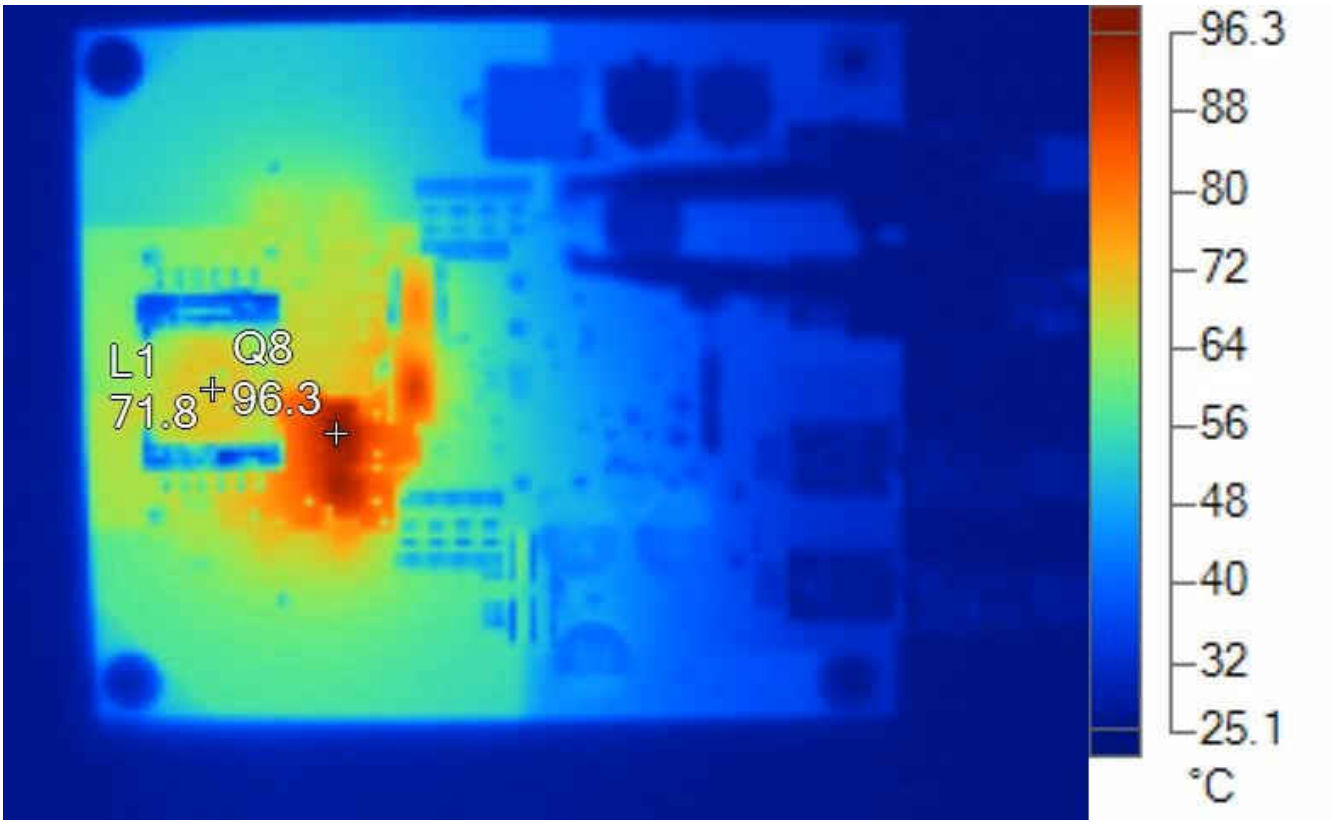
Name	Temperature
Q8	**118.9°C**
L1	116.4°C
R7	104.4°C

2.4.1 Further Extensive Thermal Measurements

2.4.1.1 No Forced Cooling

2.4.1.1.1 Thermal Images 4.5 V_{IN} and 20 A_{OUT}

2.4.1.1.1.1 After 1 Minute of Operation

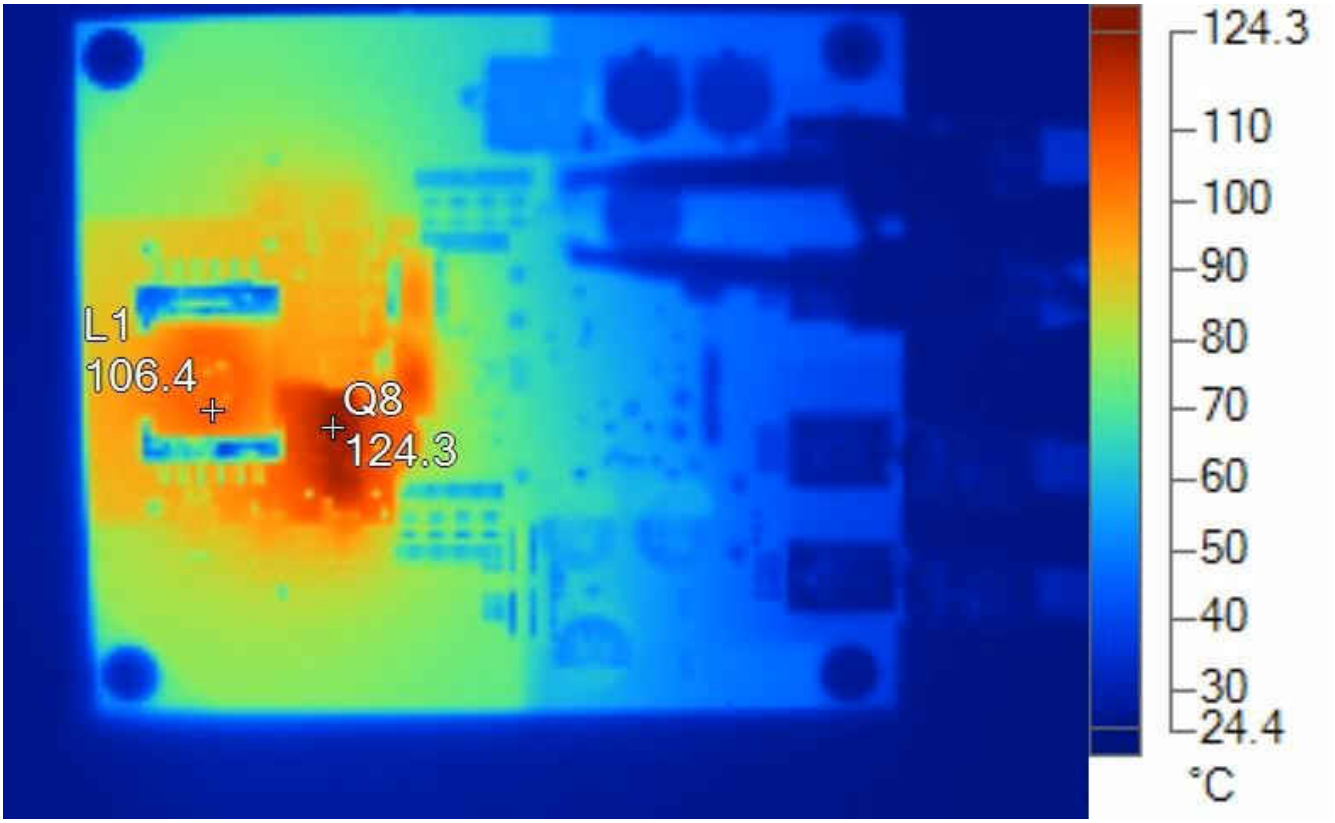


Low-side FETs at boost leg is the hot spot.

Figure 2-10. 4.5 V_{in} / 20 A_{out}, After Operating for 1 Minute

Name	Temperature
L1	71.8°C
Q8	**96.3°C**

2.4.1.1.1.2 After 2 Minutes of Operation

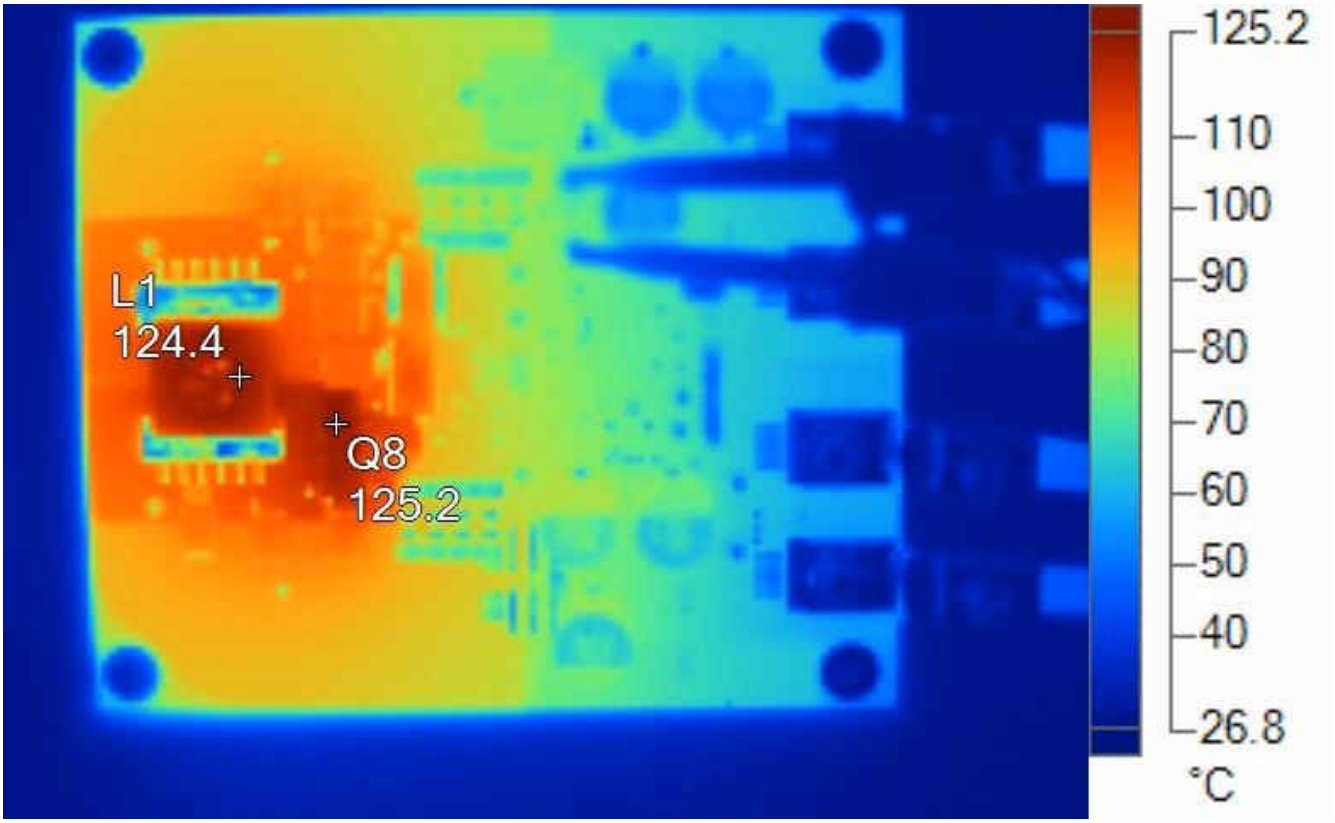


Low-side FETs at boost leg is the hot spot.

Figure 2-11. 4.5 V_{IN}, 20 A_{OUT}, After Operating for 2 Minutes

Name	Temperature
L1	106.4°C
Q8	**124.3°C**

2.4.1.1.2 Thermal Image 5.5 V_{IN} and 20 A_{OUT}

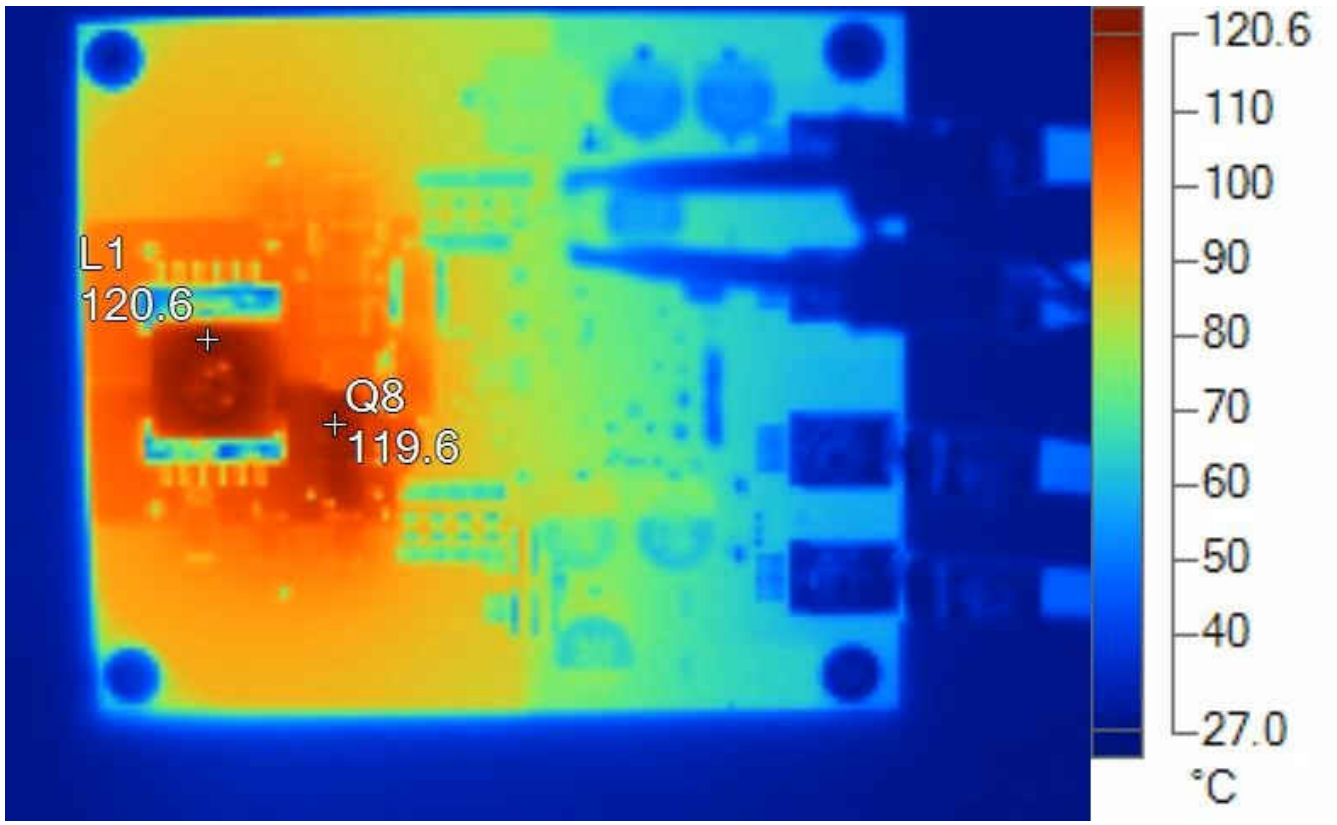


Low-side FETs at boost leg is the hot spot, high-current stress is present at inductor.

Figure 2-12. 5.5 V_{IN}, 20 A_{OUT}, Continuous Operation

Name	Temperature
L1	124.4°C
Q8	125.2°C

2.4.1.1.3 Thermal Image 7 V_{IN} and 25 A_{OUT}

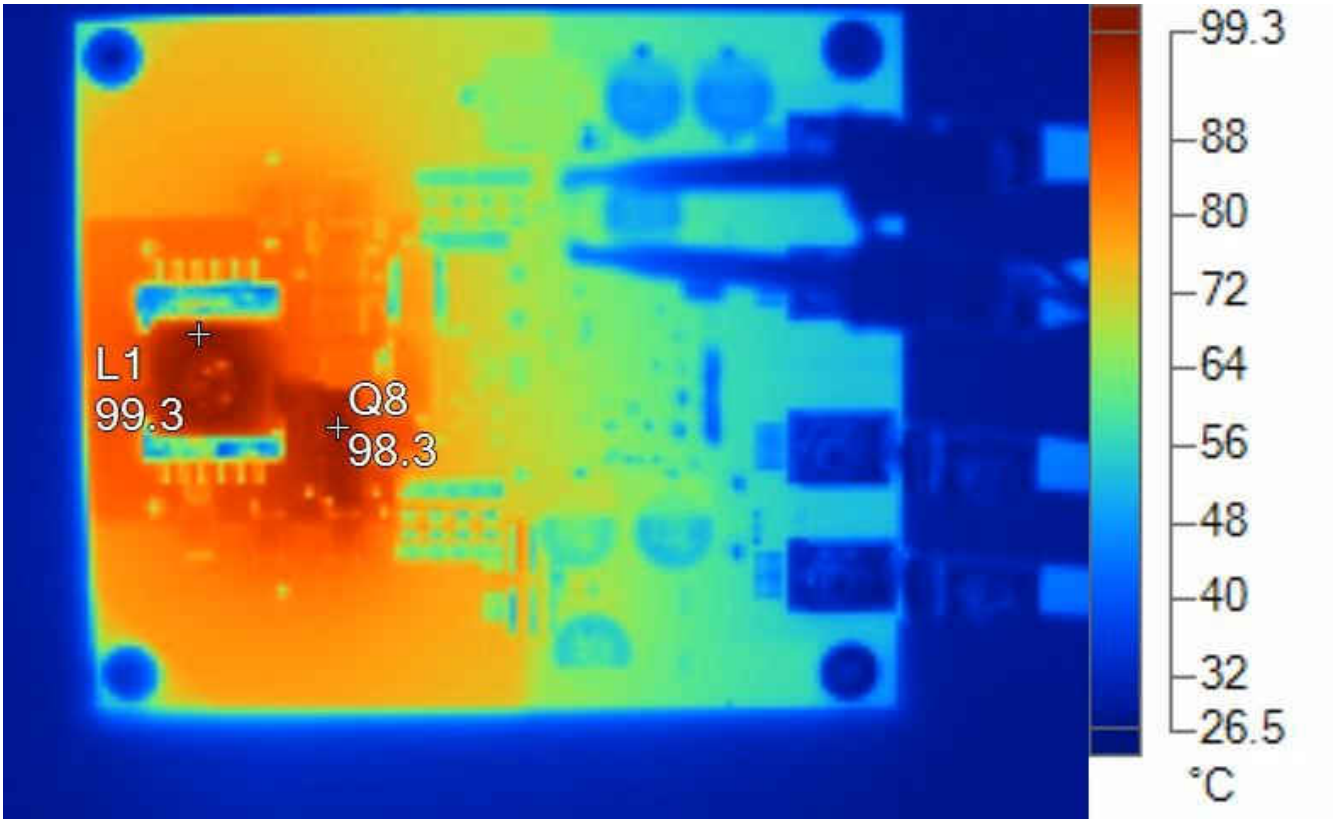


Low-side FETs at boost leg is the hot spot, high-current stress is present at the inductor.

Figure 2-13. 7.0-V_{IN}, 25-A_{OUT}, Continuous Operation

Name	Temperature
L1	120.6°C
Q8	119.6°C

2.4.1.1.4 Thermal Image 9 V_{IN} and 30 A_{OUT}



Low-side FETs at boost leg is the hot spot, high-current stress is present at the inductor.

Figure 2-14. 9.0 V_{IN}, 30 A_{OUT}, Continuous Operation

Name	Temperature
L1	99.3°C
Q8	98.3°C

2.4.1.1.5 Thermal Image 12 V_{IN} and 30 A_{OUT}

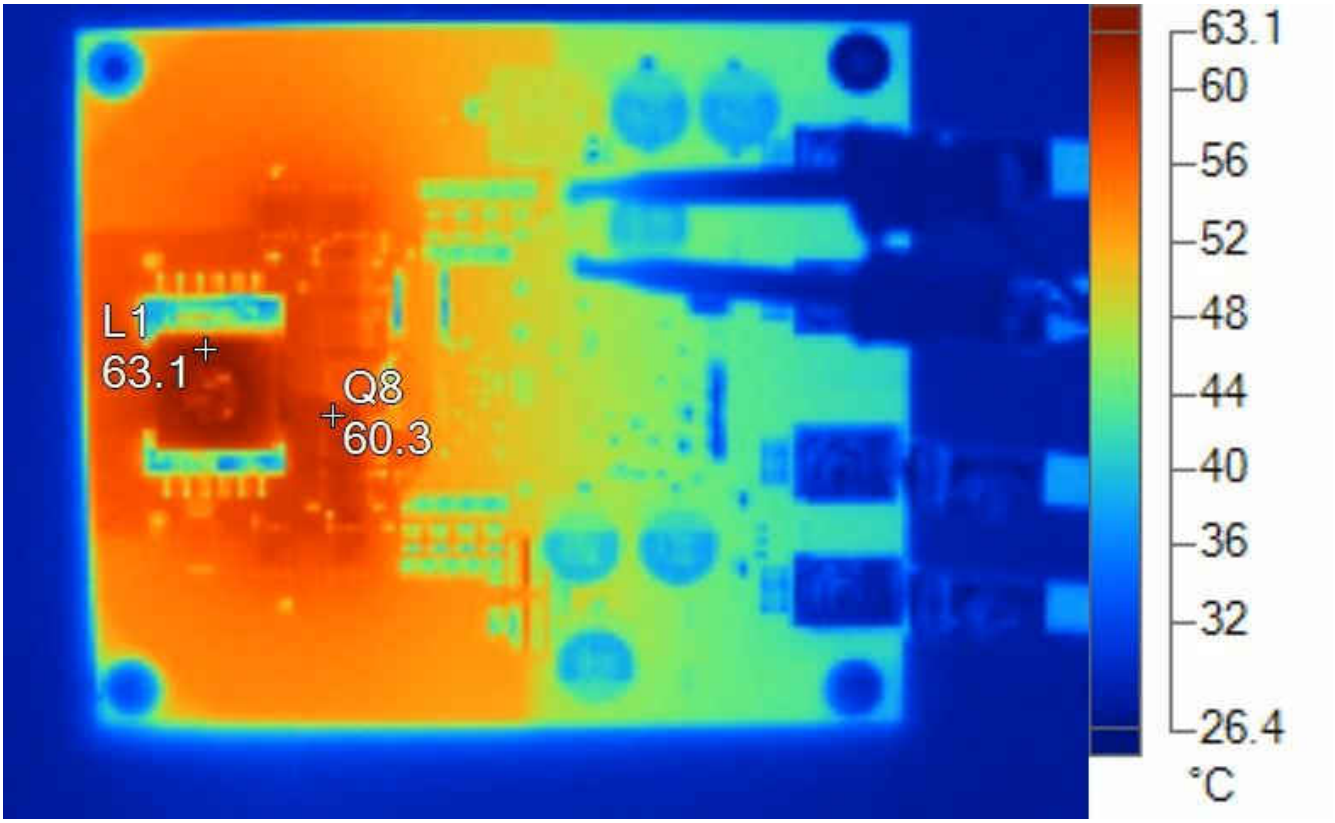


Figure 2-15. 12.0 V_{IN}, 30 A_{OUT}, Continuous Operation, Transition Mode at ½ F_{SW}

Name	Temperature
L1	63.1°C
Q8	60.3°C

2.4.1.1.6 Thermal Image 15 V_{IN} and 30 A_{OUT}

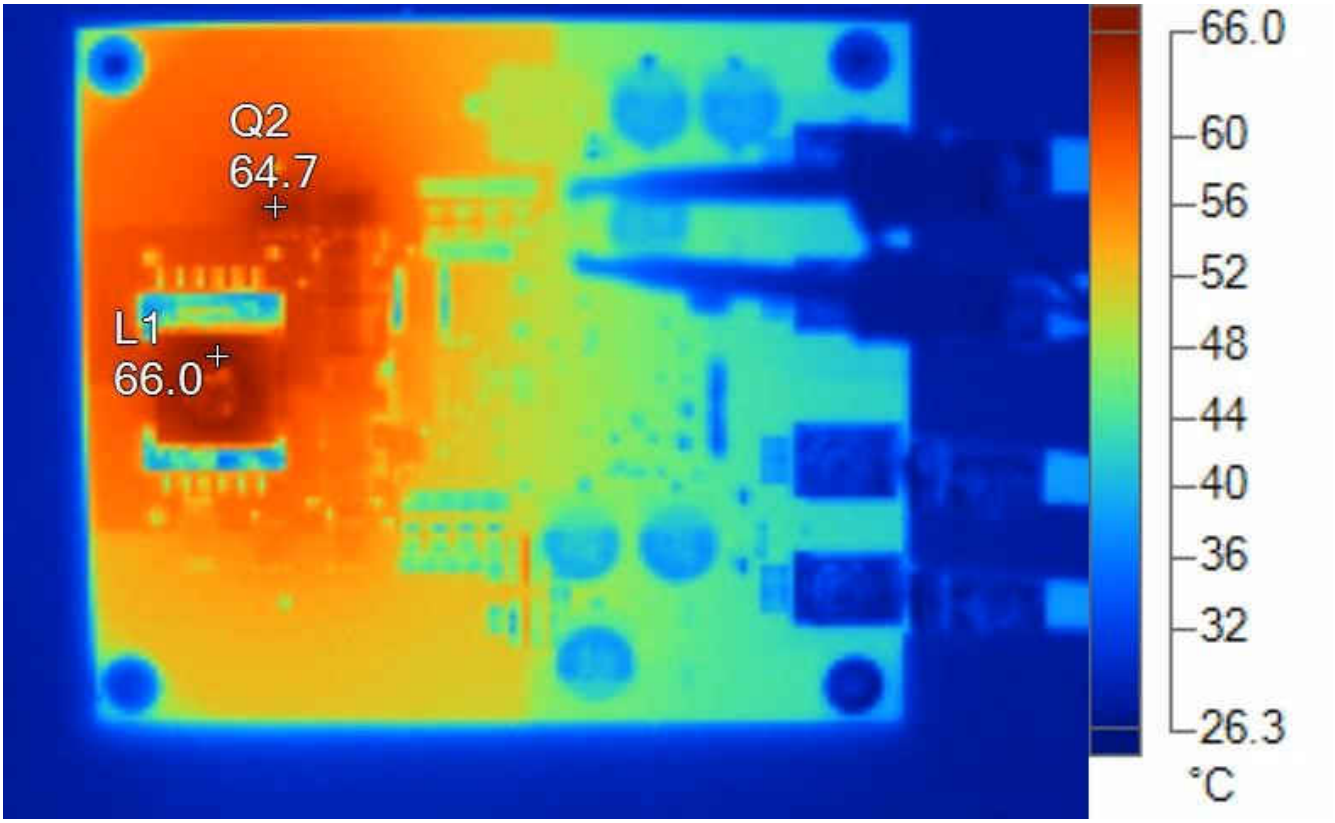
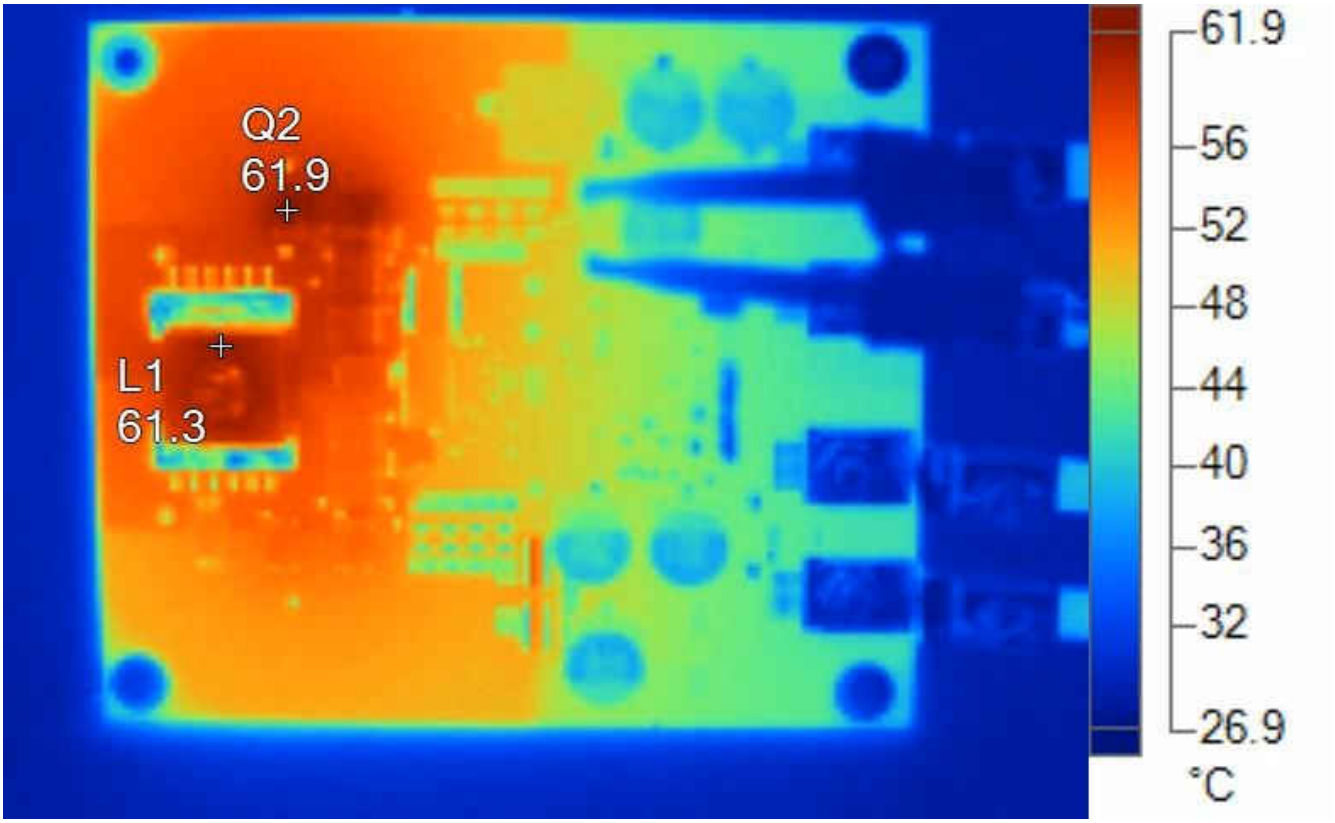


Figure 2-16. 15.0 V_{IN}, 30 A_{OUT}, Continuous Operation

Name	Temperature
L1	66.0°C
Q2	64.7°C

2.4.1.1.7 Thermal Image 13.8 V_{IN} and 30 A_{OUT}



Temperature rise dT +40°K at nominal operation.

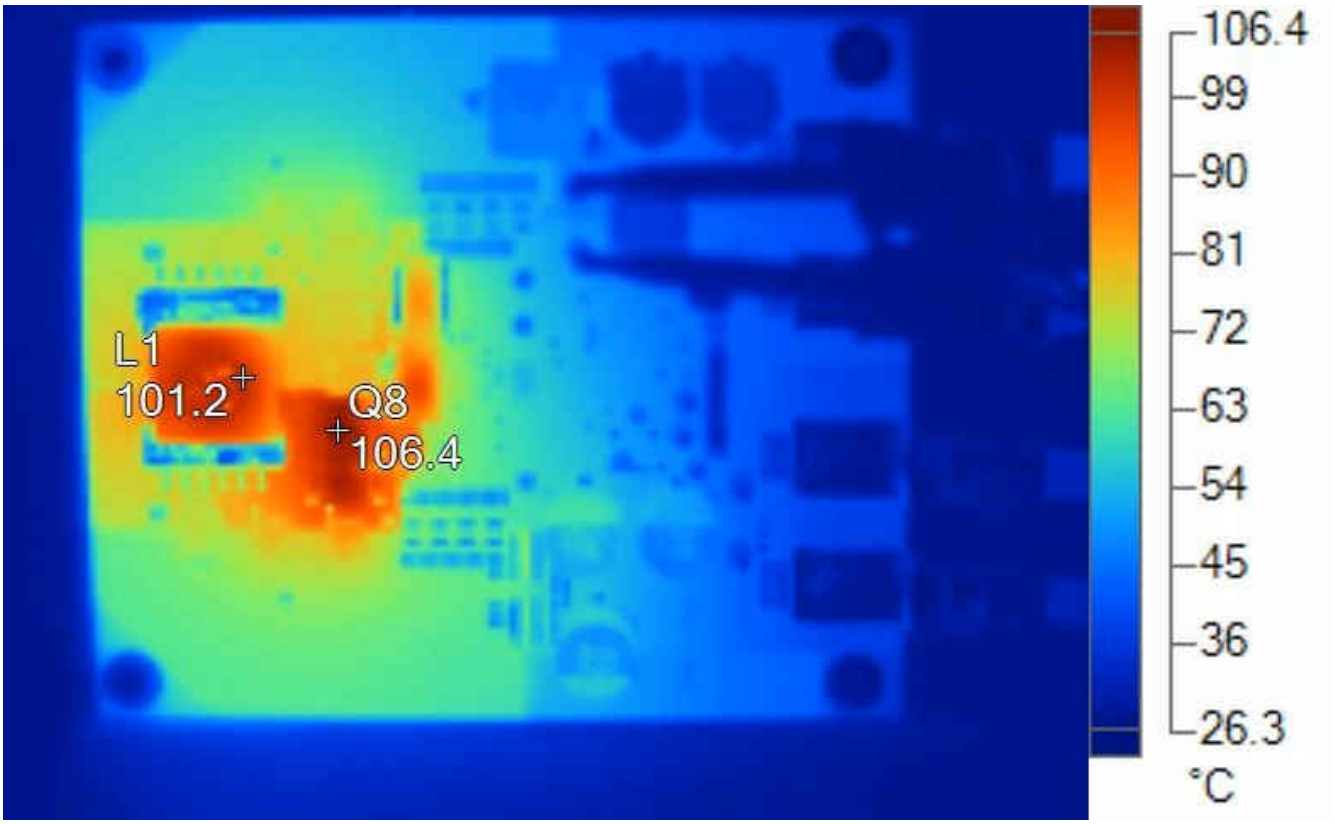
Figure 2-17. Typical Operation, 13.8 V_{IN}, 30 A_{OUT} Continuous, Buck Mode

Name	Temperature
L1	61.3°C
Q2	61.9°C

2.4.1.2 Forced Cooling

Forced cooling is applied with around 1-m/s, 200 lfm.

2.4.1.2.1 Thermal Image 4.5 V_{IN} and 20 A_{OUT}



Low-side FETs at boost leg is the hot spot.

Figure 2-18. 4.5 V_{IN}, 20 A_{OUT}, Continuous Operation

Name	Temperature
L1	101.2°C
Q8	**106.4°C**

2.4.1.2.2 Thermal Image 5.5 V_{IN} and 20 A_{OUT}

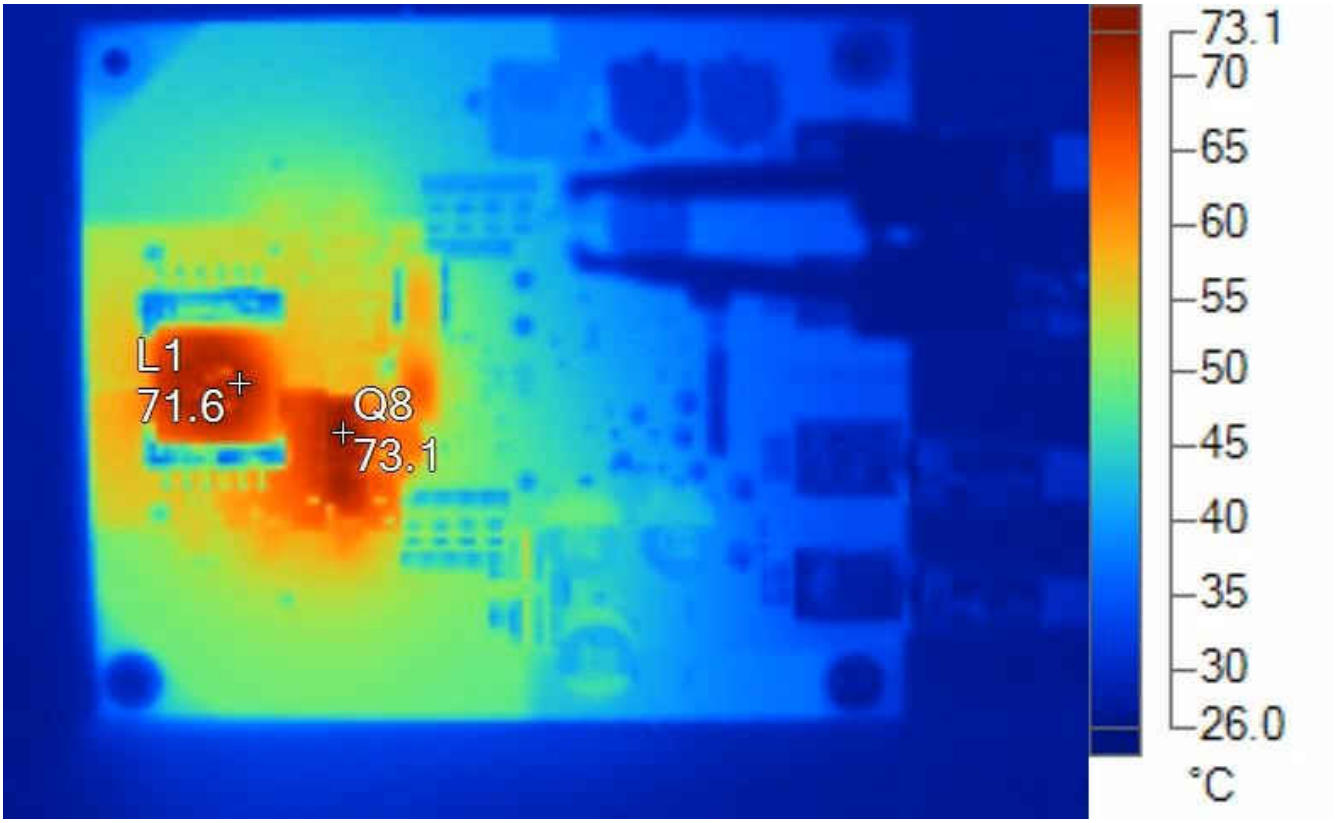


Figure 2-19. 5.5 V_{IN}, 20 A_{OUT}, Continuous Operation

Name	Temperature
L1	71.6°C
Q8	73.1°C

2.4.1.2.3 Thermal Image 7 V_{IN} and 25 A_{OUT}

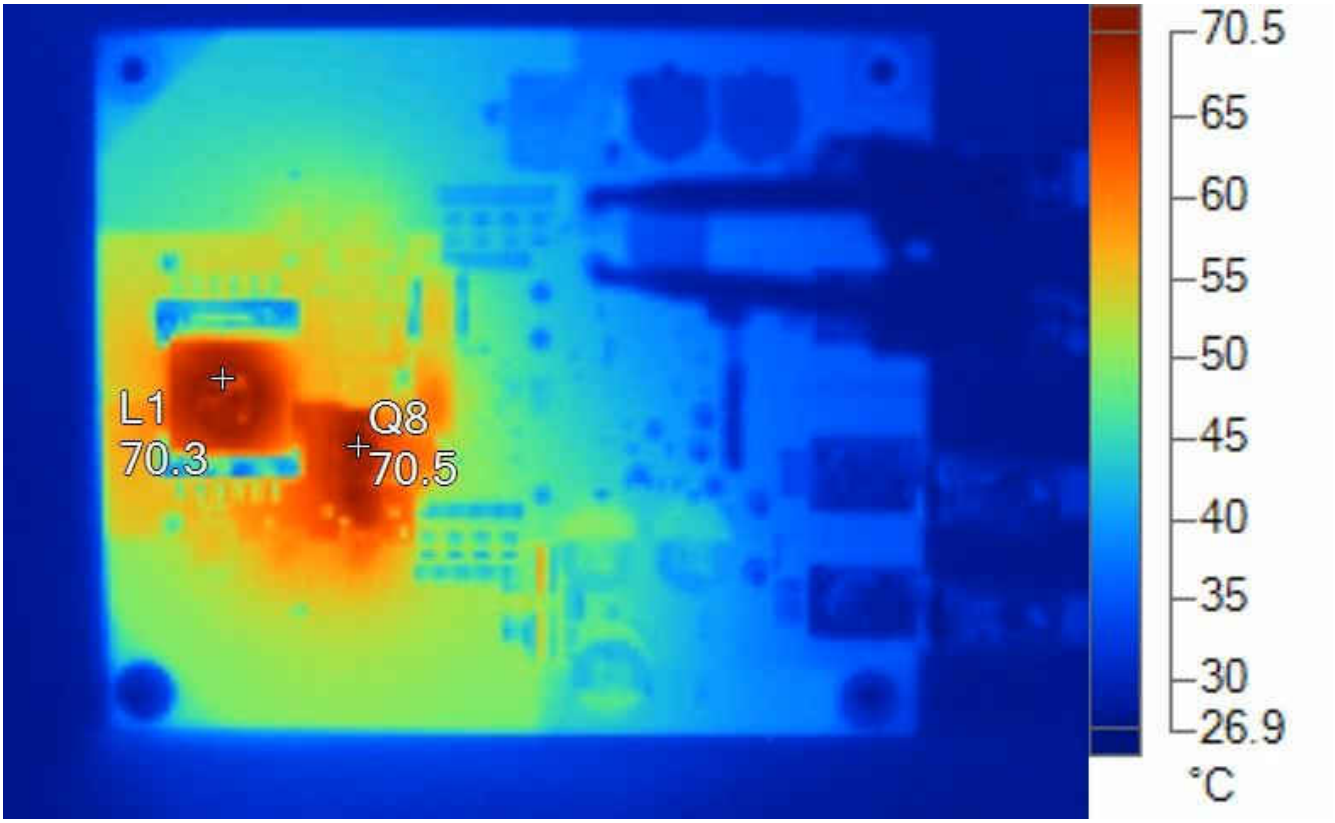


Figure 2-20. 7.0 V_{IN}, 25 A_{OUT}, Continuous Operation

Name	Temperature
L1	70.3°C
Q8	70.5°C

2.4.1.2.4 Thermal Image 9 V_{IN} and 30 A_{OUT}

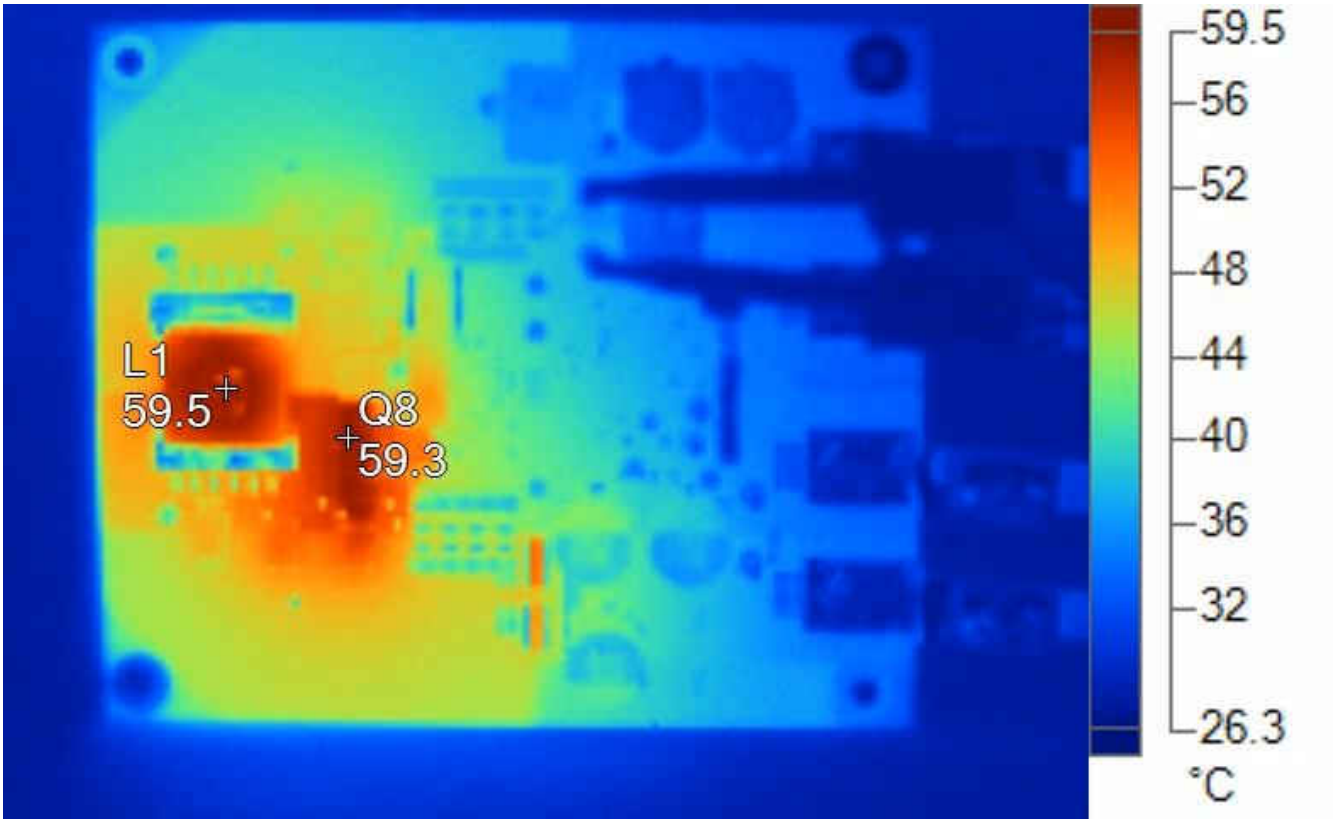


Figure 2-21. 9.0 V_{IN}, 30 A_{OUT}, Continuous Operation

Name	Temperature
L1	59.5°C
Q8	59.3°C

2.4.1.2.5 Thermal Image 12 V_{IN} and 30 A_{OUT}

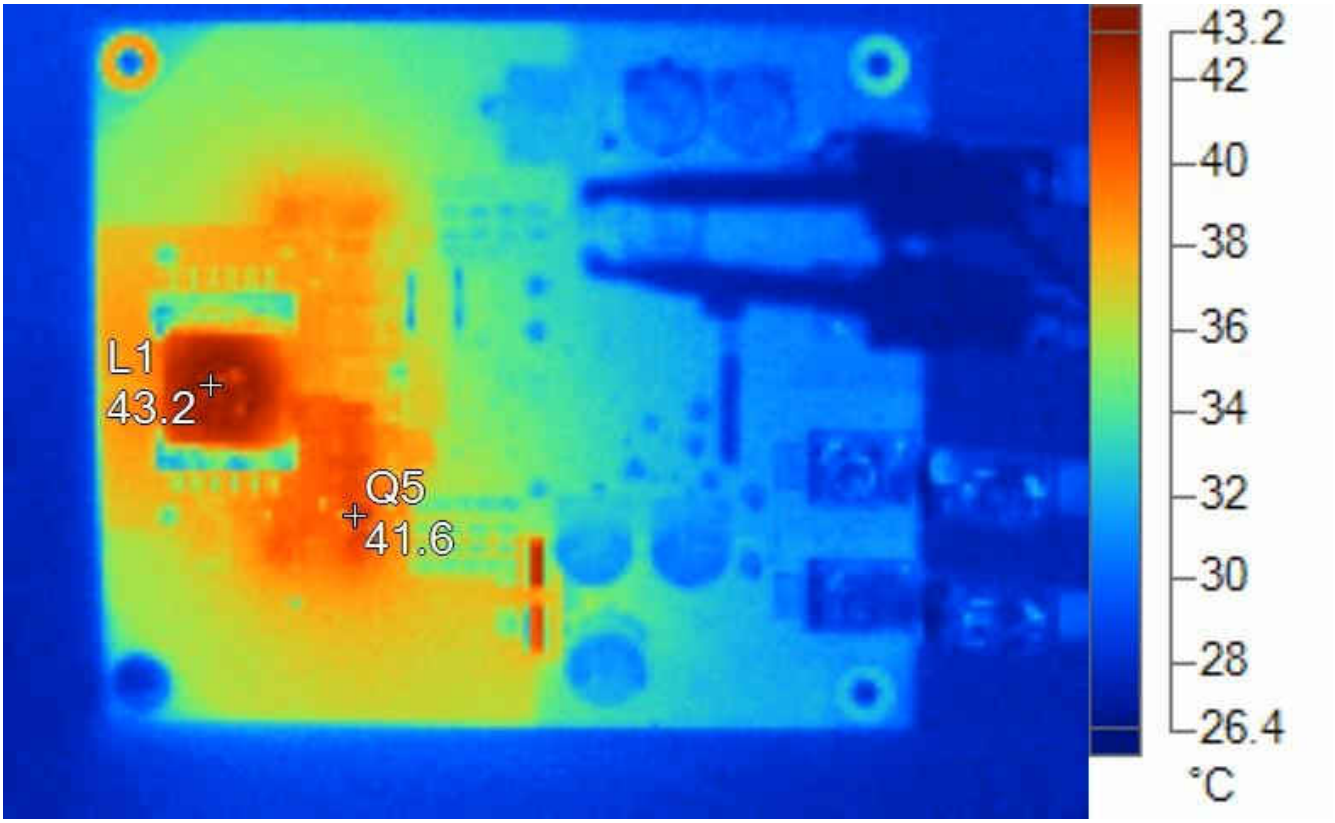
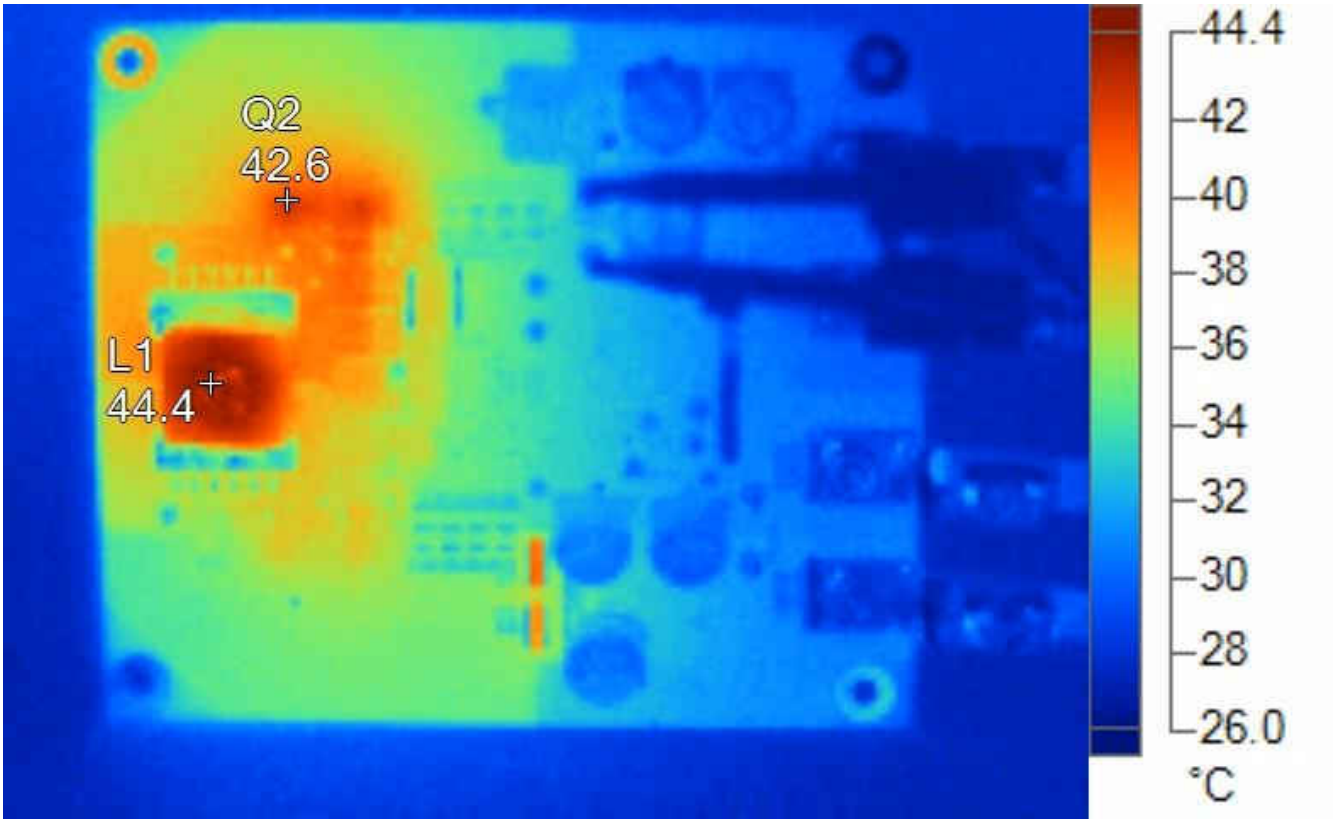


Figure 2-22. 12.0 V_{IN}, 30 A_{OUT}, Continuous Operation, Transition Mode at ½ F_{SW}

Name	Temperature
L1	43.2°C
Q5	41.6°C

2.4.1.2.6 Thermal Image 15 V_{IN} and 30 A_{OUT}



Nominal operation in buck mode or transition mode shows a temperature rise around +20°K by forced cooling.

Figure 2-23. 15 V_{IN}, 30 A_{OUT}, Continuous Operation

Name	Temperature
L1	44.4°C
Q2	42.6°C

2.5 Bode Plots

Table 2-1 details a summary of the test results from the bode plots.

Table 2-1. Summary of the Bode Plots Test Results

V_{IN}	4.5 V	7 V	9 V	12 V	16 V	27 V
Bandwidth (kHz)	0.956	1.54	2.0	2.72	3.75	3.68
Phase Margin	61.2°	73.7°	78°	80.9°	77.4°	82.2
Slope (20 dB/ decade)	–1.18	–1	–1.1	–0.77	–1.2	–1
Gain Margin (dB)	–14.8	20.2	–20.5	–18.4	25	–26.5
Slope (20 dB/ decade)	–1.3	–1.4	–1.11	–1.41	–2.4	–2.3
Freq (kHz)	5.59	23.8	–24.9	24.4	39.7	46

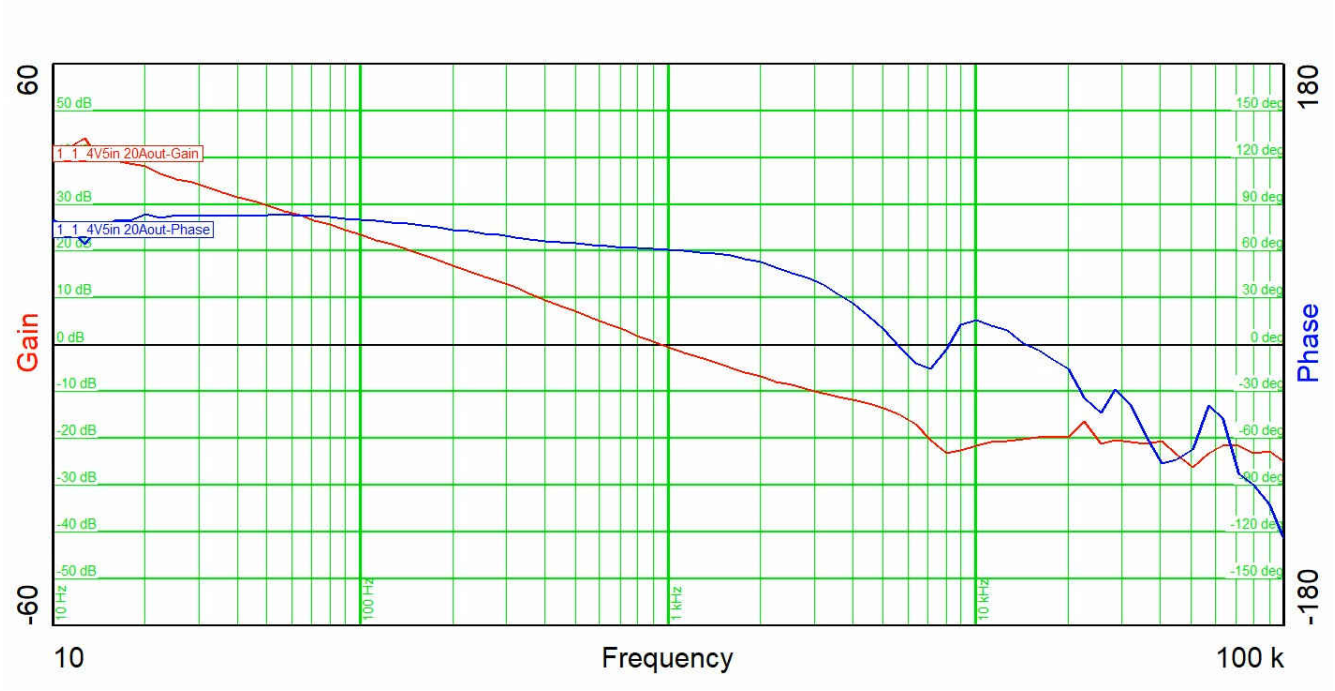


Figure 2-24. Bode Plot for 4.5-V Input Voltage and 20-A Output Voltage

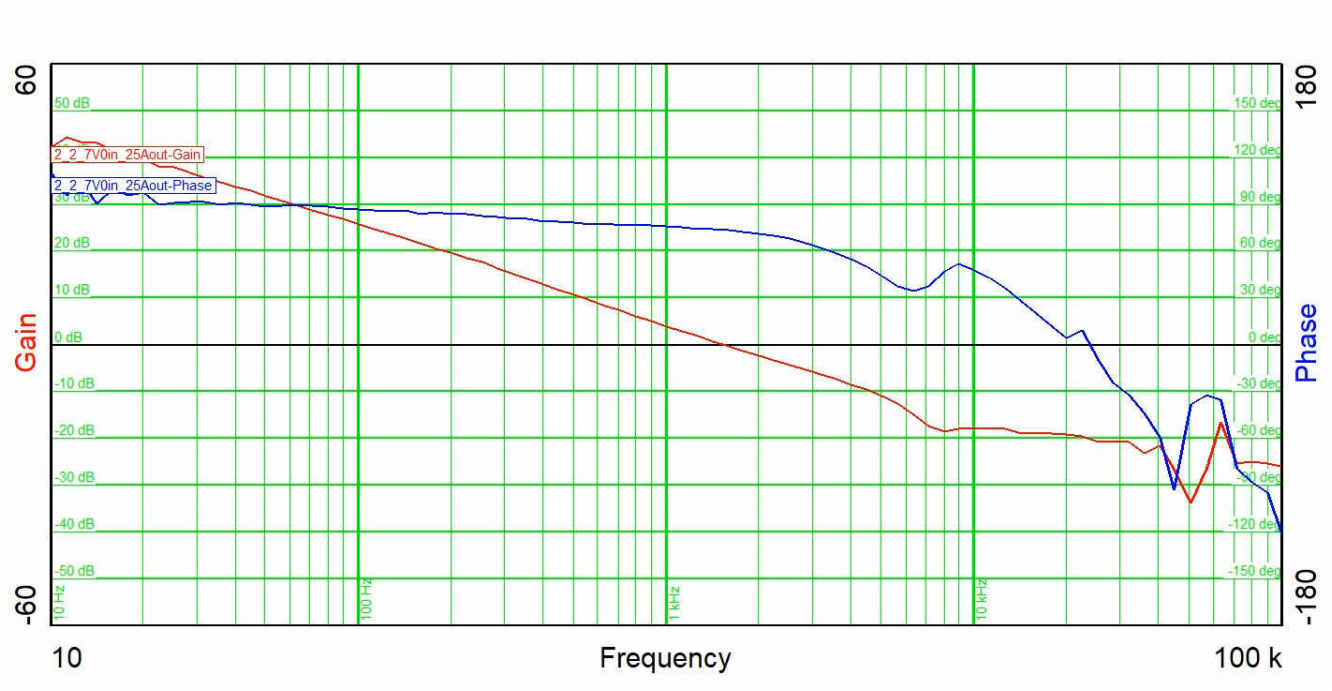


Figure 2-25. Bode Plot for 7-V Input Voltage and 25-A Output Voltage

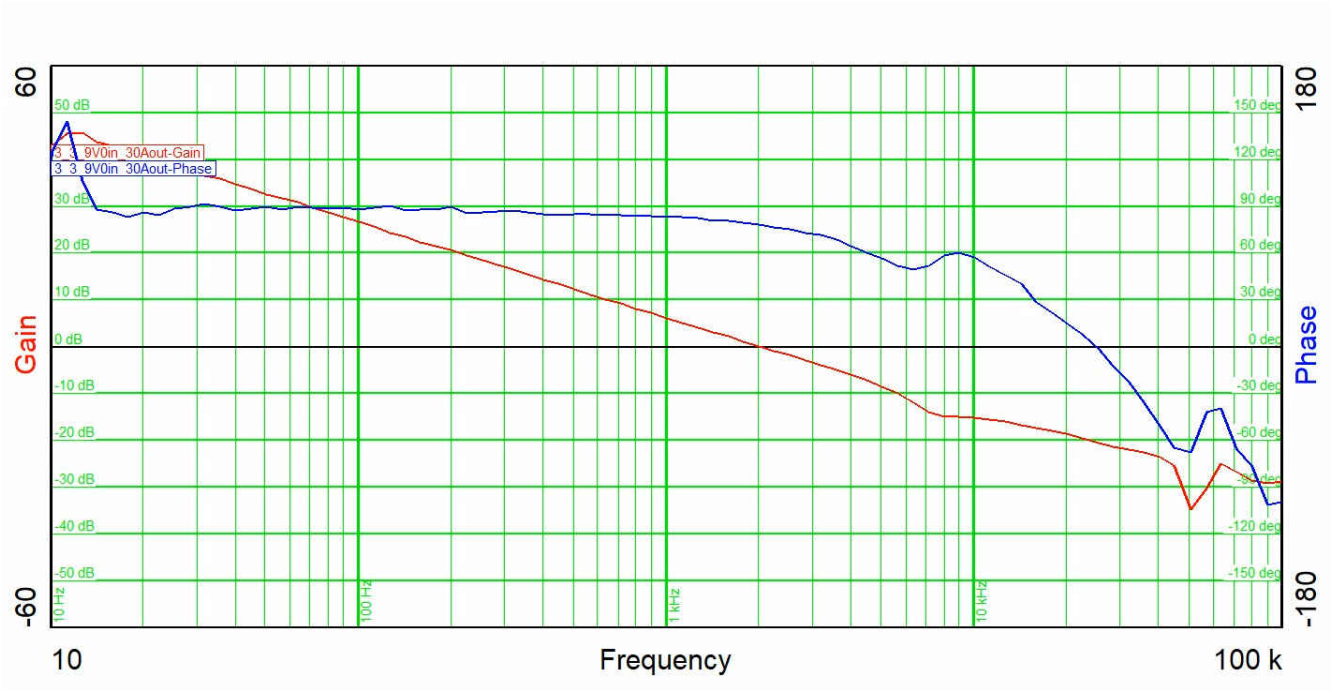


Figure 2-26. Bode Plot for 9-V Input Voltage and 30-A Output Voltage

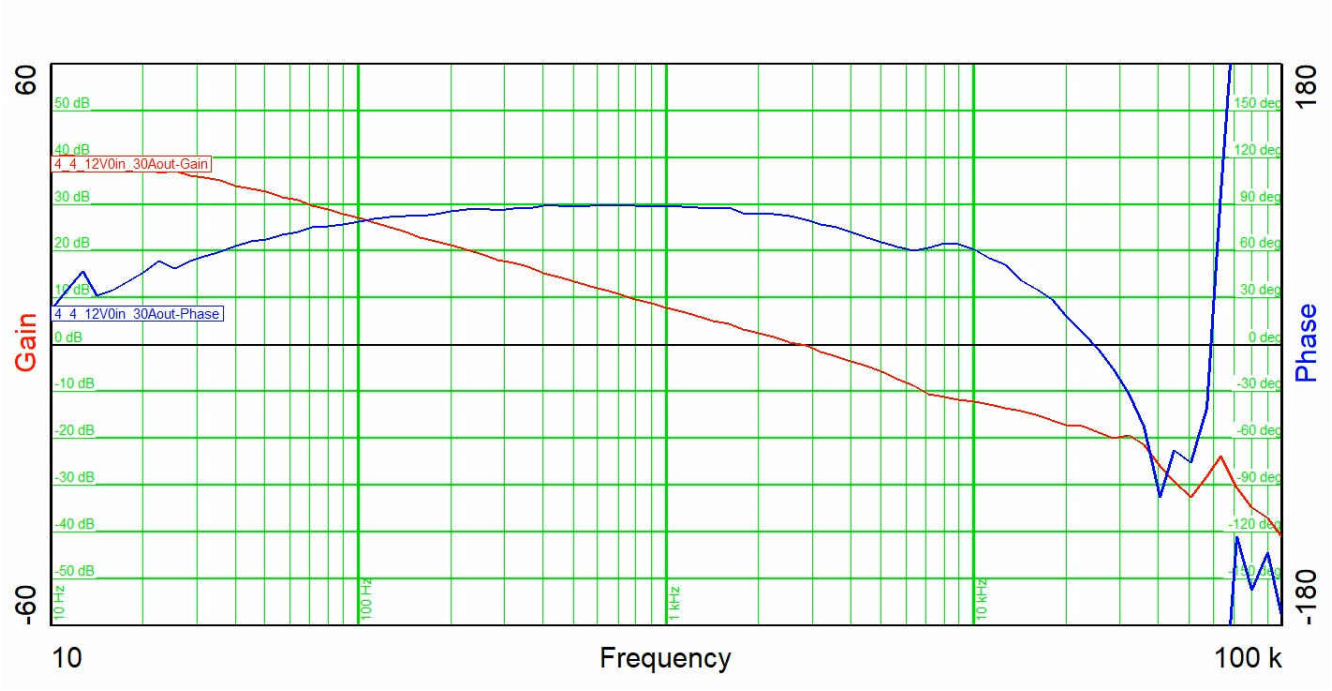


Figure 2-27. Bode Plot for 12-V Input Voltage and 30-A Output Voltage

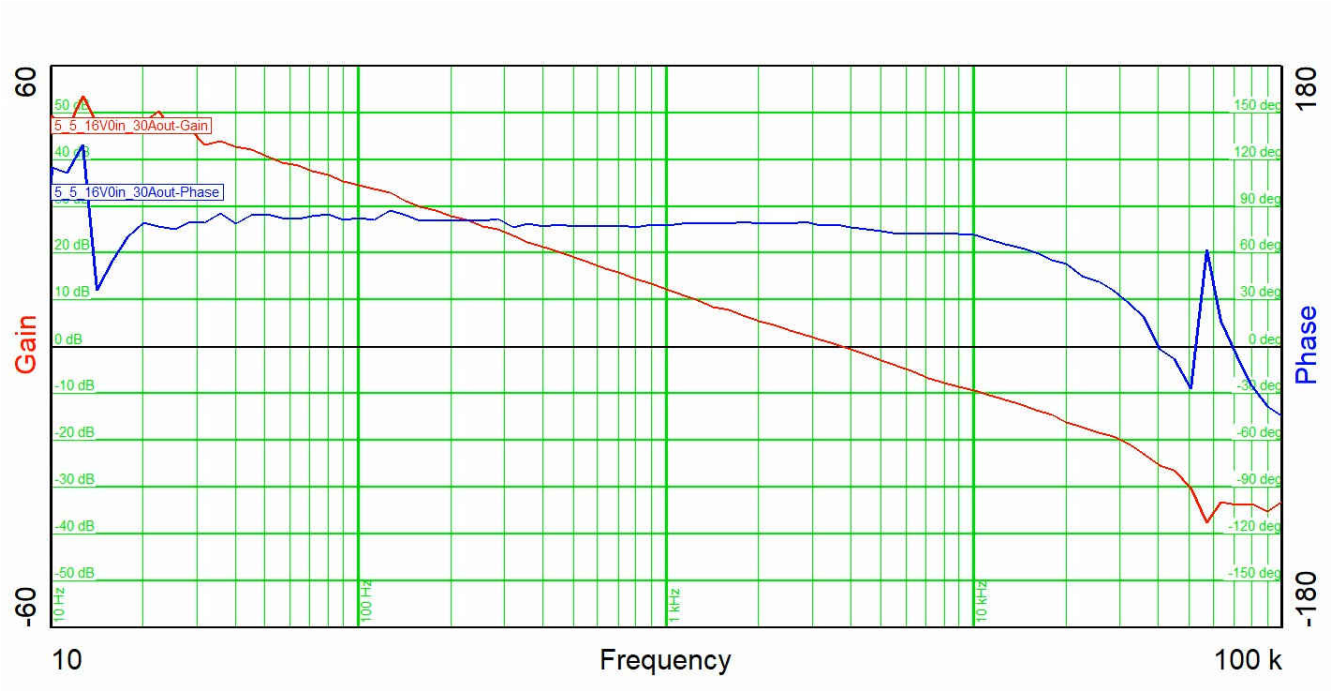


Figure 2-28. Bode Plot for 16-V Input Voltage and 30-A Output Voltage

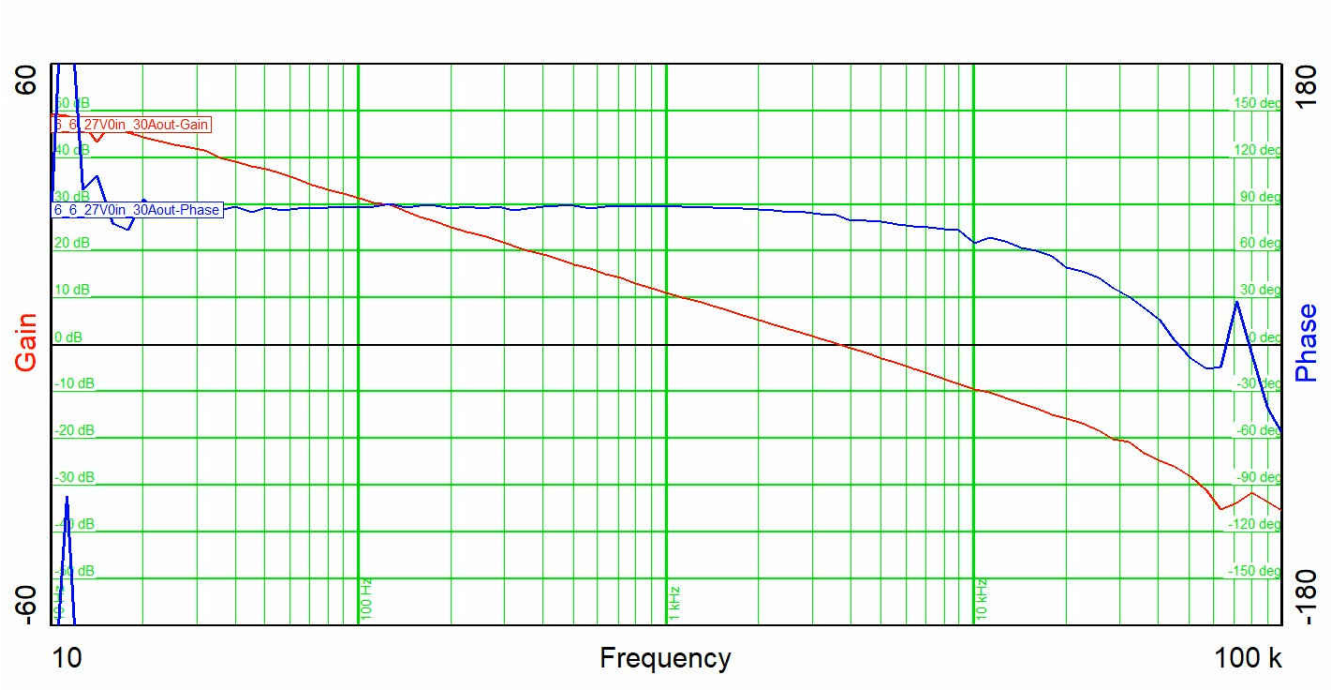
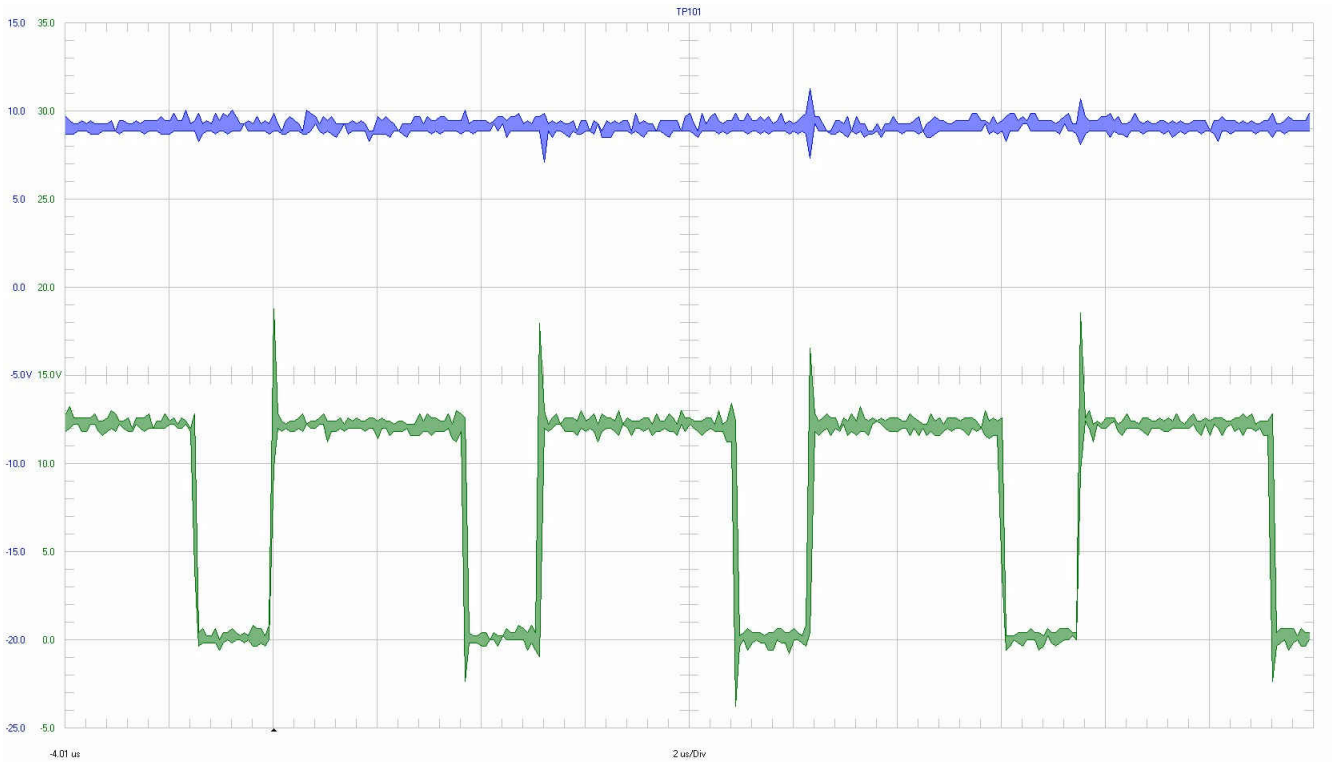


Figure 2-29. Bode Plot for 27-V Input Voltage and 30-A Output Voltage

3 Waveforms

3.1 Switching

3.1.1 9-V Input Voltage (Boost Mode)

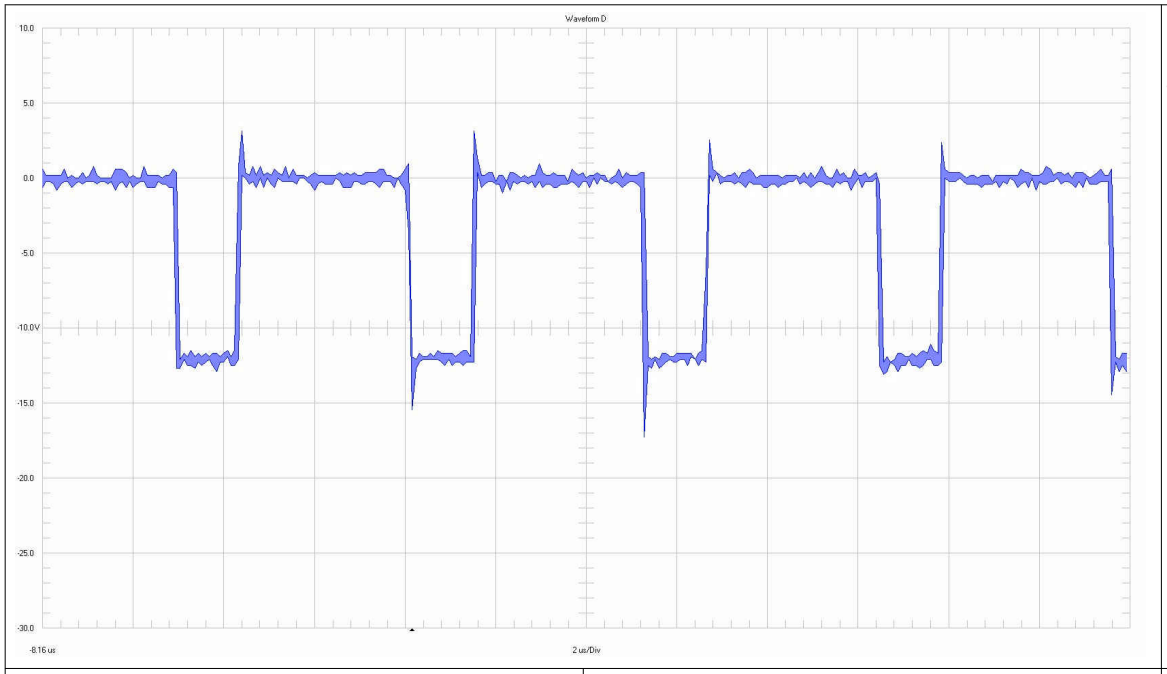


Ch1 ⇒ TP101 (Q3, Q4: drain to GND)
Ch2 ⇒ TP102 (Q7, Q8: drain to GND)
5 V / div
2 µs / div
full bandwidth

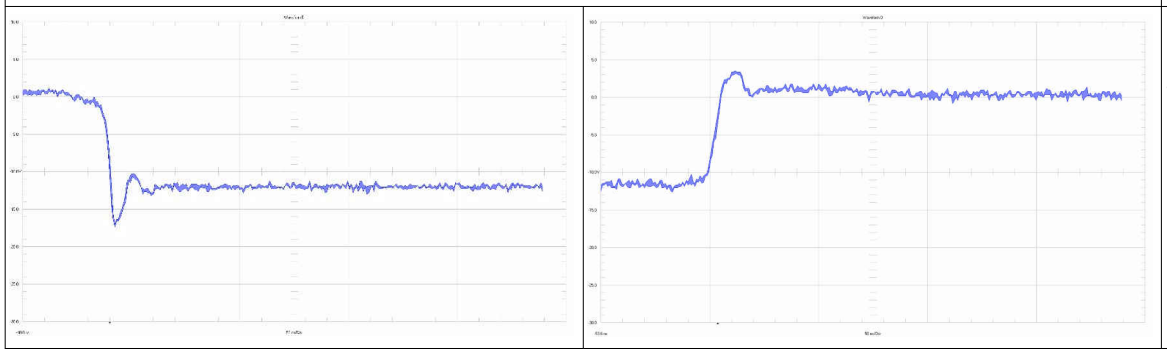
Figure 3-1. Waveform Low-Side FETs (Drain to GND) Boost Mode

3.1.1.1 Boost High Side FETs (Q5, Q6)

3.1.1.1.1 Source-Drain (Referenced to V_{OUT}')



CH1 ⇒ 5 V / div
2 µs /div
full bandwidth



CH1 ⇒ 5 V / div
50 ns / major div
full bandwidth

Figure 3-2. Waveform High-Side FET Source-Drain

3.1.1.1.2 Gate-Source

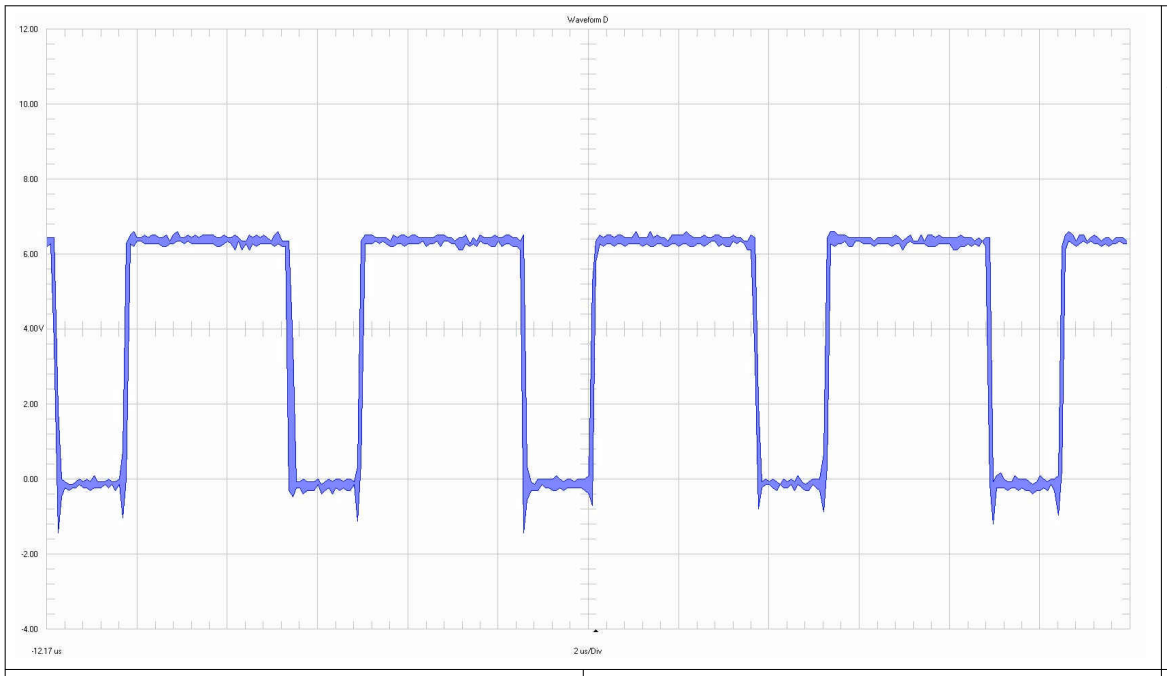
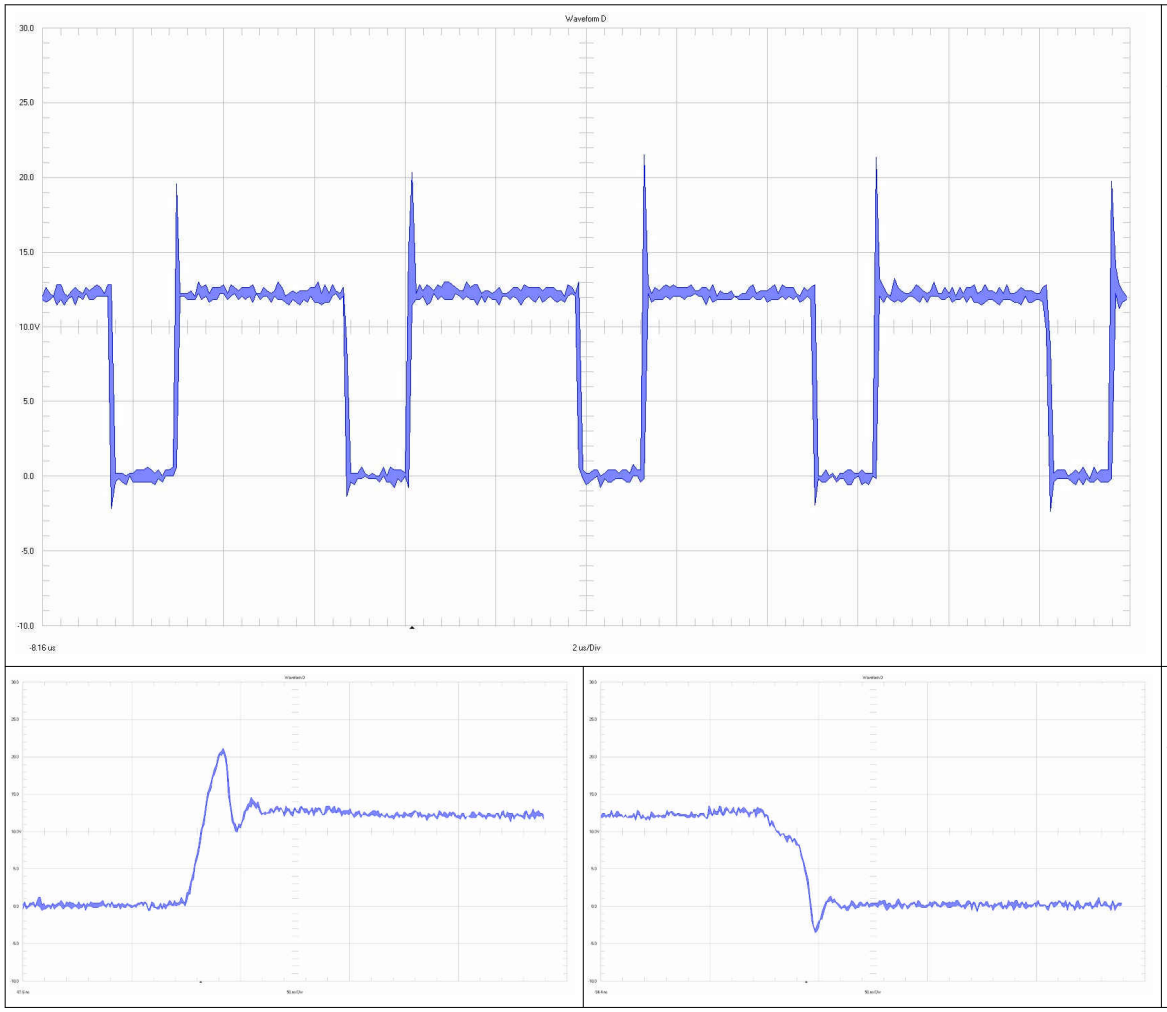


Figure 3-3. Waveform High-Side FET Gate - Source

3.1.1.2 Boost Low Side (Q7, Q8)

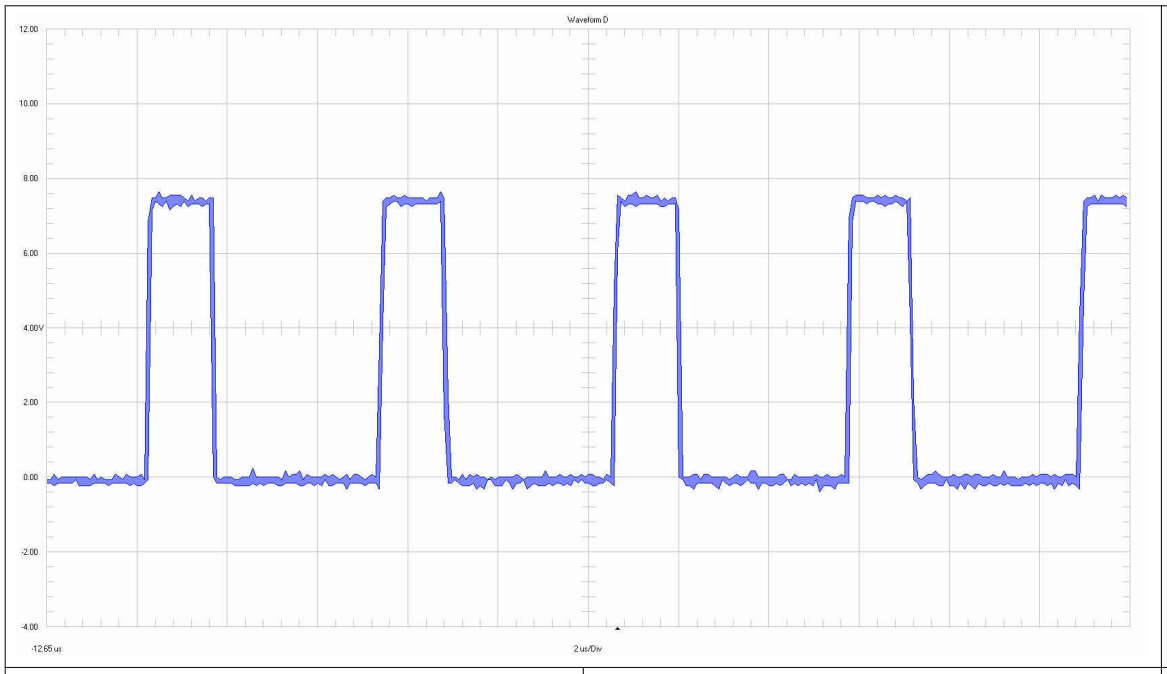
3.1.1.2.1 Drain-GND



	CH1 ⇒ 5 V / div 2 µs /div full bandwidth
	CH1 ⇒ 5 V / div 50 ns / major div full bandwidth

Figure 3-4. Waveform Low Side FET Drain-GND

3.1.1.2.2 Gate-GND

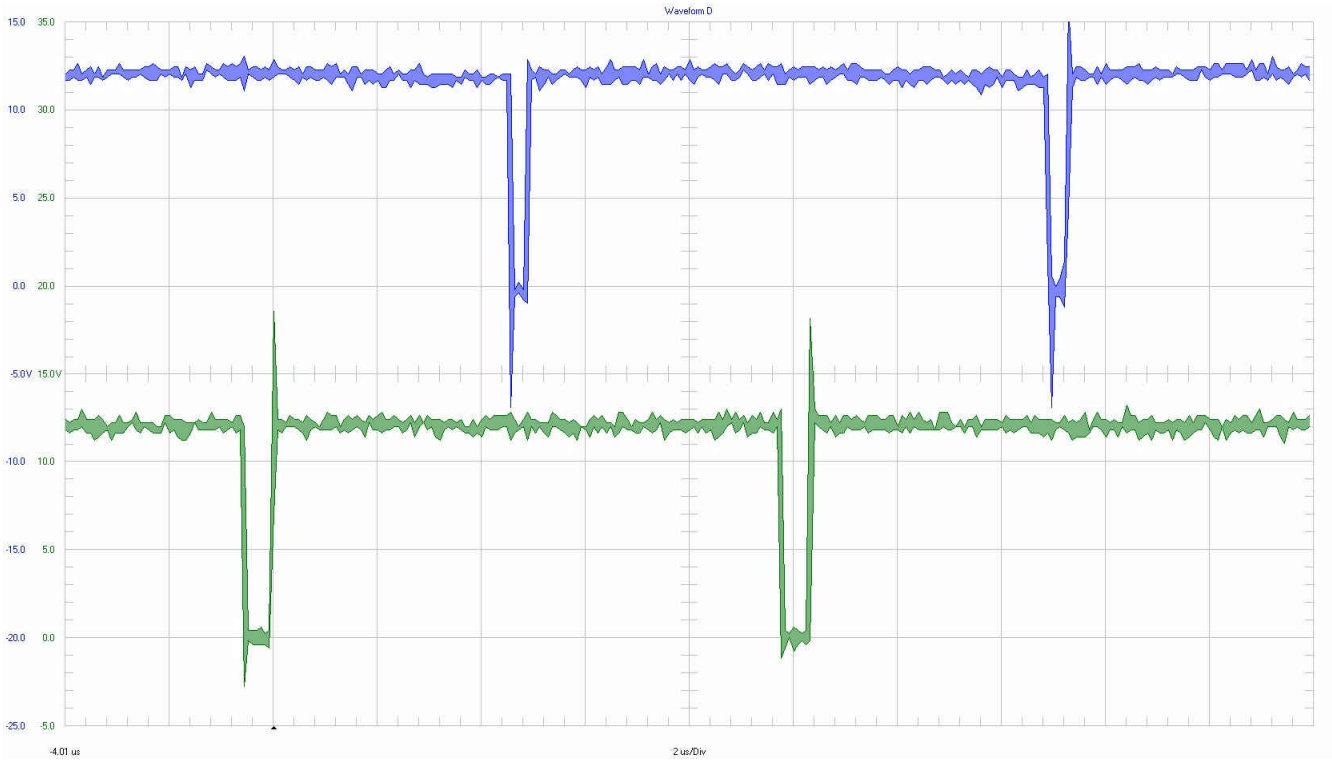


CH1 ⇒ 2 V / div
2 µs /div
full bandwidth

CH1 ⇒ 2 V / div
50 ns / major div
full bandwidth

Figure 3-5. Waveform Low-Side FET Gate – GND

3.1.2 12-V Input Voltage, Transition Mode, Both Legs Switching at ½ F_{SW}



Ch1 ⇒ TP101 (Q3, Q4: drain to GND)
Ch2 ⇒ TP102 (Q7, Q8: drain to GND)
5 V / div
2 µs / div
full bandwidth

Figure 3-6. Waveform Low-Side FETs (Drain to GND) Buck-Boost Mode

3.1.2.1 Boost High Side FETs (Q5, Q6)

3.1.2.1.1 Source-Drain (Referenced to V_{OUT}')

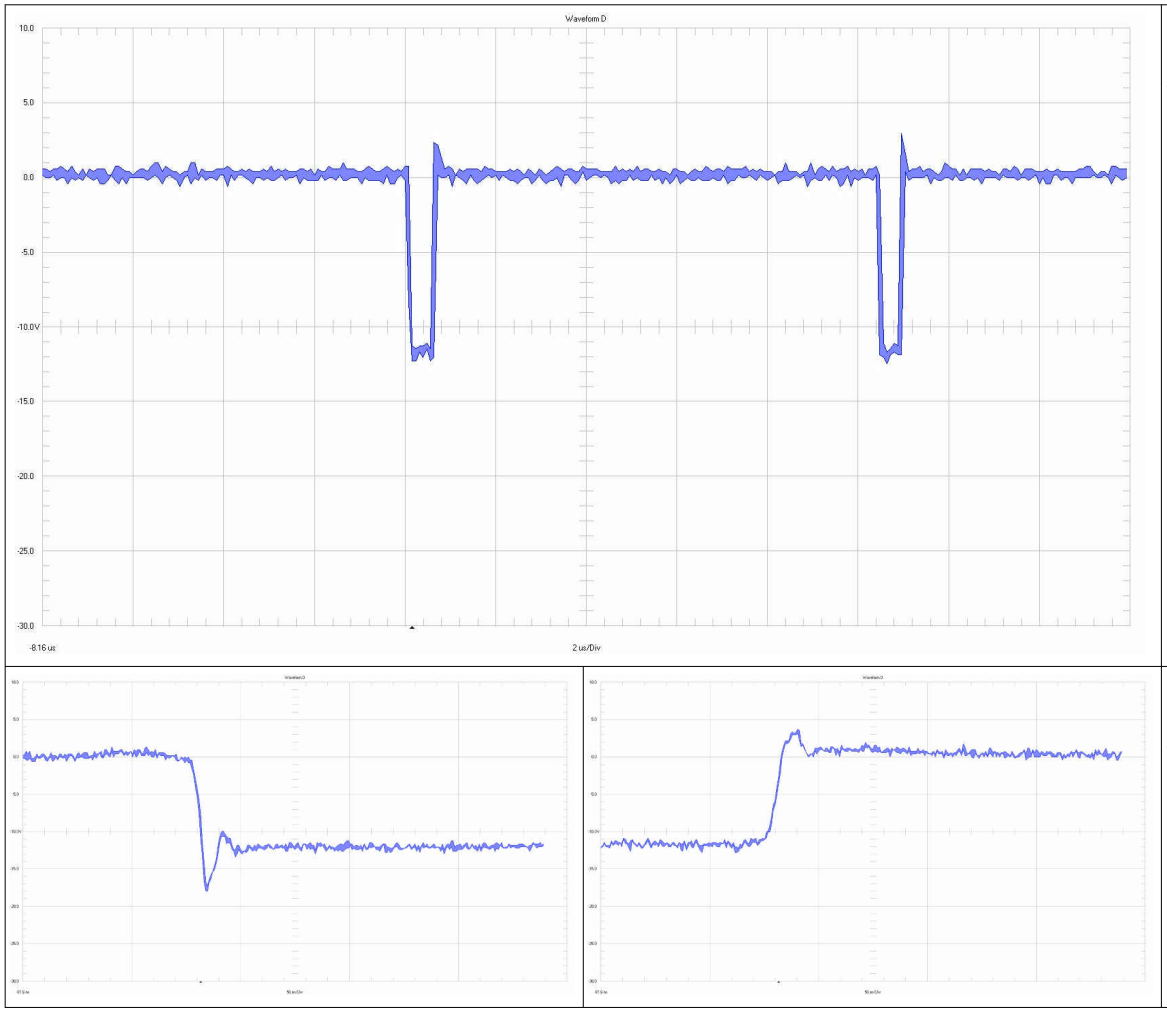
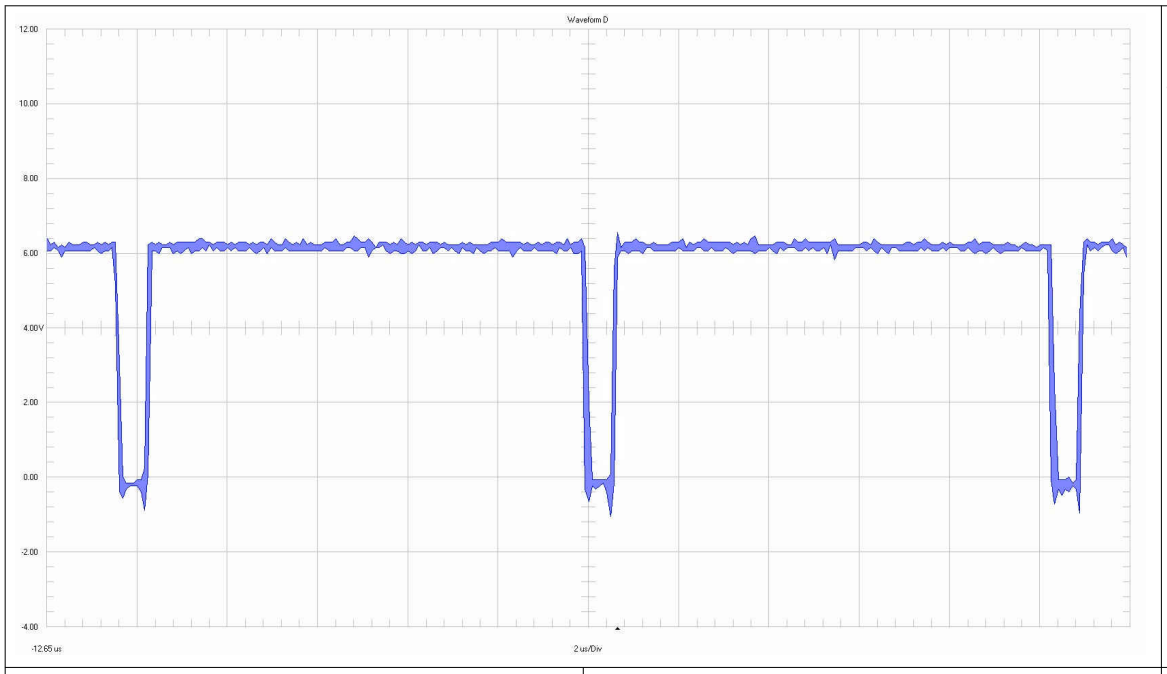


Figure 3-7. Waveform High Side FET Source-Drain

3.1.2.1.2 Gate-Source



CH1 ⇒ 2 V / div
2 µs /div
full bandwidth

CH1 ⇒ 2 V / div
50 ns / div
full bandwidth

Figure 3-8. Waveform High-Side FET Gate - Source

3.1.2.2 Boost Low Side (Q7, Q8)

3.1.2.2.1 Drain-GND

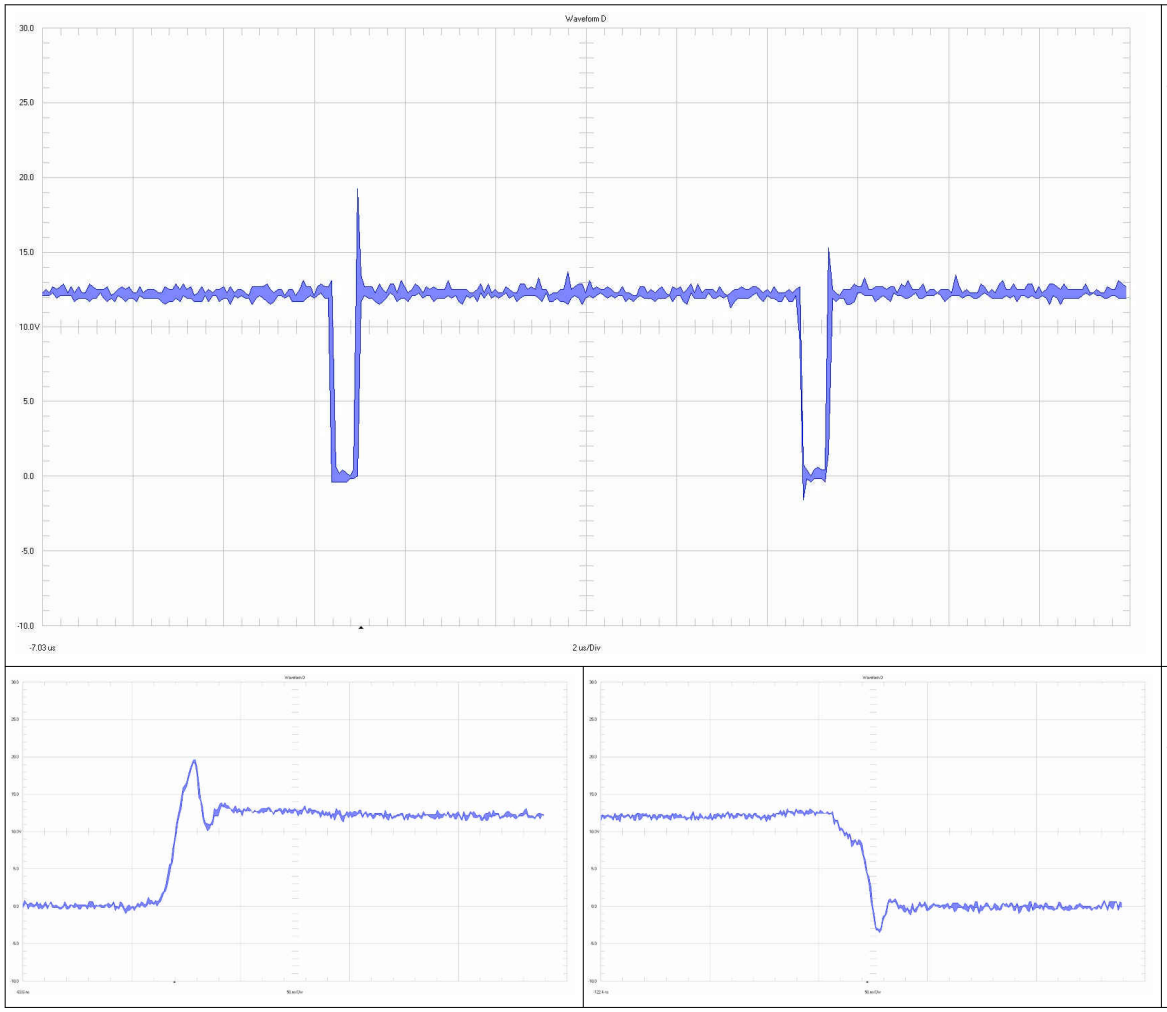
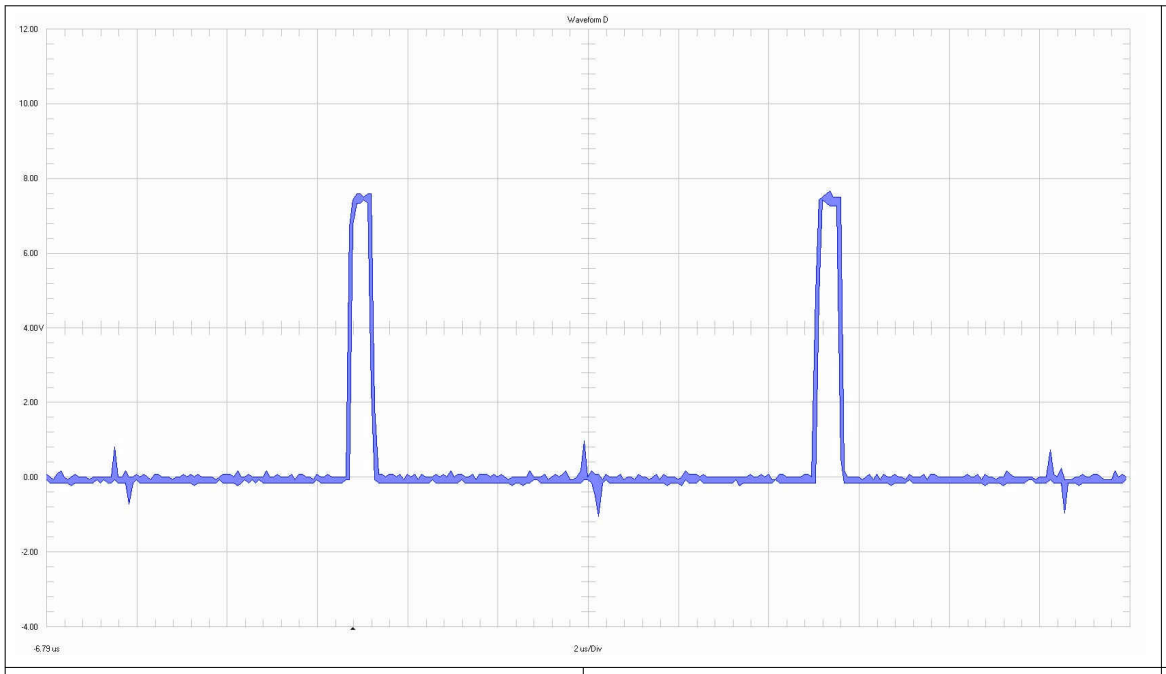
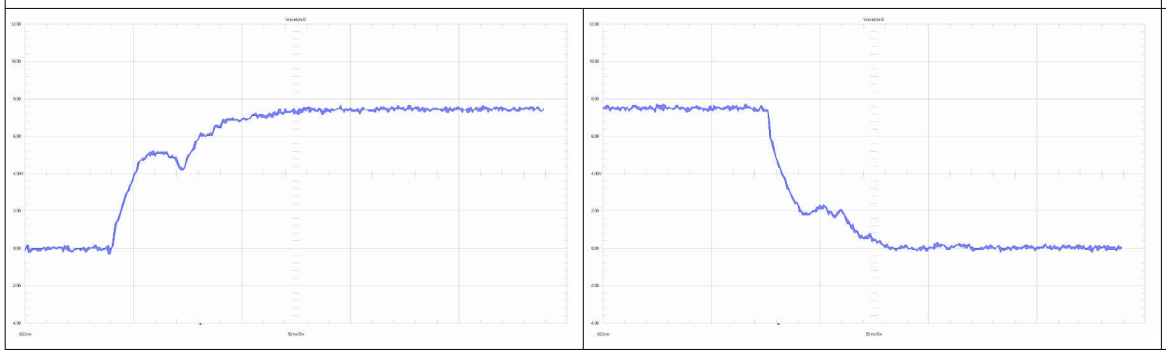


Figure 3-9. Waveform Low Side FET Drain-GND

3.1.2.2.2 Gate-GND



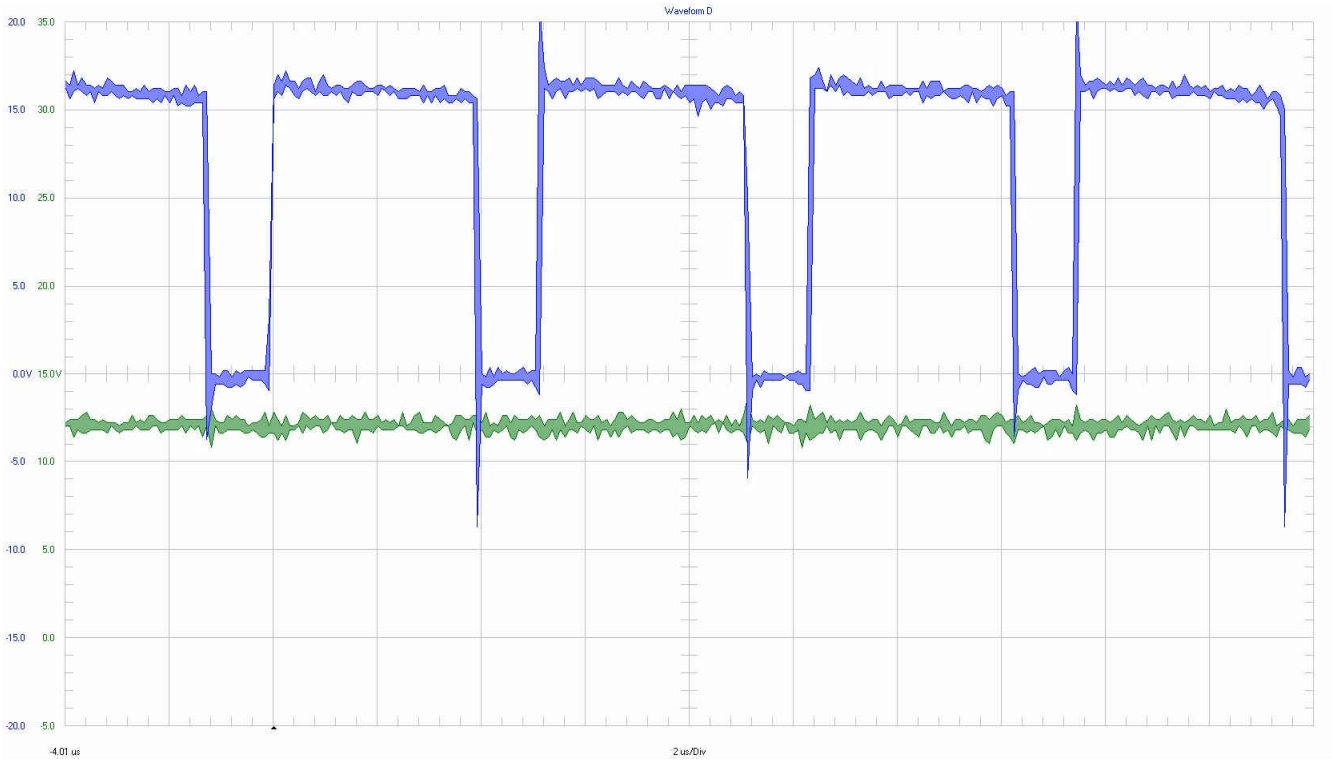
CH1 ⇒ 2 V / div
50 ns / major div
full bandwidth



CH1 ⇒ 2 V / div
50 ns / major div
full bandwidth

Figure 3-10. Waveform Low-Side FET Gate – GND

3.1.3 16-V Input Voltage, Buck Mode

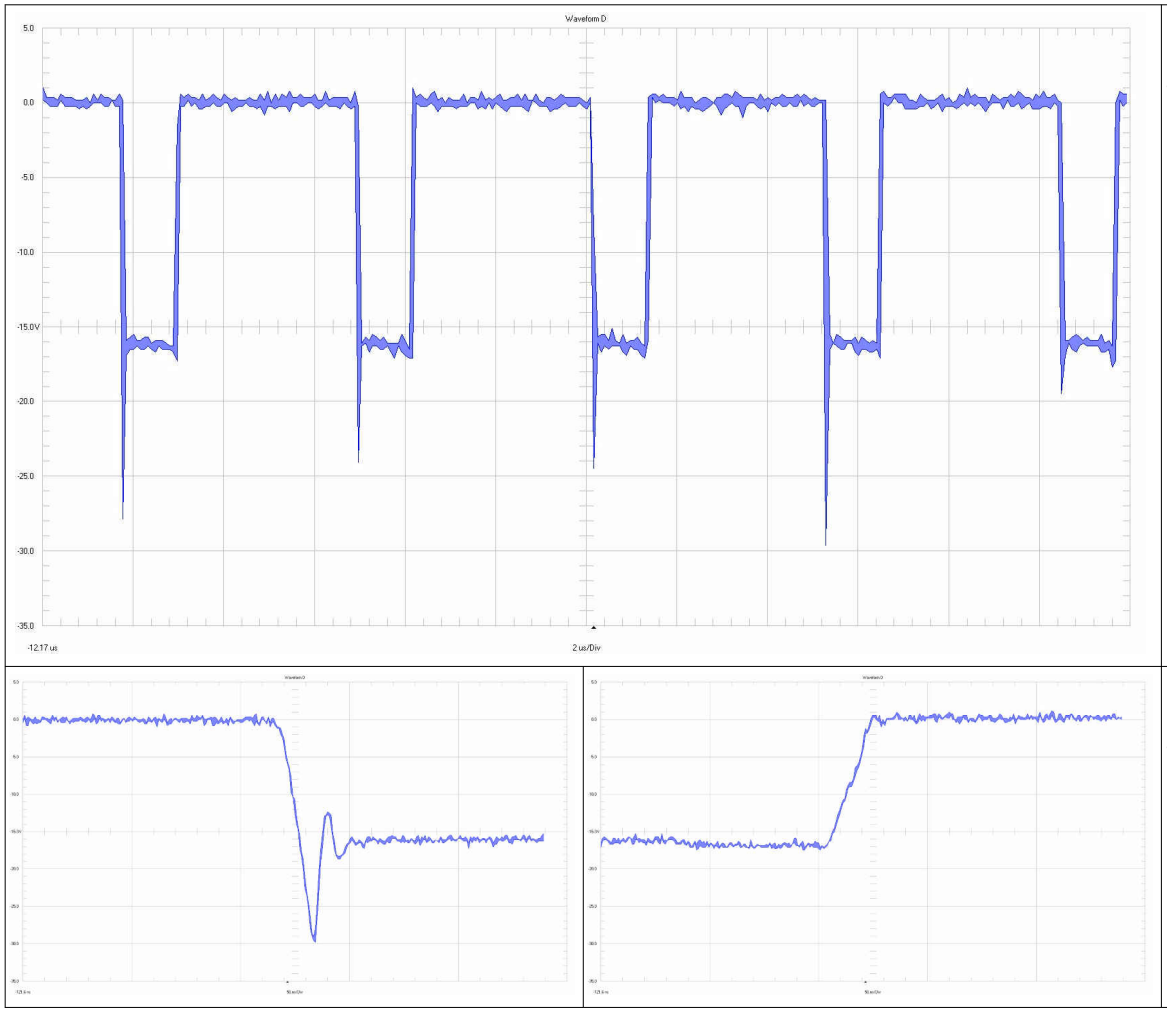


Ch1 ⇒ TP101 (Q3, Q4: drain to GND)
Ch2 ⇒ TP102 (Q7, Q8: drain to GND)
5 V / div
2 µs / div
full bandwidth

Figure 3-11. Waveform Low-Side FETs (Drain to GND) Boost Mode

3.1.3.1 Buck High Side FETs (Q1, Q2)

3.1.3.1.1 Source-Drain (Referenced to V_{IN}')



	CH1 ⇒ 5 V / div 2 µs /div full bandwidth
	CH1 ⇒ 5 V / div 50 ns / div full bandwidth

Figure 3-12. Waveform High Side FET Source-Drain

3.1.3.1.2 Gate-Source

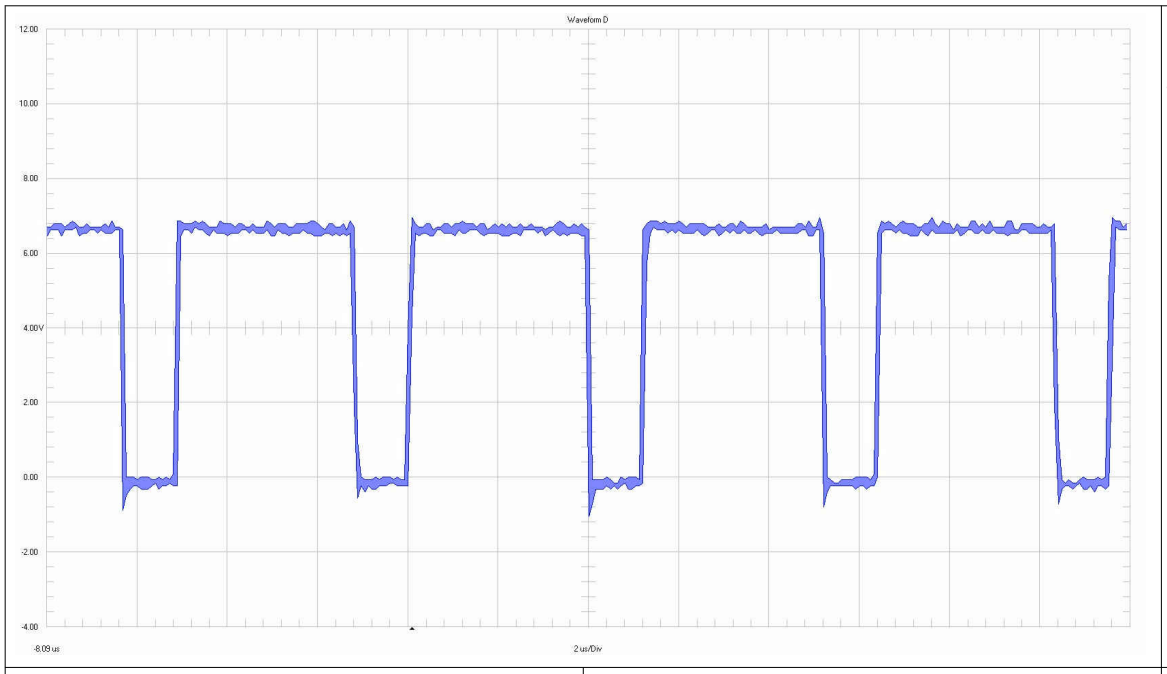
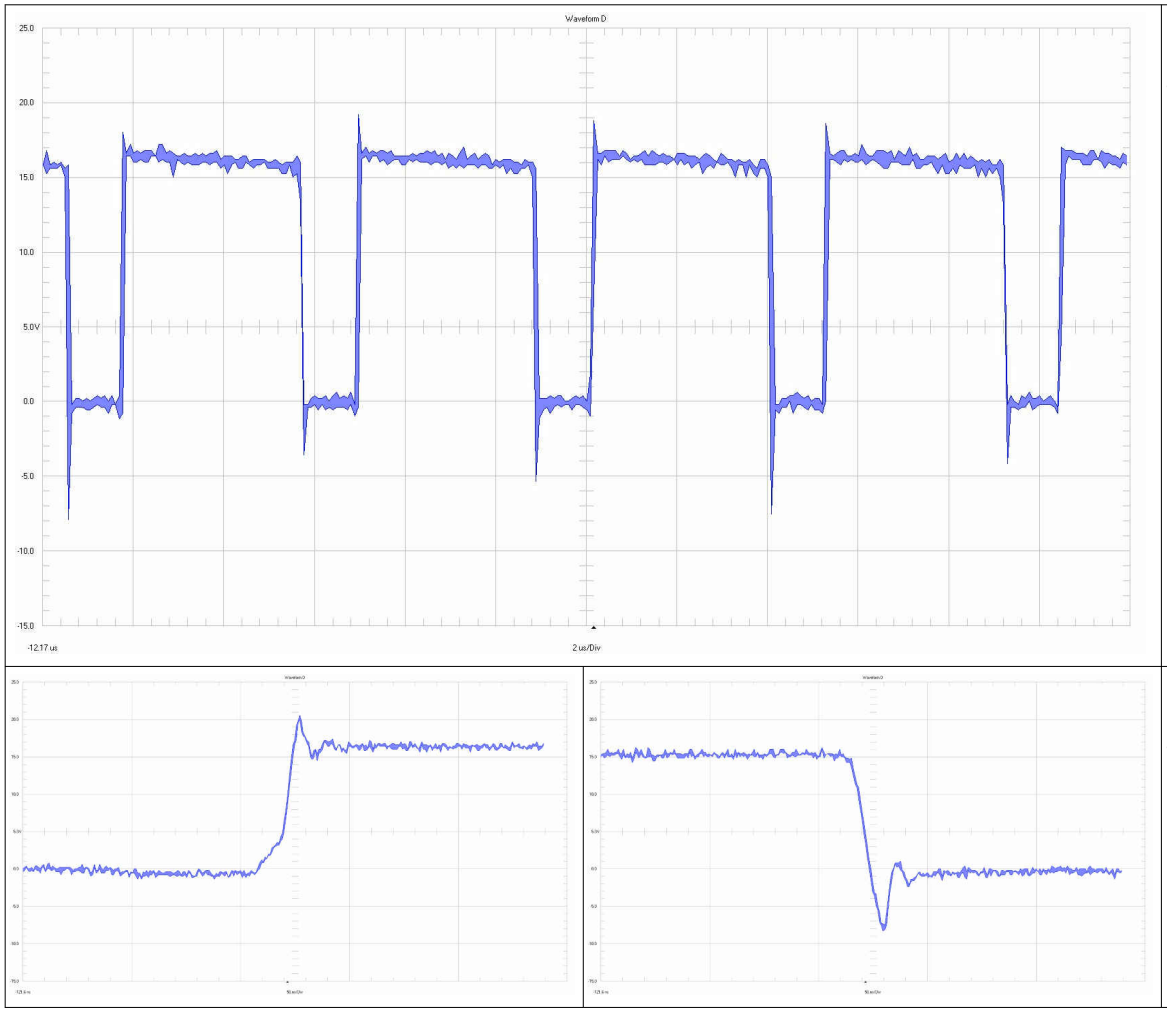


Figure 3-13. Waveform High-Side FET Gate - Source

3.1.3.2 Buck Low Side (Q3, Q4)

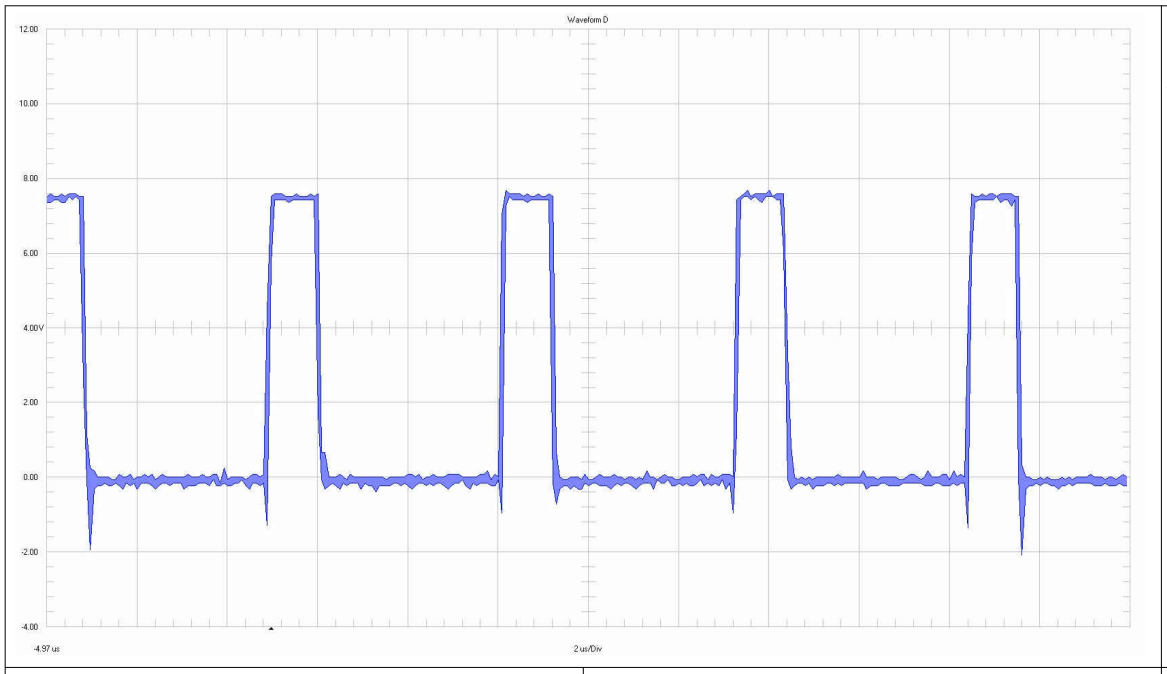
3.1.3.2.1 Drain-GND



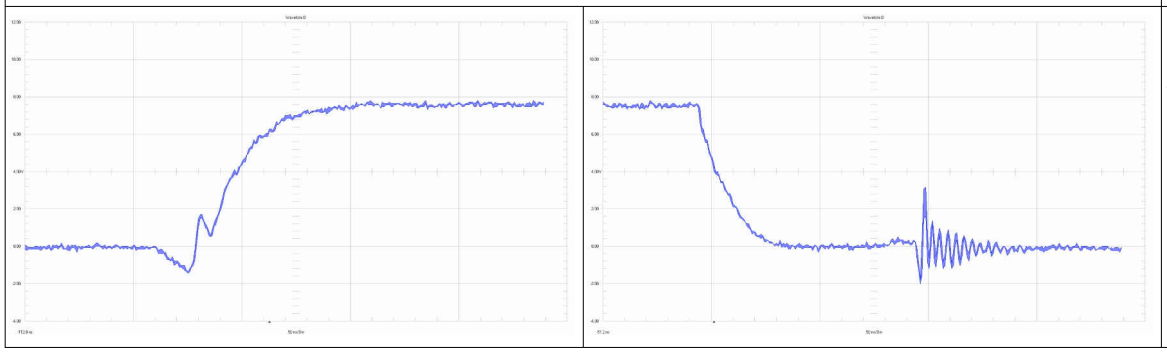
	CH1 ⇒ 5 V / div 2 µs /div full bandwidth
	CH1 ⇒ 5 V / div 50 ns / div full bandwidth

Figure 3-14. Waveform Low Side FET Drain-GND

3.1.3.2.2 Gate-GND



CH1 ⇒ 2 V / div
2 µs /div
full bandwidth

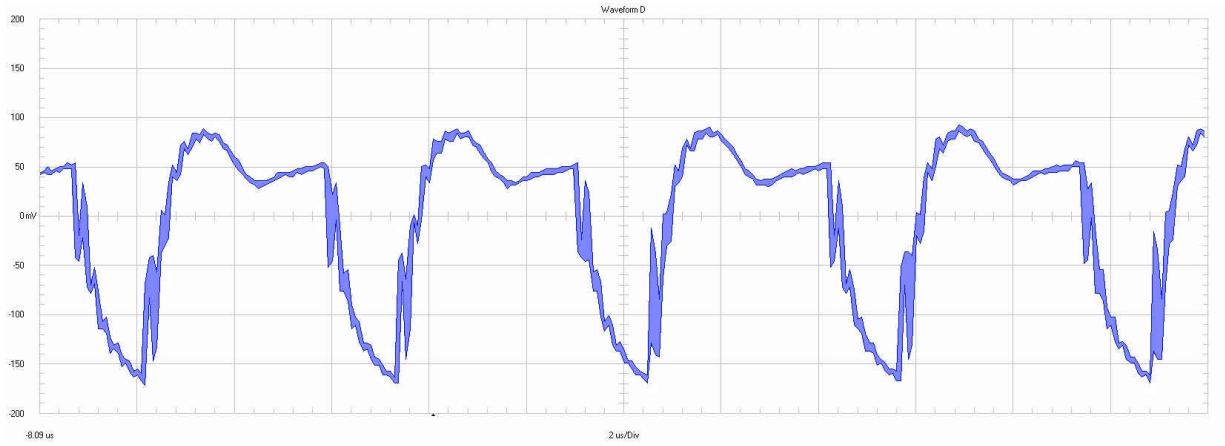


CH1 ⇒ 2 V / div
50 ns / major div
full bandwidth

Figure 3-15. Waveform Low-Side FET Gate – GND

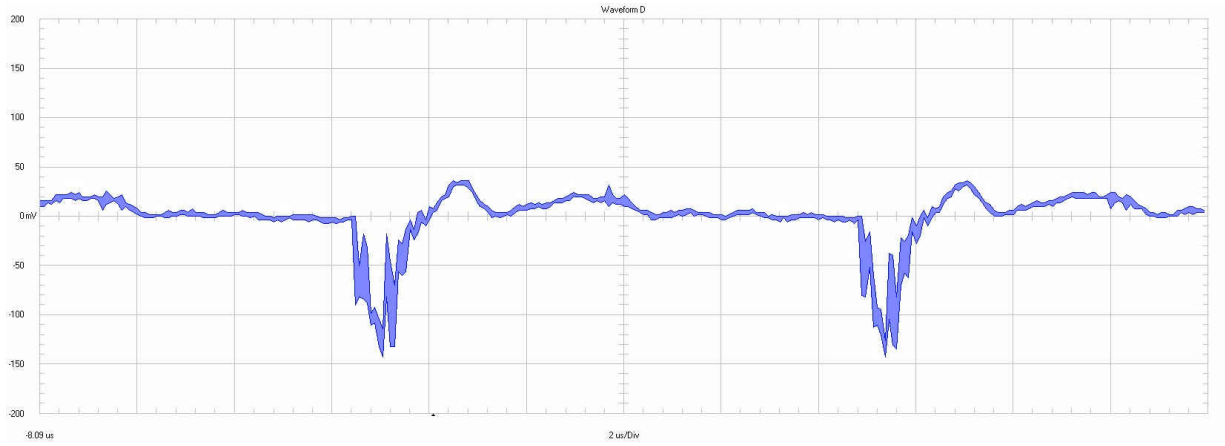
3.2 Output Voltage Ripple

Output voltage ripple is shown in the following figures.



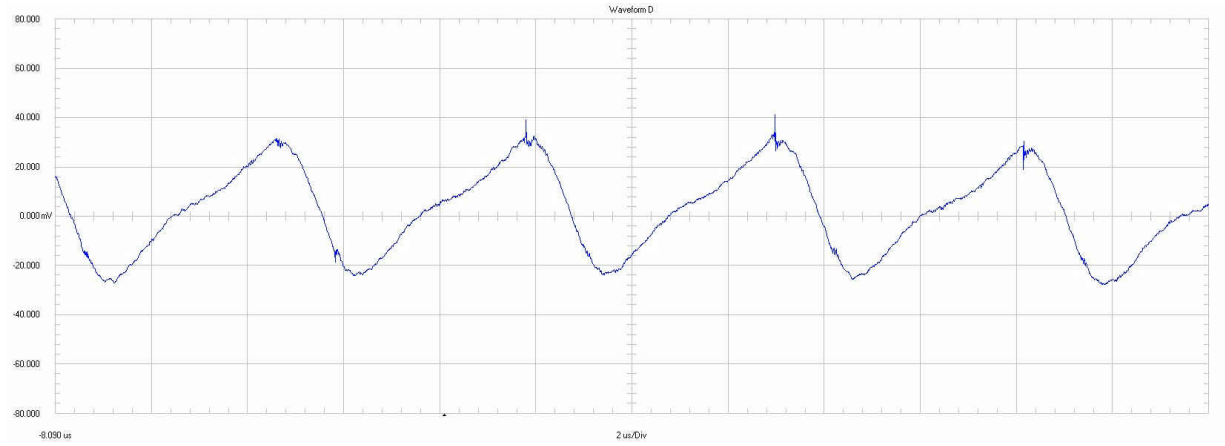
50 mV / div, 2 µs / div, 20-MHz bandwidth

Figure 3-16. Output Voltage Ripple at 9-V Input Voltage



50 mV / div, 2 µs / div, 20-MHz bandwidth

Figure 3-17. Output Voltage Ripple at 12-V Input Voltage



20 mV / div, 2 µs / div, 20-MHz bandwidth

Figure 3-18. Output Voltage Ripple at 16-V Input Voltage

3.3 Input Voltage Ripple

3.3.1 Power Stage

All three waveforms in this section were measured with following settings:

- 200 mV / div
- 2 µs / div
- 20-MHz bandwidth

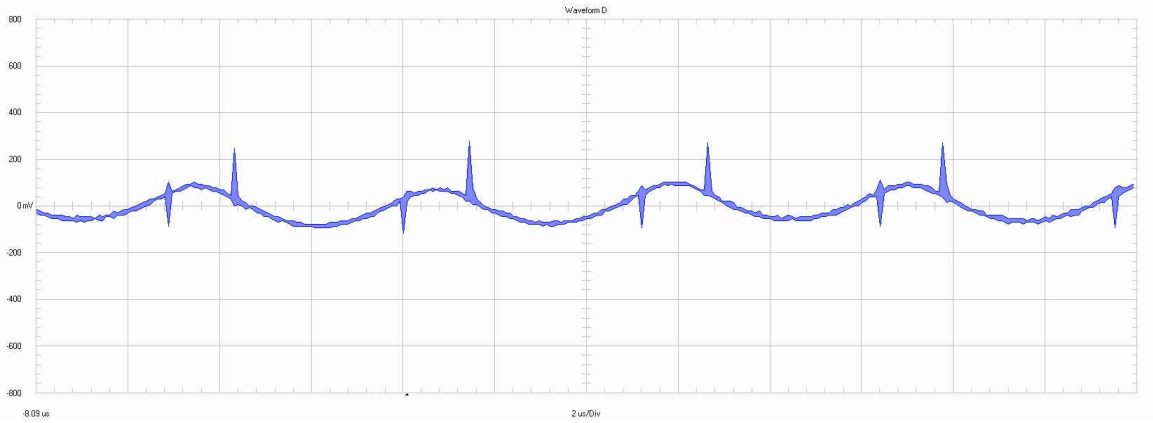


Figure 3-19. Input Voltage Ripple for 6 V_{IN}

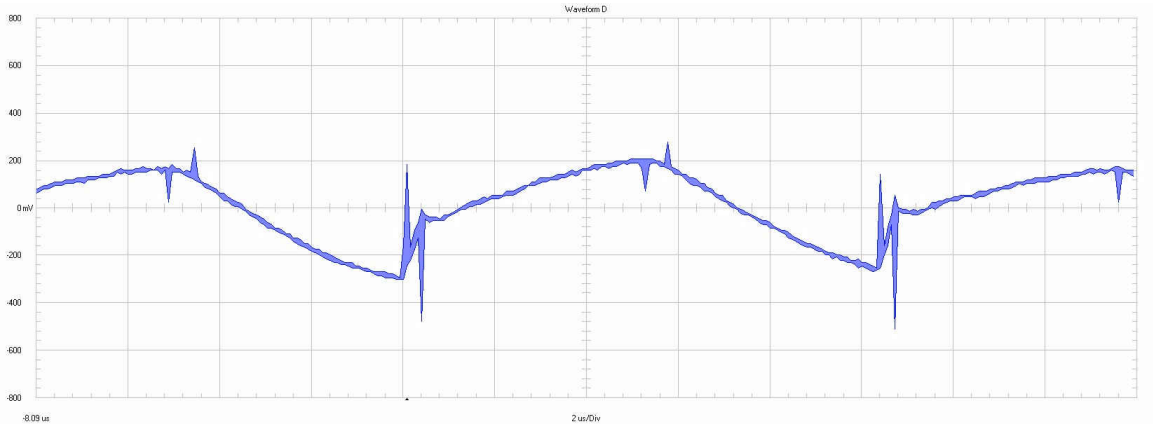


Figure 3-20. Input Voltage Ripple for 12 V_{IN}

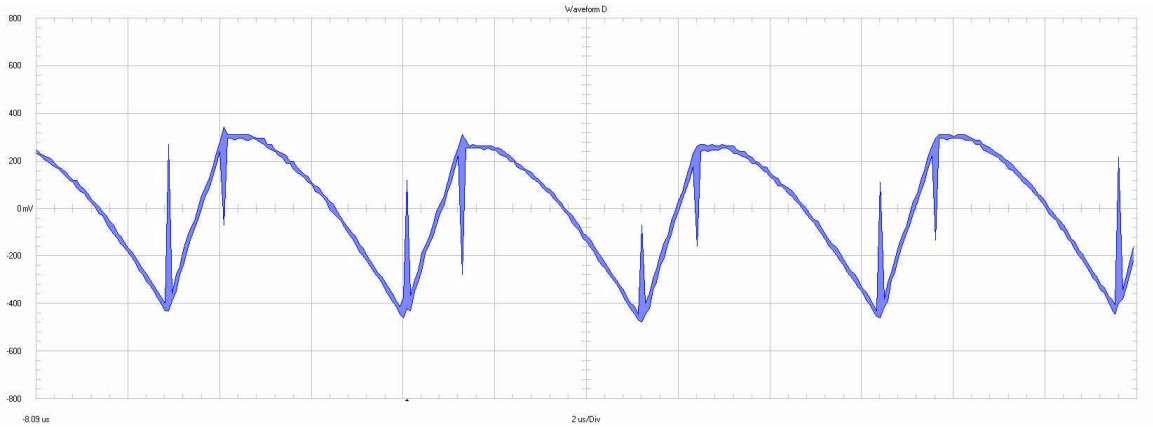


Figure 3-21. Input Voltage Ripple for 16 V_{IN}

3.3.2 Input Terminal, Differential Input Filter Acting

All three waveforms below were measured with following settings:

- 20 mV / div
- 2 µs / div
- 20-MHz bandwidth

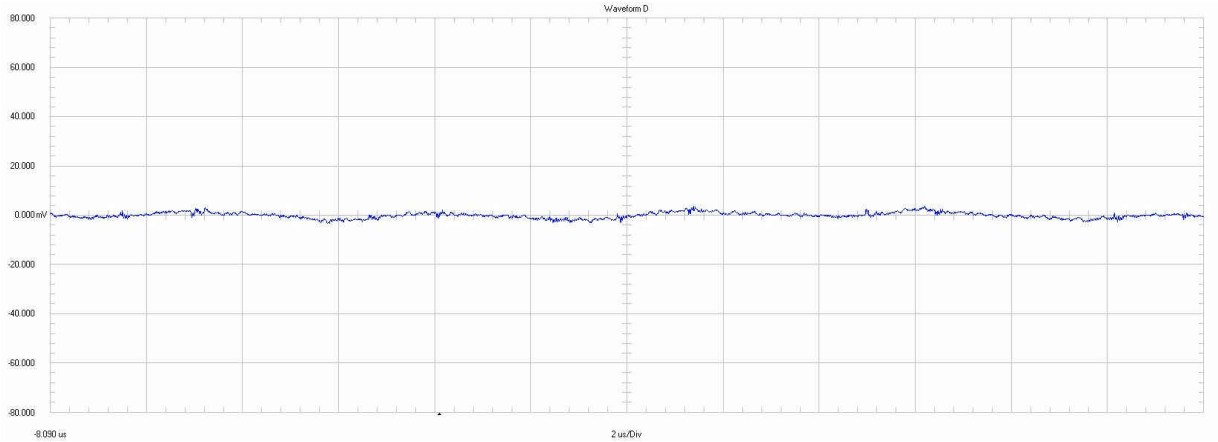


Figure 3-22. Input Voltage Ripple for 6 V_{IN}

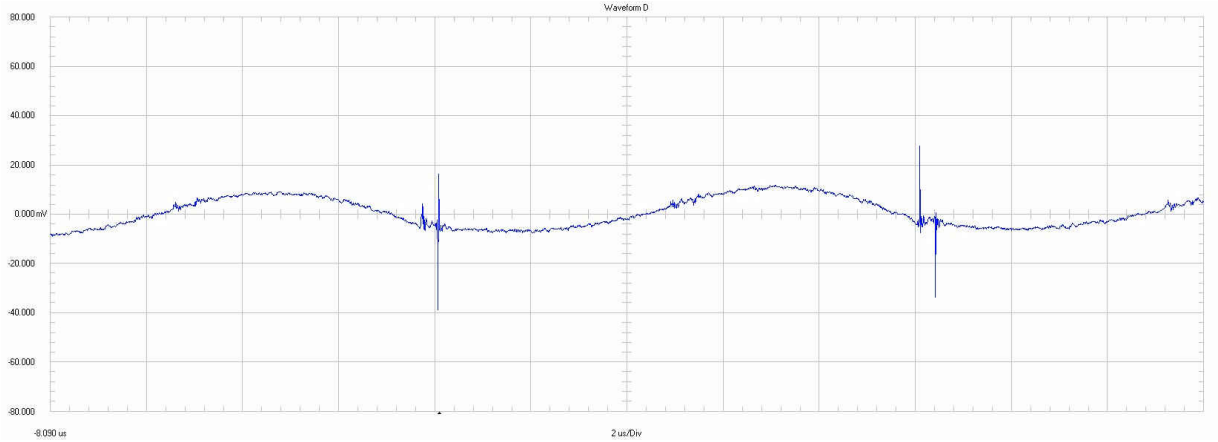


Figure 3-23. Input Voltage Ripple for 12 V_{IN}

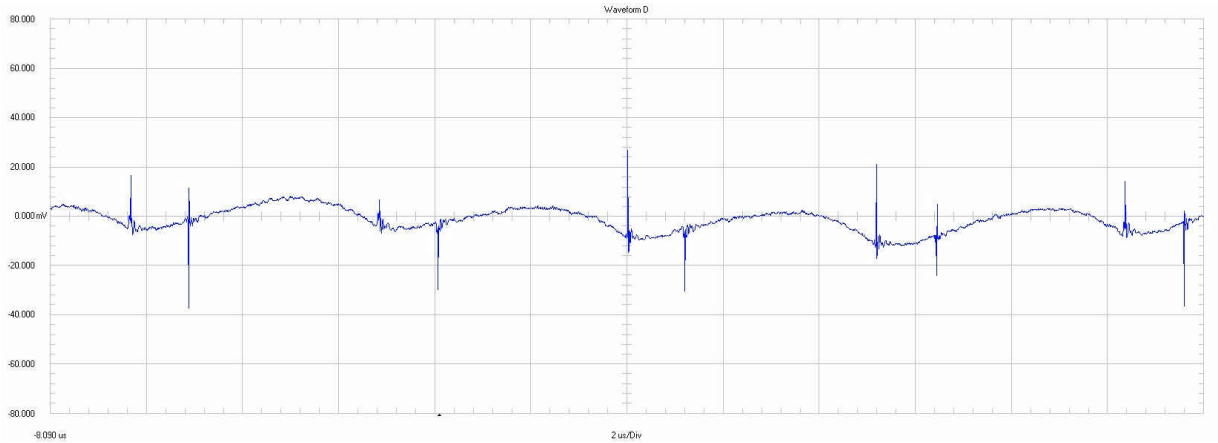
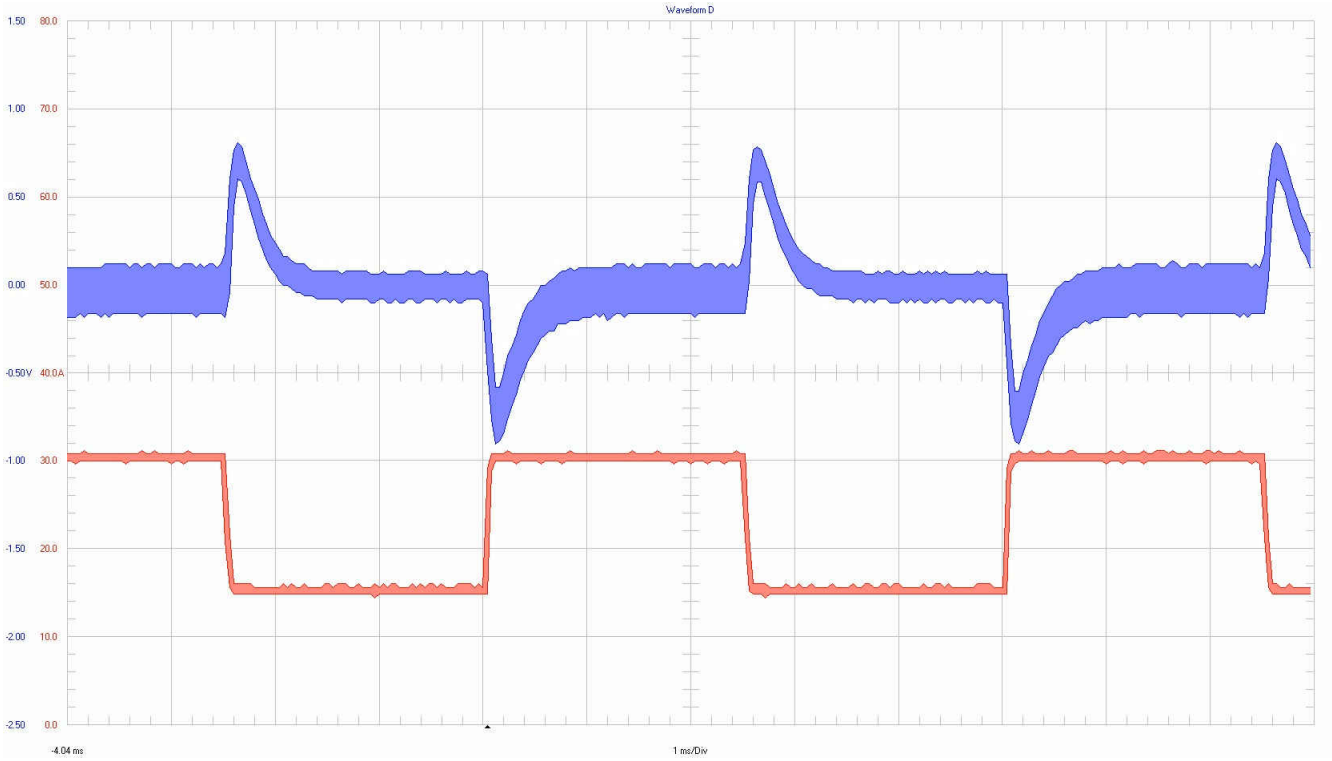


Figure 3-24. Input Voltage Ripple for 16 V_{IN}

3.4 Load Transients

The electronic load (N3305A) is switching from 15 A to 30 A with a frequency of 200 Hz.

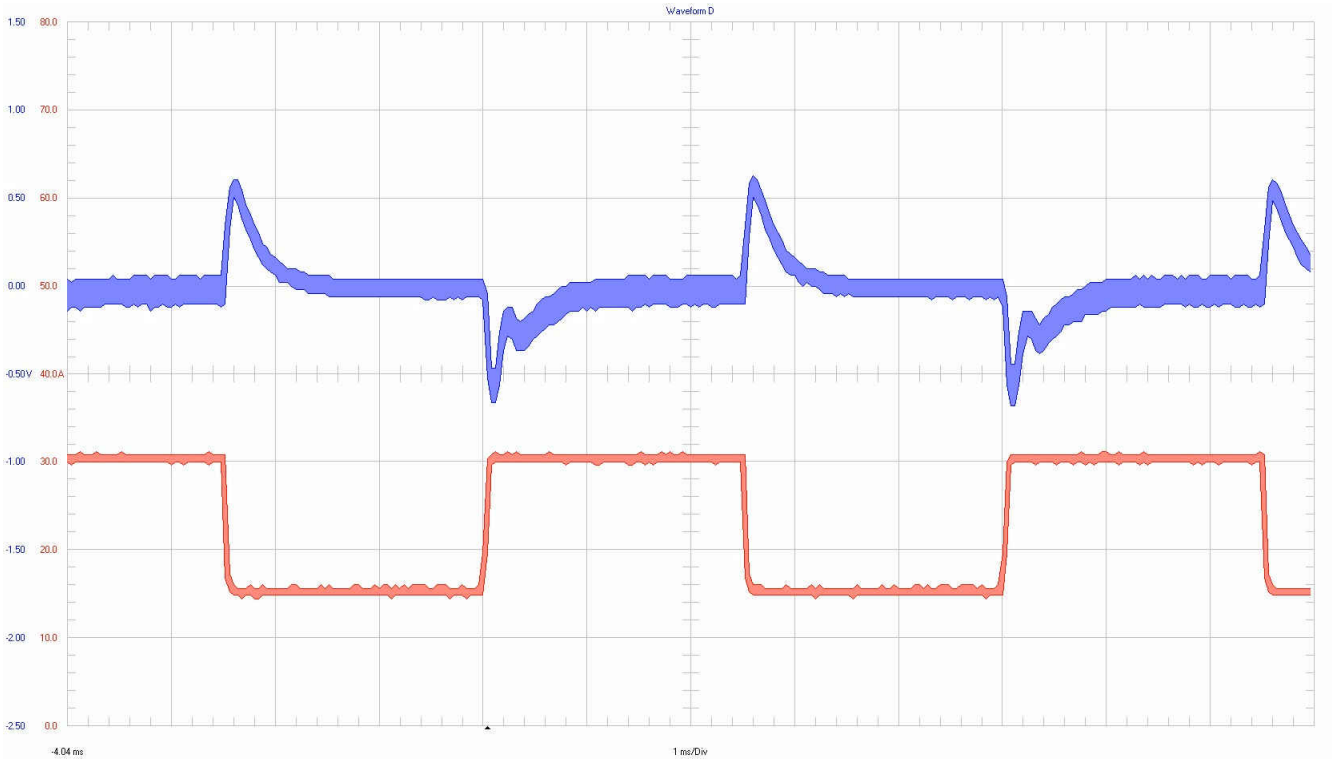
3.4.1 9-V Input Voltage



Ch1 ⇒ V_{OUT} 0.5 V / div
Ch2 ⇒ I_{OUT} 10 A / div
1 ms / div
20-MHz bandwidth

Figure 3-25. Load Transient for 9-V Input Voltage

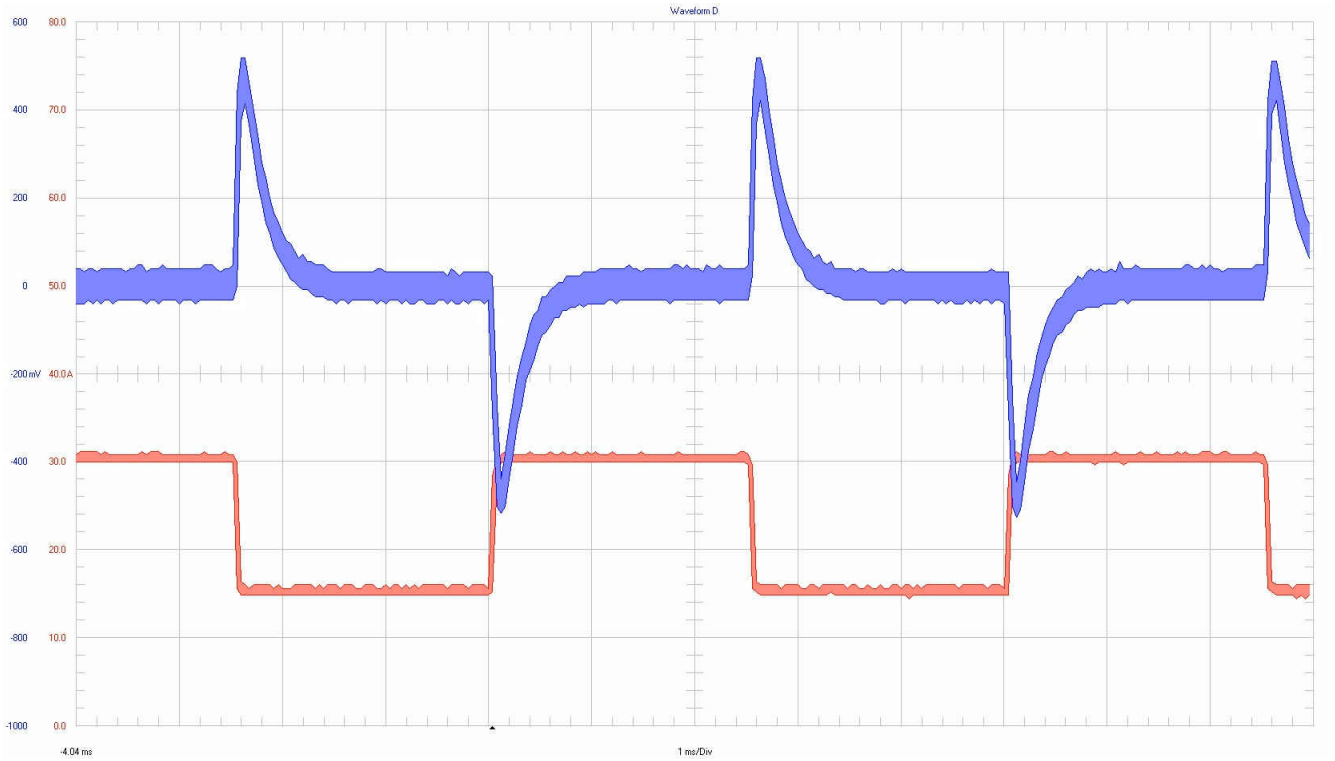
3.4.2 12-V Input Voltage



Ch1 ⇒ V_{OUT} 0.5 V / div
Ch2 ⇒ I_{OUT} 10 A / div
1 ms / div
20-MHz bandwidth

Figure 3-26. Load Transient for 12-V Input Voltage

3.4.3 16-V Input Voltage



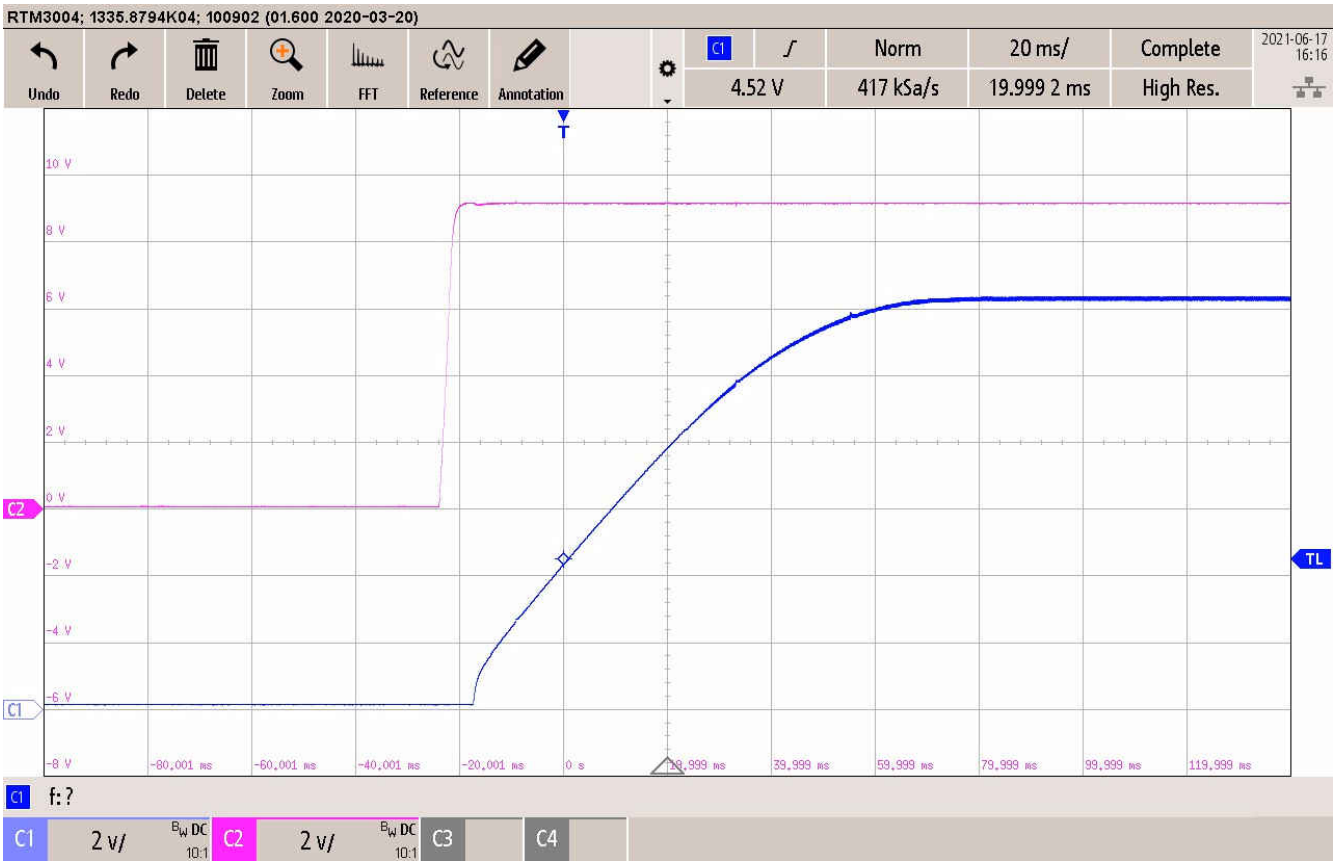
Ch1 ⇒ V_{OUT} 0.2 V / div
Ch2 ⇒ I_{OUT} 10 A / div
1 ms / div
20-MHz bandwidth

Figure 3-27. Load Transient for 16-V Input Voltage

3.5 Start-Up Sequence

Start-up behavior is shown in the following figures.

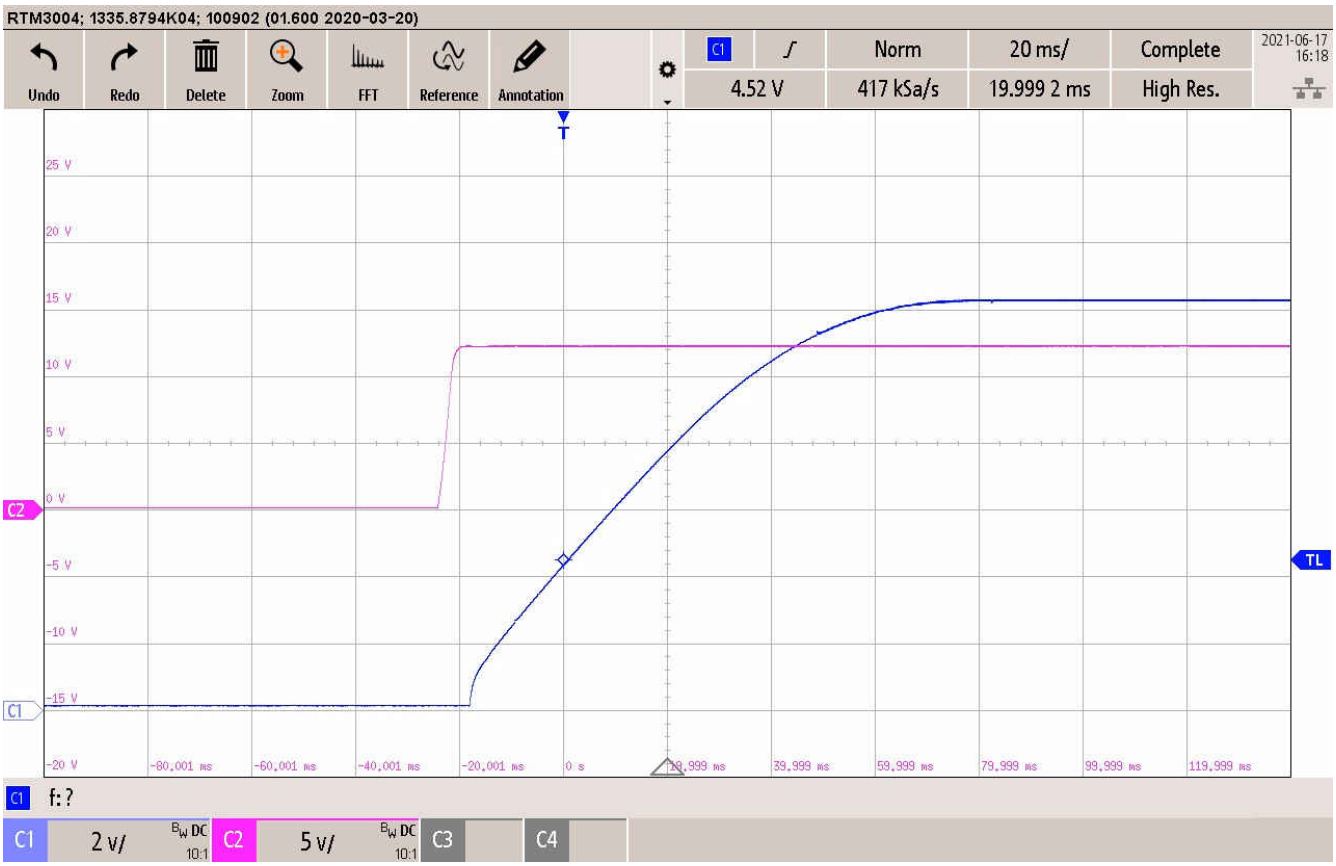
3.5.1 9-V Input Voltage



C2 ⇒ Input Voltage
C1 ⇒ Output Voltage

Figure 3-28. Start-Up 9-V Input Voltage

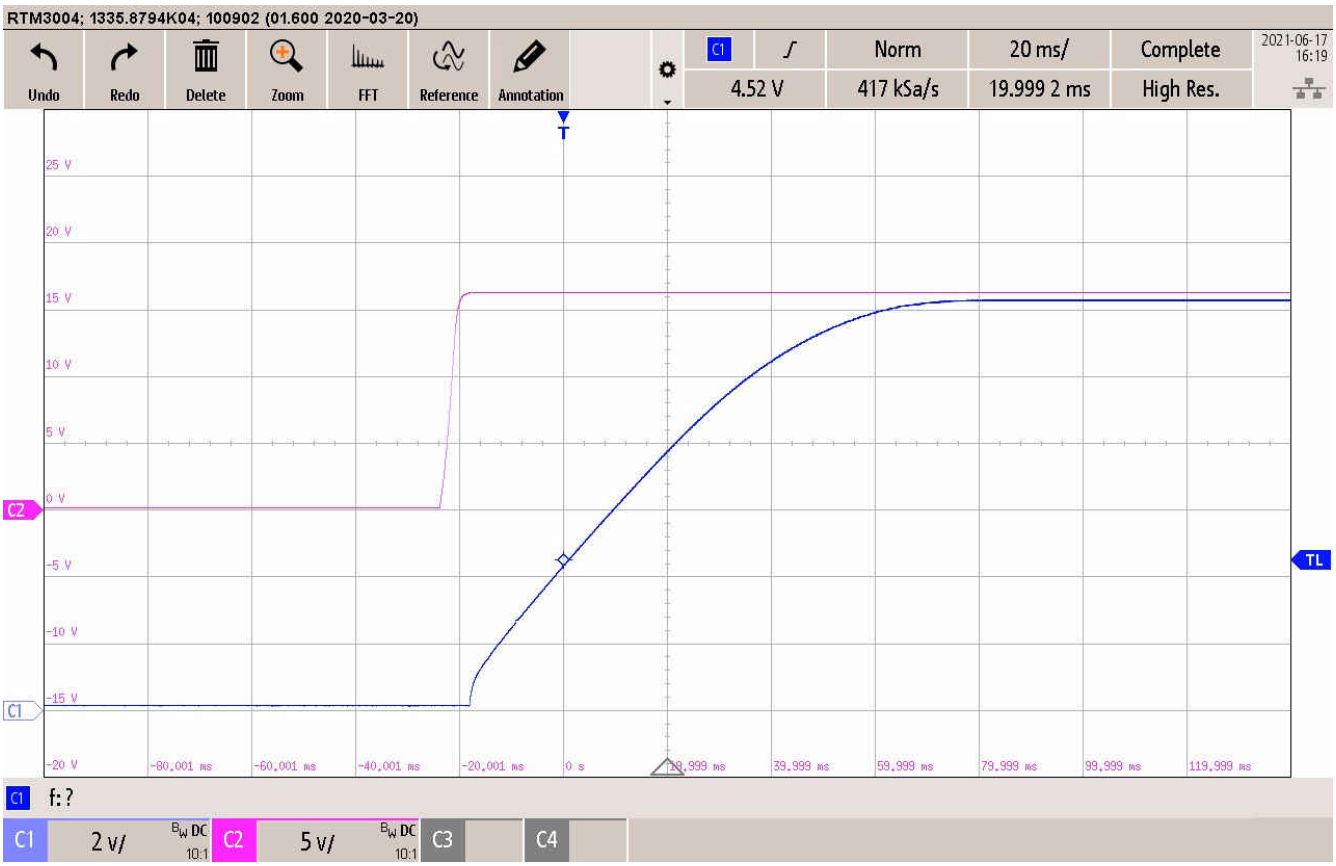
3.5.2 12-V Input Voltage



C2 ⇒ Input Voltage
C1 ⇒ Output Voltage

Figure 3-29. Start-Up 12-V Input Voltage

3.5.3 16-V Input Voltage

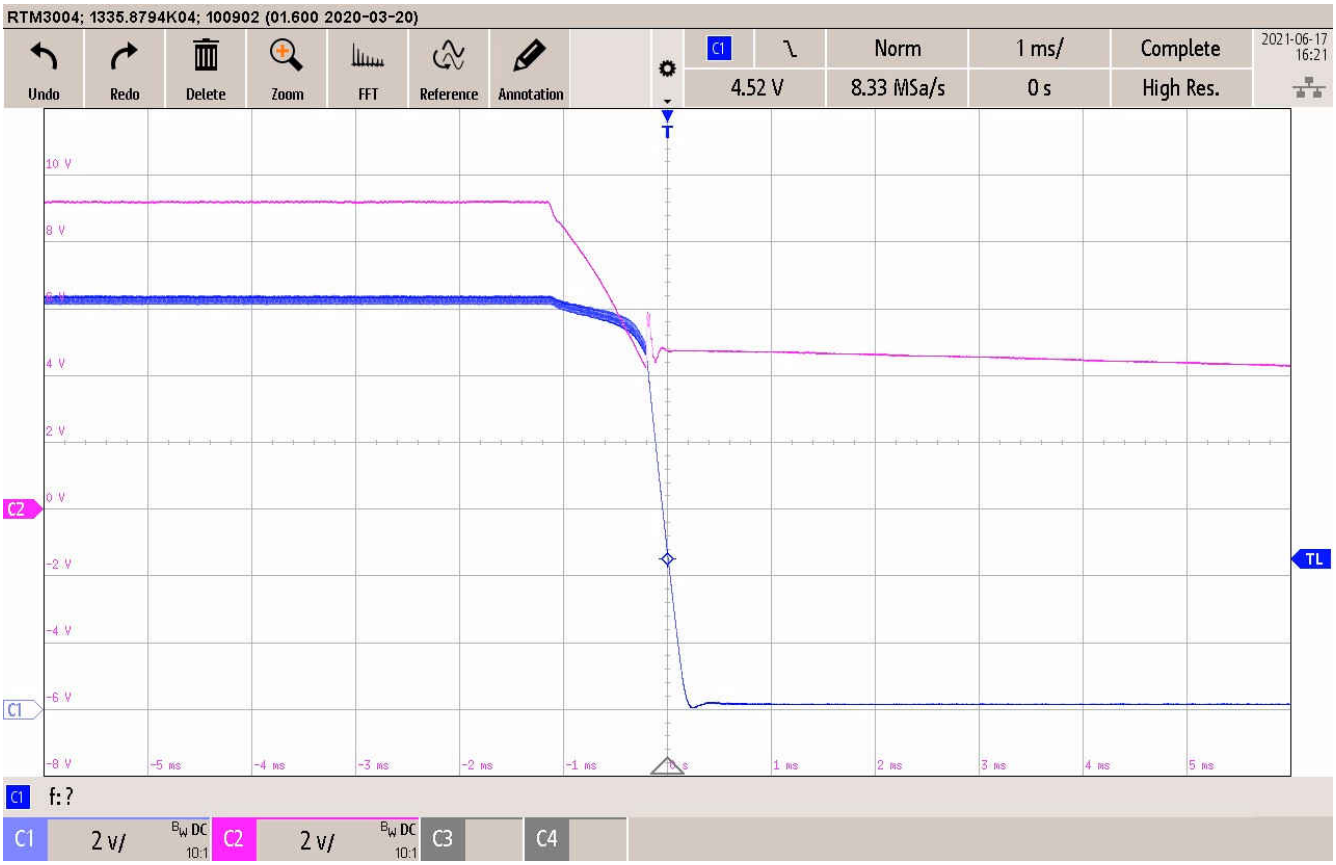


C2 ⇒ Input Voltage
C1 ⇒ Output Voltage

Figure 3-30. Start-Up 16-V Input Voltage

3.6 Shutdown Sequence

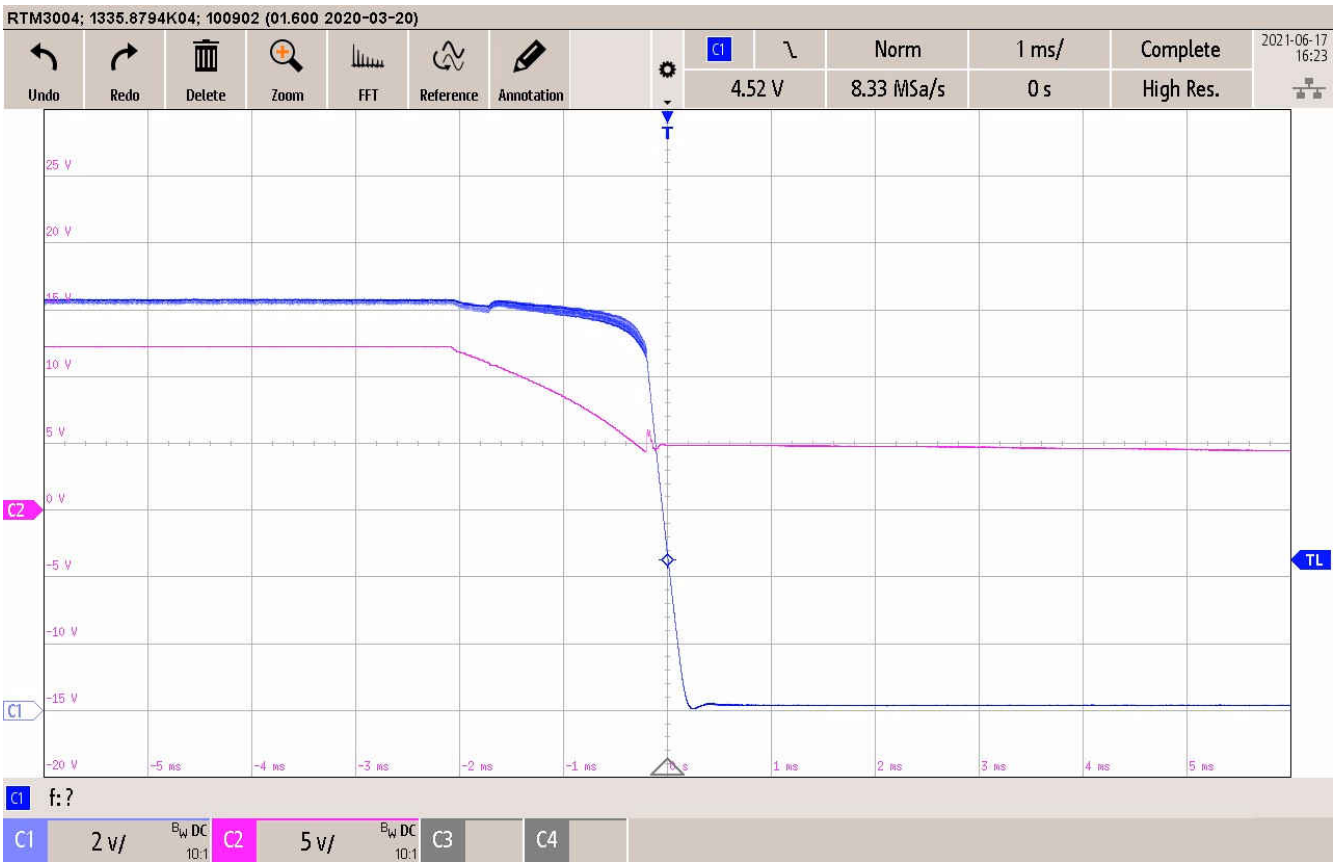
3.6.1 9-V Input Voltage



C2 ⇒ Input Voltage
C1 ⇒ Output Voltage

Figure 3-31. Shutdown 9-V Input Voltage

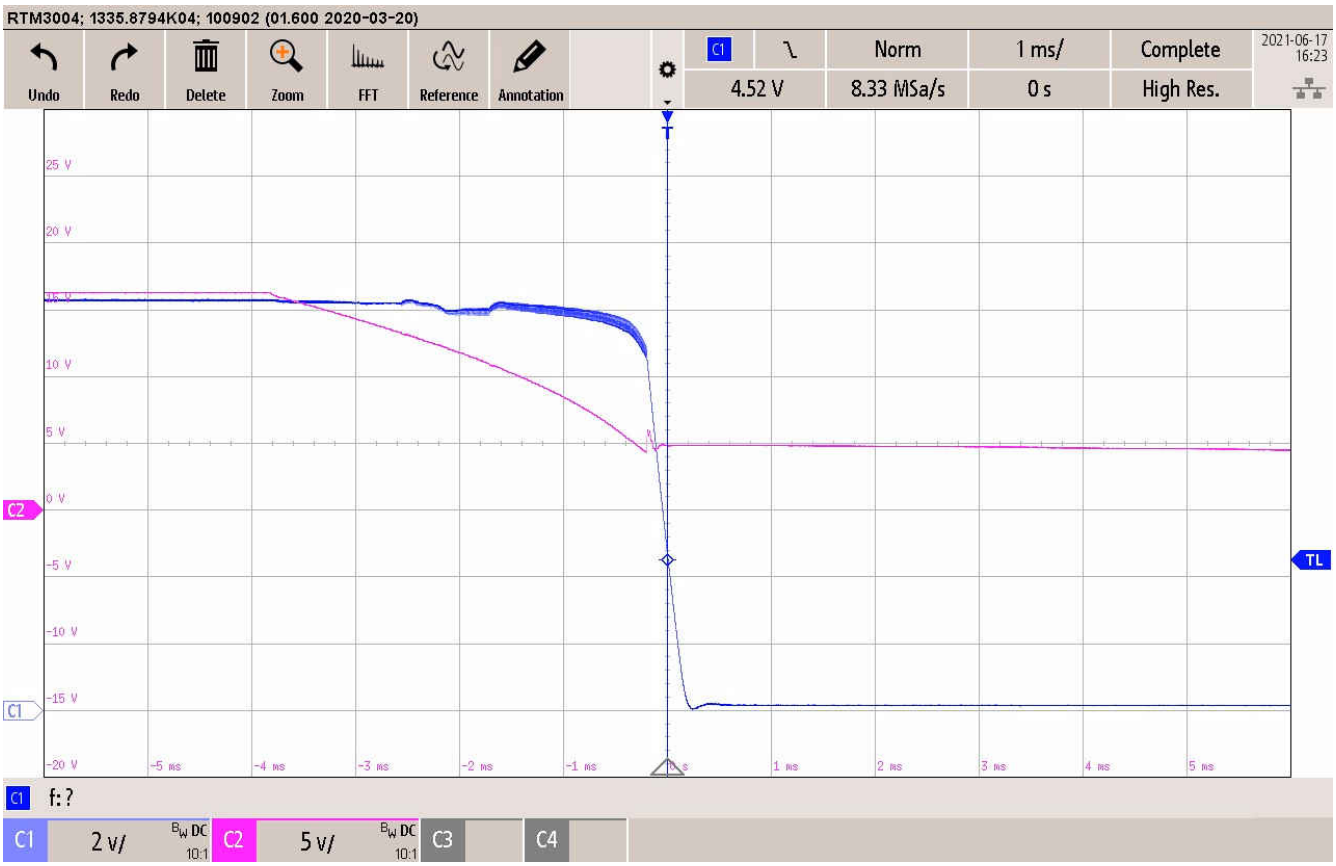
3.6.2 12-V Input Voltage



C2 ⇒ Input Voltage
C1 ⇒ Output Voltage

Figure 3-32. 12-V Input Voltage

3.6.3 16-V Input Voltage



C2 ⇒ Input Voltage
C1 ⇒ Output Voltage

Figure 3-33. Shutdown 16-V Input Voltage

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