Test Report: PMP23216

Highly-Integrated, Dual-Output Isolated Bias Supply Reference Design With Reinforced Insulation

Description

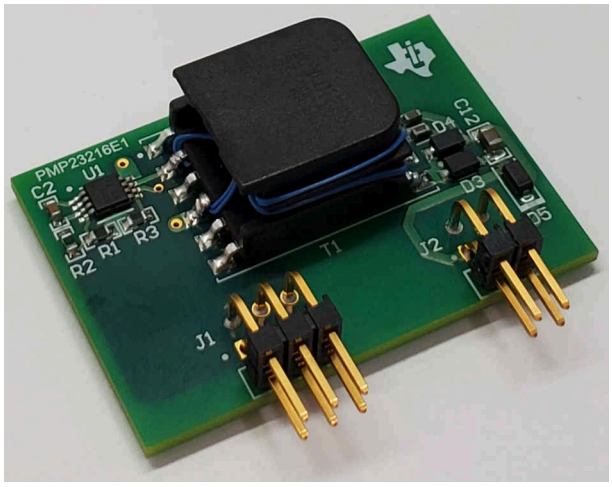
This reference design generates two isolated +12-V rails at 100 mA each from a 12-V_{DC} input voltage. The design is optimized for a small footprint by employing a primary resonant LLC topology with a single UCC25800 driver and a transformer with reinforced insulation. This design is well-suited for an application where bias power is needed across a high-voltage isolation barrier.

Features

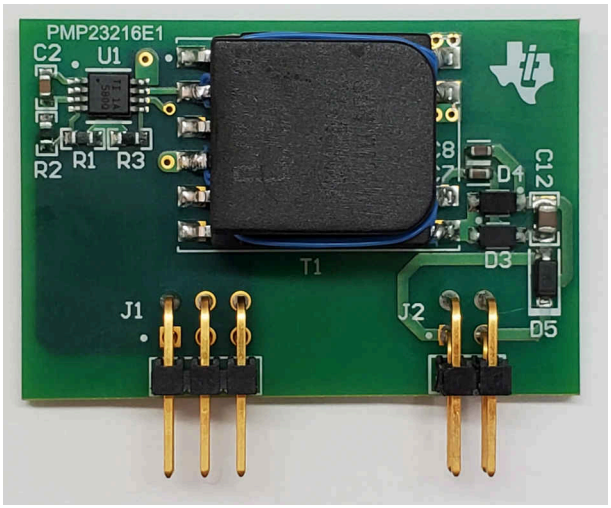
- Small size with simplified LLC design
- High efficiency: 85% at full load
- Dual output for high-side (HS) and low-side (LS) drivers
- Employs small and low-cost transformer
- Reinforced insulation for bias supplies crossing high-voltage isolation barriers

Applications

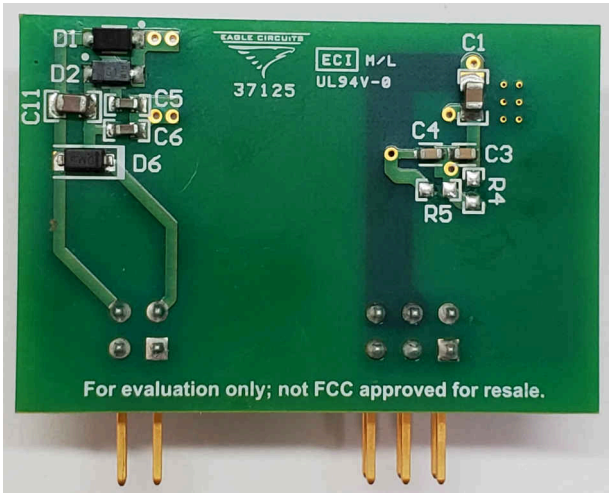
- GaN, IGBT and SiC gate transformer driver bias supply
- Automotive onboard charger (OBC)
- Automotive DC/DC converter
- Automotive traction inverter and motor control



Top of Board (Angled)



Top of Board



Bottom of Board

1 Design Information

1.1 Voltage and Current Specifications

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
V_{IN}	12 V
V_{OUT} HS, V_{OUT} LS	12 V, ±10%
I_{OUT} LS, I_{OUT} HS	100 mA

1.2 Dimensions

The dimensions of the board are 32 mm × 27 mm × 10 mm.

1.3 System Schematic

The following image illustrates the simplified schematic.

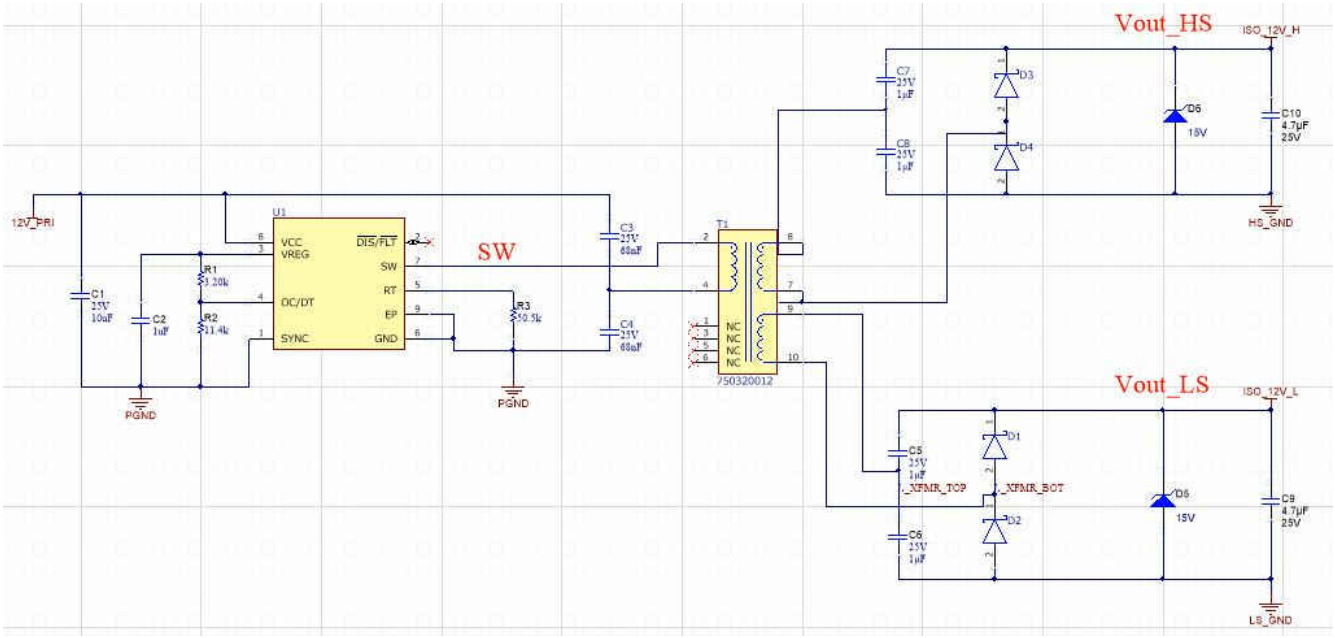


Figure 1-1. PMP23216 Schematic

2 Testing and Results

2.1 Output Voltage Regulation

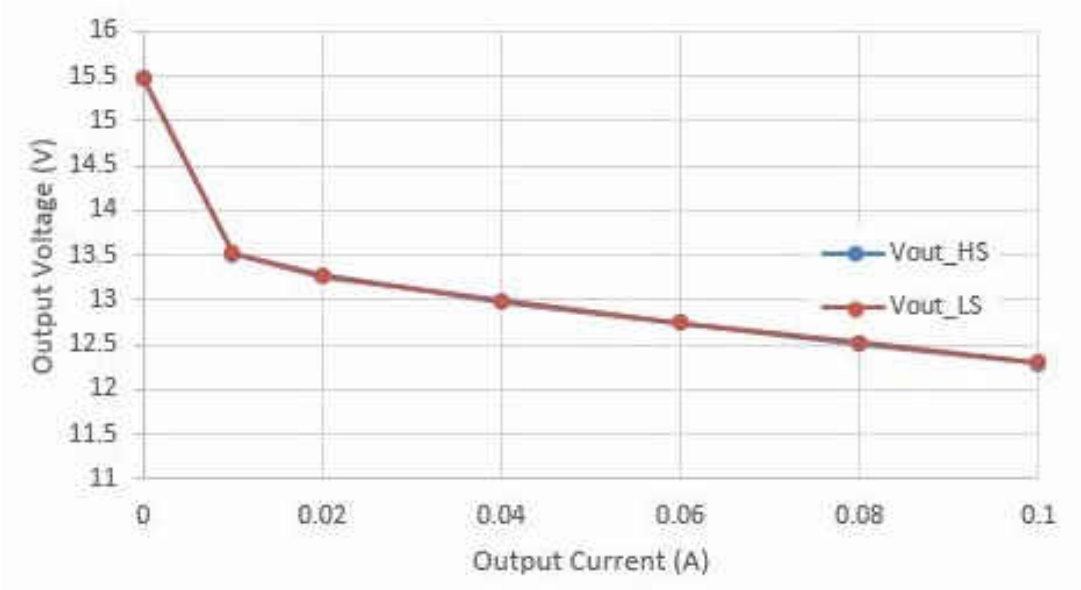


Figure 2-1. Open Loop Output Voltage vs Output Current

2.2 Efficiency Graphs

Efficiency and power loss are shown in the following figures.

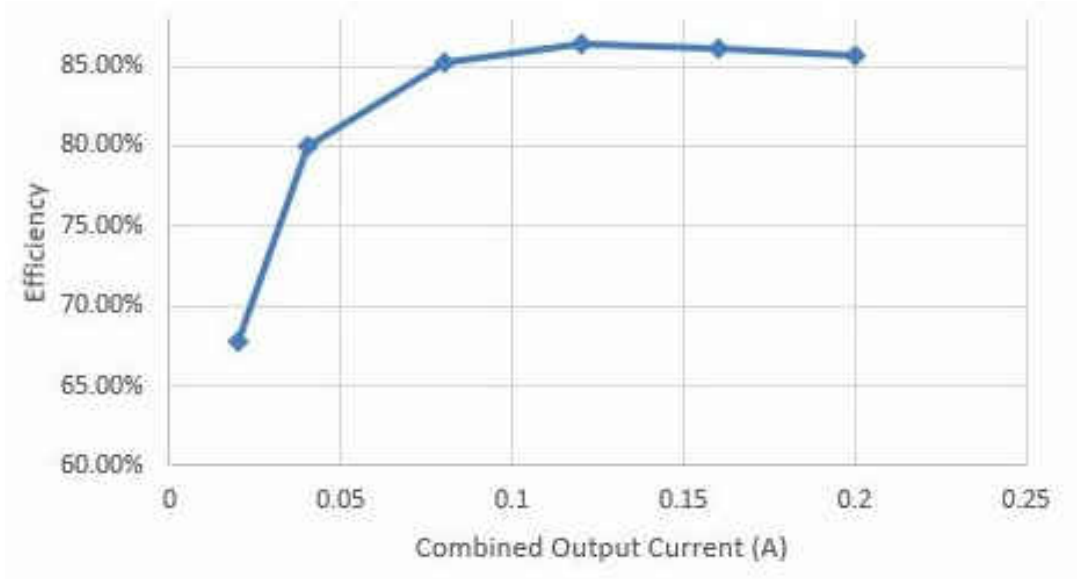


Figure 2-2. Efficiency Graph – HS and LS Rail Current Split Evenly

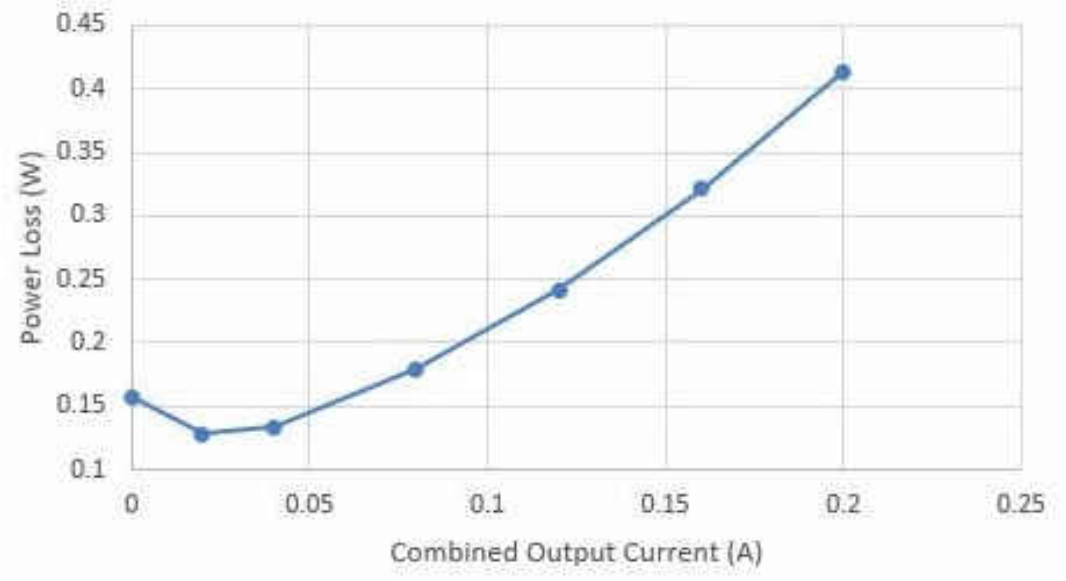


Figure 2-3. Power Loss Graph – HS and LS Rail Current Split Evenly

2.3 Efficiency Data

Efficiency data is shown in the following table.

V_{IN} (V)	I_{IN} (A)	V_{OUT_HS} (V)	I_{OUT_HS} (A)	V_{OUT_LS} (V)	I_{OUT_LS} (A)	P_{IN} (W)	P_{OUT} (W)	P_{loss} (W)	Efficiency
12.09	0.013	15.48	0	15.48	0	0.15717	0	0.15717	0.00%
12.08	0.033	13.51	0.010	13.52	0.010	0.39864	0.2703	0.12834	67.81%
12.08	0.055	13.28	0.020	13.27	0.020	0.6644	0.531	0.1334	79.92%
12.06	0.101	12.98	0.040	12.99	0.040	1.21806	1.0388	0.17926	85.28%
12.05	0.147	12.74	0.060	12.75	0.060	1.77135	1.5294	0.24195	86.34%
12.04	0.193	12.51	0.080	12.52	0.080	2.32372	2.0024	0.32132	86.17%
12.02	0.239	12.29	0.100	12.3	0.100	2.87278	2.459	0.41378	85.60%

2.4 Thermal Images

All images were captured with the DUT at 25ºC ambient, after a 30-minute warm up. The output was loaded with 100 mA on both HS and LS rails.

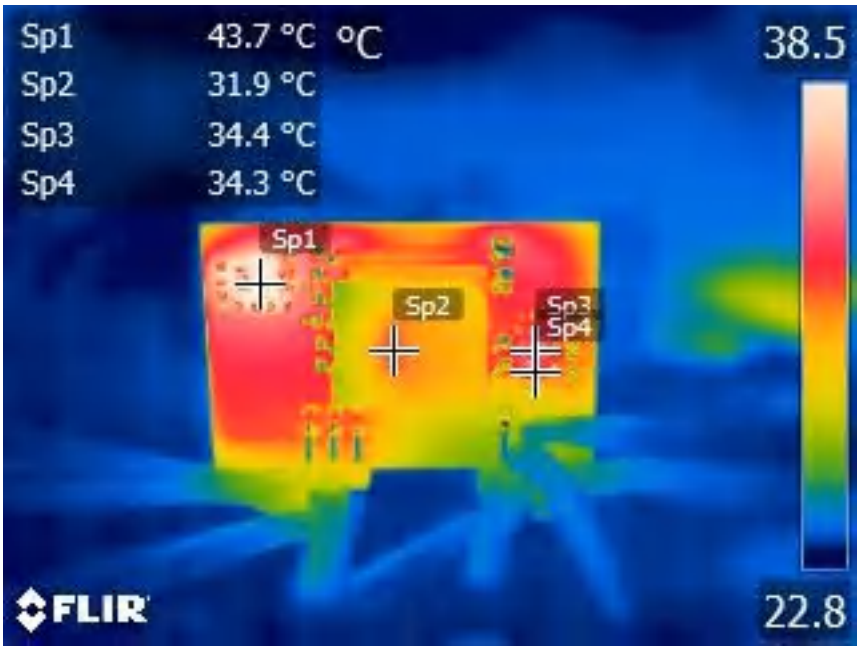


Figure 2-4. Front

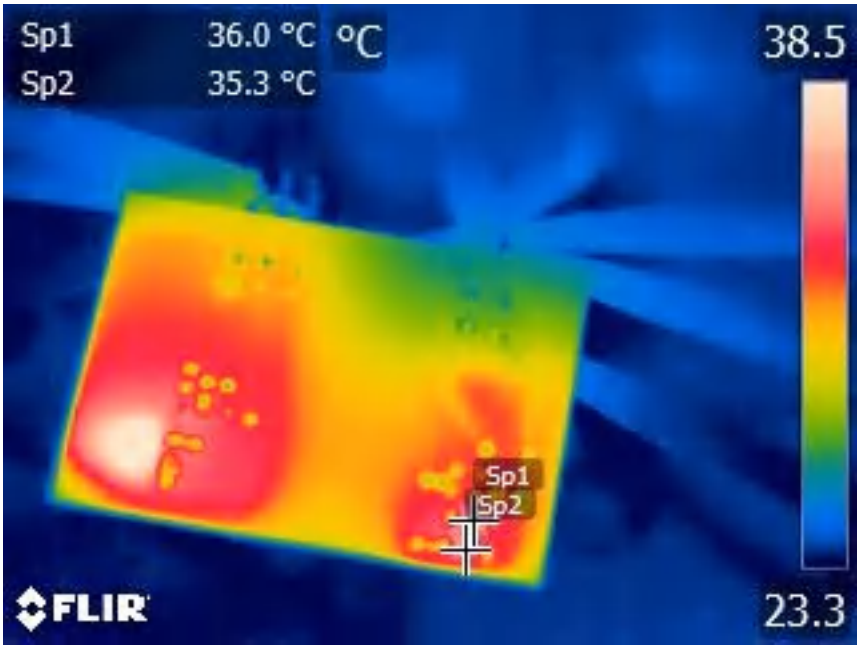


Figure 2-5. Back

3 Waveforms

3.1 Switching

Switching behavior is shown in the following figure.

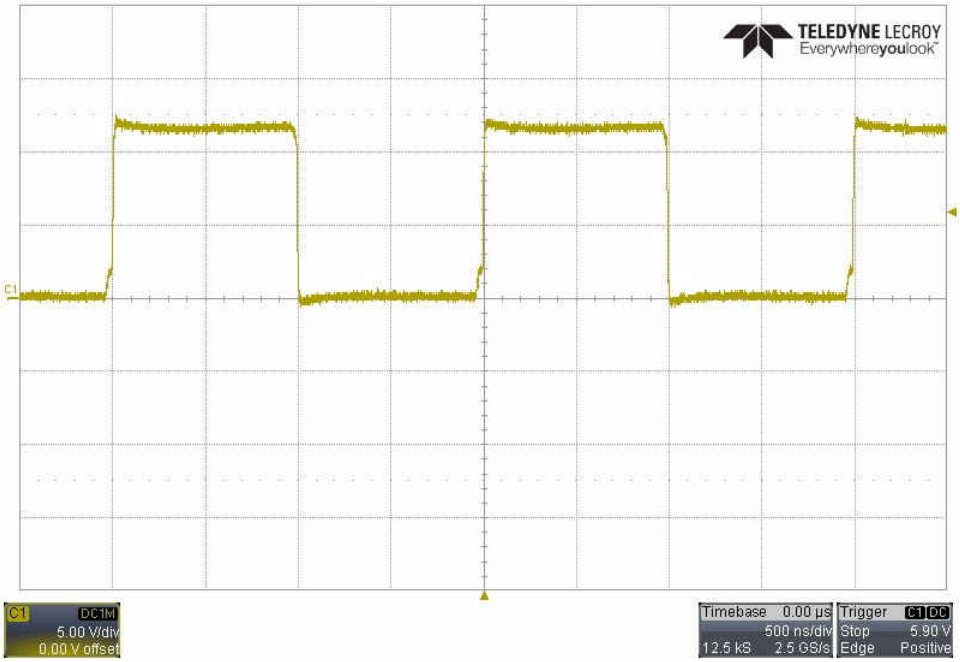


Figure 3-1. Switch Node: 12-V Input, 100 mA on Both HS and LS Rails

3.2 Output Voltage Ripple

Output voltage ripple waveforms are shown in the following figures.

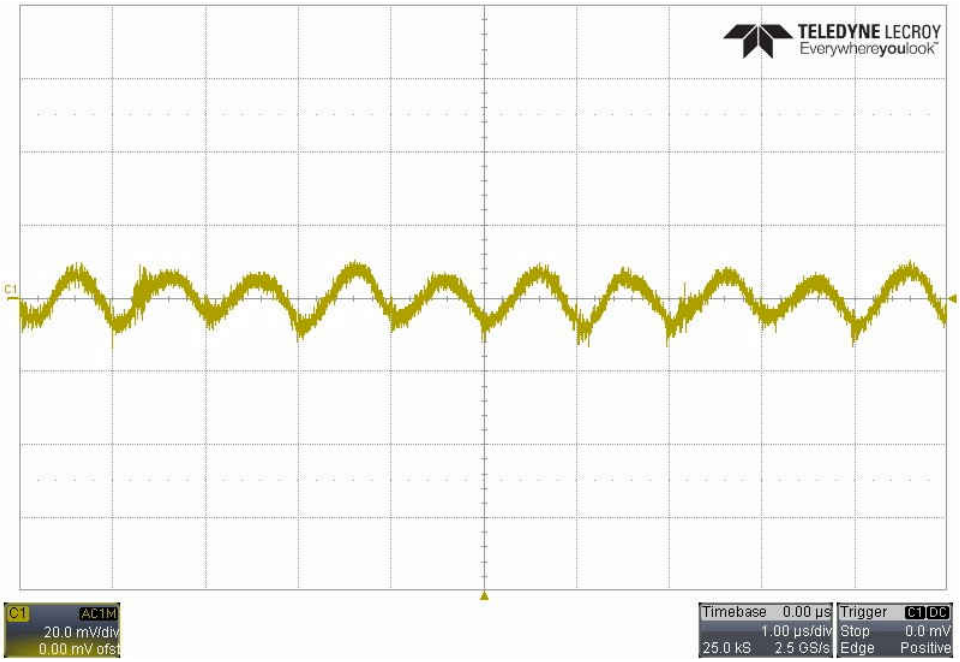


Figure 3-2. Output Voltage Ripple of HS Rail

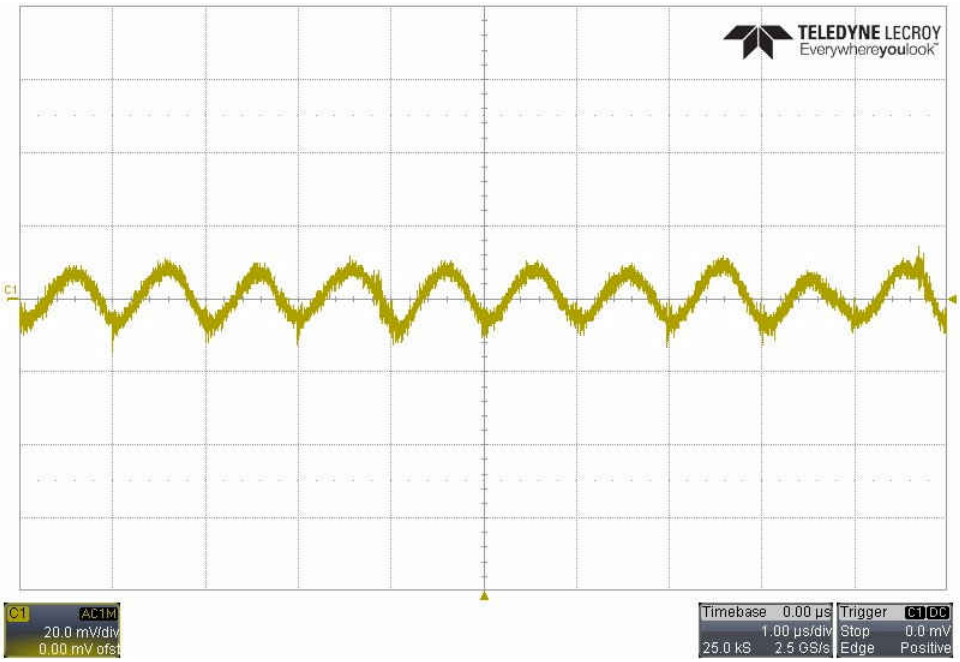


Figure 3-3. Output Voltage Ripple of LS Rail

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