Test Report: PMP31182

Isolated Bias Power Supply Reference Designs Using Four Different Topologies

Description

This reference design features four isolated bias power supply designs using different topologies such as PSR flyback, push-pull, LLC resonant, and isolated DCDC module. These topologies provide specific benefits but at the same time the topologies come with trade-offs. An ample comparison of these topologies is done using four hardware designs while keeping the electrical parameters as similar as possible. The input and output voltage of these designs are 15V and the maximum load current is 100mA.

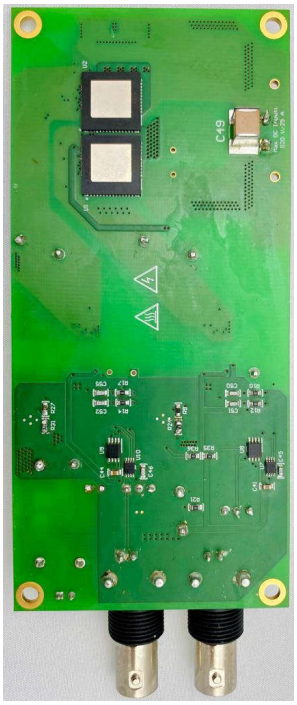
Features

- Isolated bias power supply design using different topologies like PSR-flyback, push-pull, isolated DCDC module, and LLC resonant
- An ample comparison of different isolated bias power supply topologies
- Comparative analysis using similar electrical parameters in circuit designs for different topologies

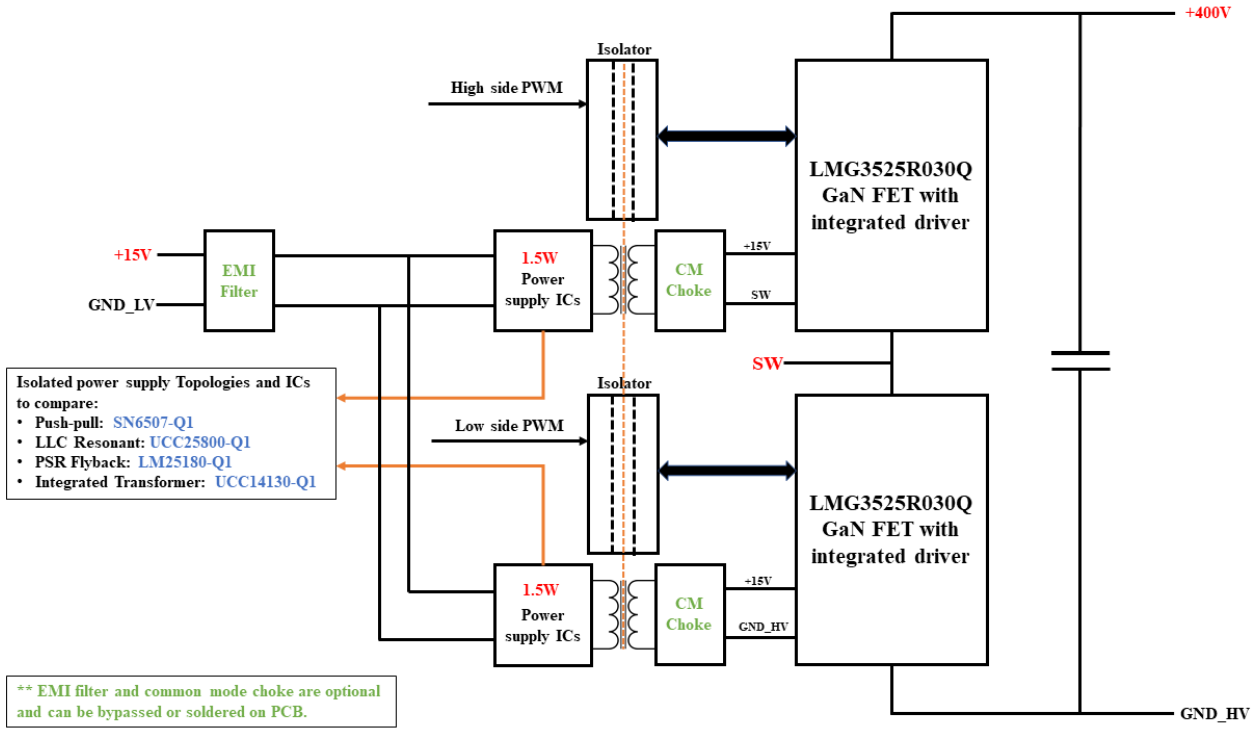
Applications

- Auxiliary-power supplies
- Unidirectional 400V and 800V to LV
- Bidirectional 400V and 800V to LV
- Traction inverter-high voltage
- Traction inverter-low voltage
- 1-phase AC-digital control
- 3-phase AC-analog control
- 1-phase AC-analog control
- 3-phase AC-digital control
- OBC-wireless charging

Top of Board



Bottom of Board



Project Block Diagram

1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

Parameter	Specifications
V_{IN}	15V
V_{OUT}	15V
I_{OUT}	100mA
F_{SW}	20kHz–350kHz for LM25180-Q1 500kHz for SN6507-Q1 and UCC25800-Q1 11–15MHz for UCC14130-Q1

1.2 Considerations

- To do comparative analysis, a device designed for each of the following topologies was chosen:
  - PSR-flyback: LM25180-Q1
  - Push-pull: SN6507-Q1
  - Isolated DCDC module: UCC14130-Q1
  - LLC resonant: UCC25800-Q1
- All the electrical parameters kept as similar as possible.
- As shown in the project bock diagram, these isolated bias power supply devices are used in a distributed kind of architecture. Each device is used to supply one GaN switch with integrated driver. In each design, two isolated bias power supply circuits are used for a GaN half bridge.
- Measurements, including efficiency, were taken at room temperature.
- Efficiency reading was taken running one isolated bias power supply circuit only, while the other power supply circuit was disabled.
- Efficiency measurement was done without EMI filter circuit.

1.3 Dimensions

Table 1-2. Board Dimensions

Board	Dimensions(1)
PMP31182-LM25180 PCB	125.02mm × 57.56mm
PMP31182-SN6507 PCB	125.02mm × 57.56mm
PMP31182-UCC14130 PCB	125.02mm × 60.94mm
PMP31182-UCC25800 PCB	125.02mm × 57.56mm

(1) The length of the portion of the BNC connector outside of the PCB was not included in these dimensions.

2 Testing and Results

2.1 Efficiency Graphs

2.1.1 LM25180-Q1 Efficiency Graph

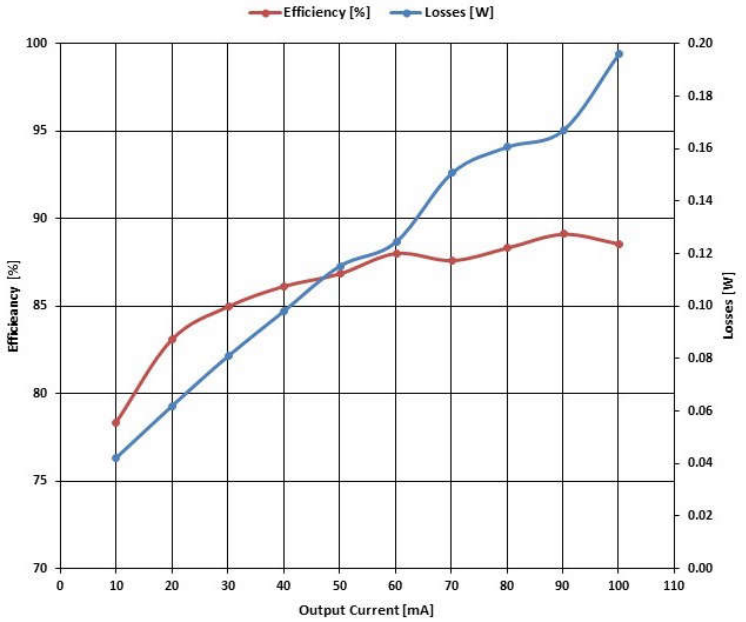


Figure 2-1. LM25180-Q1 Efficiency at 15 V_{IN}

2.1.2 SN6507-Q1 Efficiency Graph

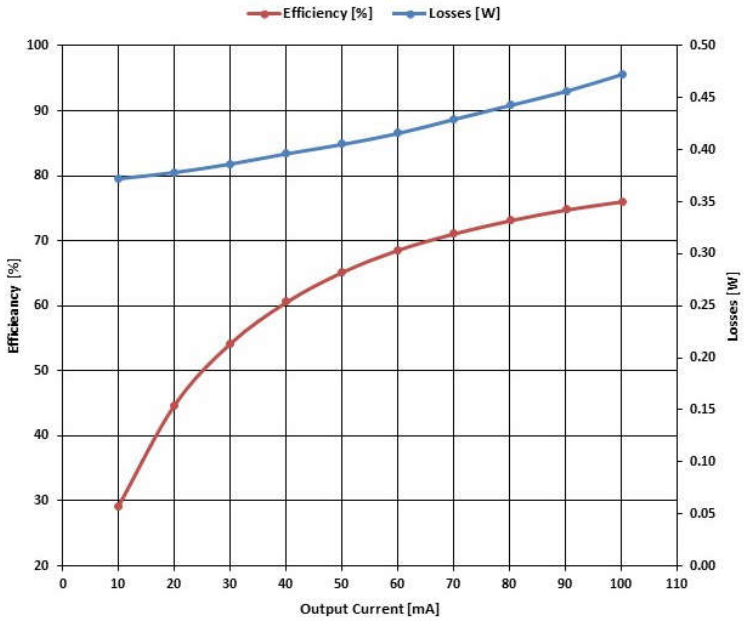


Figure 2-2. SN6507-Q1 Efficiency at 15 V_{IN}

Note

The efficiency graph shows only up to 100mA load current. The SN6507-Q1 device has 0.5A rated power switches. Maximum efficiency of this device can be achieved in the range of 250mA–300mA load current.

2.1.3 UCC14130-Q1 Efficiency Graph

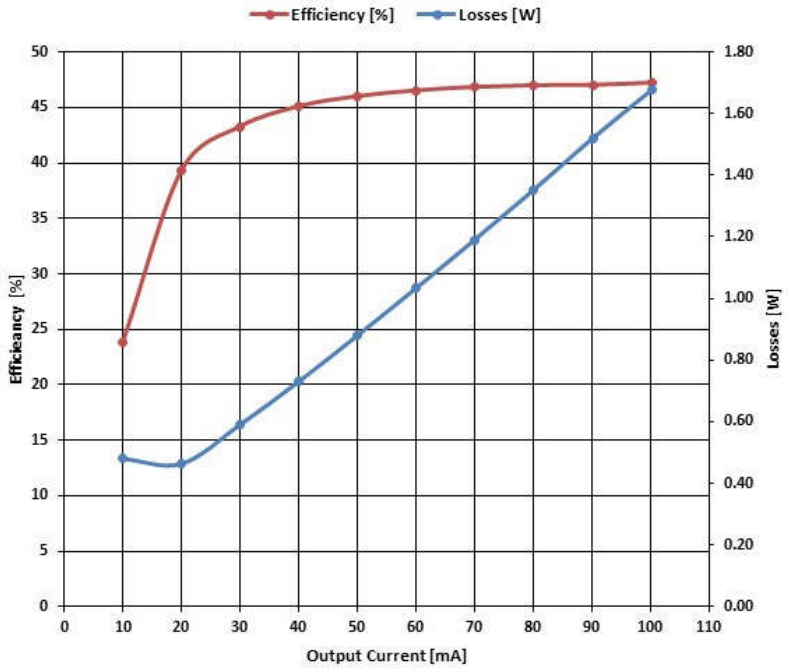


Figure 2-3. UCC14130-Q1 Efficiency at 15 V_{IN}

2.1.4 UCC25800-Q1 Efficiency Graph

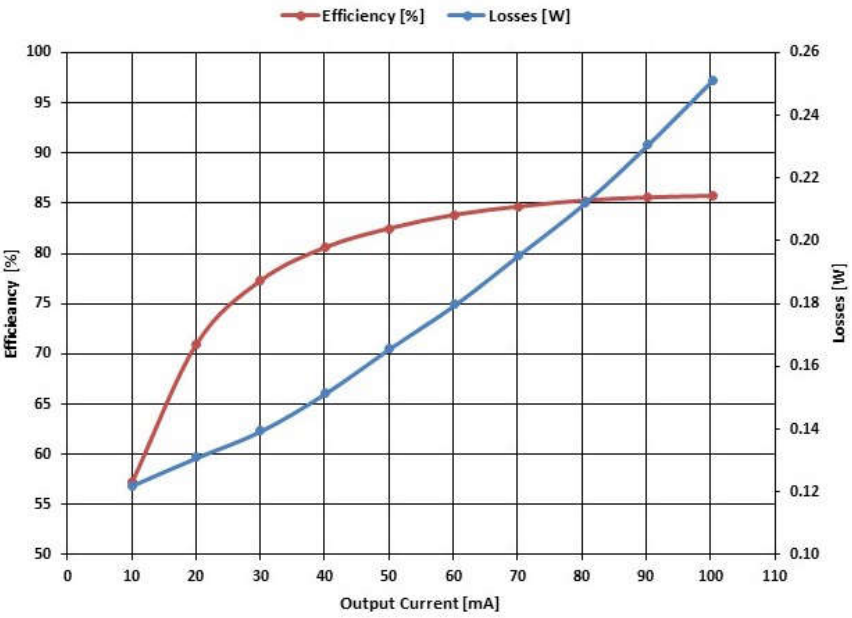


Figure 2-4. UCC25800-Q1 Efficiency at 15 V_{IN}

2.1.5 Efficiency Comparison

Efficiency comparison of the four different topologies is shown in the following figure.

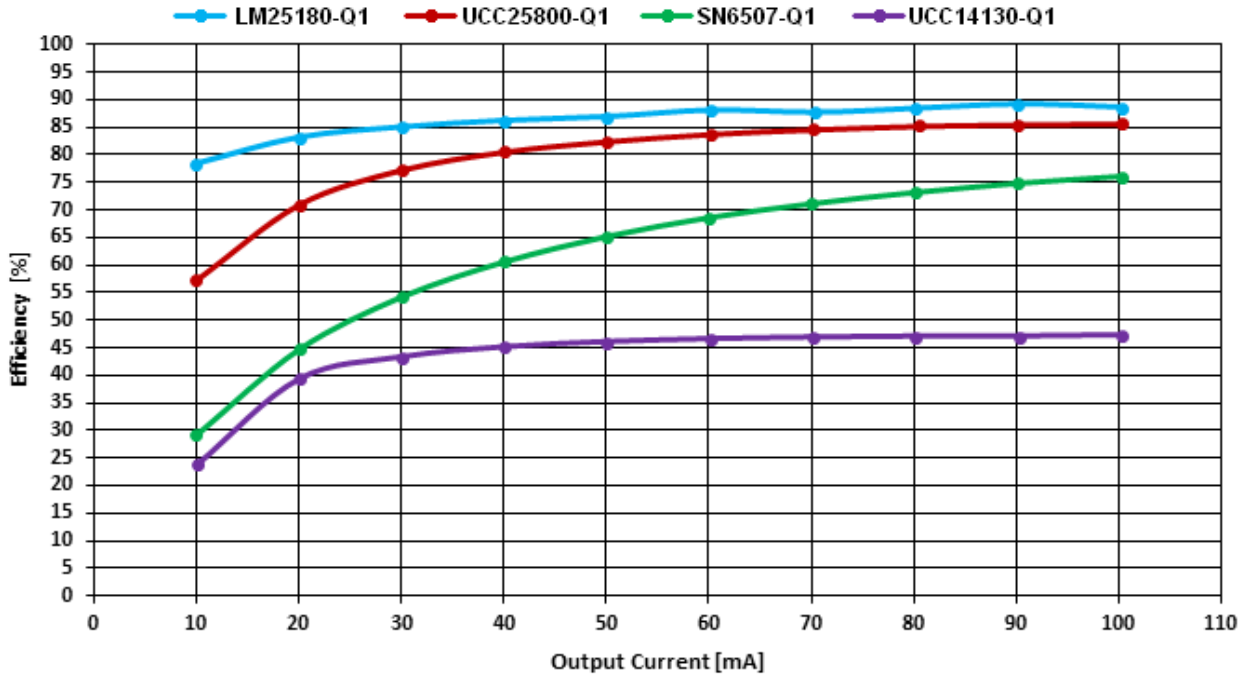


Figure 2-5. Efficiency Comparison

2.2 Efficiency Data

Efficiency data is shown in the following tables.

2.2.1 LM25180-Q1 Efficiency Data

Table 2-1. LM25180-Q1 Efficiency Data

V_{IN} (V)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	Losses (W)	Efficiency (%)
15.00	12.9	0.194	15.20	10.0	0.152	0.042	78.31
14.98	24.4	0.366	15.19	20.0	0.304	0.062	83.08
14.96	36.0	0.538	15.19	30.1	0.457	0.081	84.97
14.93	47.3	0.705	15.19	40.0	0.608	0.098	86.13
14.91	58.7	0.876	15.18	50.1	0.761	0.115	86.85
14.88	69.8	1.038	15.18	60.2	0.914	0.124	88.02
14.86	81.9	1.217	15.17	70.3	1.066	0.151	87.62
14.83	92.8	1.376	15.16	80.2	1.216	0.161	88.34
14.81	103.6	1.534	15.16	90.2	1.367	0.167	89.12
14.78	116.0	1.714	15.15	100.2	1.518	0.196	88.56

2.2.2 SN6507-Q1 Efficiency Data

Table 2-2. SN6507-Q1 Efficiency Data

V_{IN} (V)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	Losses (W)	Efficiency (%)
15.89	33.1	0.526	15.35	10.0	0.154	0.372	29.21
15.88	43.1	0.684	15.29	20.0	0.306	0.378	44.72
15.87	53.2	0.844	15.25	30.0	0.458	0.386	54.22
15.87	63.4	1.006	15.21	40.1	0.610	0.396	60.60
15.85	73.5	1.165	15.17	50.1	0.760	0.405	65.20
15.84	83.7	1.326	15.14	60.1	0.910	0.416	68.62
15.83	93.9	1.486	15.10	70.0	1.057	0.429	71.11
15.82	104.4	1.652	15.07	80.2	1.208	0.443	73.17
15.82	114.6	1.813	15.04	90.2	1.356	0.457	74.81
15.82	124.9	1.976	15.00	100.2	1.503	0.473	76.07

2.2.3 UCC14130-Q1 Efficiency Data

Table 2-3. UCC14130-Q1 Efficiency Data

V_{IN} (V)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	Losses (W)	Efficiency (%)
15.03	42.0	0.631	15.01	10.0	0.151	0.481	23.85
15.03	50.9	0.765	15.01	20.0	0.301	0.464	39.32
15.02	69.3	1.041	15.00	30.0	0.450	0.590	43.28
15.02	88.7	1.332	14.99	40.1	0.601	0.731	45.11
15.01	108.6	1.630	14.98	50.1	0.750	0.880	46.01
15.01	128.9	1.935	14.97	60.1	0.900	1.034	46.53
15.01	149.2	2.239	14.97	70.1	1.049	1.191	46.84
15.00	170.1	2.552	14.96	80.2	1.199	1.352	46.99
15.00	191.4	2.871	14.95	90.3	1.350	1.521	47.02
15.00	211.8	3.177	14.95	100.3	1.500	1.677	47.22

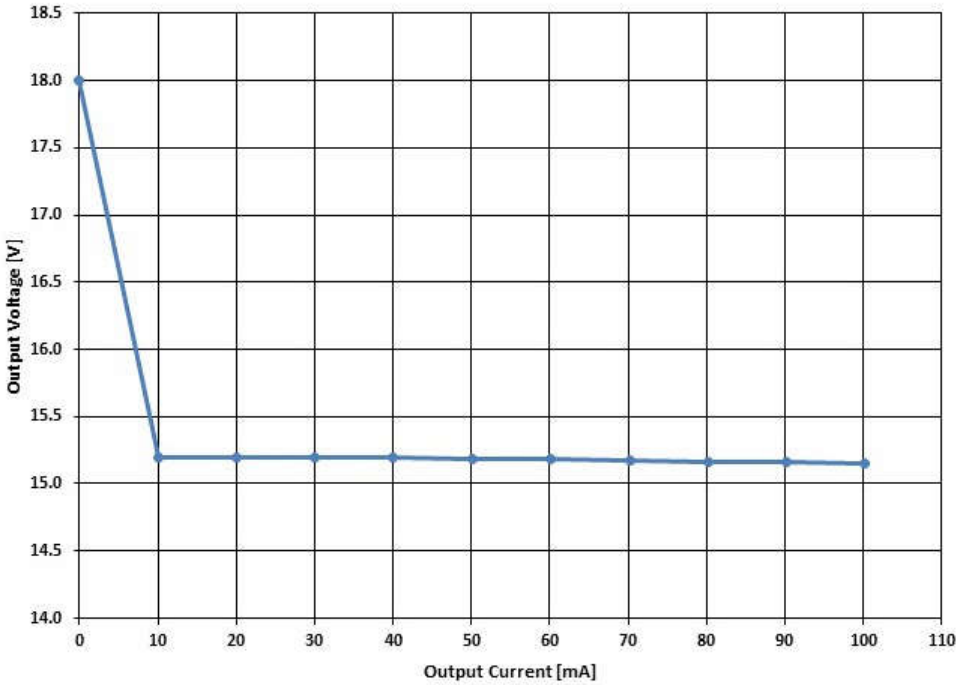
2.2.4 UCC25800-Q1 Efficiency Data

Table 2-4. UCC25800-Q1 Efficiency Data

V_{IN} (V)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	Losses (W)	Efficiency (%)
15.49	18.4	0.285	16.31	10.0	0.163	0.122	57.19
15.46	29.2	0.451	16.00	20.0	0.320	0.131	70.96
15.44	39.8	0.614	15.81	30.0	0.474	0.139	77.28
15.41	50.7	0.781	15.69	40.1	0.629	0.152	80.59
15.39	61.5	0.946	15.58	50.1	0.781	0.166	82.48
15.37	72.3	1.111	15.47	60.2	0.931	0.180	83.83
15.34	83.0	1.274	15.36	70.2	1.078	0.196	84.65
15.32	93.9	1.439	15.24	80.5	1.227	0.212	85.25
15.30	104.3	1.595	15.13	90.2	1.365	0.231	85.55
15.28	115.0	1.757	15.01	100.3	1.506	0.251	85.70

2.3 Load Regulation

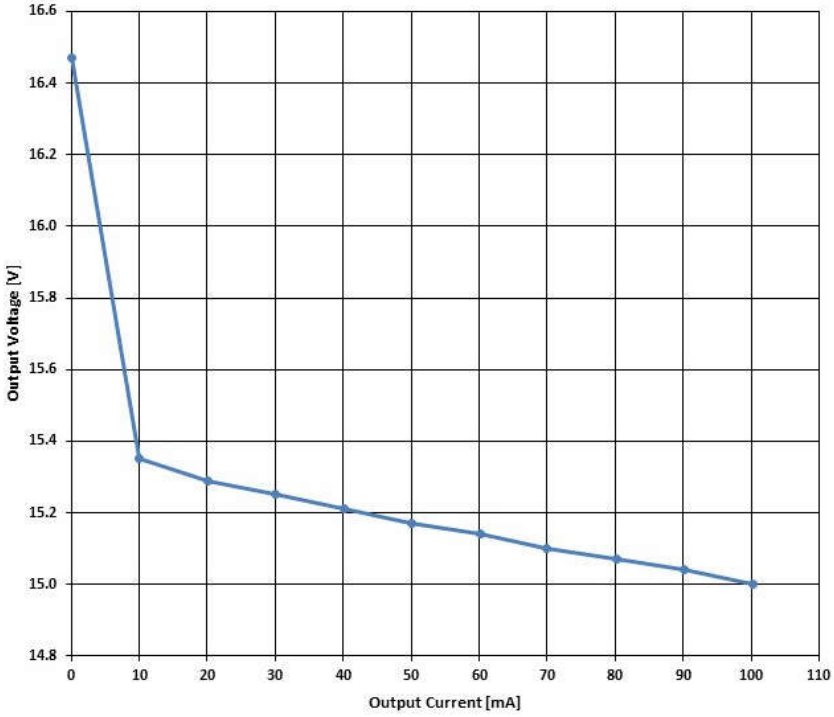
2.3.1 LM25180-Q1 Load Regulation



An 18V Zener diode is used to clamp the output voltage in case of no load condition.

Figure 2-6. LM25180-Q1 Load Regulation at 15 V_{IN}

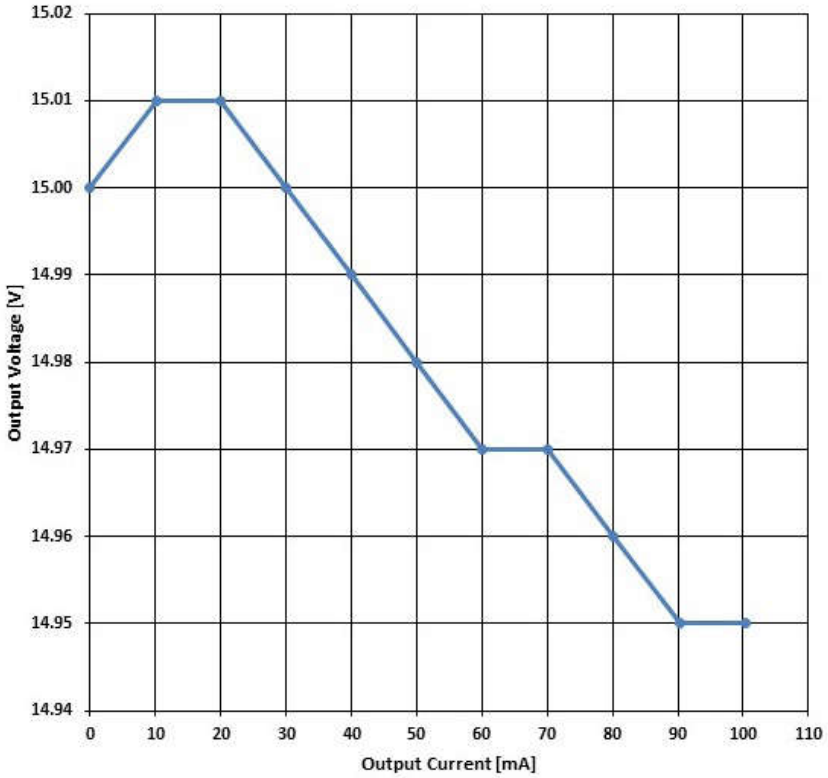
2.3.2 SN6507-Q1 Load Regulation



An 18V Zener diode is used to clamp the output voltage in case of no load condition.

Figure 2-7. SN6507-Q1 Load Regulation at 15 V_{IN}

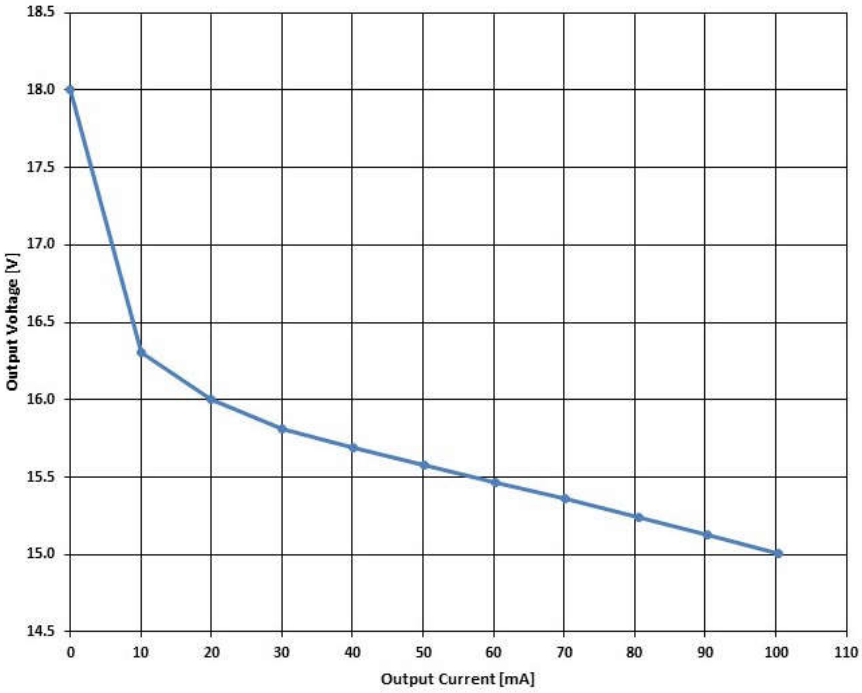
2.3.3 UCC14130-Q1 Load Regulation



An 18V Zener diode is used to clamp the output voltage in case of no load condition.

Figure 2-8. UCC14130-Q1 Load Regulation at 15 V_{IN}

2.3.4 UCC25800-Q1 Load Regulation



An 18V Zener diode is used to clamp the output voltage in case of no load condition.

Figure 2-9. UCC25800-Q1 Load Regulation at 15 V_{IN}

2.3.5 Load Regulation Comparison

Load regulation comparison of four different topologies is shown in the following figure.

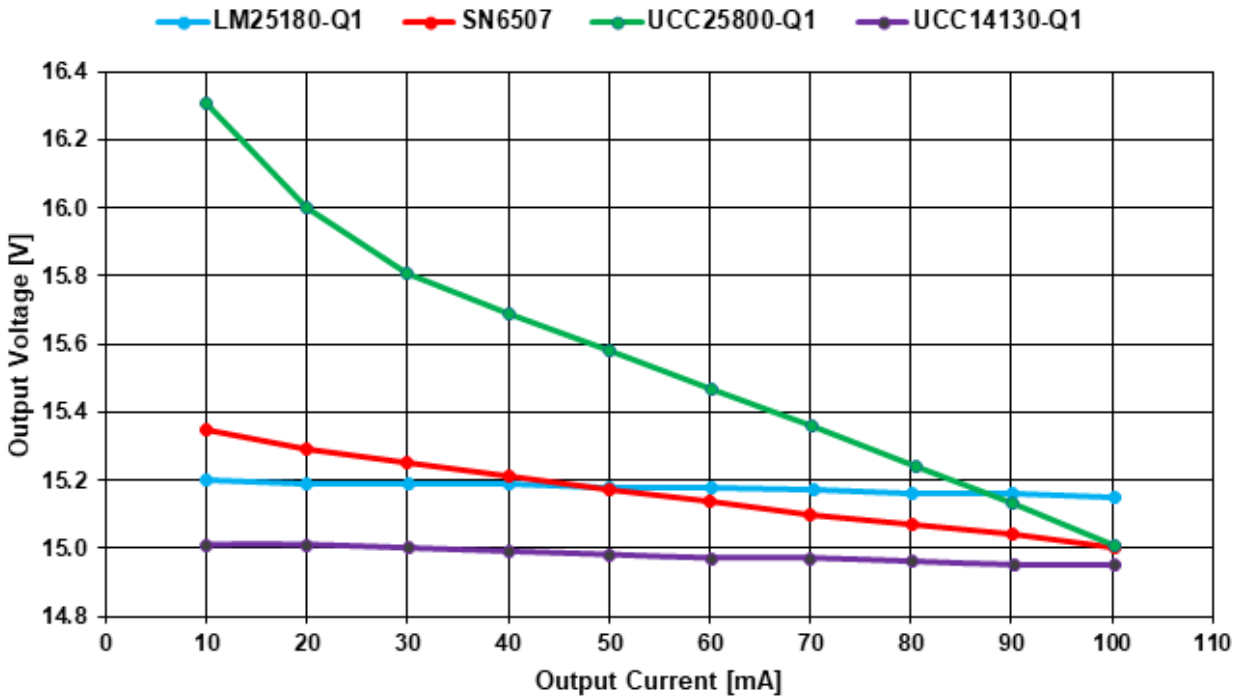


Figure 2-10. Load Regulation Comparison

2.4 Thermal Images

2.4.1 LM25180-Q1 Thermal Image

Figure 2-11 shows the thermal image captured with a thermal camera. The image shows that the transformer is the hottest component of this PCB. The thermal image was captured while running both power supplies in parallel at 15 V_{IN} and 100mA full load current.

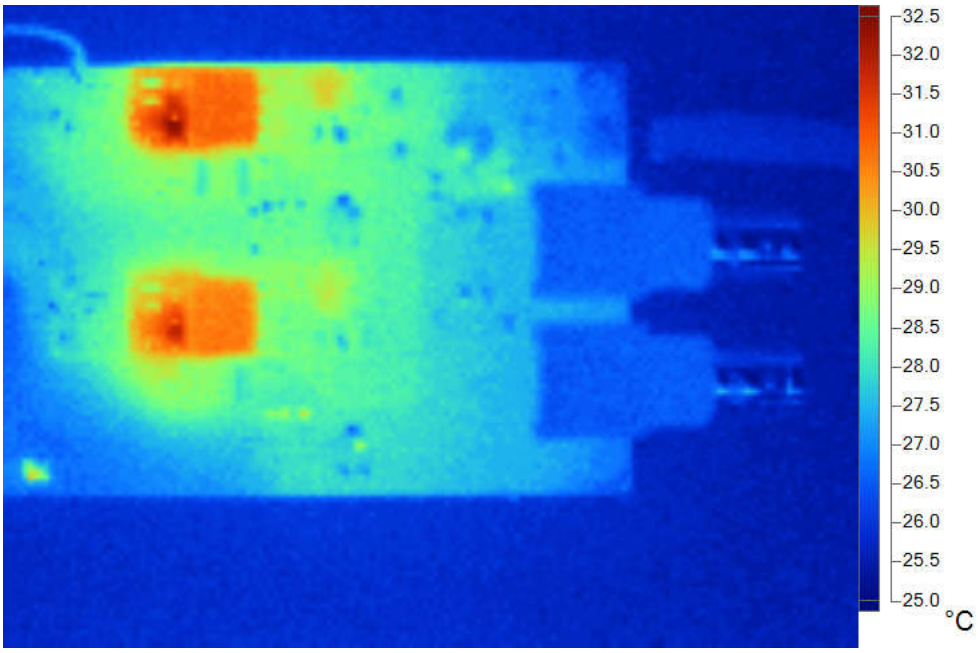


Figure 2-11. Thermal Image – Top Side of PCB at 15 V_{IN} and 100mA Full Load Current

2.4.2 SN6507-Q1 Thermal Image

Figure 2-12 shows the thermal image captured with a thermal camera. The image shows that the transformer is the hottest component of this PCB. The thermal image was captured while running both power supplies in parallel at 15 V_{IN} and 100mA full load current.

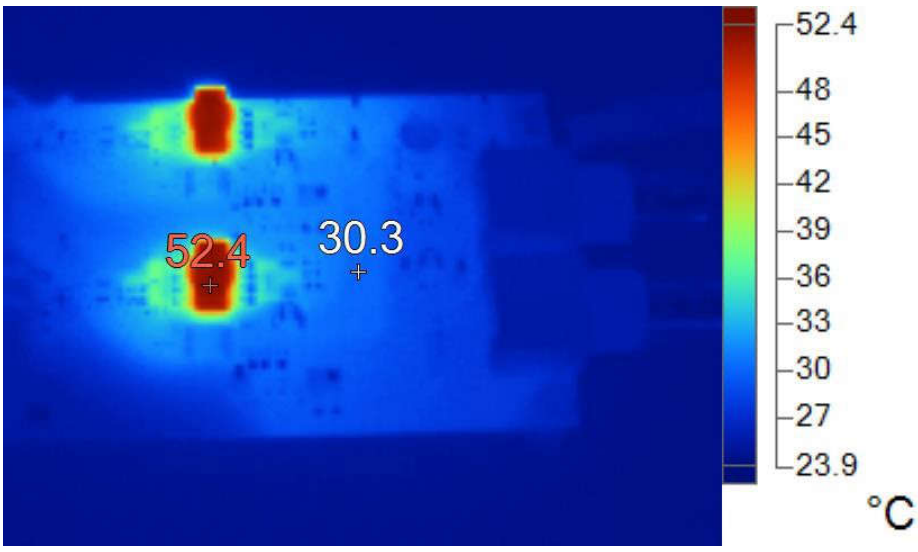


Figure 2-12. Thermal Image – Top Side of PCB at 15 V_{IN} and 100mA Full Load Current

2.4.3 UCC14130-Q1 Thermal Image

Figure 2-13 shows the thermal image captured with a thermal camera. The image shows that the integrated transformer isolated DCDC modules are the hottest component of this PCB. The thermal image was captured while running both power supplies in parallel at 15 V_{IN} and 100mA full load current.

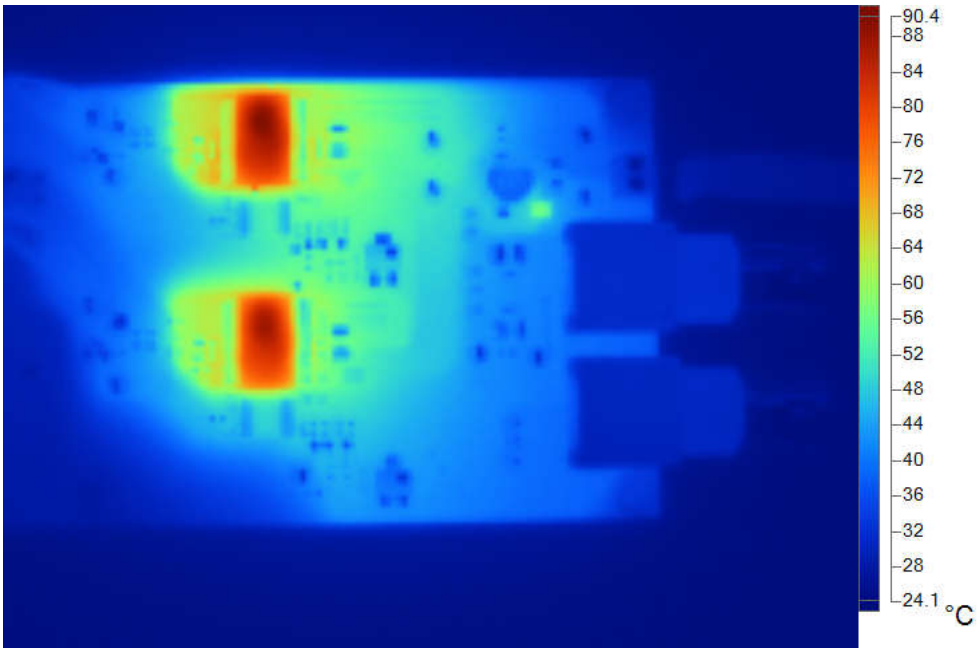


Figure 2-13. Thermal Image – Top Side of PCB at 15 V_{IN} and 100mA Full Load Current

2.4.4 UCC25800-Q1 Thermal Image

Figure 2-14 shows the thermal image captured with a thermal camera. The image shows that the transformer is the hottest component of this PCB. The thermal image was captured while running both power supplies in parallel at 15 V_{IN} and 100mA full load current.

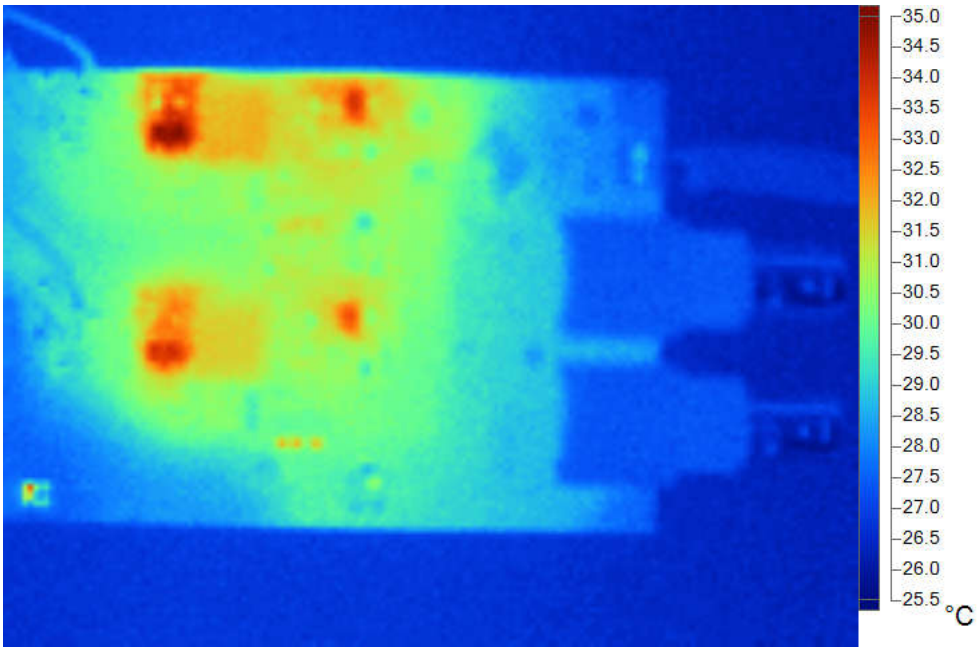


Figure 2-14. Thermal Image – Top Side of PCB at 15 V_{IN} and 100mA Full Load Current

2.5 Common-Mode Current (CMI)

Common-Mode Current (CMI) tests were done while running both isolated bias power supply converter circuits at 15V output and switching the GaN half-bridge at 400V. Common-mode current flows from the high-voltage side to the low-voltage side through the parasitic capacitance across the isolation barrier. Common mode current is generated due to switching of the high- and low-side GaN half bridge switches at a high slew rate. During the measurements, high- and low-voltage grounds were shorted using a wire (shown in Figure 2-15) to minimize the length of the common-mode current loop from high-voltage side to low-voltage side. This can be considered as a worst-case scenario for common-mode current and results in the highest possible common-mode current through the isolation barrier. CMI current measurements are taken on two different high slew rate values: 40V/ns and 100V/ns. CMI measurements are taken while bypassing the input filter. Using a potentiometer at the RDRV pin of the LMG3525R030Q, the slew rate can be varied with reference to the selected resistor value. Figure 2-15 shows the CMI test setup.

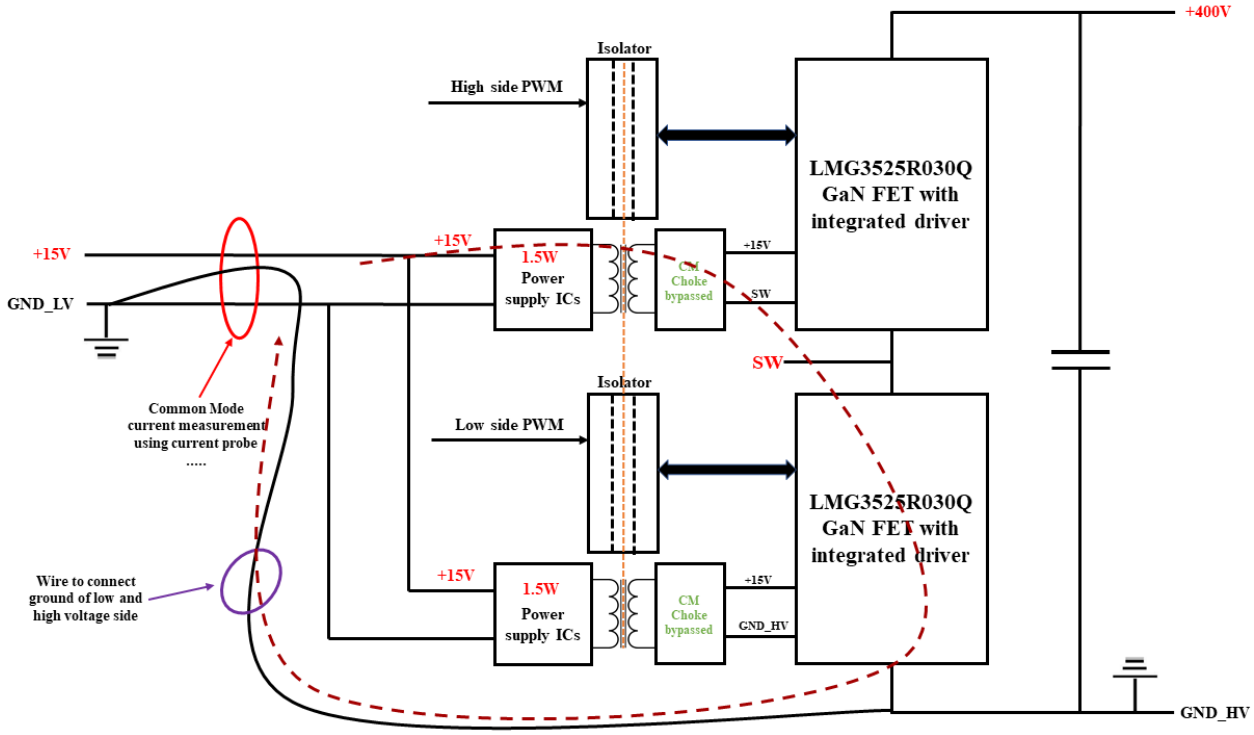
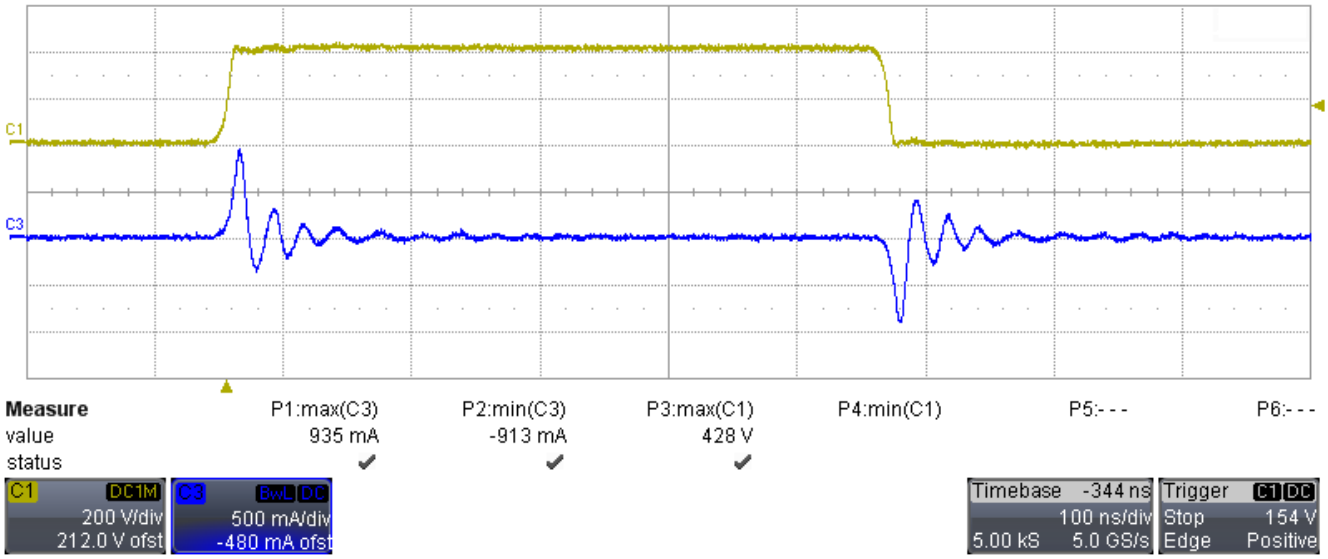


Figure 2-15. Common-Mode Current (CMI) Test Setup

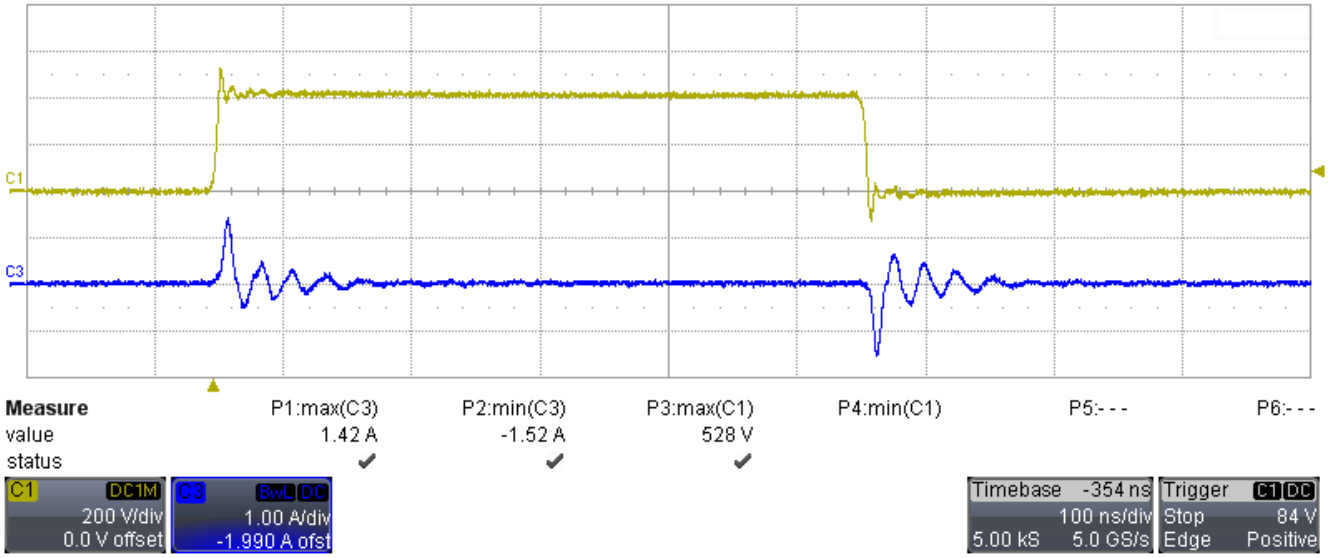
2.5.1 LM25180-Q1 CMI

The LM25180-Q1 CMI waveforms are illustrated in the following images.



Channel 1: HV switch node, [scale: 200V/div, 100ns/div]
Channel 3: CMI current, [scale: 500mA/div, 100ns/div]

Figure 2-16. Common-Mode Current at 40V/ns Slew Rate

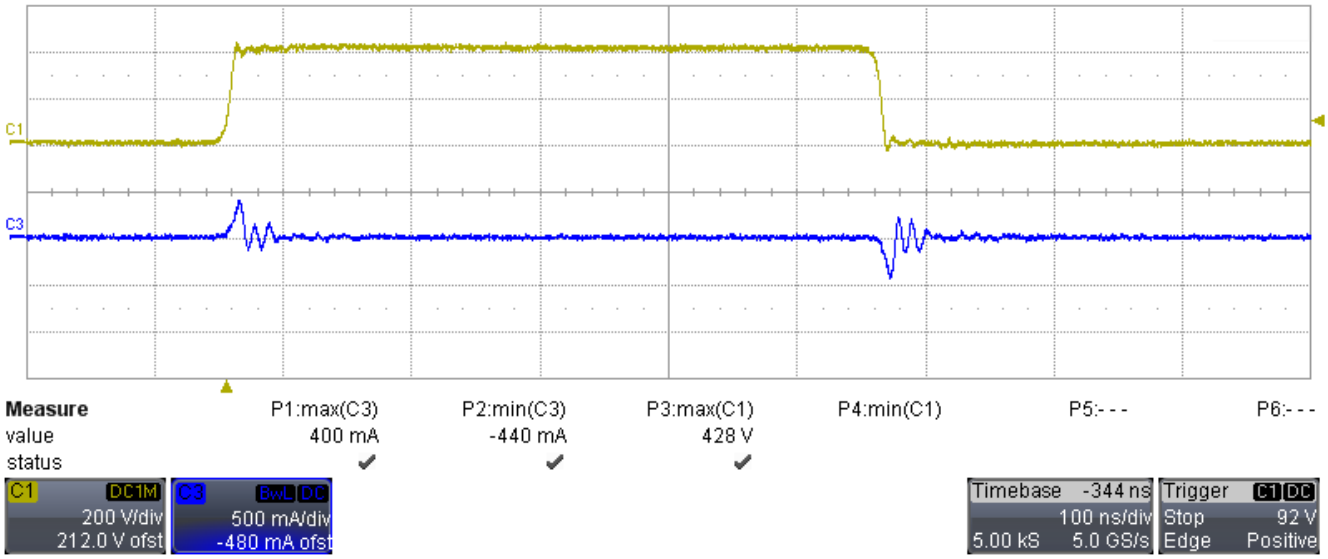


Channel 1: HV switch node, [scale: 200V/div, 100ns/div]
Channel 3: CMI current, [scale: 1A/div, 100ns/div]

Figure 2-17. Common-Mode Current at 100V/ns Slew Rate

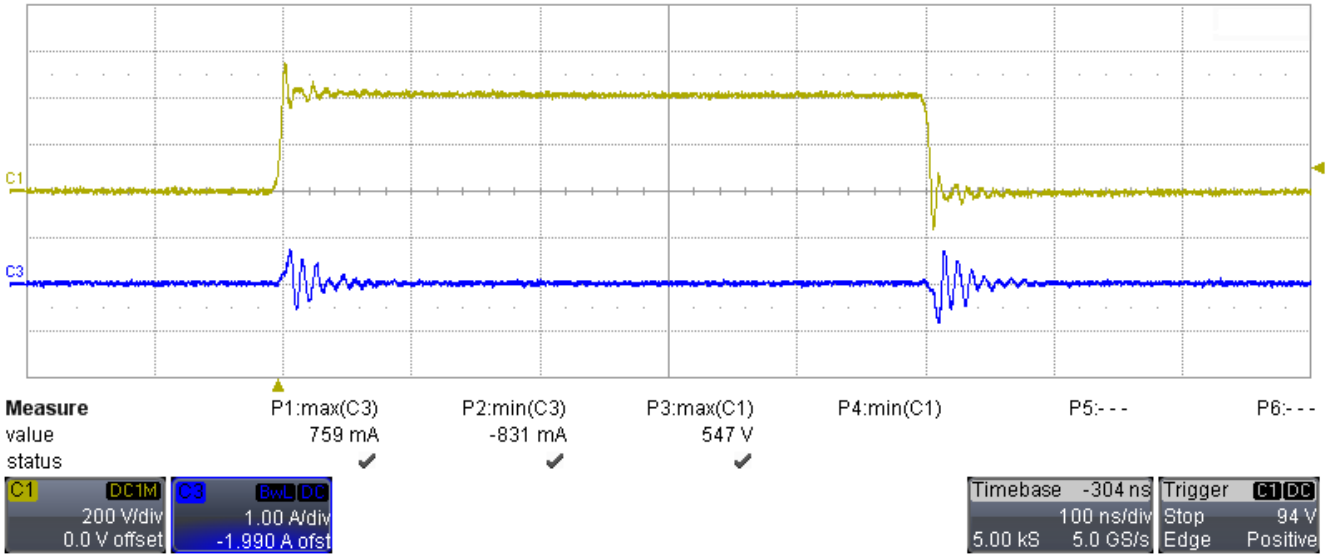
2.5.2 SN6507-Q1 CMI

The SN6507-Q1 CMI waveforms are illustrated in the following images.



Channel 1: HV switch node, [scale: 200V/div, 100ns/div]
Channel 3: CMI current, [scale: 500mA/div, 100ns/div]

Figure 2-18. Common-Mode Current at 40V/ns Slew Rate

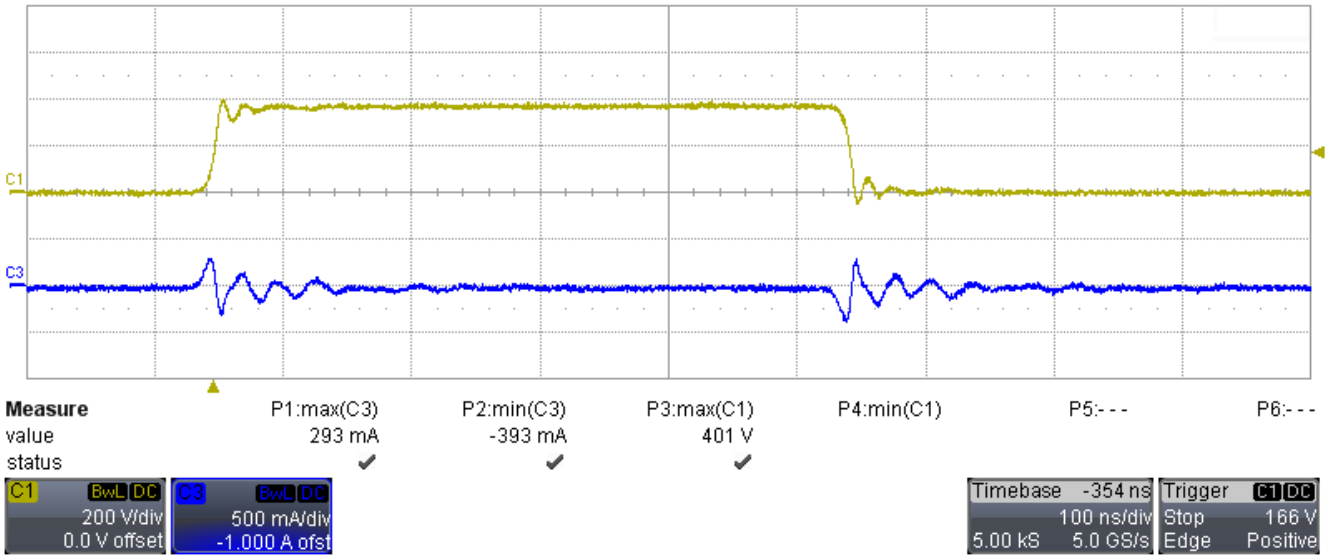


Channel 1: HV switch node, [scale: 200V/div, 100ns/div]
Channel 3: CMI current, [scale: 1A/div, 100ns/div]

Figure 2-19. Common-Mode Current at 100V/ns Slew Rate

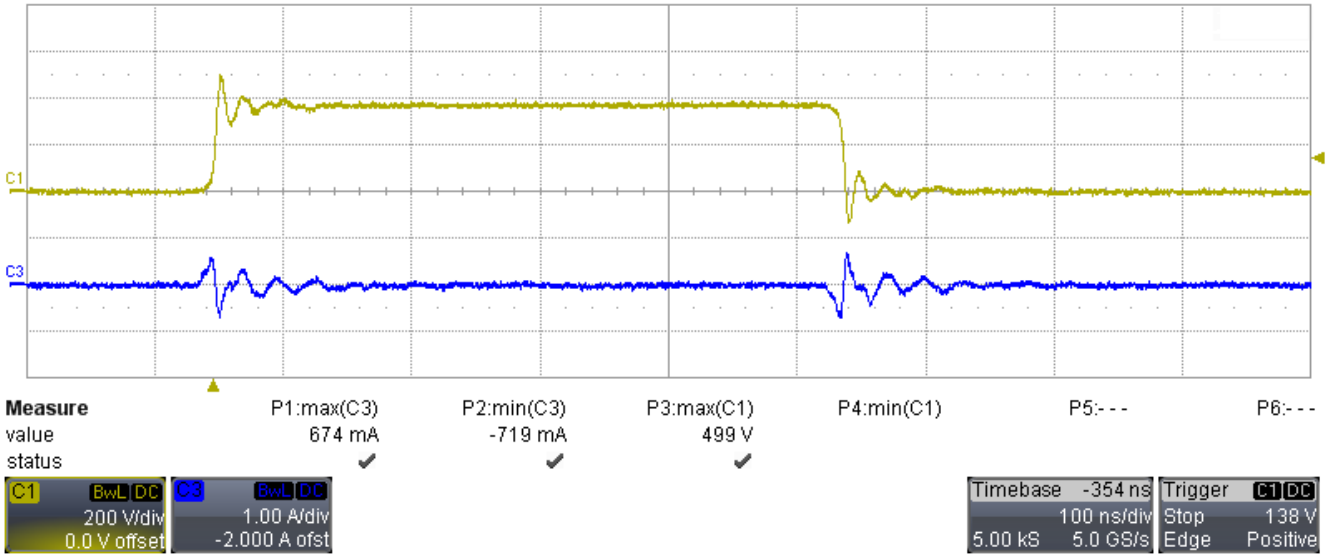
2.5.3 UCC14130-Q1 CMI

The UCC14130-Q1 CMI waveforms are illustrated in the following images.



Channel 1: HV switch node, [scale: 200V/div, 100ns/div]
Channel 3: CMI current, [scale: 500mA/div, 100ns/div]

Figure 2-20. Common-Mode Current at 40V/ns Slew Rate

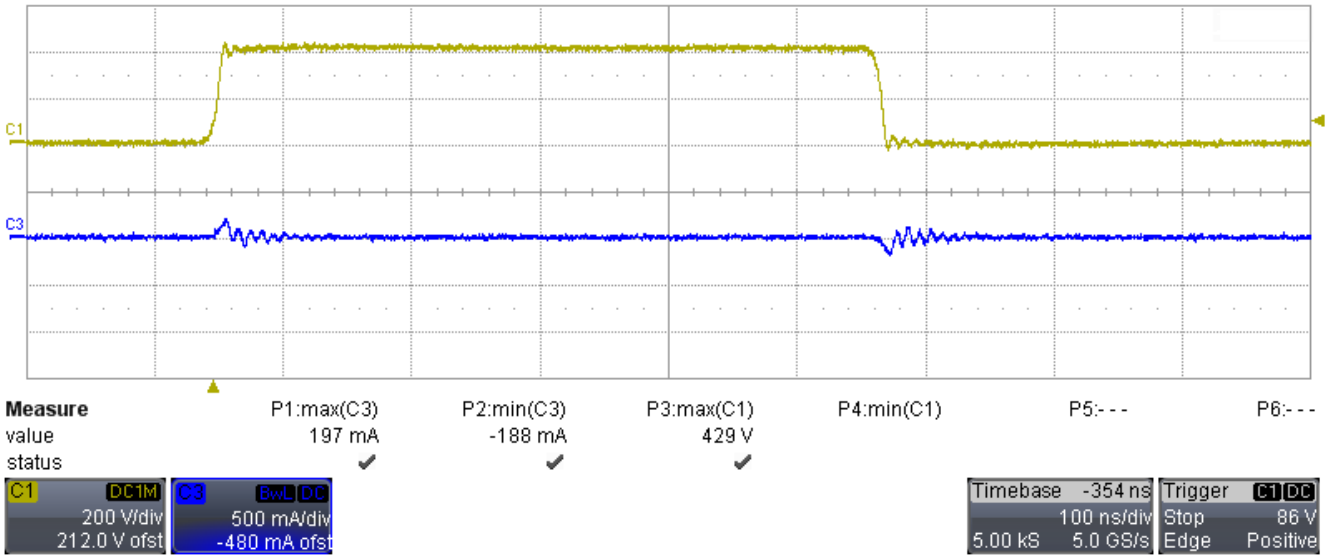


Channel 1: HV switch node, [scale: 200V/div, 100ns/div]
Channel 3: CMI current, [scale: 1A/div, 100ns/div]

Figure 2-21. Common-Mode Current at 100V/ns Slew Rate

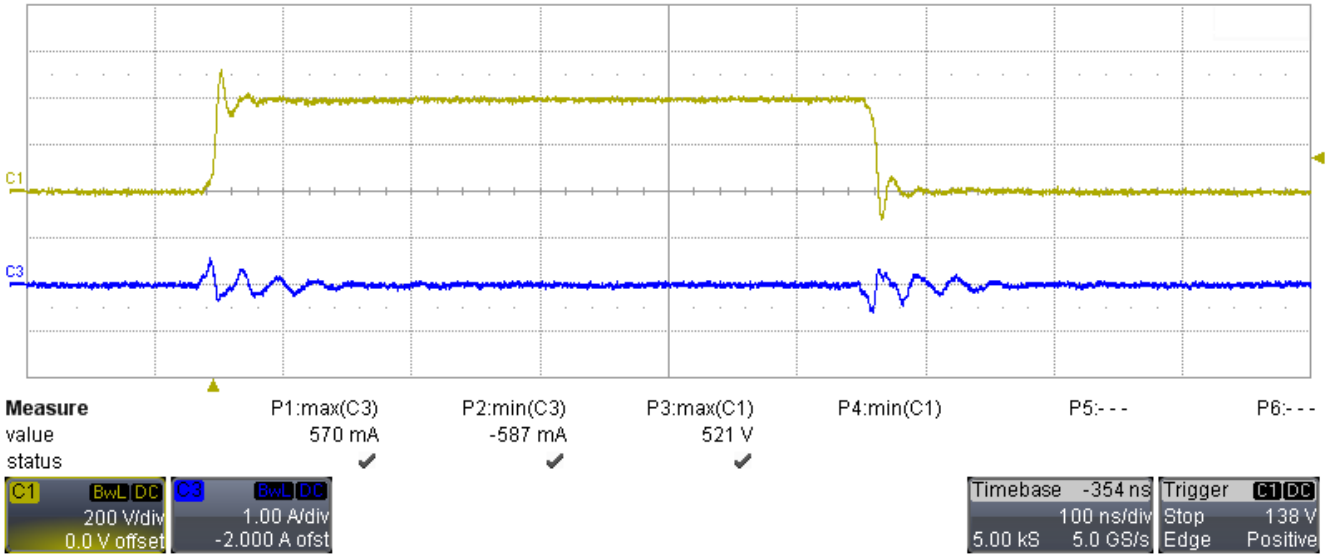
2.5.4 UCC25800-Q1 CMI

The UCC25800-Q1 CMI waveforms are illustrated in the following images.



Channel 1: HV switch node, [scale: 200V/div, 100ns/div]
Channel 3: CMI current, [scale: 500mA/div, 100ns/div]

Figure 2-22. Common-Mode Current at 40V/ns Slew Rate

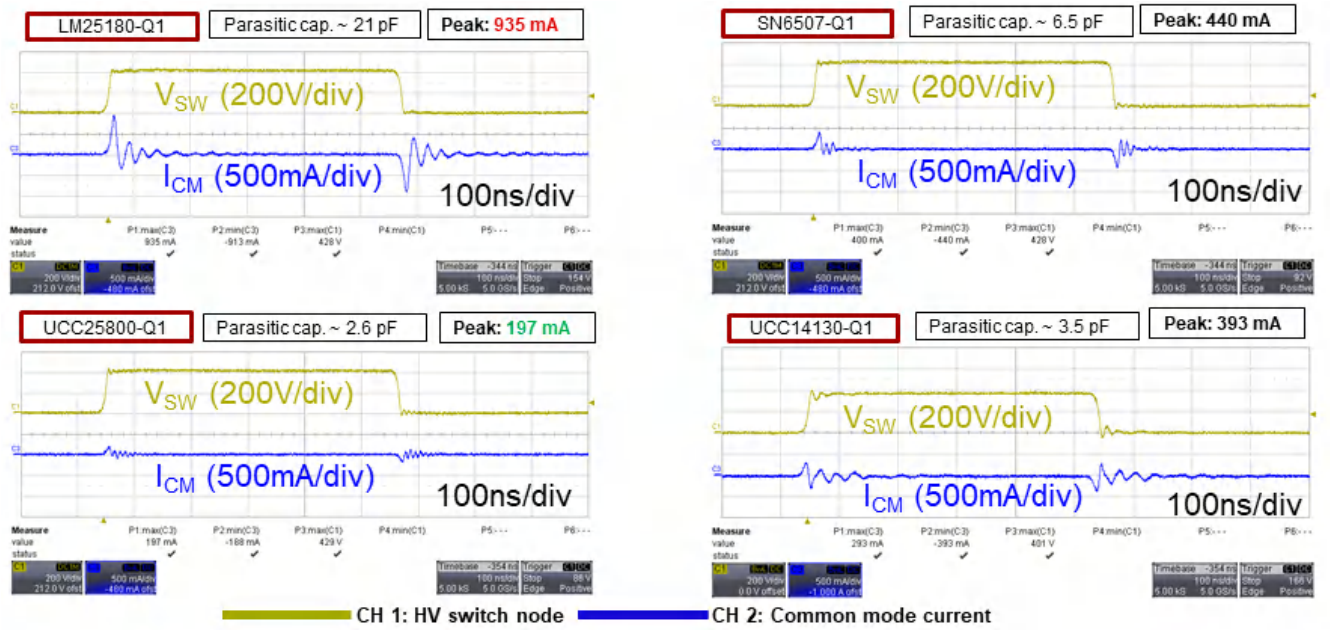


Channel 1: HV switch node, [scale: 200V/div, 100ns/div]
Channel 3: CMI current, [scale: 1A/div, 100ns/div]

Figure 2-23. Common-Mode Current at 100V/ns Slew Rate

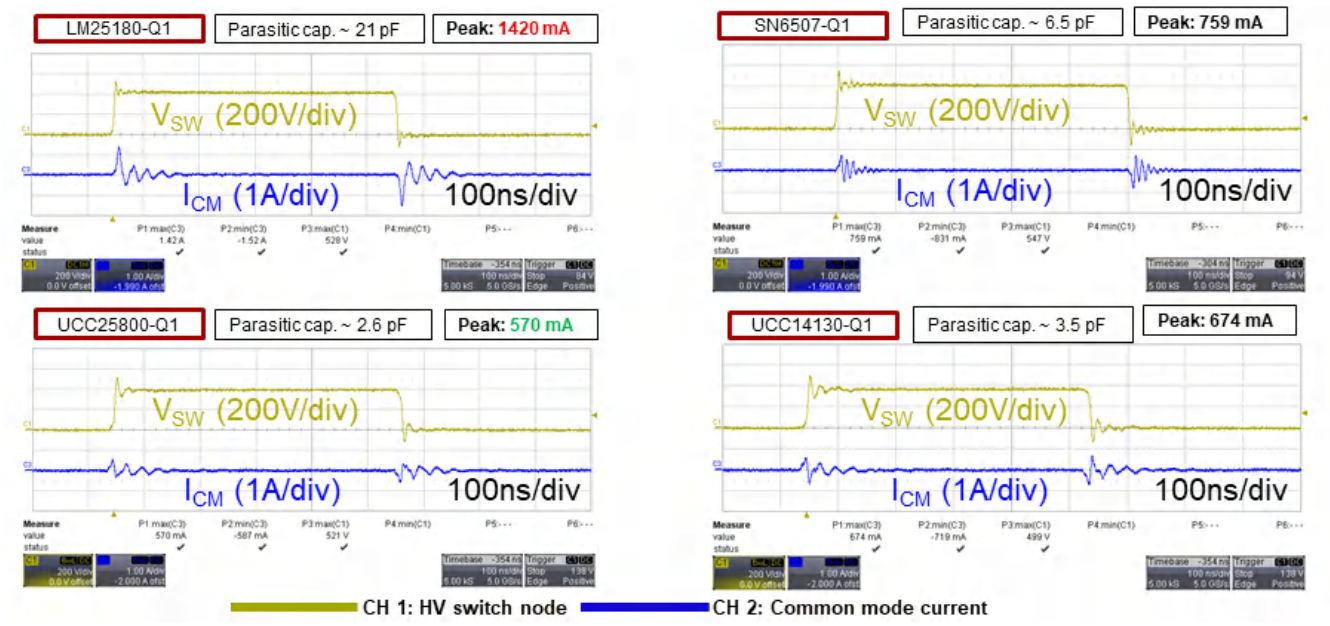
2.5.5 Common-Mode Current Comparison

The CMI comparison waveforms of the four topologies are illustrated in the following images.



Channel 1: HV switch node, [scale: 200V/div, 100ns/div]
Channel 3: CMI current, [scale: 500mA/div, 100ns/div]

Figure 2-24. Common-Mode Current Comparison at 40V/ns Slew Rate



Channel 1: HV switch node, [scale: 200V/div, 100ns/div]
Channel 3: CMI current, [scale: 1A/div, 100ns/div]

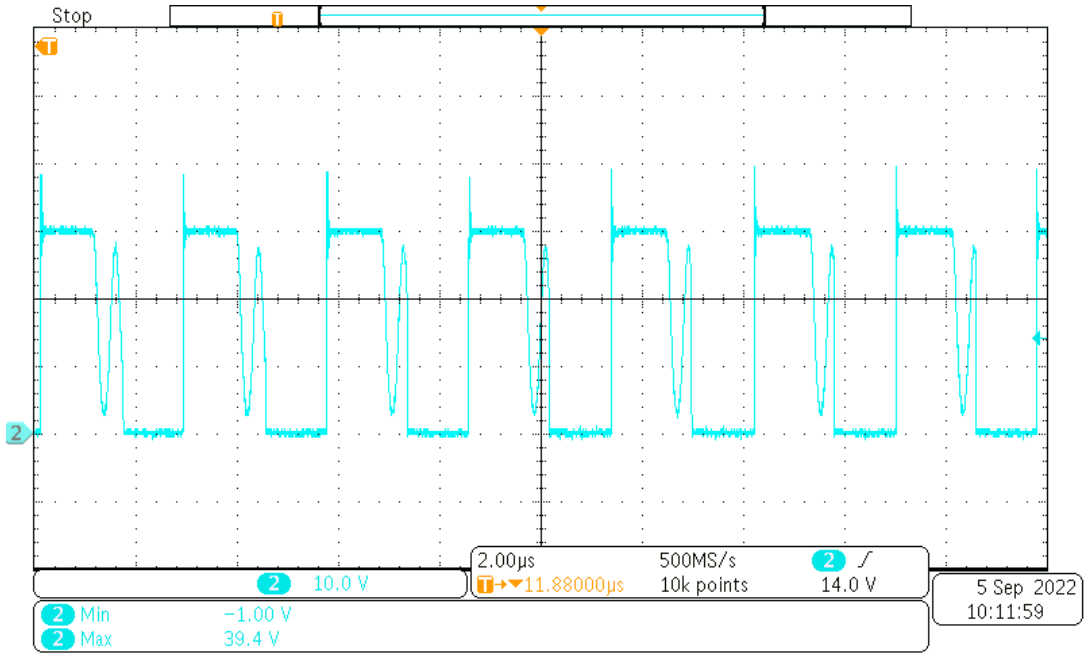
Figure 2-25. Common-Mode Current Comparison at 100V/ns Slew Rate

3 Waveforms

3.1 Switching

3.1.1 LM25180-Q1 Switching

The LM25180-Q1 switching waveform is shown in the following figure.

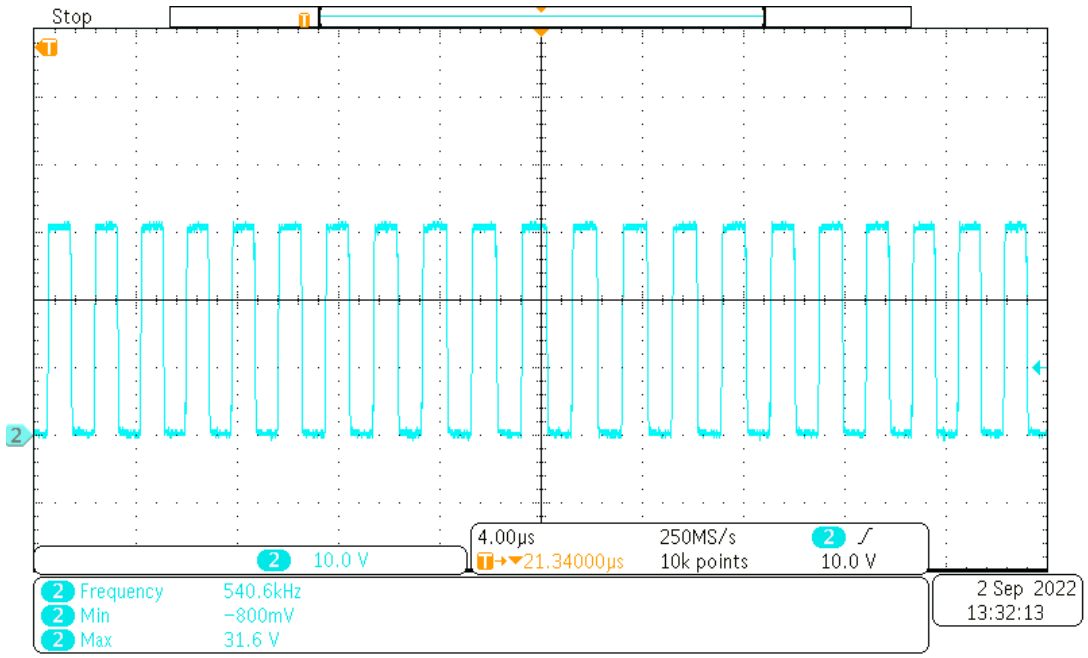


Channel 2: Switching node at 15 V_{OUT} and 100mA load current [scale: 10.0V/div, 2.0µs/div]

Figure 3-1. LM25180-Q1 Switch Node Voltage

3.1.2 SN6507-Q1 Switching

The SN6507-Q1 switching waveform is shown in the following figure.

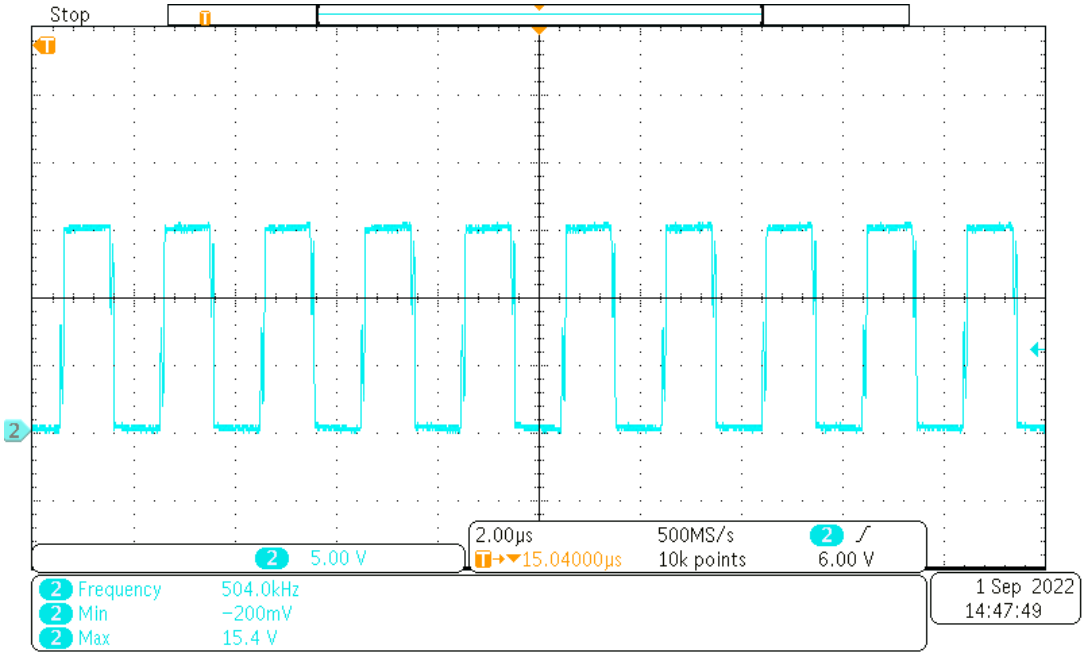


Channel 2: Switching node at 15 V_{OUT} and 100mA load current [scale: 10.0V/div, 4.0µs/div]

Figure 3-2. SN6507-Q1 Switch Node Voltage

3.1.3 UCC25800-Q1 Switching

The UCC25800-Q1 switching waveform is shown in the following figure.



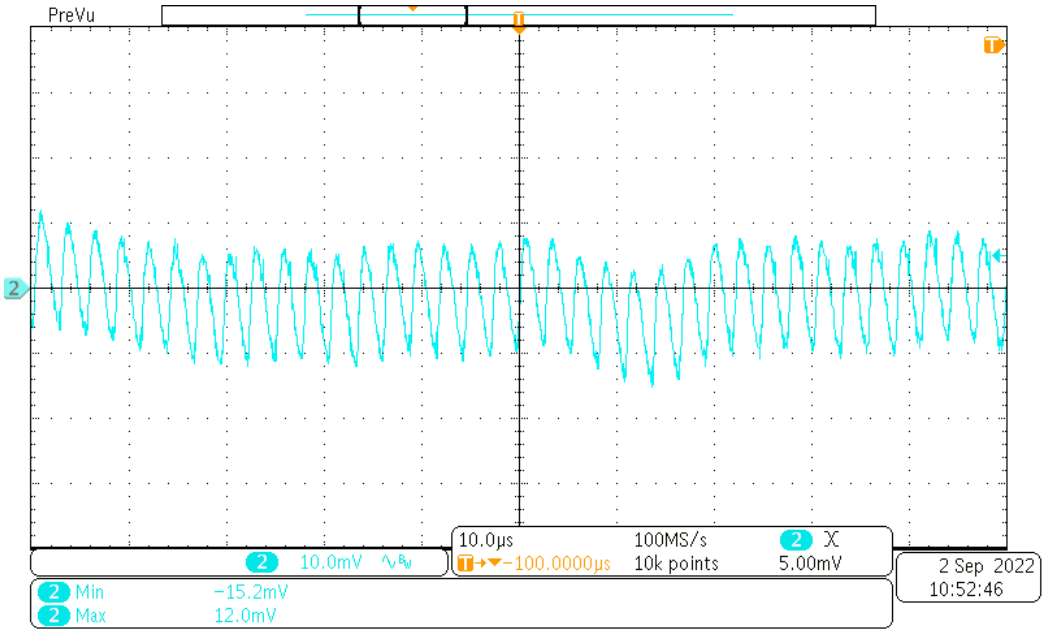
Channel 2: Switching node at 15 V_{OUT} and 100mA load current [scale: 5.0V/div, 2.0µs/div]

Figure 3-3. UCC25800-Q1 Switch Node Voltage

3.2 Output Voltage Ripple

3.2.1 LM25180-Q1 Output Voltage Ripple

The LM25180-Q1 output voltage ripple waveform is shown in the following figure.

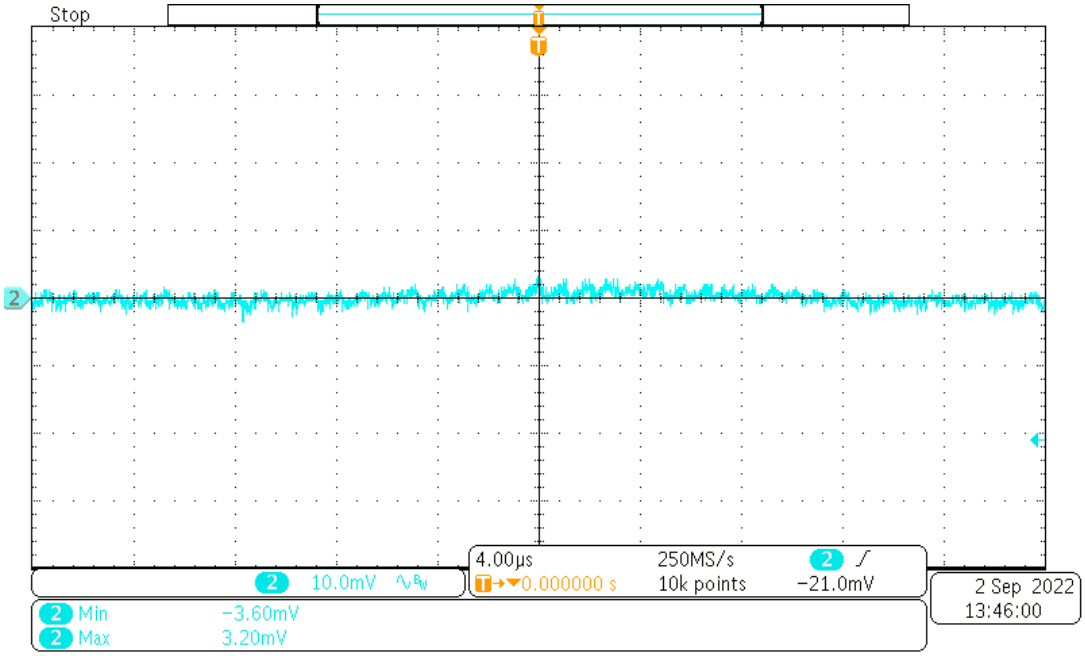


Channel 2: AC coupled output voltage ripple at 15 V_{OUT} and 100mA load current, bandwidth limited (20MHz), [scale: 10mV/div, 10.0µs/div]. The output voltage ripple was measured at output capacitor C34.

Figure 3-4. LM25180-Q1 Output Voltage Ripple

3.2.2 SN6507-Q1 Output Voltage Ripple

The SN6507-Q1 output voltage ripple waveform is shown in the following figure.

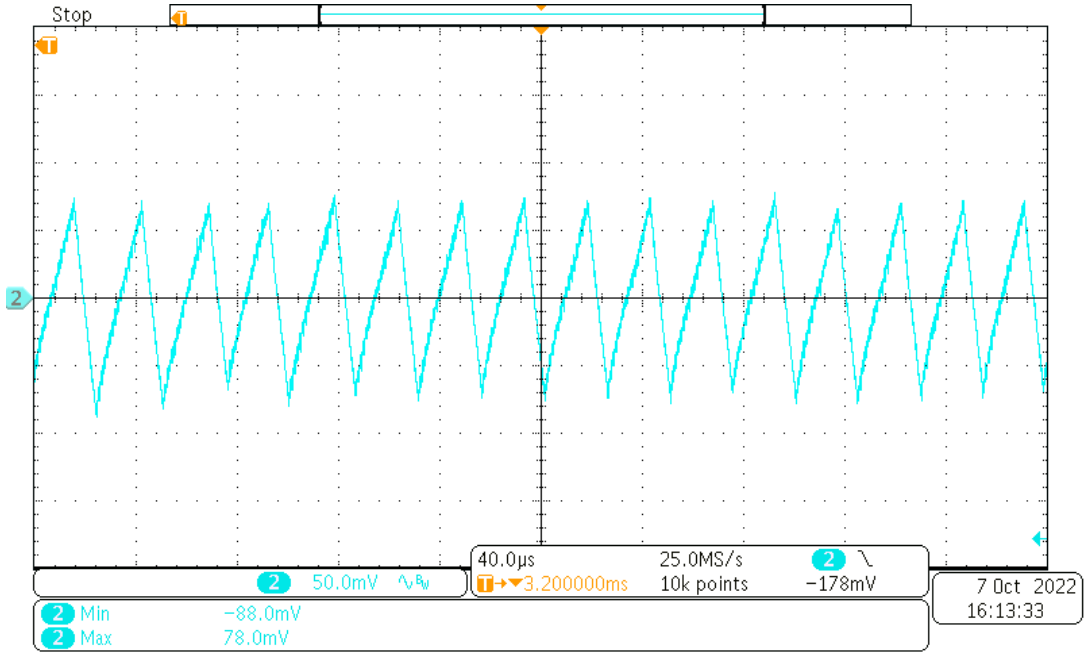


Channel 2: AC coupled output voltage ripple at 15 V_{OUT} and 100mA load current, bandwidth limited (20MHz), [scale: 10mV/div, 4.0µs/div]. The output voltage ripple was measured at output capacitor C34.

Figure 3-5. SN6507-Q1 Output Voltage Ripple

3.2.3 UCC14130-Q1 Output Voltage Ripple

The UCC14130-Q1 output voltage ripple waveform is shown in the following figure.

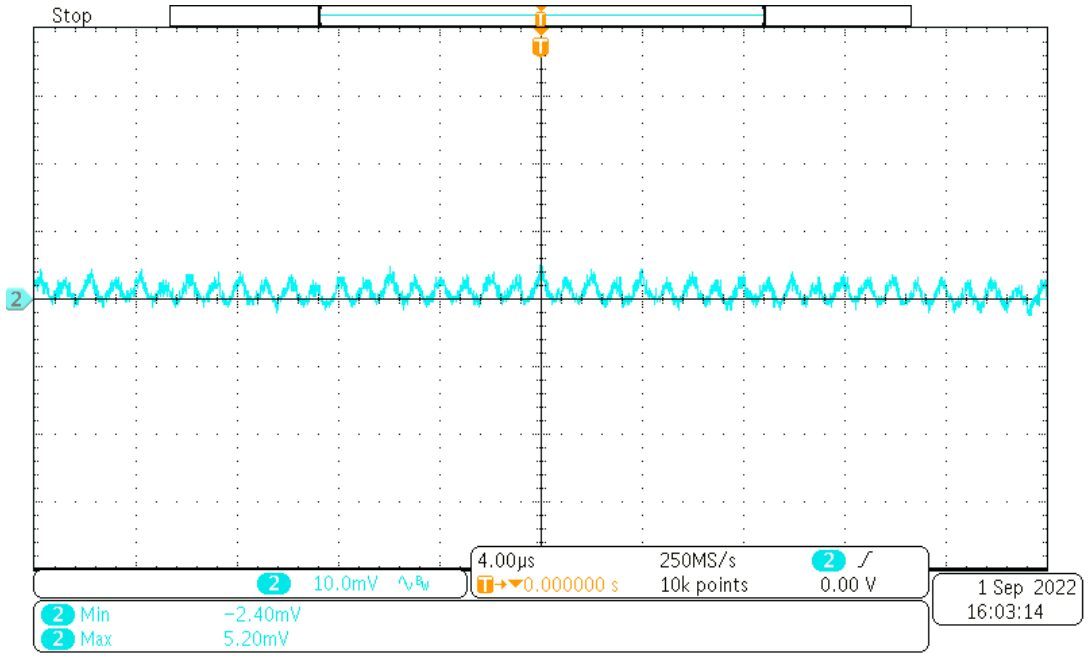


Channel 2: AC coupled output voltage ripple at 15 V_{OUT} and 100mA load current, bandwidth limited (20MHz), [scale: 50mV/div, 40.0µs/div]. The output voltage ripple was measured at output capacitor C36.
The isolated DCDC module uses an ON-OFF control scheme that results in larger input ripple or output ripple

Figure 3-6. UCC14130-Q1 Output Voltage Ripple

3.2.4 UCC25800-Q1 Output Voltage Ripple

The UCC25800-Q1 output voltage ripple waveform is shown in the following figure.

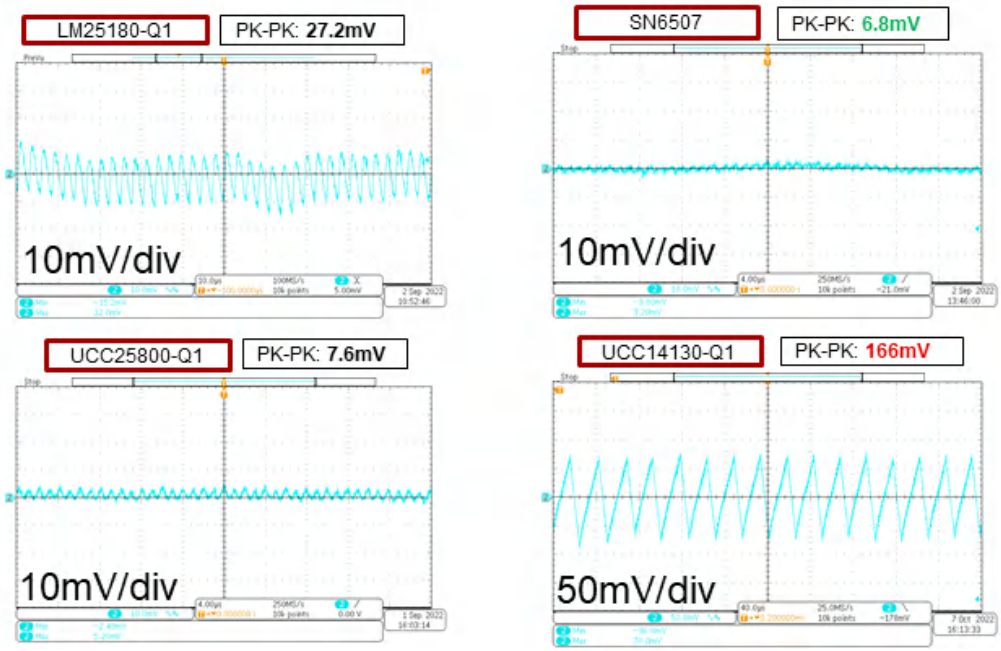


Channel 2: AC coupled output voltage Ripple at 15 V_{OUT} and 100mA load current, bandwidth limited (20MHz), [scale: 10mV/div, 4.0µs/div]. The output voltage ripple was measured at output capacitor C64.

Figure 3-7. UCC25800-Q1 Output Voltage Ripple

3.2.5 Output Voltage Ripple Comparison

The output voltage ripple comparison waveforms are shown in the following figure.



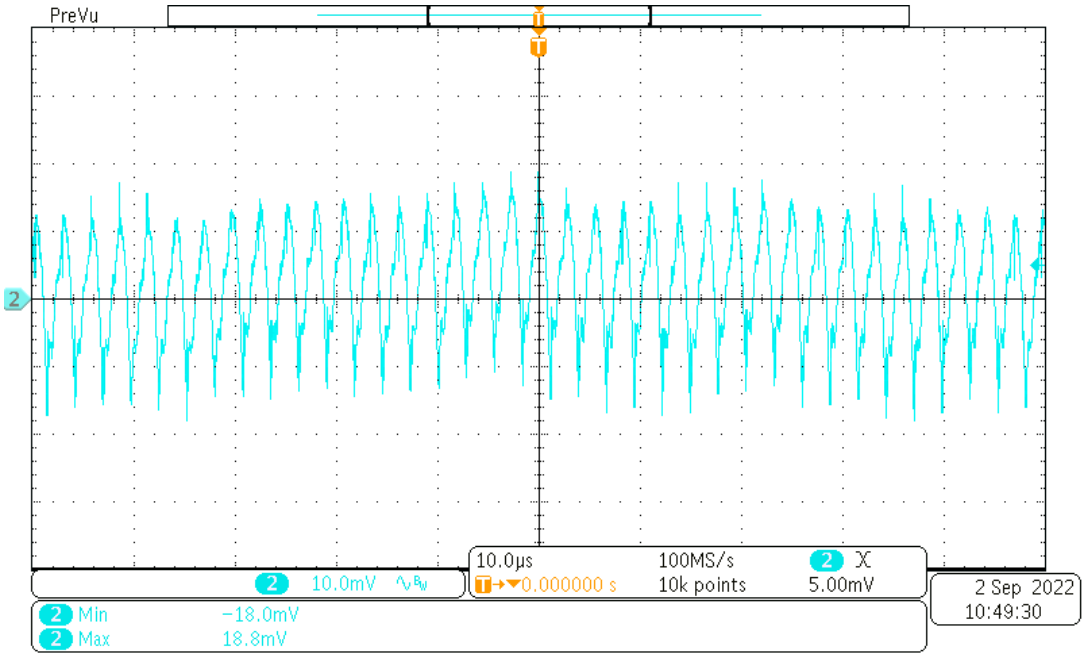
The isolated DCDC module uses an ON-OFF control scheme that results in larger input ripple and output ripple.

Figure 3-8. Output Voltage Ripple Comparison

3.3 Input Voltage Ripple

3.3.1 LM25180-Q1 Input Voltage Ripple

The LM25180-Q1 input voltage ripple waveform is shown in the following figure.

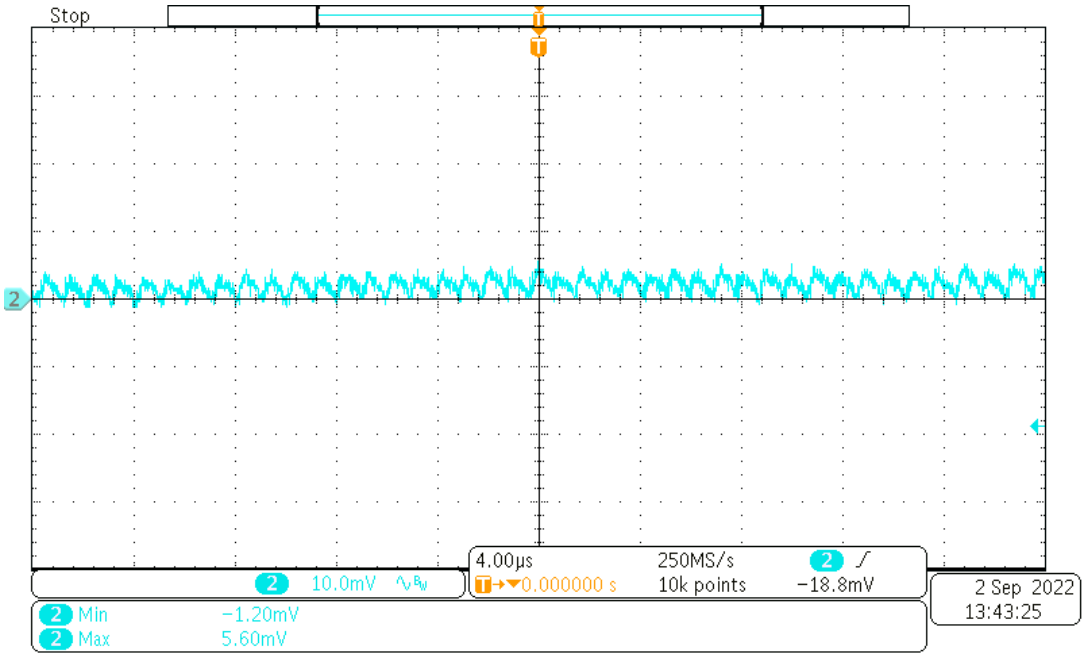


Channel 2: AC coupled input voltage ripple at 15 V_{OUT} and 100mA load current, bandwidth limited (20MHz), [scale: 10mV/div, 10.0µs/div]. The input voltage ripple was measured at input capacitor C35.

Figure 3-9. LM25180-Q1 Input Voltage Ripple

3.3.2 SN6507-Q1 Input Voltage Ripple

The SN6507-Q1 input voltage ripple waveform is shown in the following figure.

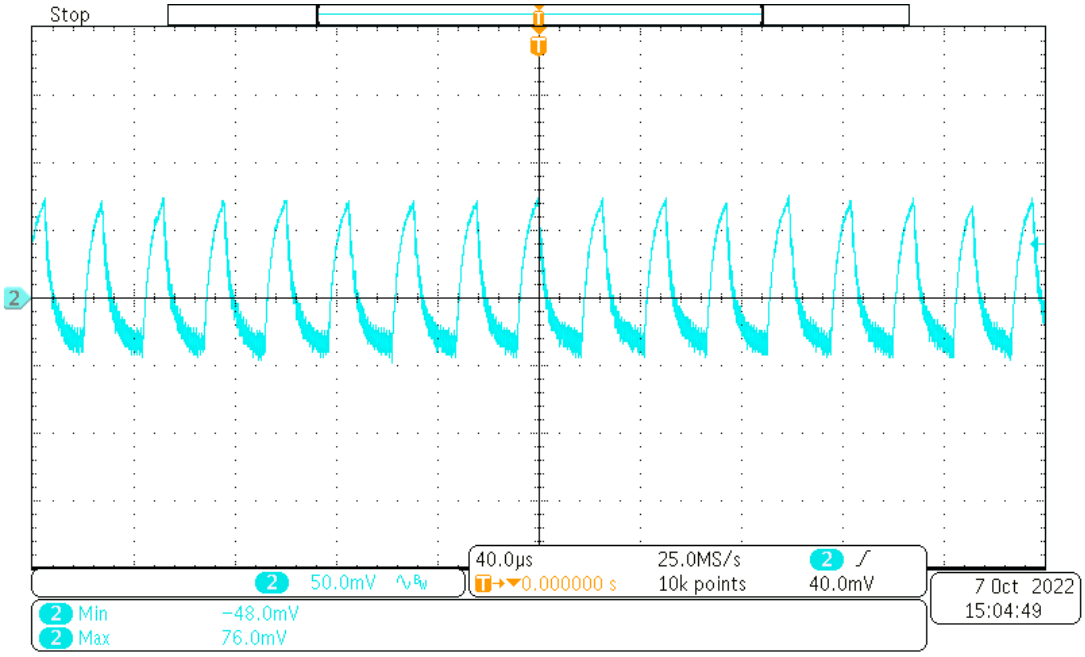


Channel 2: AC coupled Input Voltage Ripple at 15 V_{OUT} and 100mA load current, bandwidth limited (20MHz), [scale: 10mV/div, 4.0µs/div]. The input voltage ripple was measured at input capacitor C31.

Figure 3-10. SN6507-Q1 Input Voltage Ripple

3.3.3 UCC14130-Q1 Input Voltage Ripple

The UCC14130-Q1 input voltage ripple waveform is shown in the following figure.

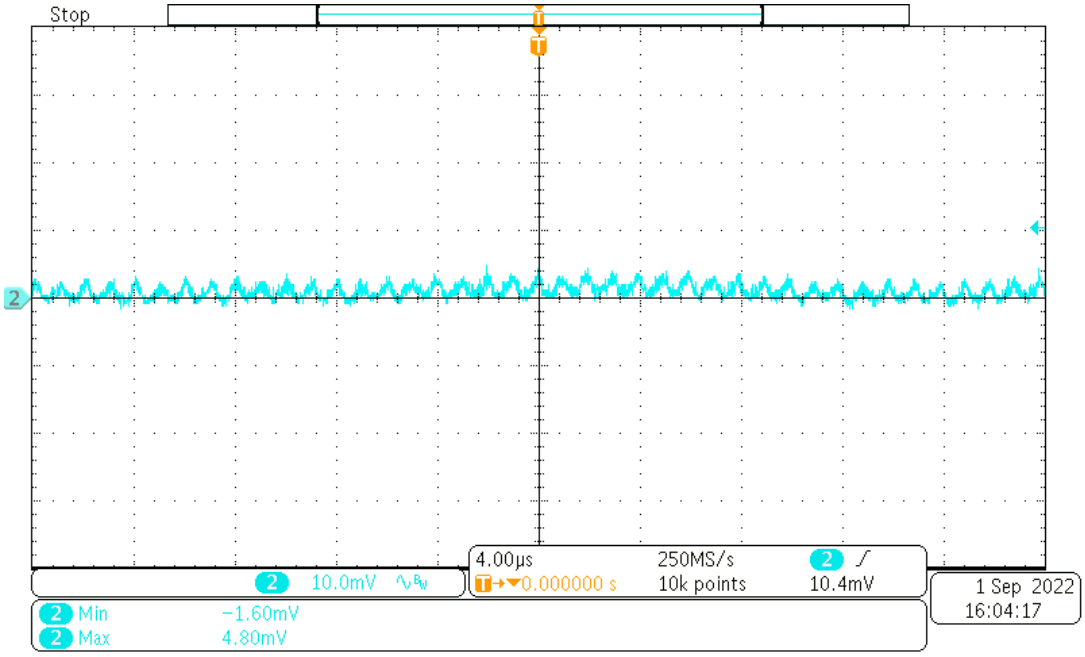


Channel 2: AC coupled Input Voltage Ripple at 15 V_{OUT} and 100mA load current, bandwidth limited (20MHz), [scale: 50mV/div, 40.0µs/div]. The input voltage ripple was measured at input capacitor C33.

Figure 3-11. UCC14130-Q1 Input Voltage Ripple

3.3.4 UCC25800-Q1 Input Voltage Ripple

The UCC25800-Q1 input voltage ripple waveform is shown in the following figure.

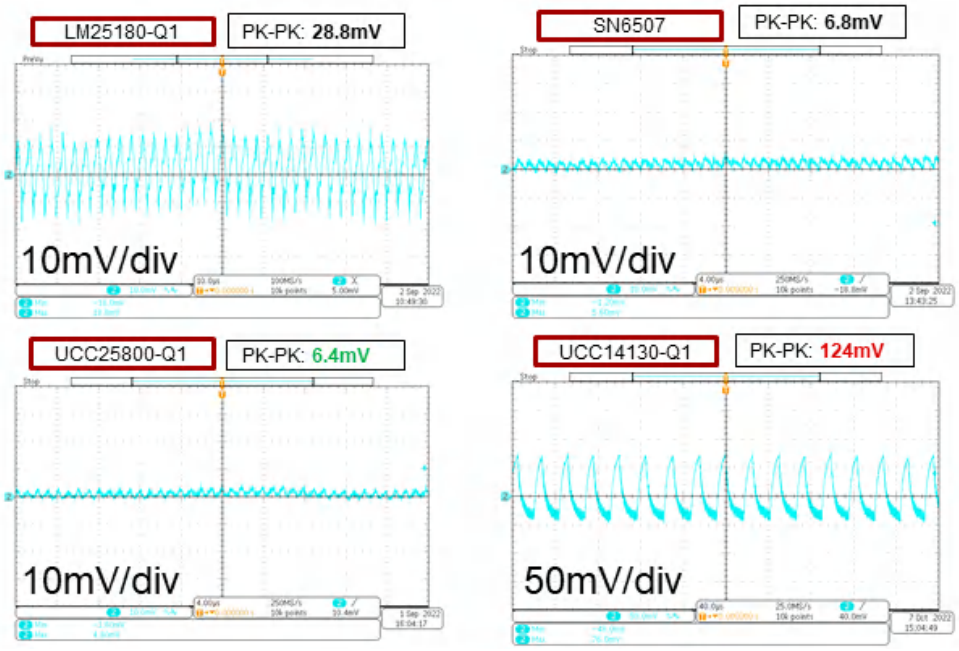


Channel 2: AC coupled input voltage ripple at 15 V_{OUT} and 100mA load current, bandwidth limited (20MHz), [scale: 10mV/div, 4.0µs/div]. The input voltage ripple was measured at input capacitor C61.

Figure 3-12. UCC25800-Q1 Input Voltage Ripple

3.3.5 Input Voltage Ripple Comparison

The following image shows a comparison of input voltage ripple waveforms.



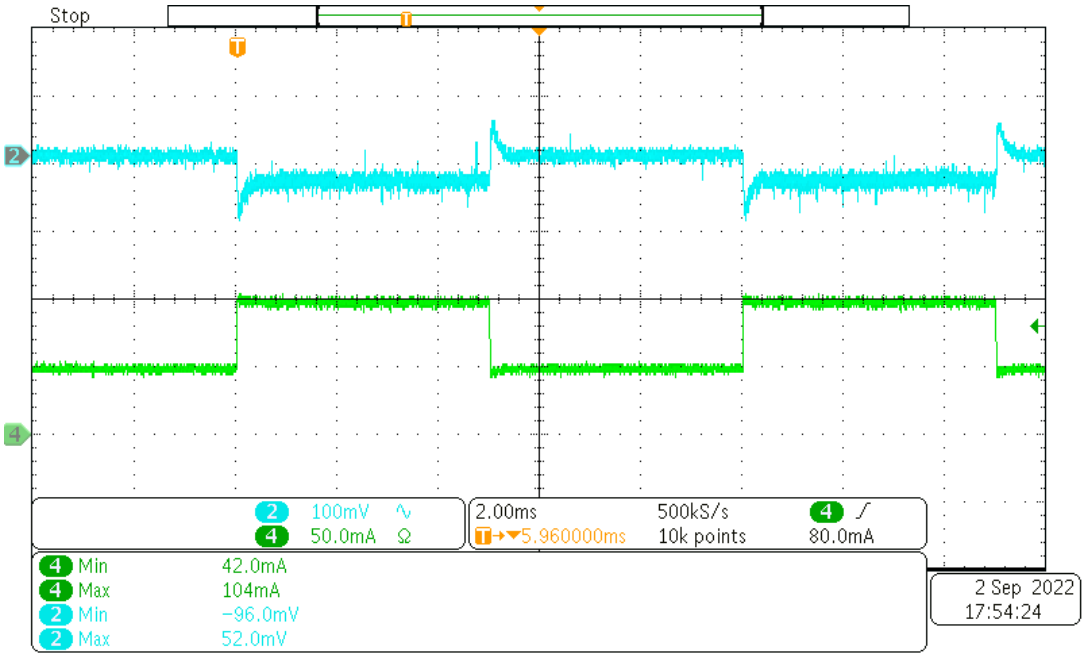
The isolated DCDC module uses an ON-OFF control scheme that results in larger input ripple and output ripple.

Figure 3-13. Input Voltage Ripple Comparison

3.4 Load Transients

3.4.1 LM25180-Q1 Load Transients

LM25180-Q1 load transient waveforms are shown in the following figure.

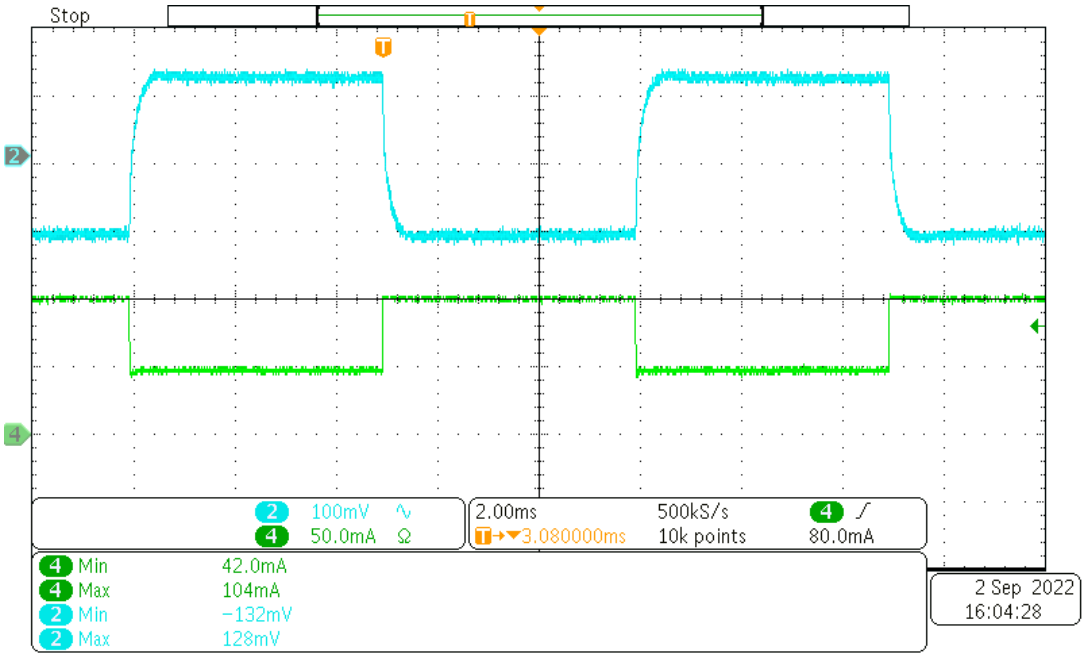


Channel 2: AC-coupled output voltage at 15 V_{OUT}, bandwidth limited (20MHz), [scale: 100mV/div, 2ms/div]
Channel 4: Load transient from 50mA to 100mA and 100mA to 50mA, slew rate 0.25A/µs [scale: 50mA/div, 2ms/div]

Figure 3-14. LM25180-Q1 Load Transient

3.4.2 SN6507-Q1 Load Transients

SN6507-Q1 load transient waveforms are shown in the following figure.

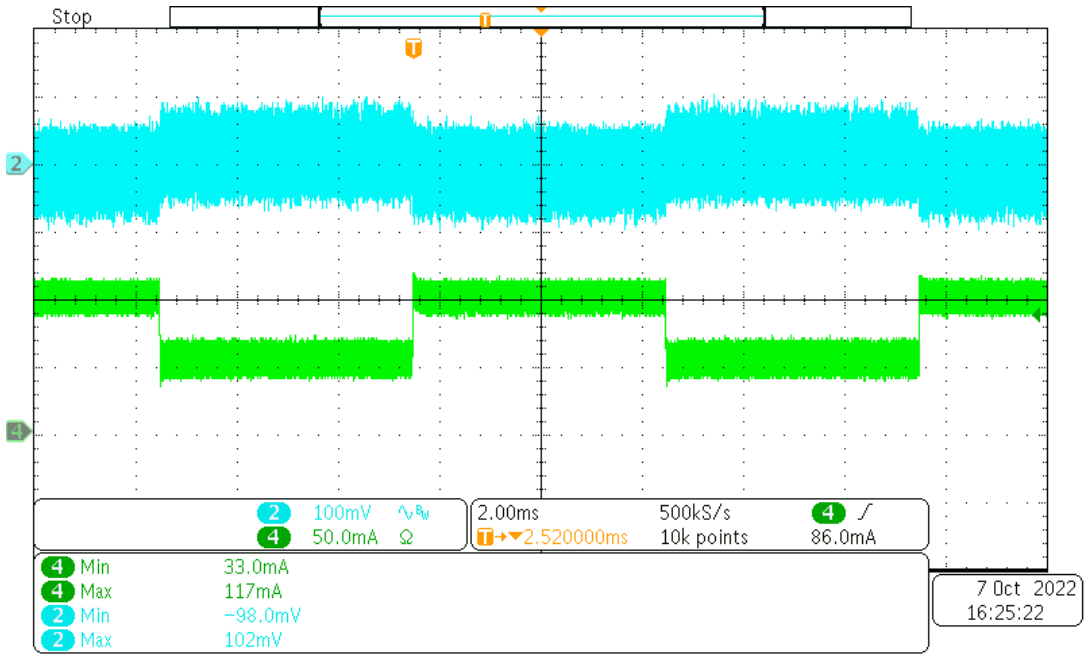


Channel 2: AC-coupled output voltage at 15 V_{OUT}, bandwidth limited (20MHz), [scale: 100mV/div, 2ms/div]
Channel 4: Load transient from 50mA to 100mA and 100mA to 50mA, slew rate 0.25A/µs [scale: 50mA/div, 2ms/div]

Figure 3-15. SN6507-Q1 Load Transient

3.4.3 UCC14130-Q1 Load Transients

UCC14130-Q1 load transient waveforms are shown in the following figure.

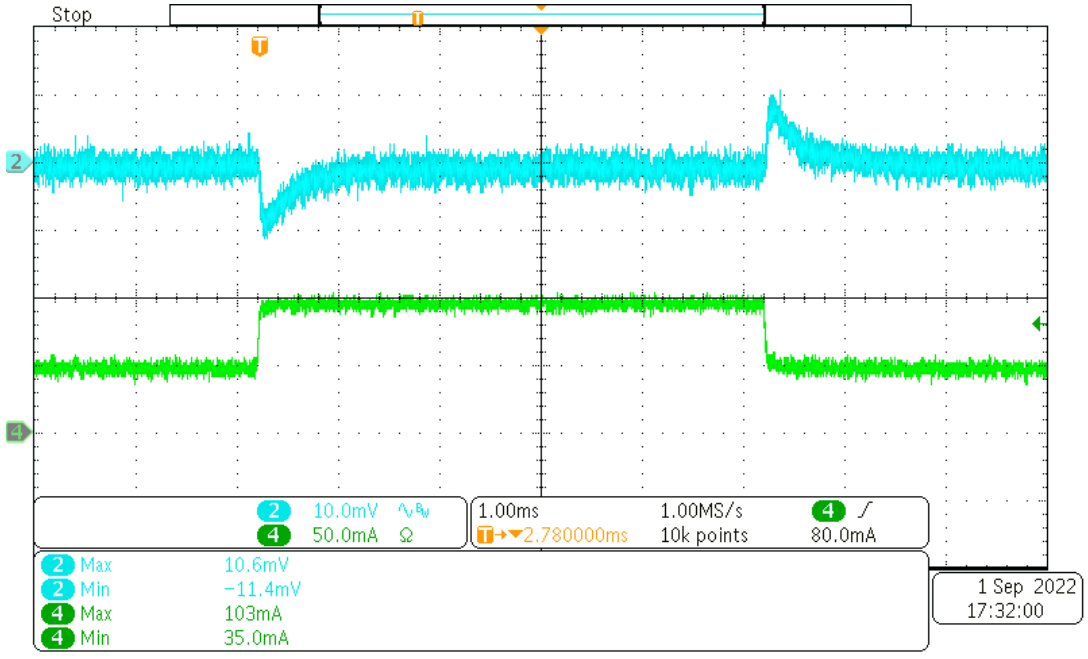


Channel 2: AC-coupled output voltage at 15 V_{OUT}, bandwidth limited (20MHz), [scale: 100mV/div, 2ms/div]
Channel 4: Load transient from 50mA to 100mA and 100mA to 50mA, slew rate 0.25A/µs [scale: 50mA/div, 2ms/div]

Figure 3-16. UCC14130-Q1 Load Transient

3.4.4 UCC25800-Q1 Load Transients

UCC25800-Q1 load transient waveforms are shown in the following figure.



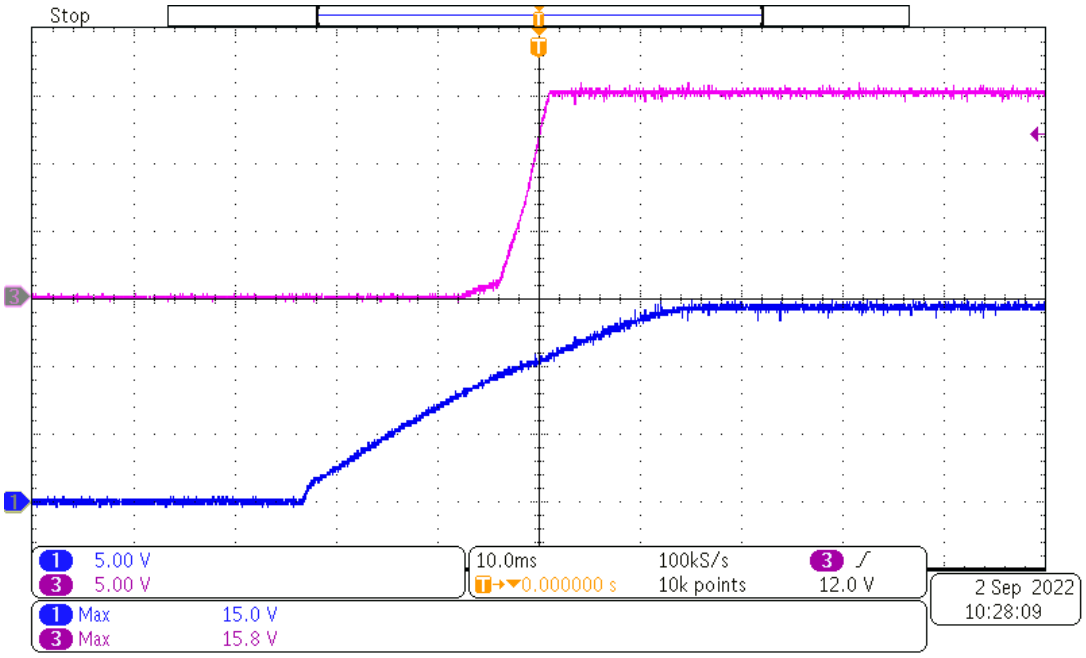
Channel 2: AC-coupled output voltage at 15 V_{OUT}, bandwidth limited (20MHz), [scale: 10mV/div, 1ms/div]
Channel 4: Load transient from 50mA to 100mA and 100mA to 50mA, slew rate 0.25A/µs [scale: 50mA/div, 1ms/div]

Figure 3-17. UCC25800-Q1 Load Transient

3.5 Start-Up Sequence

3.5.1 LM25180-Q1 Start-Up Sequence

LM25180-Q1 start-up sequence waveforms are shown in the following figure.

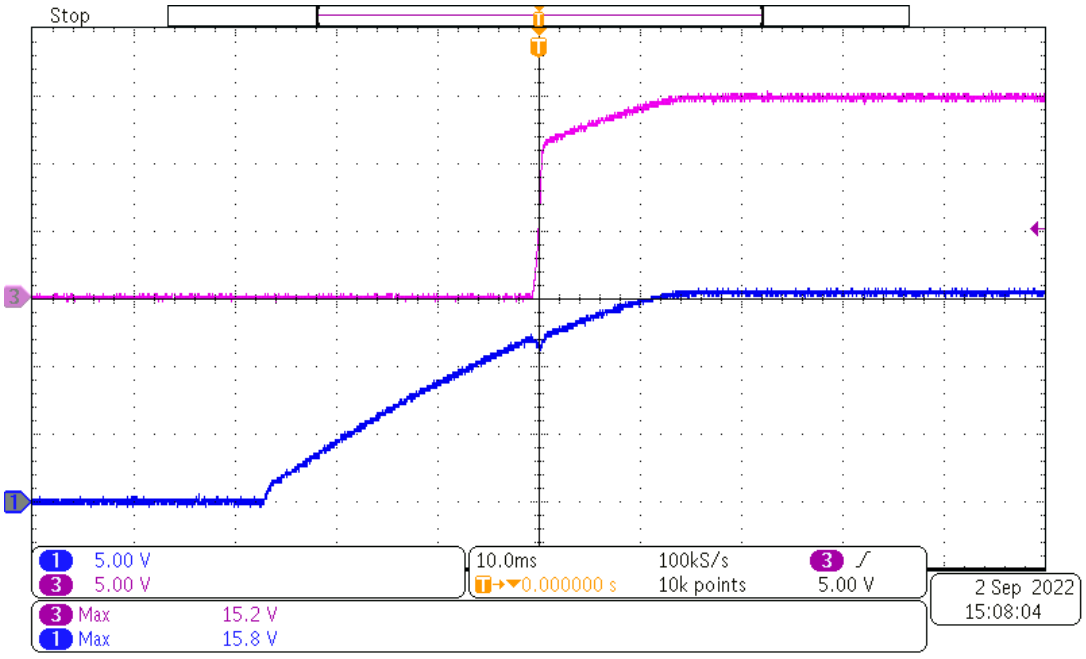


Channel 1: Start-up with input voltage of 15V at full load of 100mA, [scale: 5V/div, 10ms/div]
Channel 3: Output voltage at start-up with 15 V_{OUT} at full load of 100mA, [scale: 5V/div, 10ms/div]

Figure 3-18. LM25180-Q1 Start-Up at Full Load

3.5.2 SN6507 Q1 Start Up Sequence

SN6507 Q1 start up sequence waveforms are shown in the following figure.

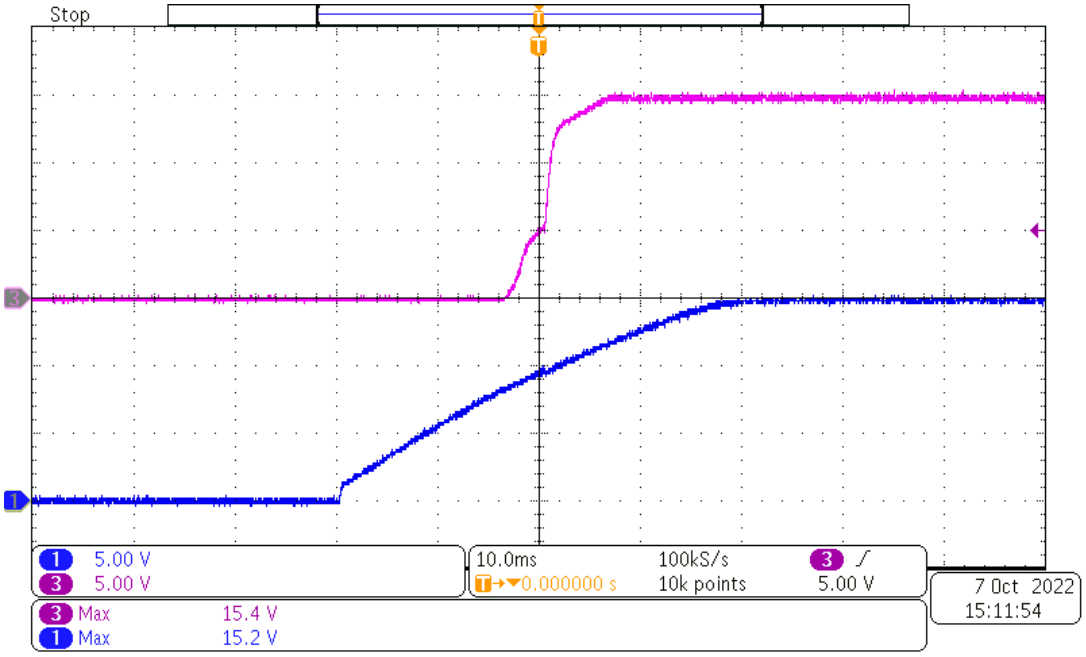


Channel 1: Start-up with input voltage of 15V at full load of 100mA, [scale: 5V/div, 10ms/div]
Channel 3: Output voltage at start-up with 15 V_{OUT} at full load of 100mA, [scale: 5V/div, 10ms/div]

Figure 3-19. SN6507-Q1 Start-Up at Full Load

3.5.3 UCC14130-Q1 Start-Up Sequence

UCC14130-Q1 start-up sequence waveforms are shown in the following figure.

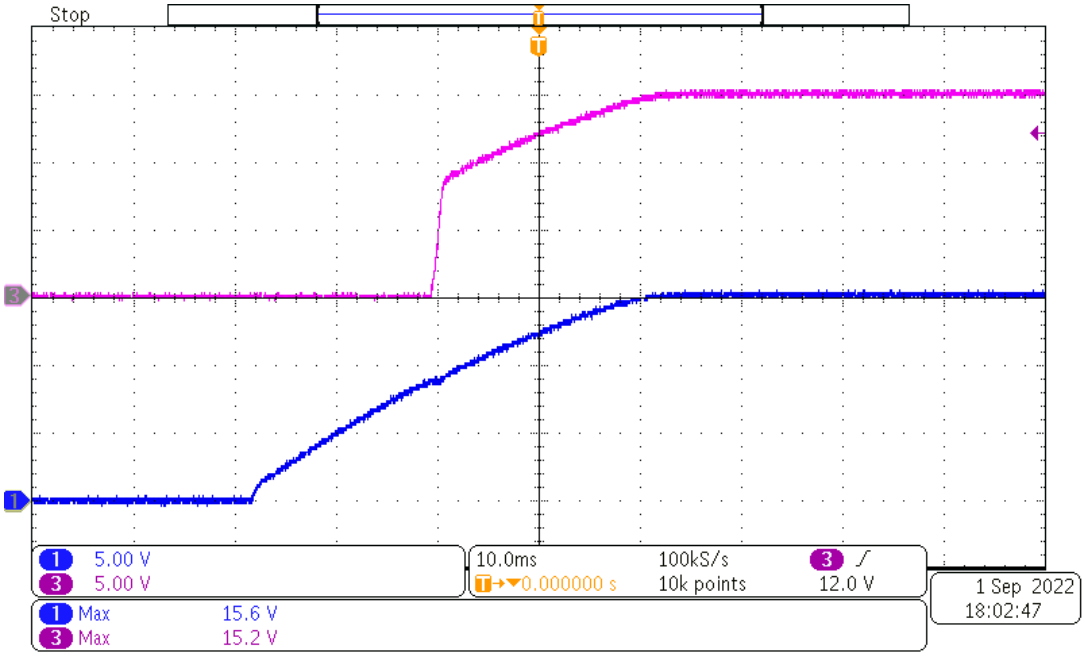


Channel 1: Start-up with input voltage of 15V at full load of 100mA, [scale: 5V/div, 10ms/div]
Channel 3: Output voltage at start up with 15 V_{OUT} at full load of 100mA, [scale: 5V/div, 10ms/div]

Figure 3-20. UCC14130-Q1 Start-Up at Full Load

3.5.4 UCC25800-Q1 Start-Up Sequence

UCC25800-Q1 start-up sequence waveforms are shown in the following figure.



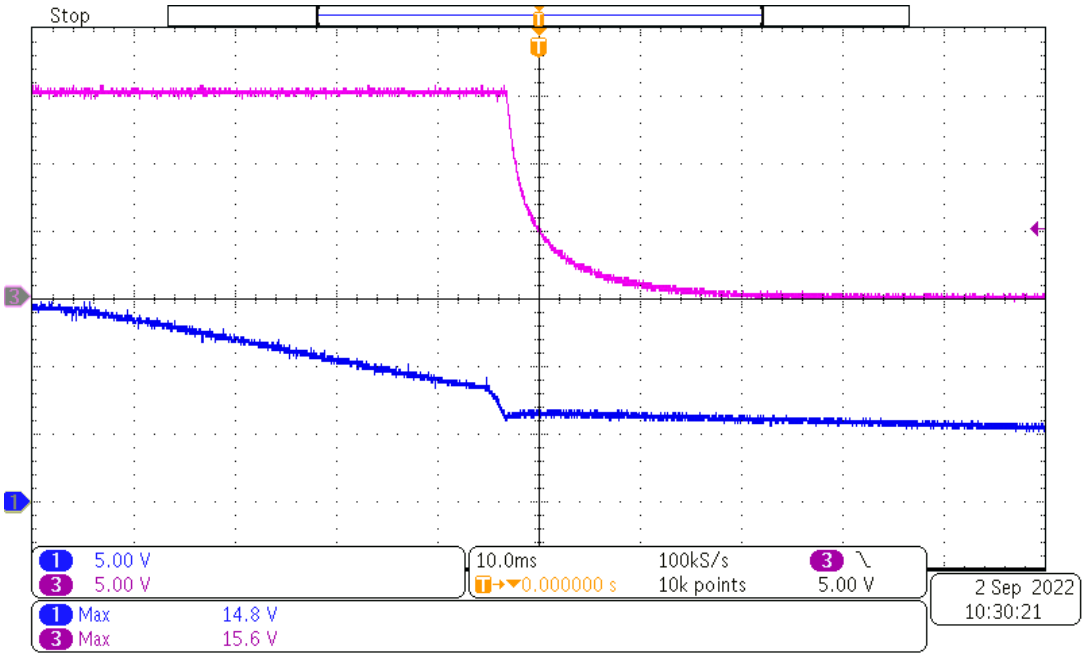
Channel 1: Start-up with input voltage of 15V at full load of 100mA, [scale: 5V/div, 10ms/div]
Channel 3: Output voltage at start-up with 15 V_{OUT} at full load of 100mA, [scale: 5V/div, 10ms/div]

Figure 3-21. UCC25800-Q1 Start-Up at Full Load

3.6 Shutdown Sequence

3.6.1 LM25180-Q1 Shutdown Sequence

LM25180-Q1 shutdown sequence waveforms are shown in the following figure.

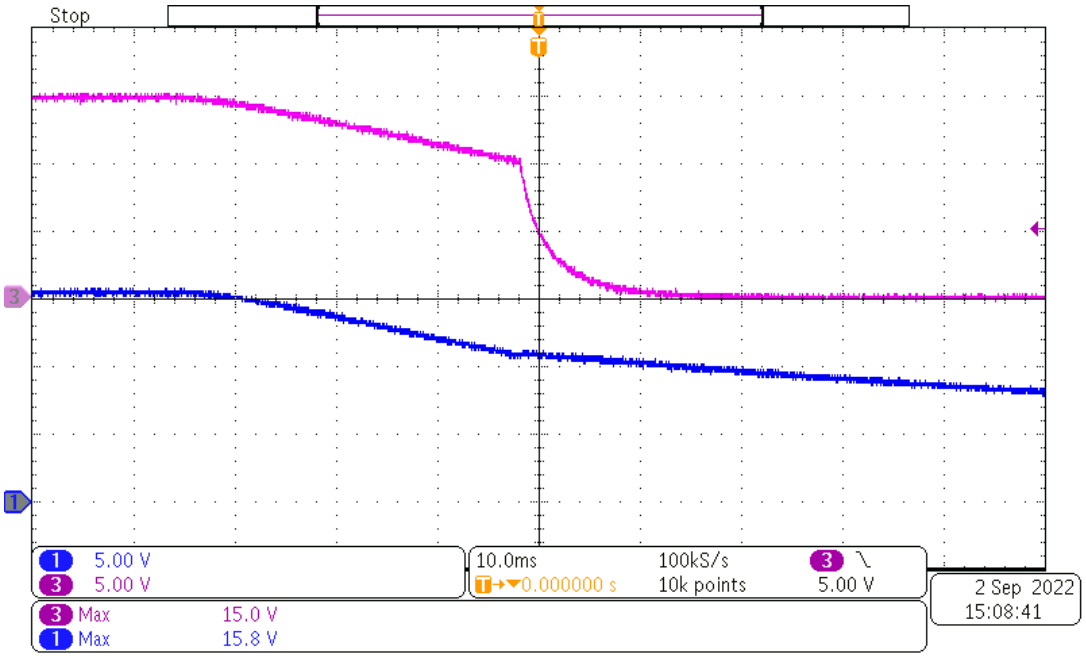


Channel 1: Start-up with input voltage of 15V at full load of 100mA, [scale: 5V/div, 10ms/div]
Channel 3: Output voltage at start-up with 15 V_{OUT} at full load of 100mA, [scale: 5V/div, 10ms/div]

Figure 3-22. LM25180-Q1 Shutoff at Full Load

3.6.2 SN6507-Q1 Shutdown Sequence

SN6507-Q1 shutdown sequence waveforms are shown in the following figure.

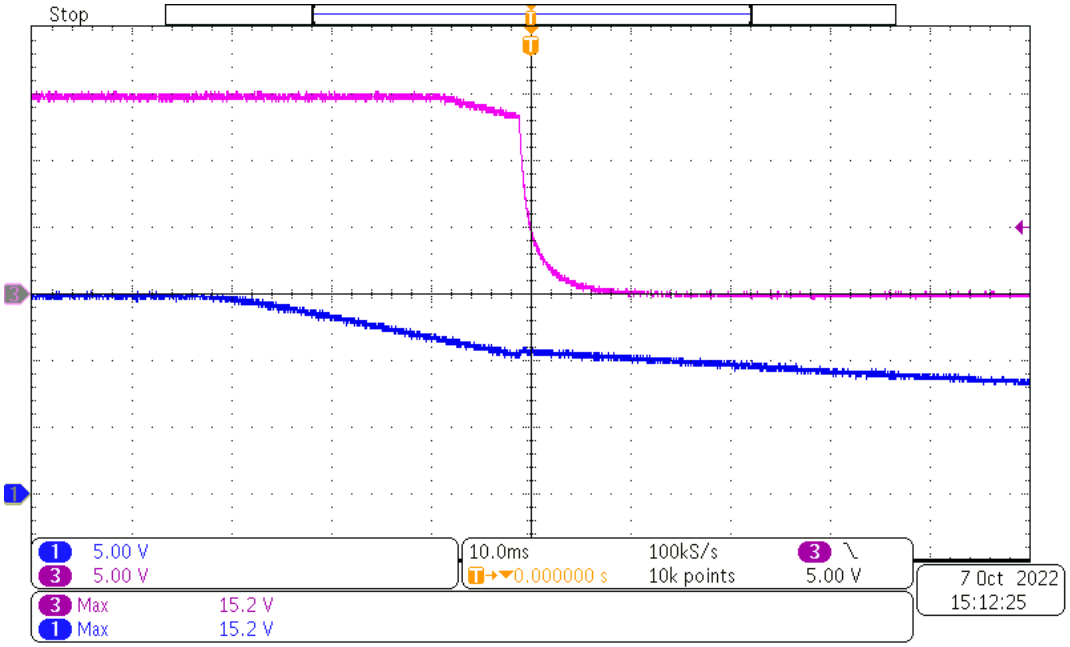


Channel 1: Shutoff with input voltage of 15V at full load of 100mA, [scale: 5V/div, 10ms/div]
Channel 3: Output voltage at shutoff with 15 V_{OUT} at full load of 100mA, [scale: 5V/div, 10ms/div]

Figure 3-23. SN6507-Q1 Shutoff at Full Load

3.6.3 UCC14130-Q1 Shutdown Sequence

UCC14130-Q1 shutdown sequence waveforms are shown in the following figure.

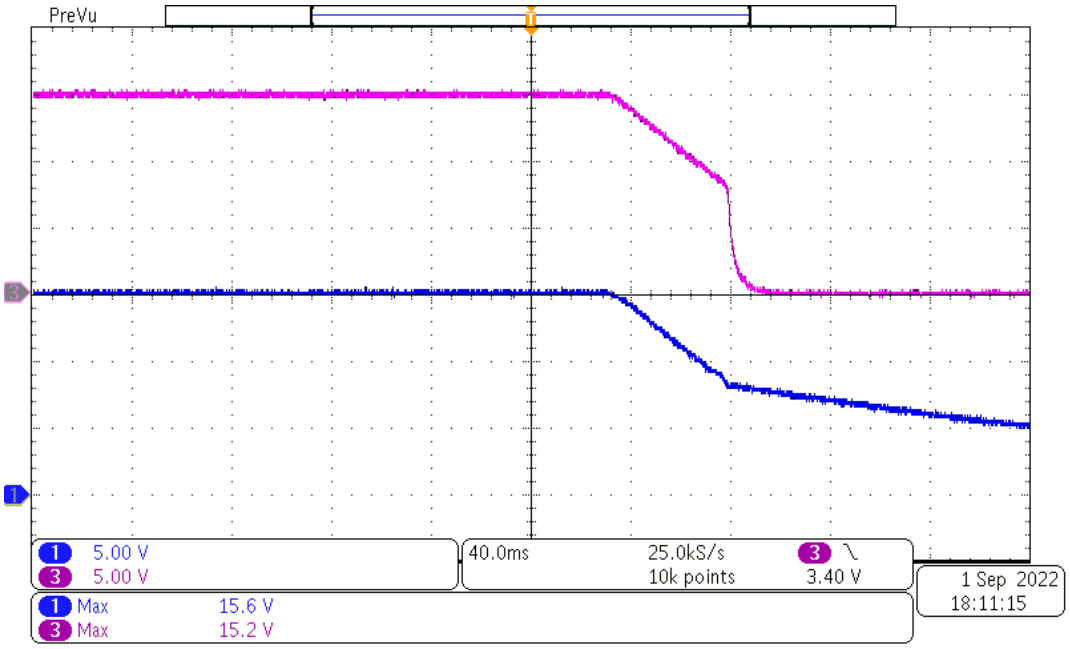


Channel 1: Shutoff with input voltage of 15V at full load of 100mA, [scale: 5V/div, 10ms/div]
Channel 3: Output voltage at shutoff with 15 V_{OUT} at full load of 100mA, [scale: 5V/div, 10ms/div]

Figure 3-24. UCC14130-Q1 Shutoff at Full Load

3.6.4 UCC25800-Q1 Shutdown Sequence

UCC25800-Q1 shutdown sequence waveforms are shown in the following figure.



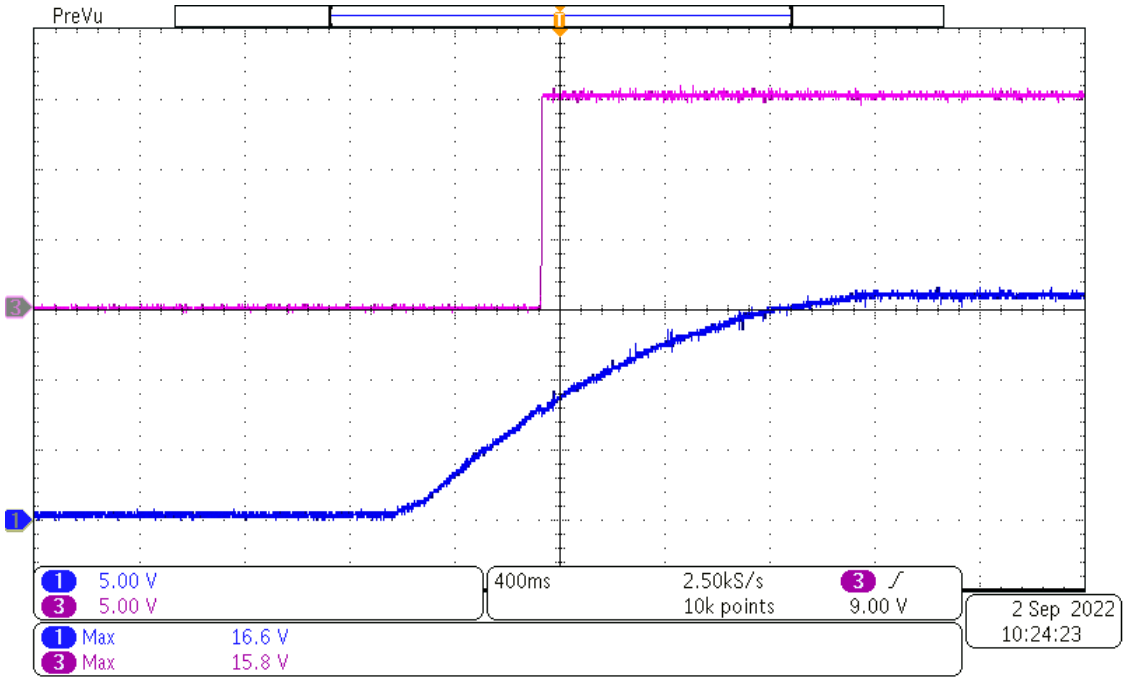
Channel 1: Shutoff with input voltage of 15V at full load of 100mA, [scale: 5V/div, 10ms/div]
Channel 3: Output voltage at shutoff with 15 V_{OUT} at full load of 100mA, [scale: 5V/div, 10ms/div]

Figure 3-25. UCC25800-Q1 Shutoff at Full Load

3.7 Undervoltage Protection

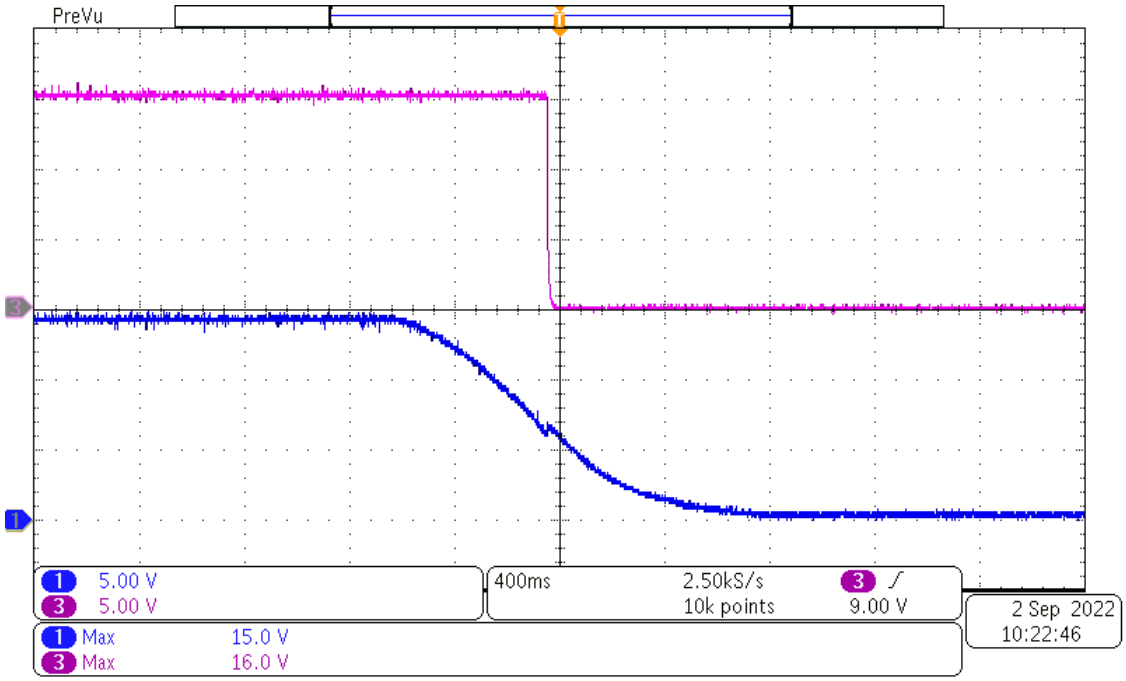
3.7.1 LM25180-Q1 Undervoltage Protection

LM25180-Q1 undervoltage protection waveforms are shown in the following figures.



Channel 1: Input voltage at start-up with UVLO protection at full Load, [scale: 5V/div, 400ms/div]
Channel 3: Output voltage at start-up with UVLO protection at full Load, [scale: 5V/div, 400ms/div]

Figure 3-26. LM25180-Q1 UVLO Protection at Rising Input Voltage

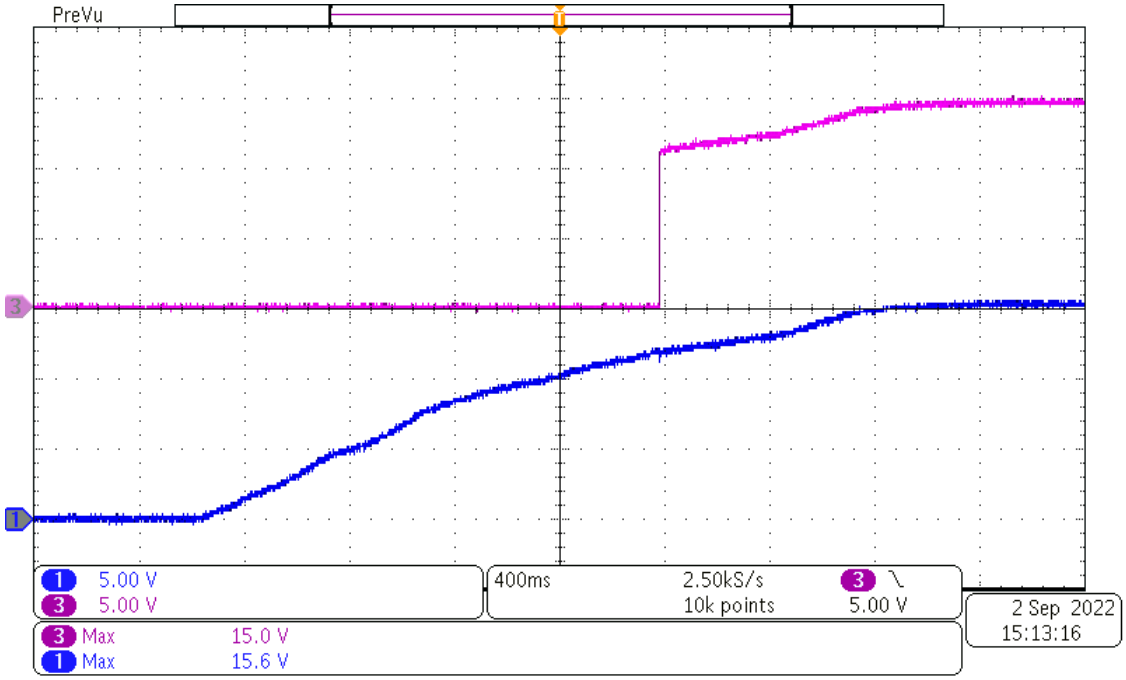


Channel 1: Input voltage at shutoff with UVLO protection at full Load, [scale: 5V/div, 400ms/div]
Channel 3: Output voltage at shutoff with UVLO protection at full Load, [scale: 5V/div, 400ms/div]

Figure 3-27. LM25180-Q1 UVLO Protection at Falling Input Voltage

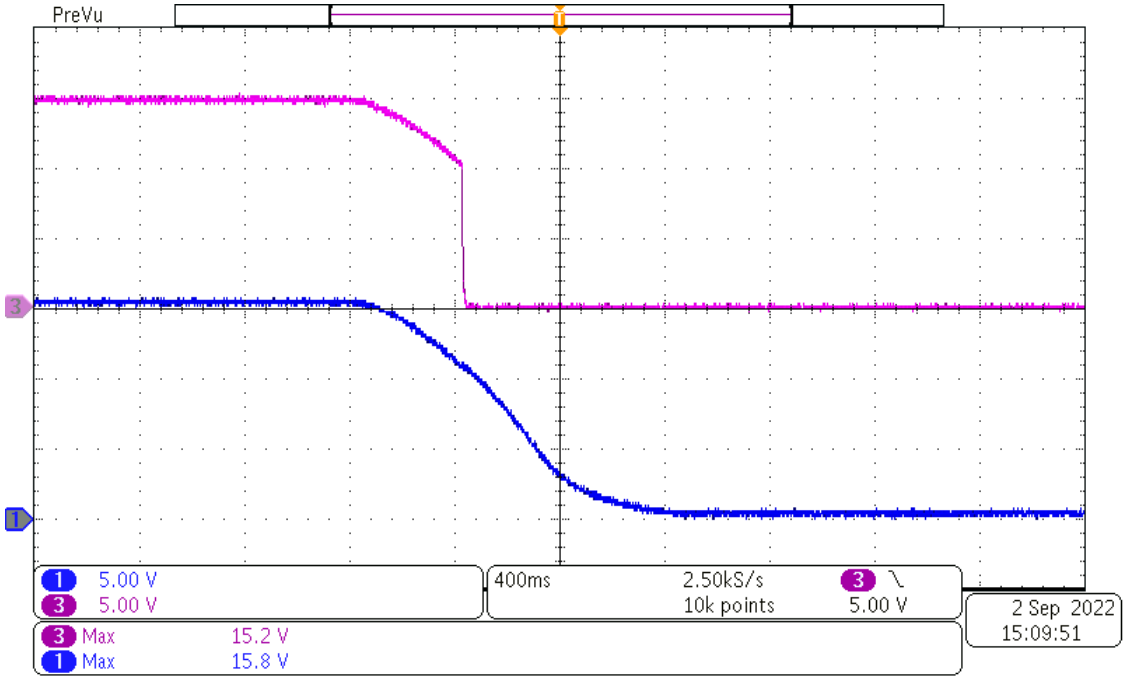
3.7.2 SN6507-Q1 Undervoltage Protection

SN6507-Q1 undervoltage protection waveforms are shown in the following figures.



Channel 1: Input voltage at start-up with UVLO protection at full load, [scale: 5V/div, 400ms/div]
Channel 3: Output voltage at start-up with UVLO protection at full load, [scale: 5V/div, 400ms/div]

Figure 3-28. SN6507-Q1 UVLO Protection at Rising Input Voltage

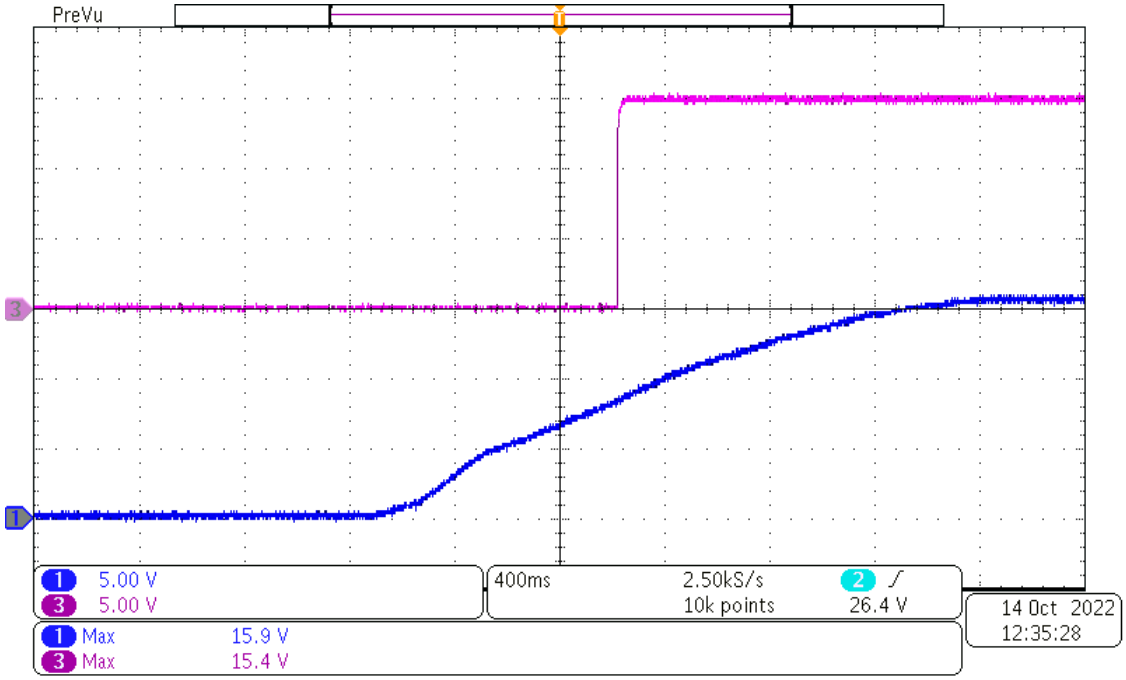


Channel 1: Input voltage at shutoff with UVLO protection at full load, [scale: 5V/div, 400ms/div]
Channel 3: Output voltage at shutoff with UVLO protection at full load, [scale: 5V/div, 400ms/div]

Figure 3-29. SN6507-Q1 UVLO Protection at Falling Input Voltage

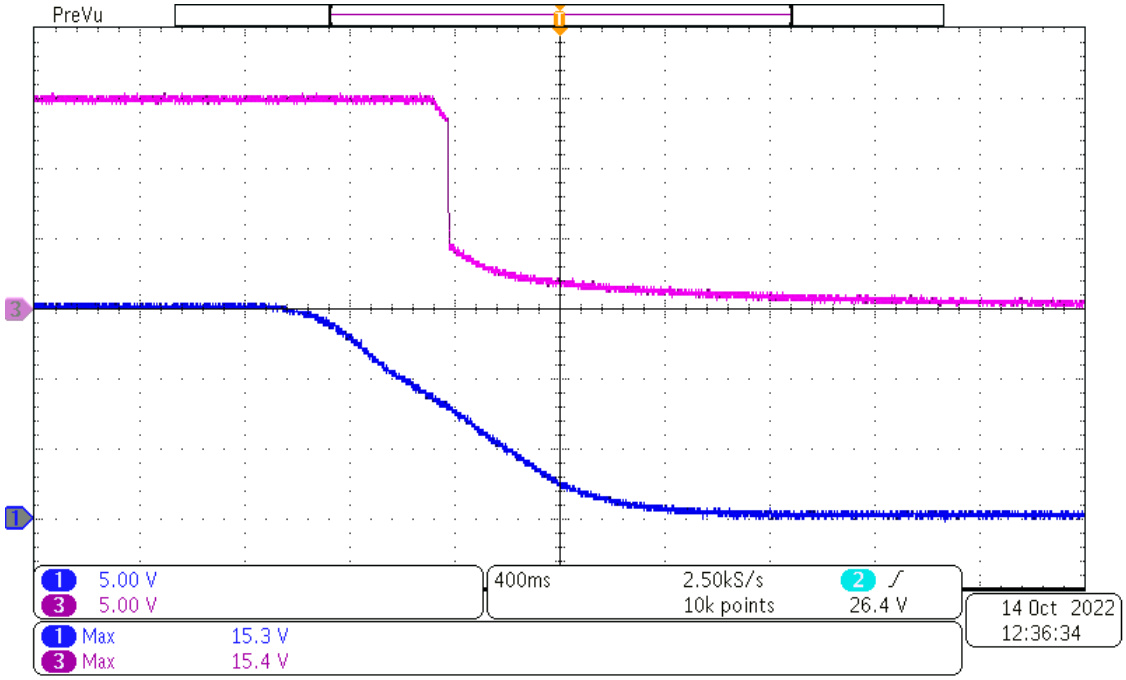
3.7.3 UCC14130-Q1 Undervoltage Protection

UCC14130-Q1 undervoltage protection waveforms are shown in the following figures.



Channel 1: Input voltage at start-up with UVLO protection at no load, [scale: 5V/div, 400ms/div]
Channel 3: Output voltage at start-up with UVLO protection at no load, [scale: 5V/div, 400ms/div]

Figure 3-30. UCC14130-Q1 UVLO Protection at Rising Input Voltage

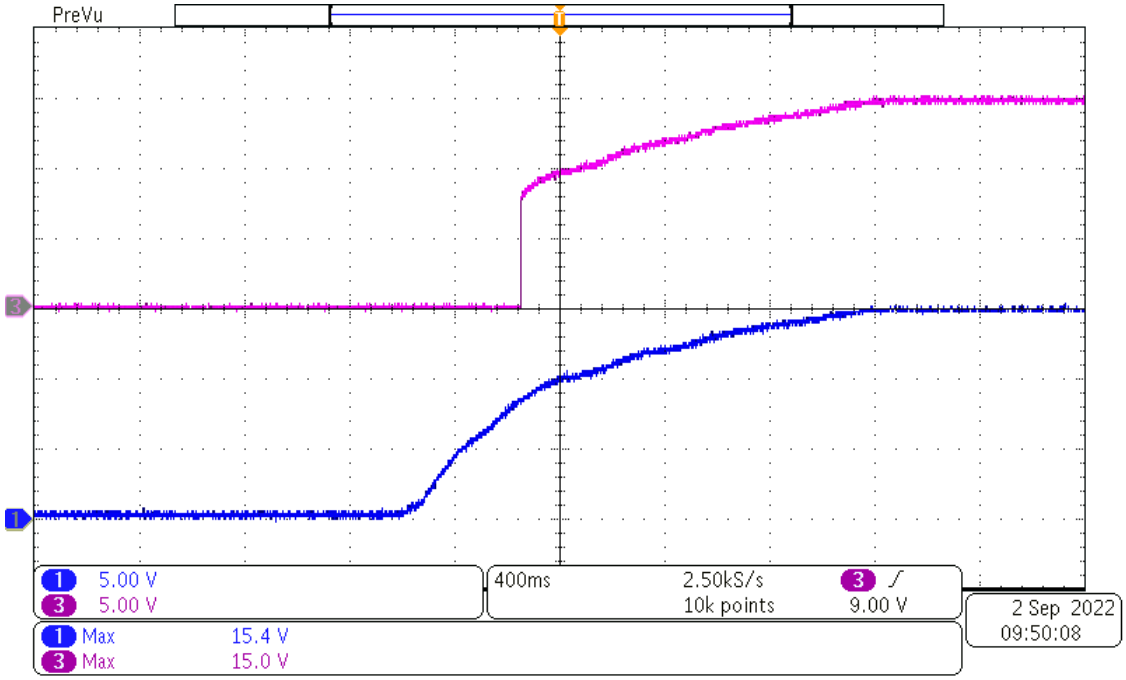


Channel 1: Input voltage at shutoff with UVLO protection at no load, [scale: 5V/div, 400ms/div]
Channel 3: Output voltage at shutoff with UVLO protection at no load, [scale: 5V/div, 400ms/div]

Figure 3-31. UCC14130-Q1 UVLO Protection at Falling Input Voltage

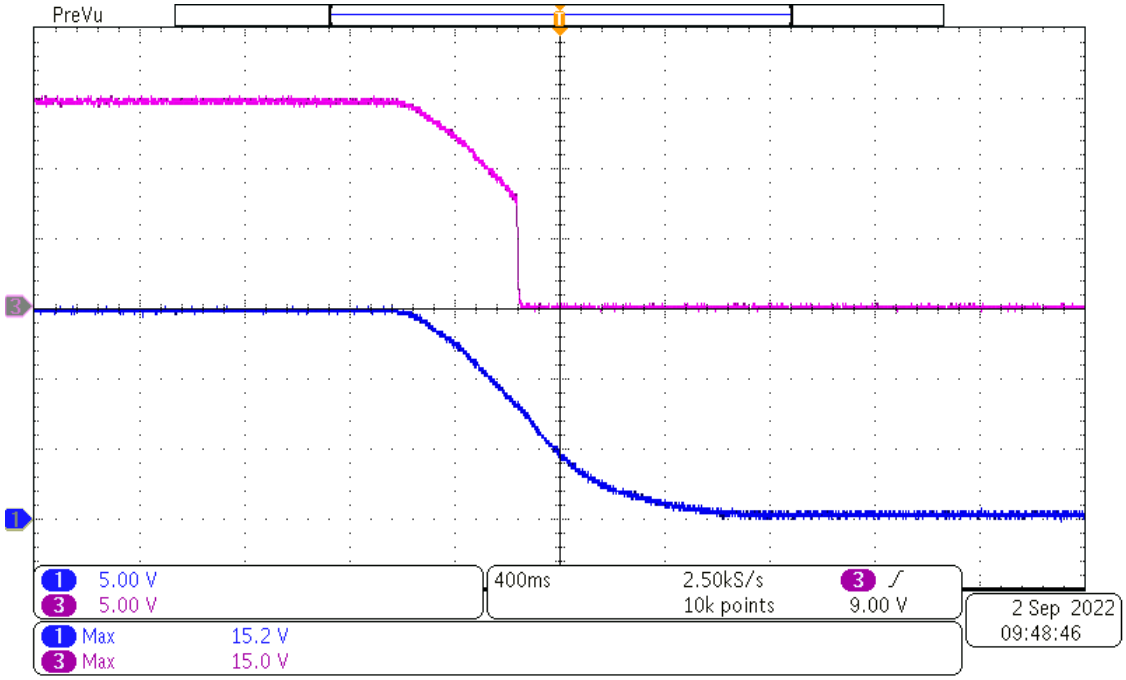
3.7.4 UCC25800-Q1 Undervoltage Protection

UCC25800-Q1 undervoltage protection waveforms are shown in the following figures.



Channel 1: Input voltage at start-up with UVLO protection at full load, [scale: 5V/div, 400ms/div]
Channel 3: Output voltage at start-up with UVLO protection at full load, [scale: 5V/div, 400ms/div]

Figure 3-32. UCC25800-Q1 UVLO Protection at Rising Input Voltage



Channel 1: Input voltage at shutoff with UVLO protection at full load, [scale: 5V/div, 400ms/div]
Channel 3: Output voltage at shutoff with UVLO protection at full load, [scale: 5V/div, 400ms/div]

Figure 3-33. UCC25800-Q1 UVLO Protection at Falling Input Voltage

4 Summary

Table 4-1 lists a summary of benefits and trade-offs by topology.

Table 4-1. Topology Summary of Benefits and Trade-Offs

Topology	Devices	Benefits	Trade-offs
Push-Pull Transformer Driver	SN6507-Q1	• Wide V**in** range • Low EMI • Power range up to 7.5W(1) • Good line regulation by duty control	• Low to moderate efficiency, especially in case of low output current (<50 mA) • Moderate load regulation accuracy
LLC Transformer Driver, Half-bridge Resonant Converter	UCC25800-Q1	• High efficiency • Power range up to 9W(1) • Low CM current • Low EMI	• Low load regulation accuracy • Requirement of pre-regulator and/or post-regulator • Large Transformer size, especially in low switching frequency range
PSR Flyback DCDC Converter	LM25180-Q1	• Wide V**in** range • High efficiency • Power range up to 15W(1) • High load & line regulation accuracy	• High EMI • High CMI current
Integrated Transformer, Magneto-MV, Isolated DCDC Module	UCC14130-Q1	• No need of external transformer • Robustness to vibration • Small size including low height • High load regulation accuracy • Low CM current	• High EMI • Low efficiency • Requirement of Pre-regulator(2)

(1) Depends on design parameters and variant of the device.
(2) Depends on the variant of the device.

5 References

1. Texas Instruments, LMG3522EVM-042 Tool Folder
2. Texas Instruments, LM25180-Q1 Product Folder
3. Texas Instruments, SN6507-Q1 Product Folder
4. Texas Instruments, UCC14130-Q1 Product Folder
5. Texas Instruments, UCC25800-Q1 Product Folder

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