Test Report: PMP41145

Universal AC Input 65W 20V, 3.25A Flyback With Integrated GaN Reference Design

Description

This reference design is a 65W, 20V fixed output voltage AC-DC power supply design with integrated flyback and Gallium nitride (GaN). This design can deliver 65W full rated power across 90VAC to 264VAC and achieve 93% efficiency at 90VAC. The design can meet efficiency standards and regulations such as DoE Level VII and CoC V5 Tier 2 efficiency standard for average efficiency across 25%, 50%, 75%, 100% and standby power consumption. The design can achieve 2.3W per cubic centimeters and eliminate auxiliary winding as well as associated VCC rectifier circuity. The design can also support a 100W peak power capability for 4ms.

Features

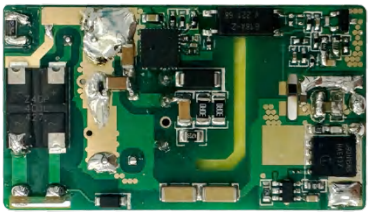
- Achieve 93% efficiency at 90VAC
- 2.3W per cubic centimeter. Power density based on PCB size
- Meet DoE Level VII and CoC V5 Tier 2 efficiency standards
- No load power consumption 18mW at 115VAC, 28mW at 230VAC
- Provide 100W peak power capability

Applications

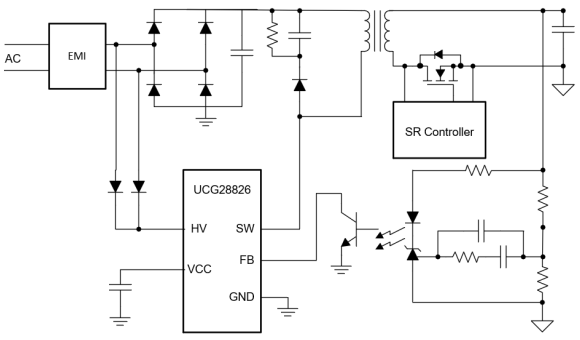
- Industrial AC-DC
- USB AC/DC adapter
- USB wall power outlet
- Battery charger

Top view

Angle view



Bottom View



Block Diagram

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1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1-1. Voltage and Current Requirements

PARAMETER	SPECIFICATIONS
Input voltage range	90VAC to 264VAC
Output voltage	20VDC
Output current	3.25A
Rated Power	65W
Peak Power	100W, 4ms

1.2 Required Equipment

- AC Source: Chroma Model 61601
- Digital Power Meter: Yokogawa WT310
- Power-Z P240 Bidirectional Multi-protocol Power Supply
- DC source: GWinstek, GPS-3303C
- Bidirectional Power Source: IT6010C-80-300
- Electronic load: Chroma, 6314A
- Oscilloscope: Tektronix, DPO 3054
- Infrared Thermal Camera: Fluke, TiS55
- Ture-RMS-Multimeter: Fluke, 287C

1.3 Dimensions

PCB board size: 27mm × 48mm × 22mm (open frame)

2 Testing and Results

2.1 Efficiency Graphs

Efficiency is shown in Figure 2-1 through Figure 2-3.

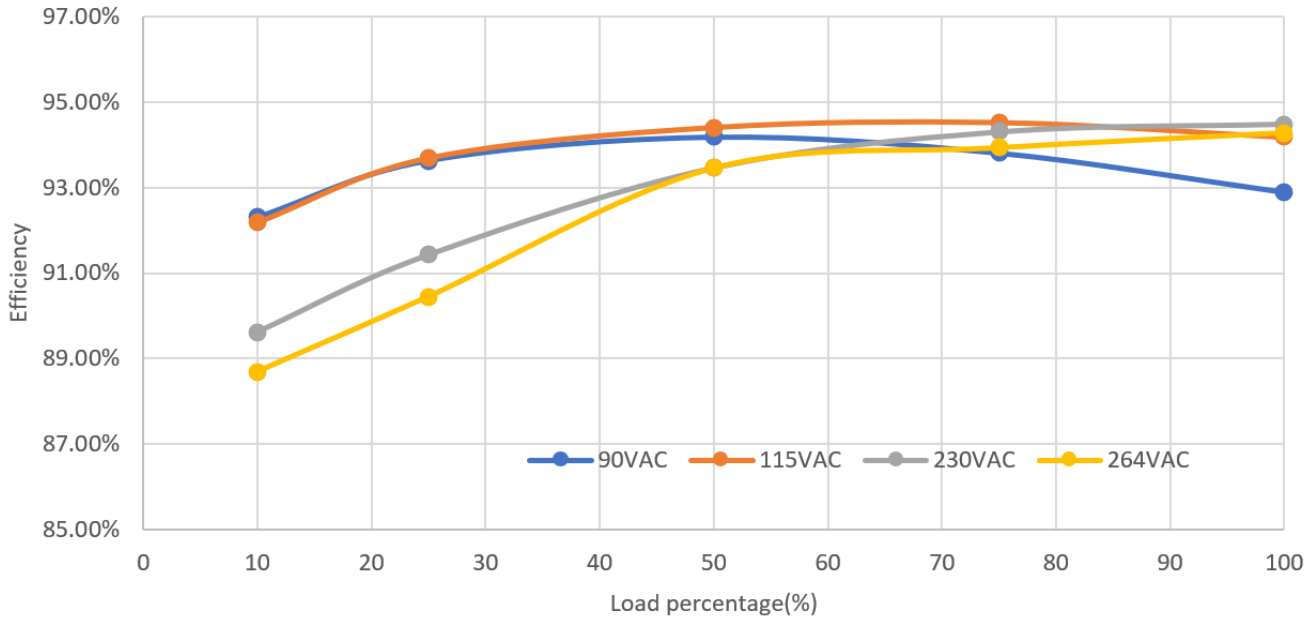

Figure 2-1. Efficiency Versus AC Input and Load

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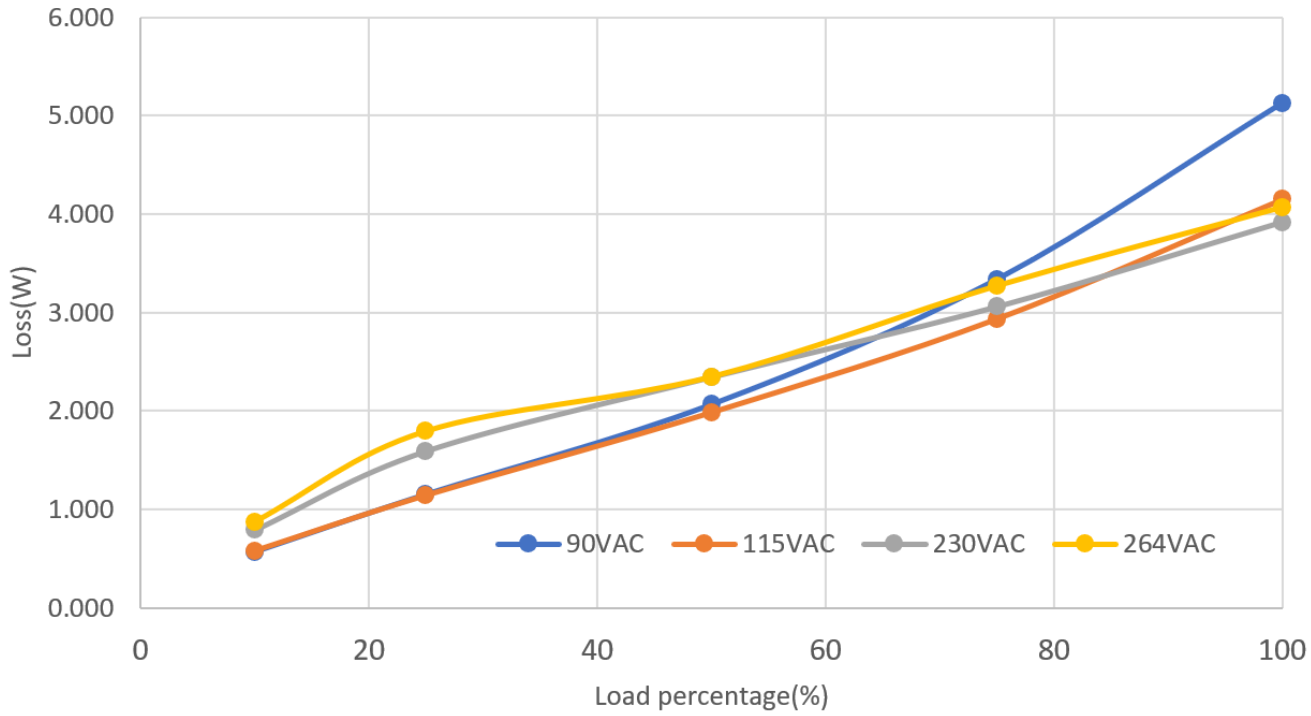

Figure 2-2. Power Loss Versus AC Input and Load

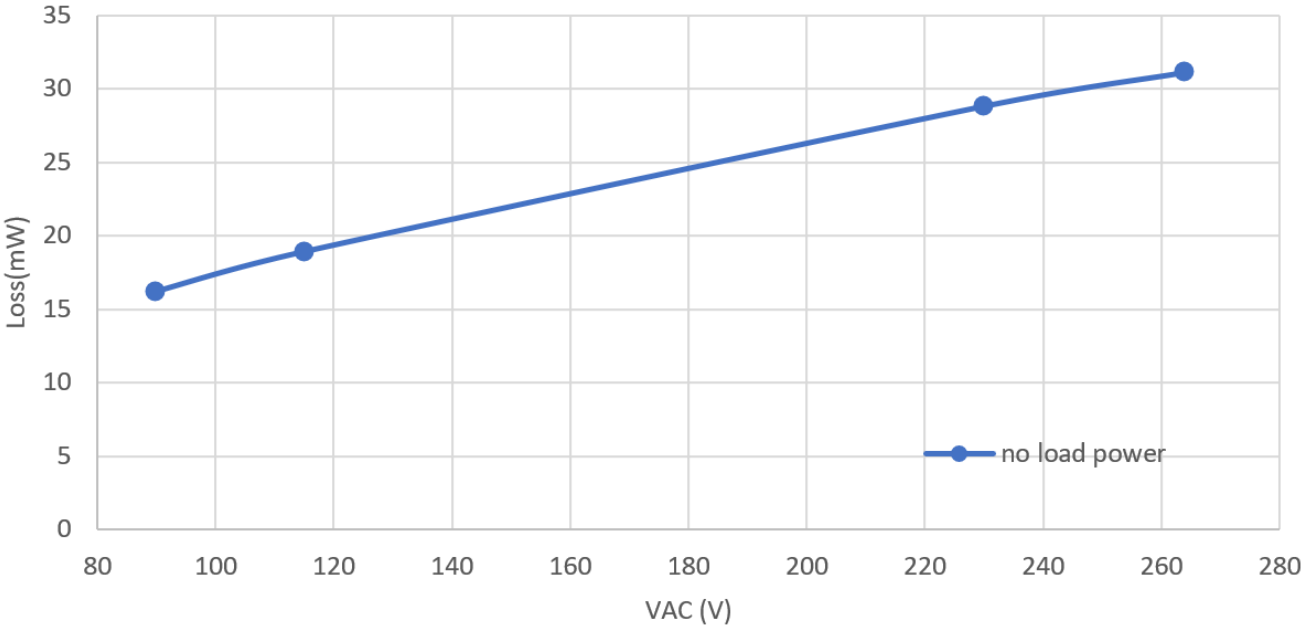

Figure 2-3. No Load Input Power Consumption Versus AC Input Voltage

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2.2 Voltage Regulation

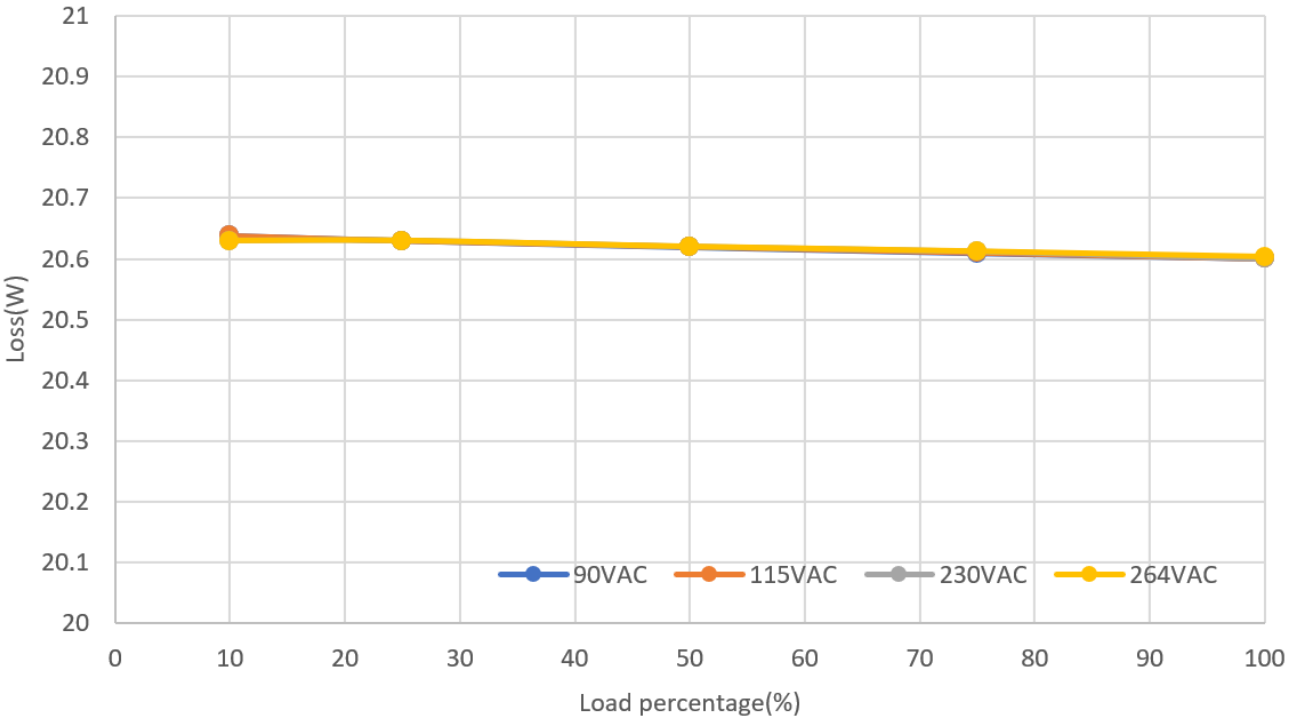

Figure 2-4. V_{out} Voltage Regulation Versus AC Input and Load

2.3 Efficiency Data

Efficiency data is shown in Table 2-1.

Table 2-1. Efficiency Data

VAC $_{IN}$(V)	P $_{IN}$(A)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	P_{LOSS} (W)	P_{OUT} (%)	Efficiency (%)	Average Efficiency at Four Point (%)
90	72.18	20.61	3.255	67.053	5.127	100	92.9	93.63
90	53.91	20.609	2.454	50.574	3.336	75	93.81	
90	35.53	20.619	1.623	33.465	2.065	50	94.19	
90	18.11	20.63	0.822	16.958	1.152	25	93.64	
90	7.4	20.638	0.331	6.831	0.569	10	92.31	
115	71.2	20.61	3.255	67.053	4.147	100	94.81	94.20
115	53.51	20.61	2.454	50.577	2.933	75	94.52	
115	35.45	20.62	1.623	33.466	1.984	50	94.40	
115	18.1	20.63	0.822	16.958	1.142	25	93.69	
115	7.41	20.638	0.331	6.831	0.579	10	92.19	
230	70.97	20.61	3.255	67.053	3.917	100	94.48	93.41
230	53.64	20.612	2.454	50.582	3.058	75	94.3	
230	35.81	20.62	1.623	33.466	2.344	50	93.46	
230	18.55	20.63	0.822	16.958	1.592	25	91.42	
230	7.62	20.63	0.331	6.829	0.791	10	89.61	

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Table 2-1. Efficiency Data (continued)

VAC_{IN}(V)	P_{IN}(A)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	P_{LOSS} (W)	P_{OUT} (%)	Efficiency (%)	Average Efficiency at Four Point (%)
264	71.13	20.603	3.255	67.063	4.067	100	94.28	93.03
264	53.85	20.612	2.454	50.582	3.268	75	93.93	
264	35.81	20.62	1.623	33.466	2.344	50	93.46	
264	18.75	20.63	0.822	16.958	1.792	25	90.44	
264	7.7	20.63	0.331	6.829	0.871	10	88.68	

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2.4 Thermal Images

Thermal image is shown in Figure 2-5 through Figure 2-8.

Table 2-2. Thermal Test Result

Parts	90VAC	115VAC	230VAC	264VAC	
	Temperature(ºC)	Temperature(ºC)	Temperature(ºC)	Temperature(ºC)	Room temperature(ºC)
AC Bridge	105	90	75	73	25
UCG28826	84	76	79	83	25
Transformer	75	75	76	77	25
SR MOSFET	68	66	67	66	25
RCD Snubber	91	83	80	79	25

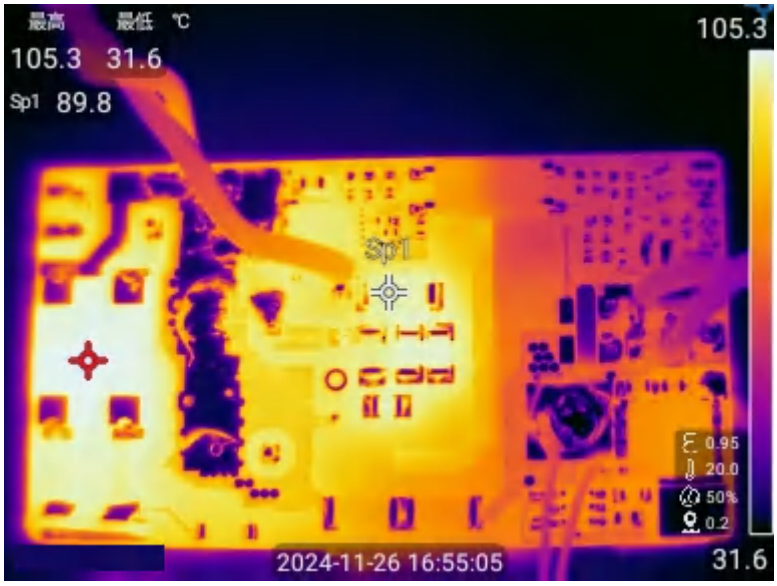

Figure 2-5. Thermal, 90VAC, Full Load

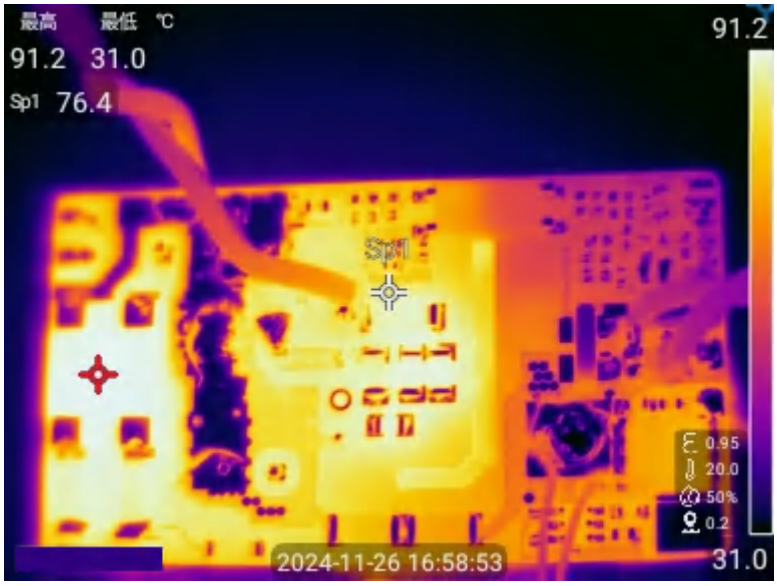

Figure 2-6. Thermal, 115VAC, Full Load

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Figure 2-7. Thermal, 230VAC, Full Load

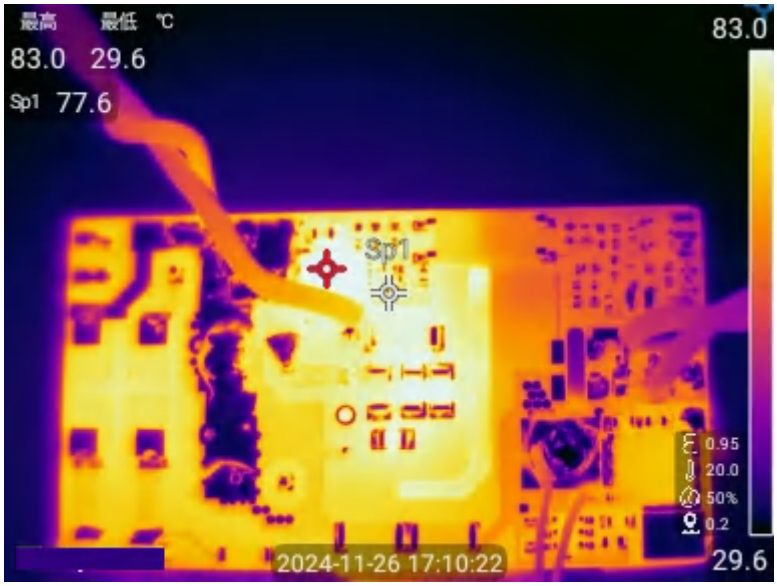

Figure 2-8. Thermal, 264VAC, Full Load

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2.5 EMI

EMI is shown in Figure 2-9 through Figure 2-12.

EMI TEST REPORT

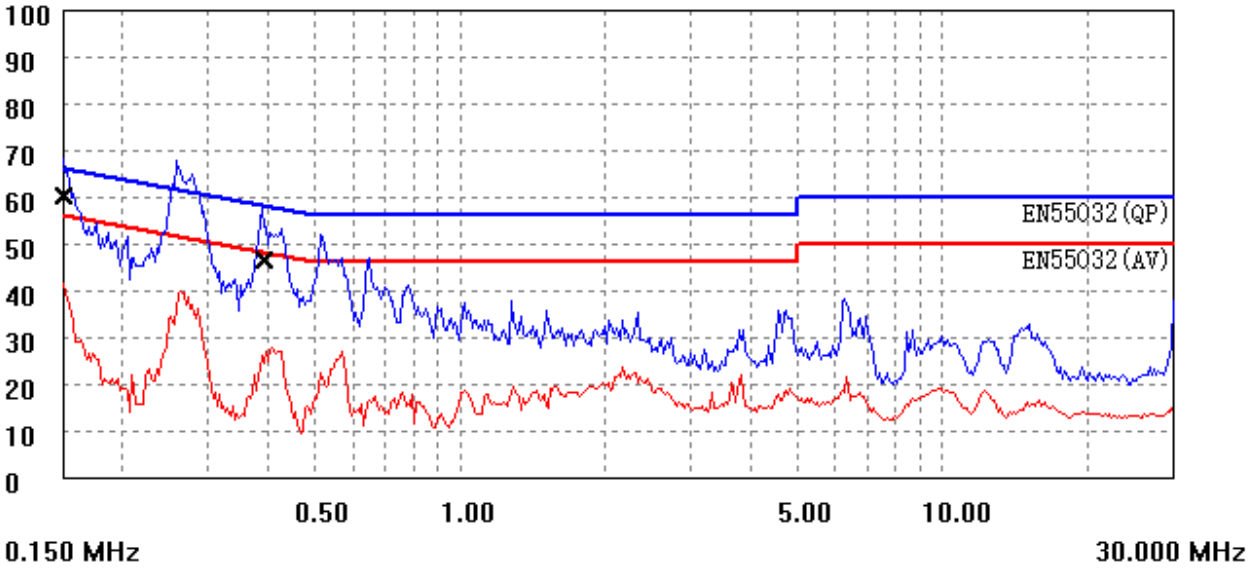
parameter

Organization:		Operator:		EUT:	
Place:		Time:	2024/12/4/12:58	Test equipment:	KH3932
Detector:	PK+AV	Test-time(ms):	30	SN:	320684
Limit:	EN55032	Transductor(PK/AV):	PK / AV	JZ:	2,15,1031
Remark:					

freq, step

Start(MHz)	End(MHz)	Step(MHz)
0.150	2.000	0.002
2.000	10.000	0.010
10.000	30.000	0.025

scan result



final test

[QP]	freq(MHz)	lev(dBuV)	Lim(dBuV)	Δ(lev-Lim)
	0.150	60.4	66.0	-5.6
	0.391	46.5	59.1	-12.6

Figure 2-9. 115VAC, Full Load, Resistive Load, Unearthed, L phase

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EMI TEST REPORT

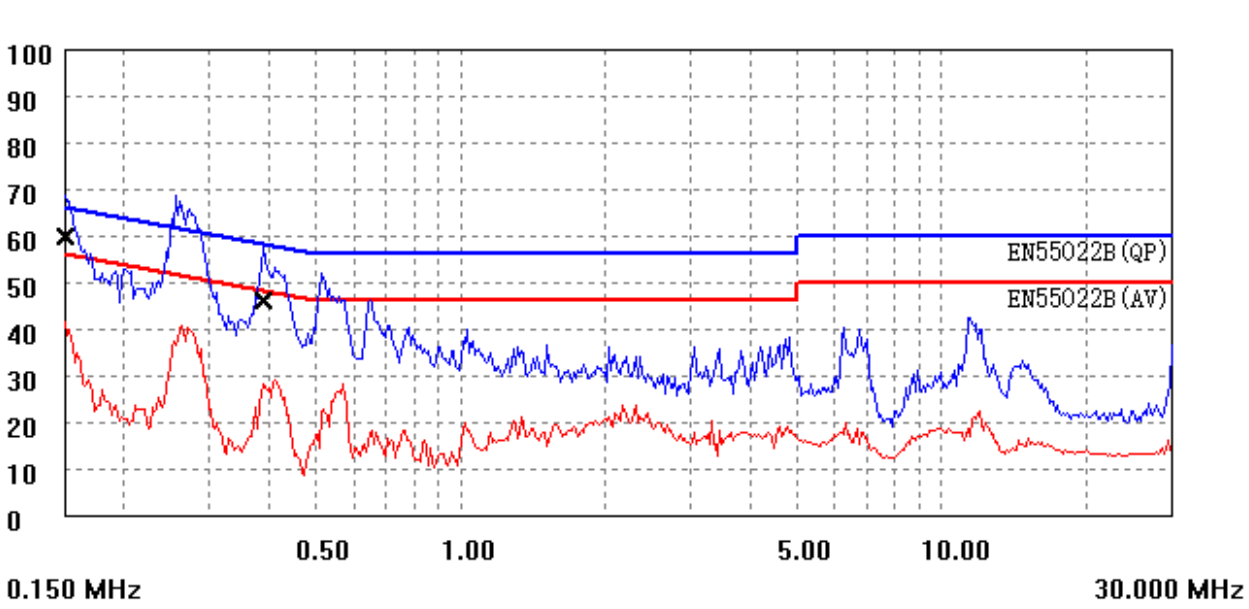
parameter

Organization:		Operator:		EUT:	
Place:		Time:	2024/12/4/14:23	Test equipment:	KH3932
Detector:	PK+AV	Test-time(ms):	30	SN:	320684
Limit:	EN55022B	Transductor(PK/AV):	PK / AV	JZ:	2,15,1039
Remark:					

freq, step

Start(MHz)	End(MHz)	Step(MHz)
0.150	2.000	0.002
2.000	10.000	0.010
10.000	30.000	0.025

scan result



final test

[QP]	freq(MHz)	lev(dBuV)	Lim(dBuV)	Δ(lev-Lim)
	0.150	60.0	66.0	-6.0
	0.390	46.0	59.1	-13.1

Figure 2-10. 115VAC, Full Load, Resistive Load, Unearthed, N phase

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EMI TEST REPORT

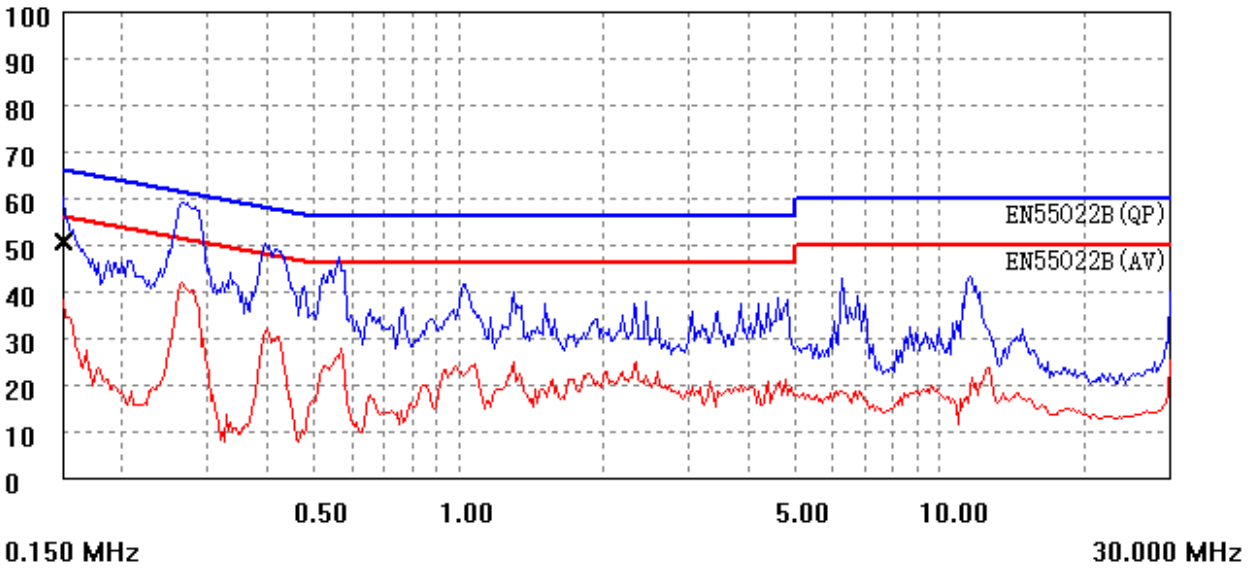
parameter

Organization:		Operator:		EUT:	
Place:		Time:	2024/12/4/14:13	Test equipment:	KH3932
Detector:	PK+AV	Test-time(ms):	30	SN:	320684
Limit:	EN55022B	Transductor(PK/AV):	PK / AV	JZ:	2,15,1044
Remark:					

freq, step

Start(MHz)	End(MHz)	Step(MHz)
0.150	2.000	0.002
2.000	10.000	0.010
10.000	30.000	0.025

scan result



final test

[QP]	freq(MHz)	lev(dBuV)	Lim(dBuV)	Δ(lev-Lim)
	0.150	50.7	66.0	-15.3

Figure 2-11. 230VAC, Full Load, Resistive Load, Unearthed, L phase

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EMI TEST REPORT

parameter

Organization:		Operator:		EUT:	
Place:		Time:	2024/12/4/14:18	Test equipment:	KH3932
Detector:	PK+AV	Test-time(ms):	30	SN:	320684
Limit:	EN55022B	Transductor(PK/AV):	PK / AV	JZ:	2,15,1040
Remark:					

freq, step

Start(MHz)	End(MHz)	Step(MHz)
0.150	2.000	0.002
2.000	10.000	0.010
10.000	30.000	0.025

scan result

dBuV

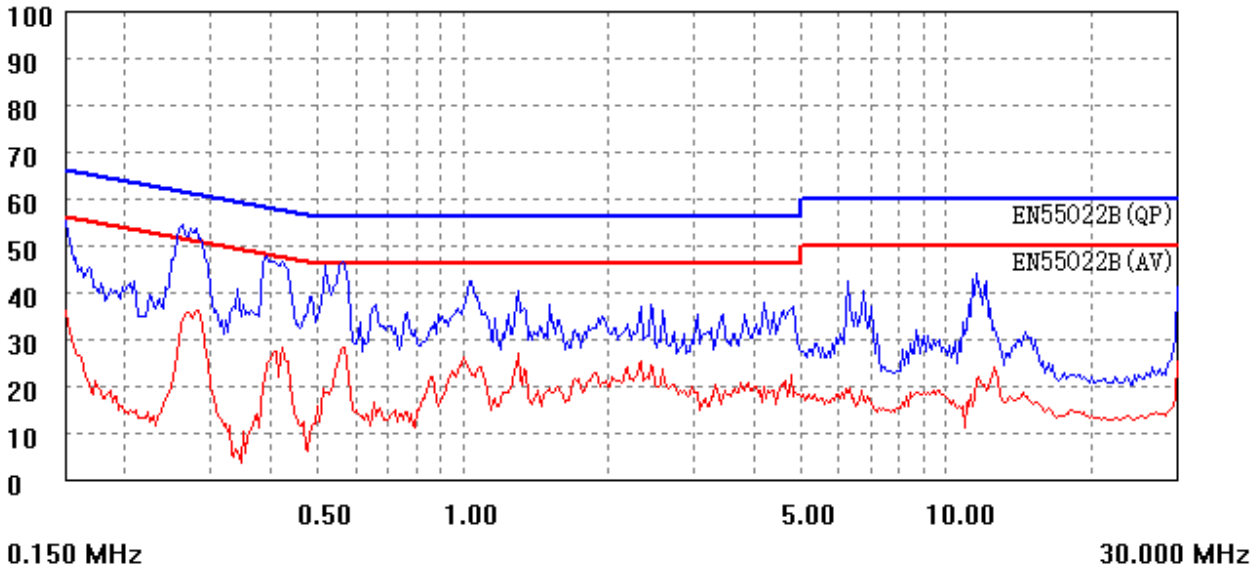

Figure 2-12. 230VAC, Full Load, Resistive Load, Unearthed, N phase

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3 Waveforms

3.1 Start-up and Shut Down Waveform

Start-up behavior is shown in Figure 3-1 through Figure 3-4.

CH1: VAC, CH2:VOUT, CH4: Iout

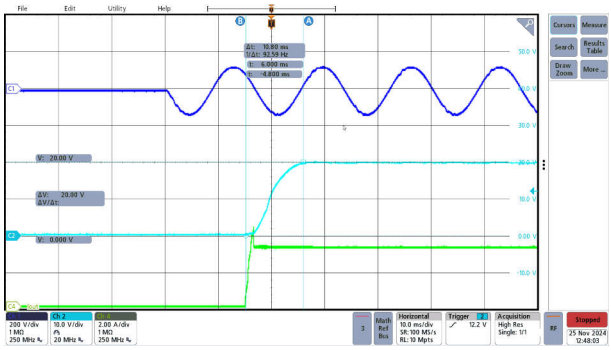

Figure 3-1. 90VAC, Soft Start-Up Time 6ms

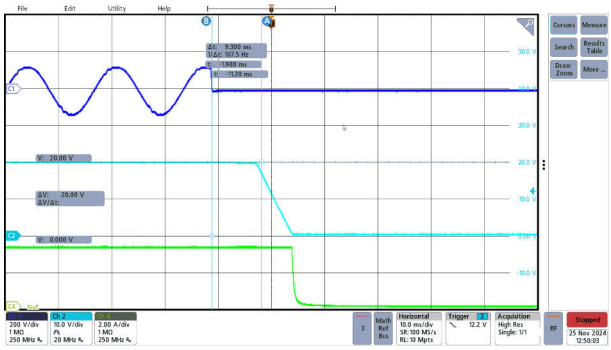

Figure 3-2. 90VAC, Shut Down, Hold Up Time 9.3ms

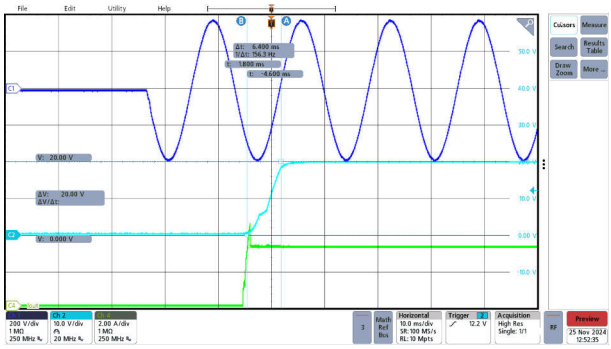

Figure 3-3. 264VAC, Soft Start-Up Time 6ms

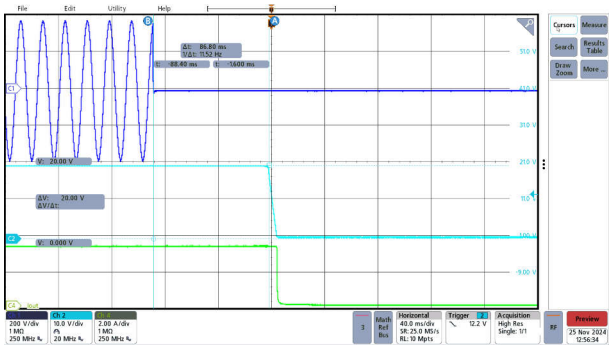

Figure 3-4. 264VAC, Shut Down, Hold-Up Time 87ms

3.2 Switching

Switching behavior is shown in Figure 3-5 through Figure 3-21.

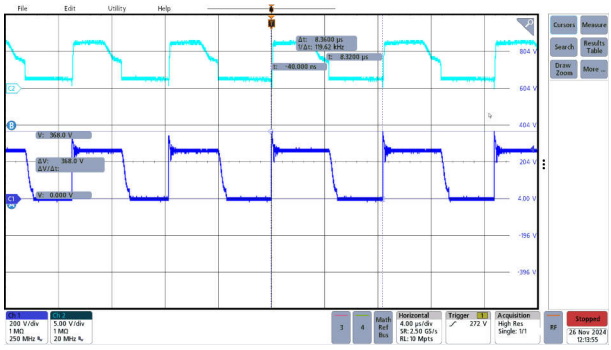

Figure 3-5. 115VAC, Vds_pri, Vsr_gate, Full Load

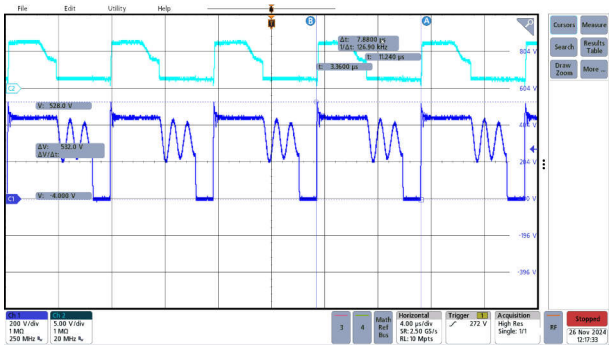

Figure 3-6. 230VAC, Vds_pri, Vsr_gate, Full Load

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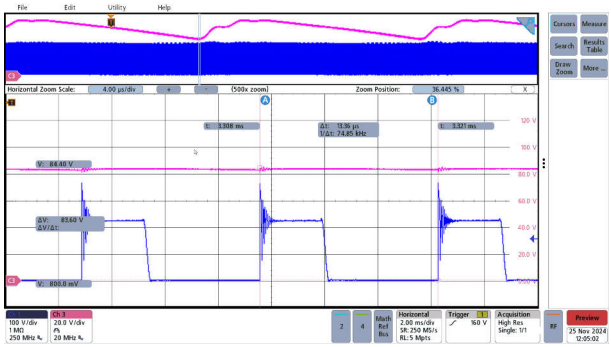

Figure 3-7. 90VAC, Full Load, Vds_pri, Vbus Valley 83V

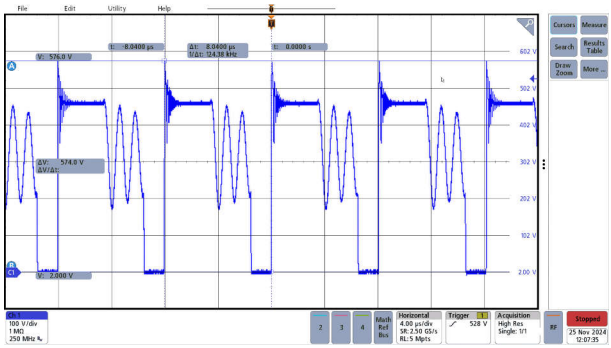

Figure 3-8. 230VAC, Full Load, 3.25A, fsw = 125kHz

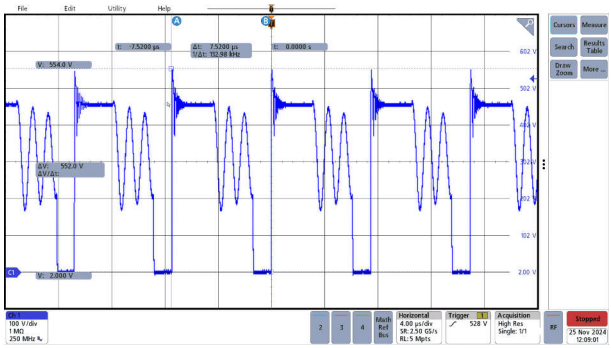

Figure 3-9. 230VAC, 75% Load, 2.45A, fsw = 133kHz

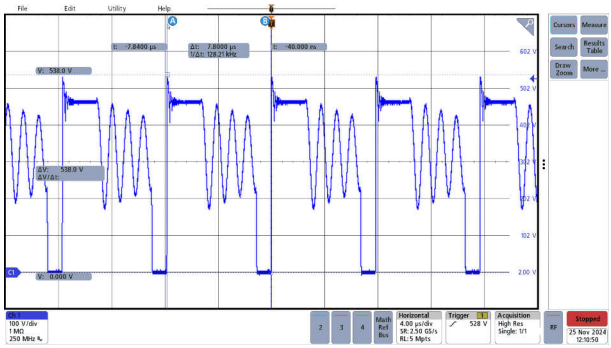

Figure 3-10. 230VAC, 50% Load, 1.6A, fsw = 128kHz

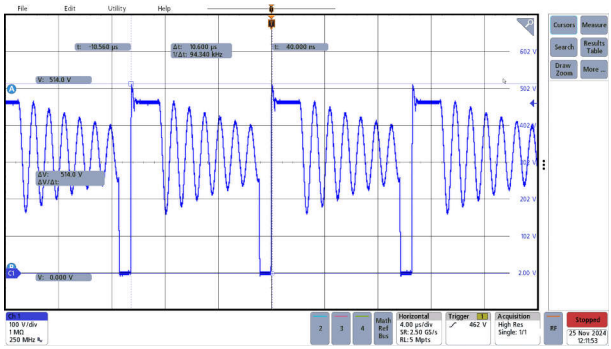

Figure 3-11. 230VAC, 25% Load 0.82A, fsw = 94kHz

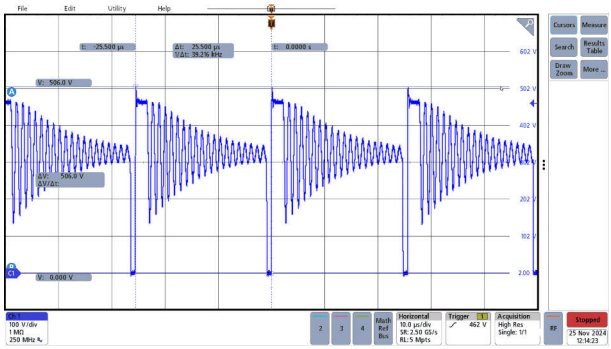

Figure 3-12. 230VAC, 10% Load 0.32A, fsw=39kHz

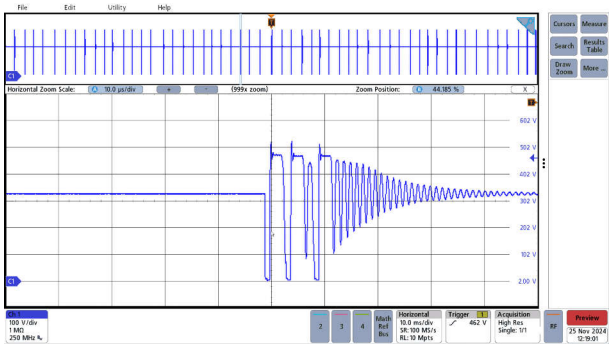

Figure 3-13. 230VAC, 20V, 200mW Load, Vds_pri

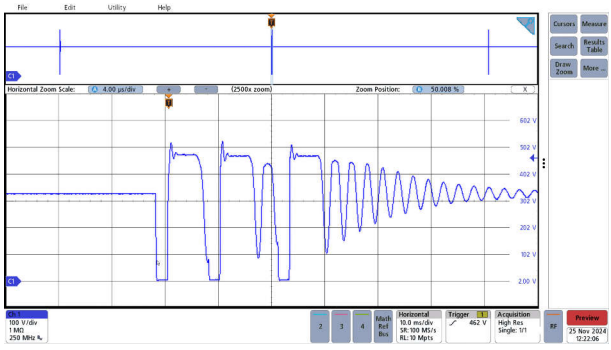

Figure 3-14. 230VAC, 20V, Open Load, Vds_pri

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Figure 3-15 through Figure 3-21 are 115VAC input switching waveforms.

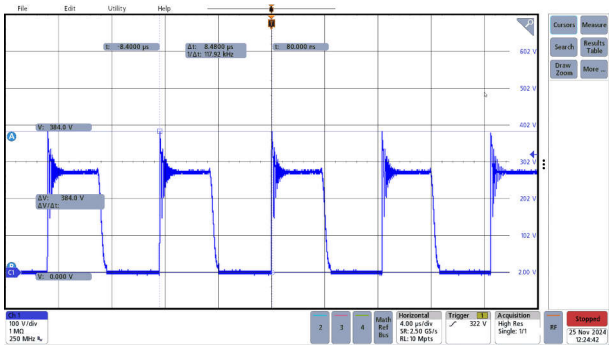

Figure 3-15. 115VAC, 20V, 3.25A Full Load, Vds_pri, fsw = 118kHz

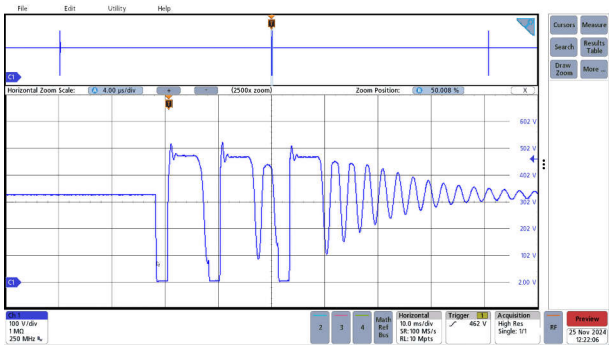

Figure 3-16. 115VAC, 20V, 2.45A 75% Load, Vds_pri, fsw = 127kHz

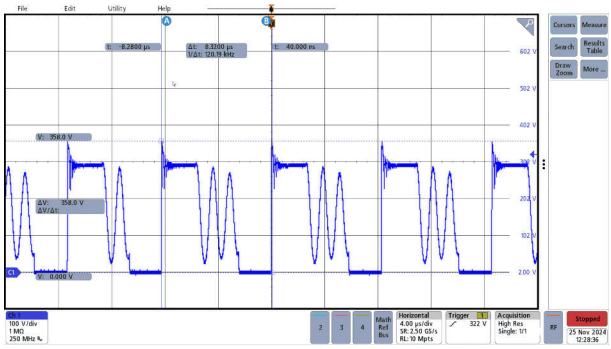

Figure 3-17. 115VAC, 20V, 1.8A 50% Load, Vds_pri, fsw = 120kHz

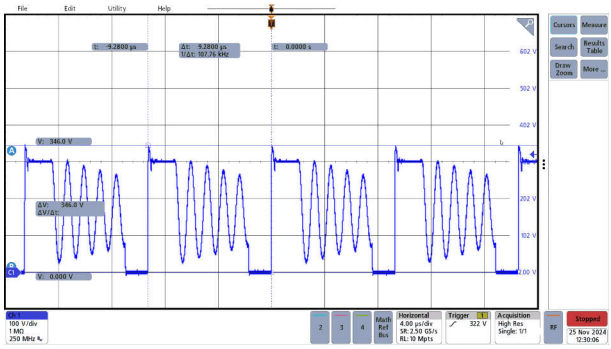

Figure 3-18. 115VAC, 20V, 0.82A 25% Load, Vds_pri, fsw = 107kHz

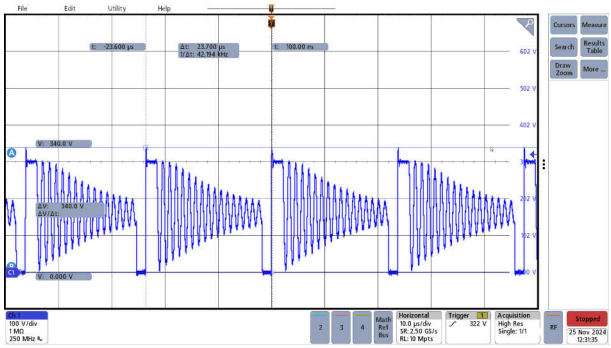

Figure 3-19. 115VAC, 20V, 0.32A 10% Load, Vds_pri, fsw = 42kHz

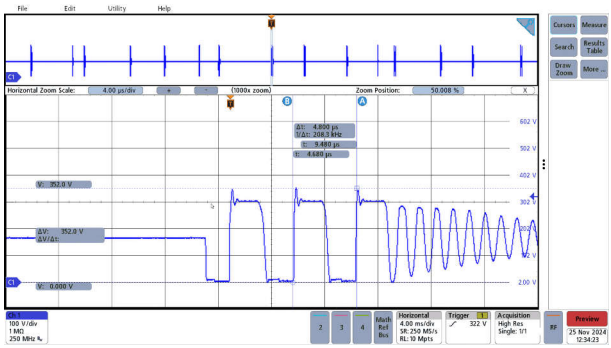

Figure 3-20. 115VAC, 20V, 200mW Load, Vds_pri

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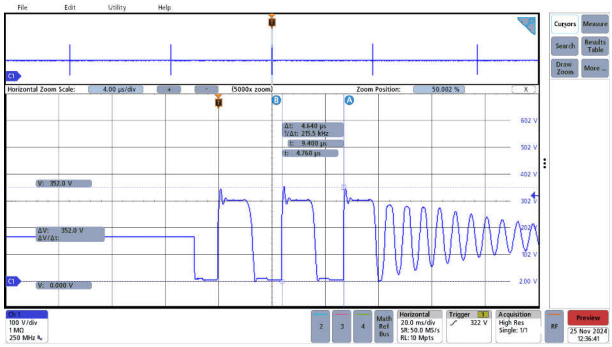

Figure 3-21. 115VAC, 20V, Open Load, Vds_pri, 3 Consecutive Switching Cycles to Achieve First Valley Switching

3.2.1 Voltage Stress

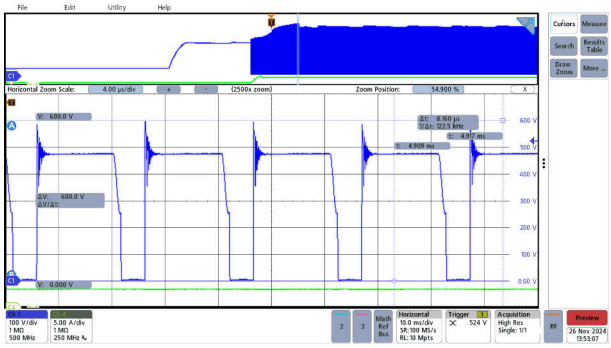

Figure 3-22. 264VAC, Full Load, Vds Peak = 600V

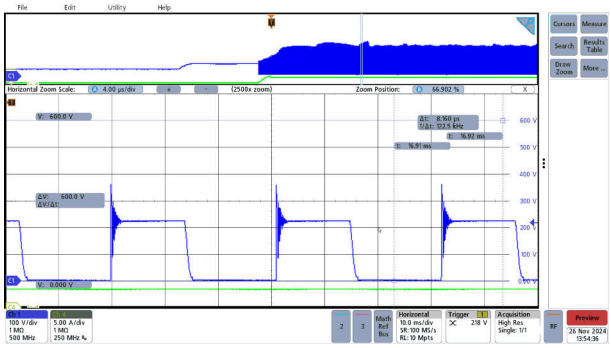

Figure 3-23. 90VAC, Full Load, Vds Peak = 360V

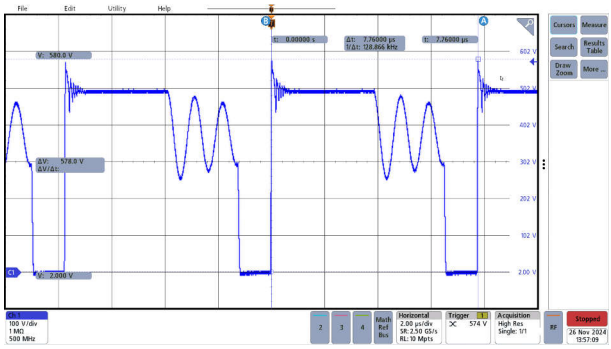

Figure 3-24. 264VAC, Full Load, Steady State Vds Primary 580V

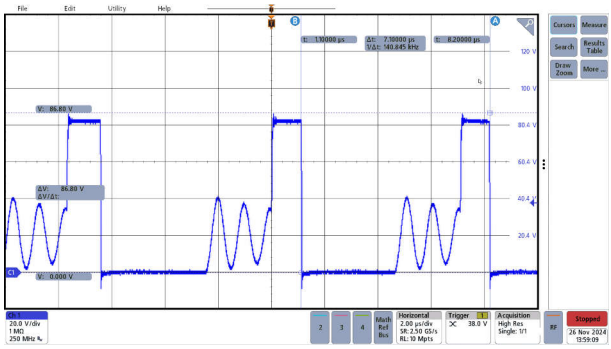

Figure 3-25. 264VAC, Full Load, Vds on Synchronous Rectifier 86.8V

3.3 VCC Self Bias

VCC was regulated across AC input and load condition. Figure 3-26 through Figure 3-31 show VCC waveforms.

CH1: Vds, CH2: VCC, CH3: HV Pin, CH4: I_{out}

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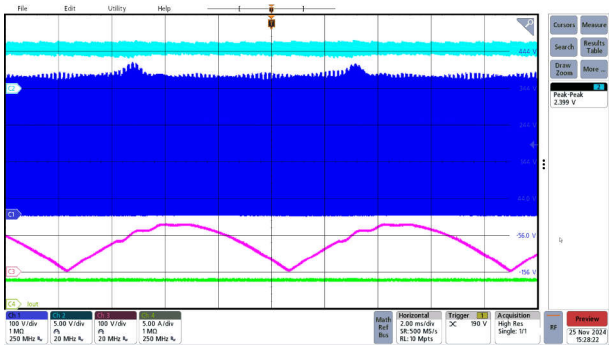

Figure 3-26. VCC Voltage, 90VAC, Full Load

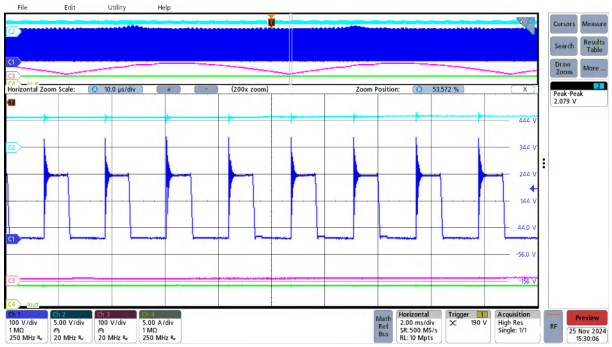

Figure 3-27. VCC Voltage, 90VAC, Full Load, Zoom in at VBUS Valley

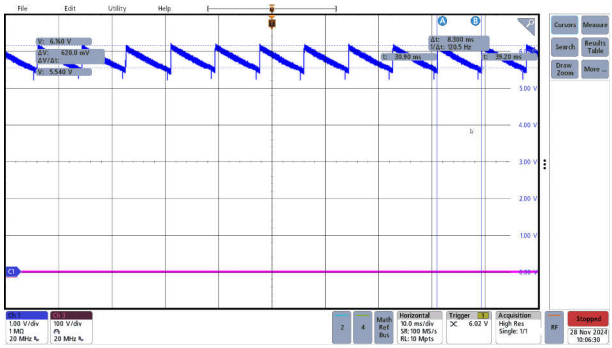

Figure 3-28. VCC Voltage, 115VAC, Open Load, VCC Charging at Around 120Hz Frequency

Figure 3-29 through Figure 3-31 shows VCC at 230VAC input.

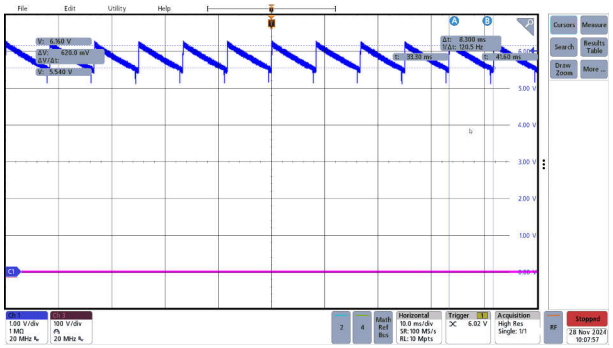

Figure 3-29. VCC Voltage, 230VAC, Open Load, VCC Charging at Around 120Hz Frequency

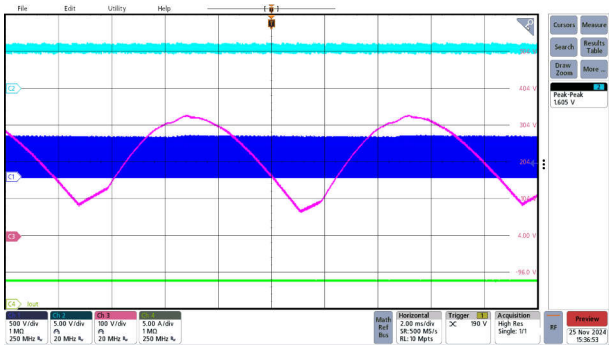

Figure 3-30. VCC Voltage, 230VAC, Full Load

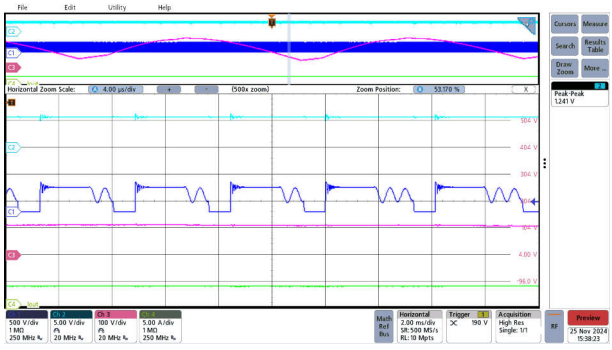

Figure 3-31. VCC Voltage, 230VAC, Full Load, Zoom-In

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3.4 Output Voltage Ripple

Output voltage ripple is shown in Figure 3-32 through Figure 3-39.

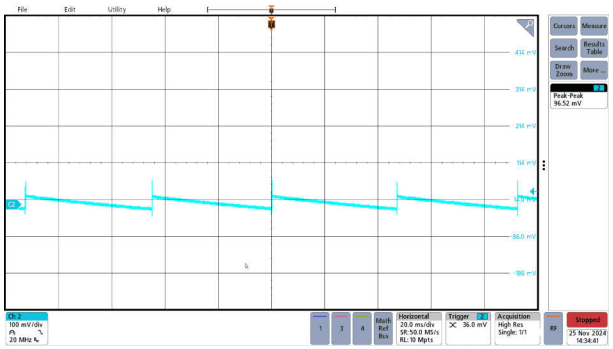

Figure 3-32. Output Voltage Ripple, 115VAC, Open Load

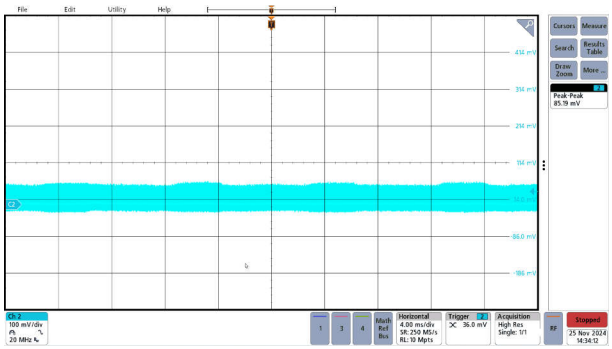

Figure 3-33. Output Voltage Ripple, 115VAC, 10% Load 0.33A

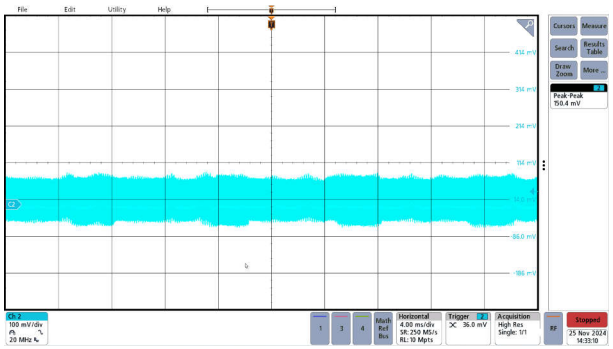

Figure 3-34. Output Voltage Ripple, 115VAC, 50% Load 1.62A

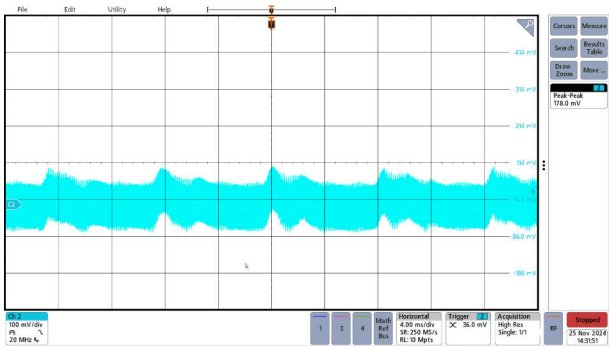

Figure 3-35. Output Voltage Ripple, 115VAC, 100% Load, 3.25A

Figure 3-36 through Figure 3-39 are tested at 230VAC.

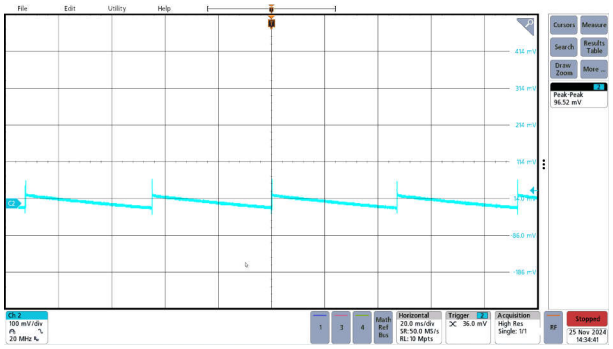

Figure 3-36. Output Voltage Ripple, 230VAC, Open Load

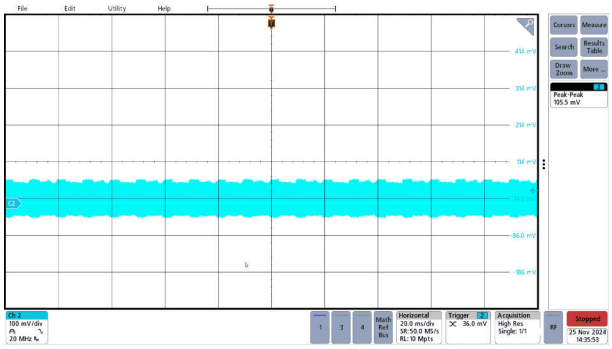

Figure 3-37. Output Voltage Ripple, 230VAC, 10% Load 0.33A

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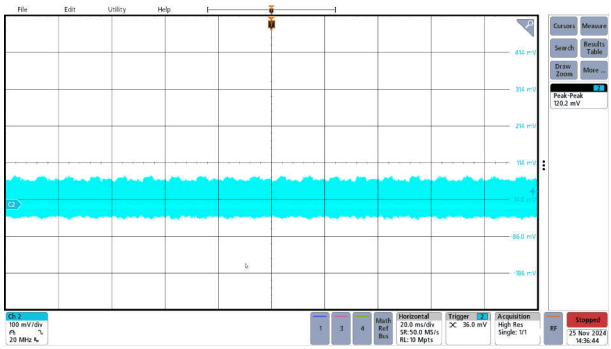

Figure 3-38. Output Voltage Ripple, 230VAC, 50% Load 1.6A

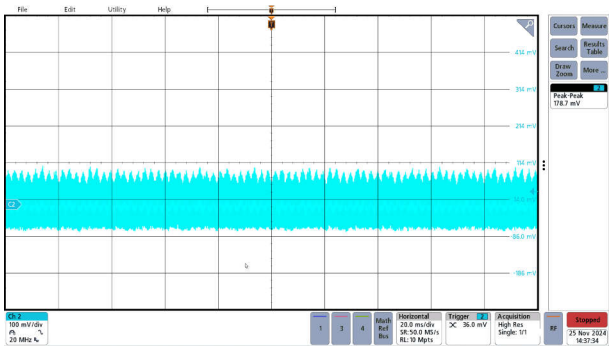

Figure 3-39. Output Voltage Ripple, 230VAC, 100% Load 3.25A

3.5 Load Dynamic Response

The load dynamic test was performed from 0.1A to full load, 3.25A. Output voltage was measured at the PCB end.

CH2: V_{out}, CH4: I_{out}

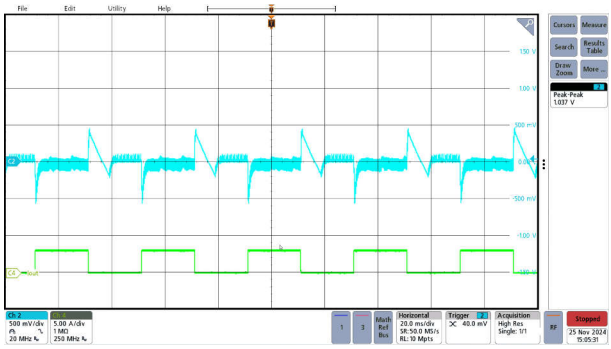

Figure 3-40. Load Transient, 115VAC, 0.1A to 3.25A Full Load

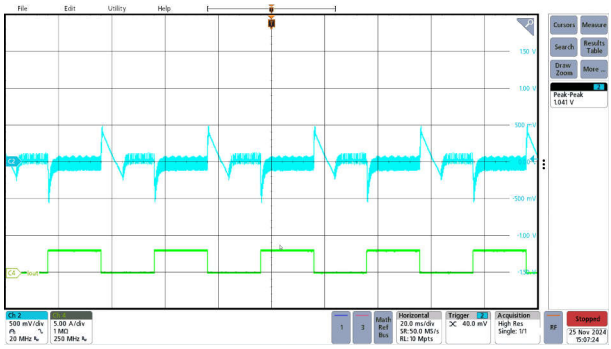

Figure 3-41. Load Transient, 230VAC, 0.1A to 3.25A Full Load

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3.6 Peak Power

Peak power test was performed by setting the peak power to 1.5 times rated power (100W) for 4ms followed by 36ms 0.9 times rated power (58W).

CH1: Vds_pri, CH2: V_{out}, C4:I_{out}

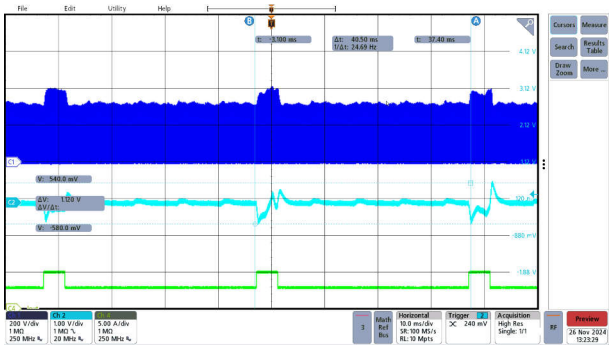

Figure 3-42. Peak Power, 90VAC, 100W Peak Power 4ms, 58W 36ms, V_{out} Drop 0.58V

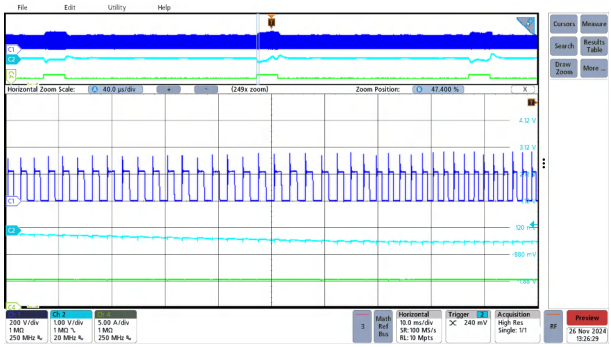

Figure 3-43. Peak Power, 90VAC, 100W Peak Power 4ms, 58W 36ms, Zoom In, fsw Increase to Provide Peak Power

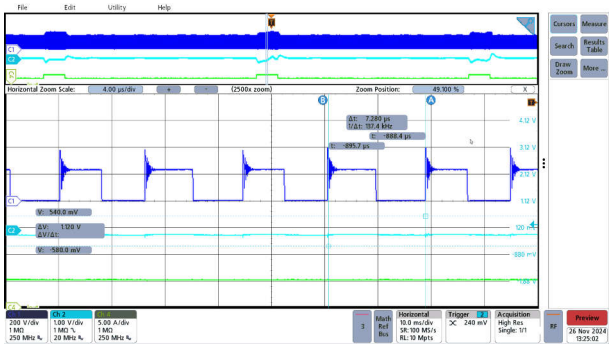

Figure 3-44. Peak Power, 90VAC, 100W Peak Power 4ms, 58W 36ms, Zoom In, CCM Mode to Provide Peak Power With fsw Increased to 137KHz

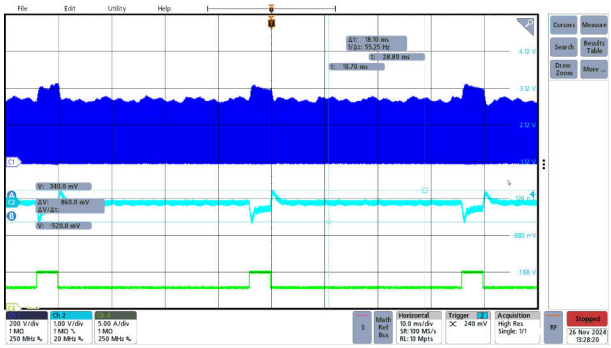

Figure 3-45. Peak Power, 115VAC, 100W Peak Power 4ms, 58W 36ms, V_{out} Drop 520mV

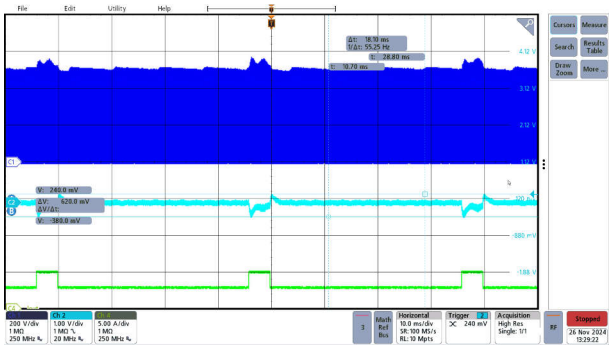

Figure 3-46. Peak Power, 230VAC, 100W Peak Power 4ms, 58W 36ms, V_{out} Drop 380mV

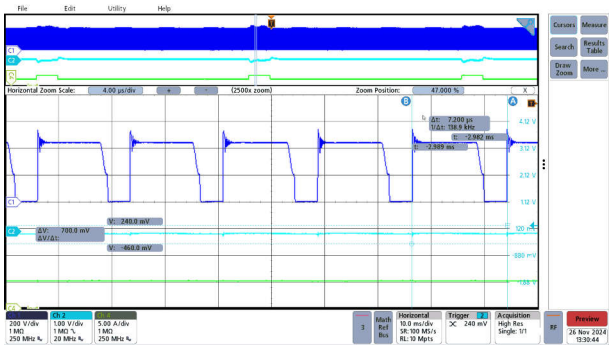

Figure 3-47. Peak Power, 230VAC, 100W Peak Power 4ms, 58W 36ms, V_{out} Drop 380mV, Zoom In

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3.7 Short-Circuit Protection

Short-circuit protection was performed at PCB board end. Auto recovery after short was removed.

CH1: Vds primary, CH2:VCC, CH3: V_{out}, CH4: I_{out}

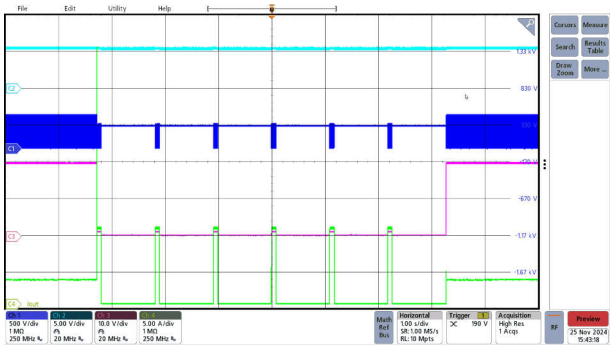

Figure 3-48. Short Circuit at PCB End and Recovery When Short Circuit Removed, 264VAC

3.8 Output Over Voltage Protection

By disconnecting output feedback, V_{out} ramps up and UCG28826 SW pin senses the output voltage. Once the sensed voltage triggers the OVP threshold, the OVP protection is triggered.

CH2: Vout, CH4: Vds primary switching

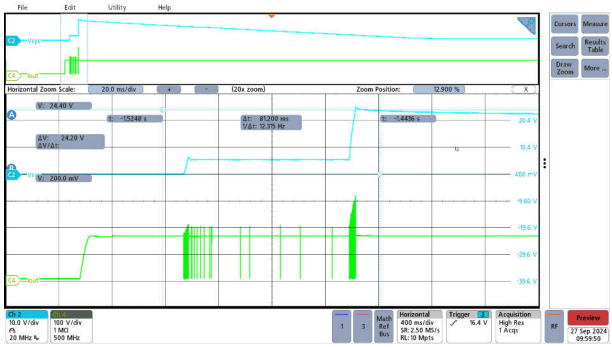

Figure 3-49. 264VAC, OVP, Open Load

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