Tim Green

TI Precision Designs: Reference Design
Single Op-Amp Slew Rate Limiter

TEXAS INSTRUMENTS

TI Precision Designs

TI Precision Designs are analog solutions created by TI's analog experts. Reference Designs offer the theory, component selection, and simulation of useful circuits. Circuit modifications that help to meet alternate design goals are also discussed.

Circuit Description

In control systems for valves or motors, abrupt changes in voltages or currents can cause mechanical damages. By controlling the slew rate of the command voltages, into the drive circuits, the load voltages can ramp up and down at a safe rate. For symmetrical slew rate applications (positive slew rate equals negative slew rate) one additional op amp can provide slew rate control for a given analog gain stage. This design will show how to achieve slew rate control for both dual and single supply systems. The desired slew rate must be less than the op amp chosen to implement the slew rate limiter.

Design Resources

Design Archive	All Design files
TINA-TI™	SPICE Simulator
OPA192	Product Folder
OPA376	Product Folder

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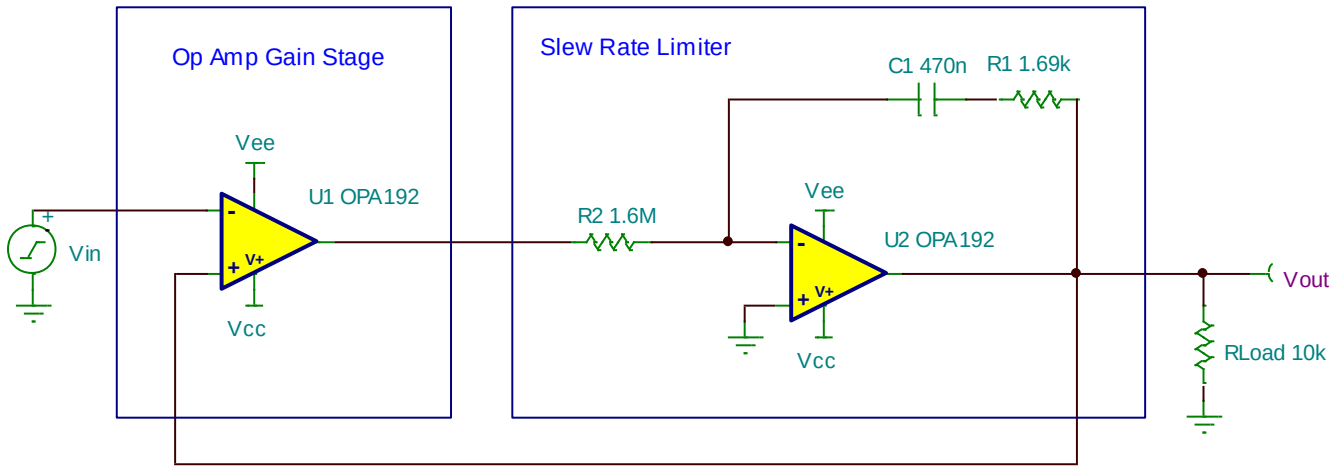


1 Design Summary

The design requirements are as follows:

- Slew Rate: +/-20V/s +/-20%
- Output Voltage: +/-10Vp
- Supply Voltage: +/-15Vdc +/-5%
- Input Frequency Range: dc to 250mHz,
- Input Amplitude: +/-10Vp Square Wave
- Input rise/fall time: 10ns min to 1s Max

Table 1 compares the design goal versus the simulated performance of the op amp slew rate limiter. Figure 1 depicts the simulated transfer function of the design and verifies the desired goal of the +/-20V/s slew rate limiter.

Table 1. Comparison of Design Goals and Simulated Performance

				Design Goal	Simulated Performance
Case	**Input Rise/Fall**	**Input Amplitude**	**Output Amplitude**	**Output Slew Rate**	**Output Slew Rate**
Typical	10ns	+/-10V	+/-20V	20V/s	19.94V/s
Typical	1s	+/-10V	+/-20V	20V/s	20V/s
Min Slew	10ns	+/-10V	+/-20V	16V/s	17V/s
Max Slew	10ns	+/-10V	+/-20V	24V/s	23.56V/s

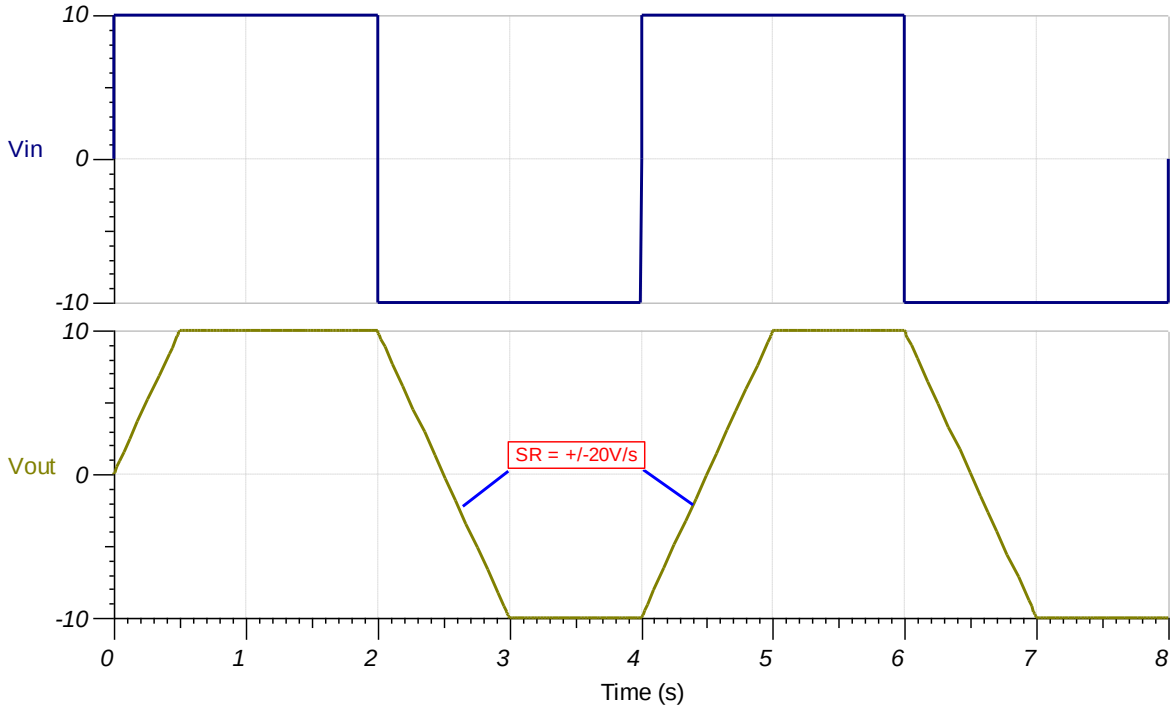


Figure 1: Simulated Transfer Function

2 Theory of Operation

Figure 2 shows the OPA192 op amp on the left standalone and with an added slew rate limiter on the right. The standalone OPA192 on the left has a slew rate of **20V/µs**. When our application requires a slower slew rate, like **20V/s**, then we need to add a slew rate limiter, as shown on the right, since no op amp has a slow enough slew rate to match 20V/s.

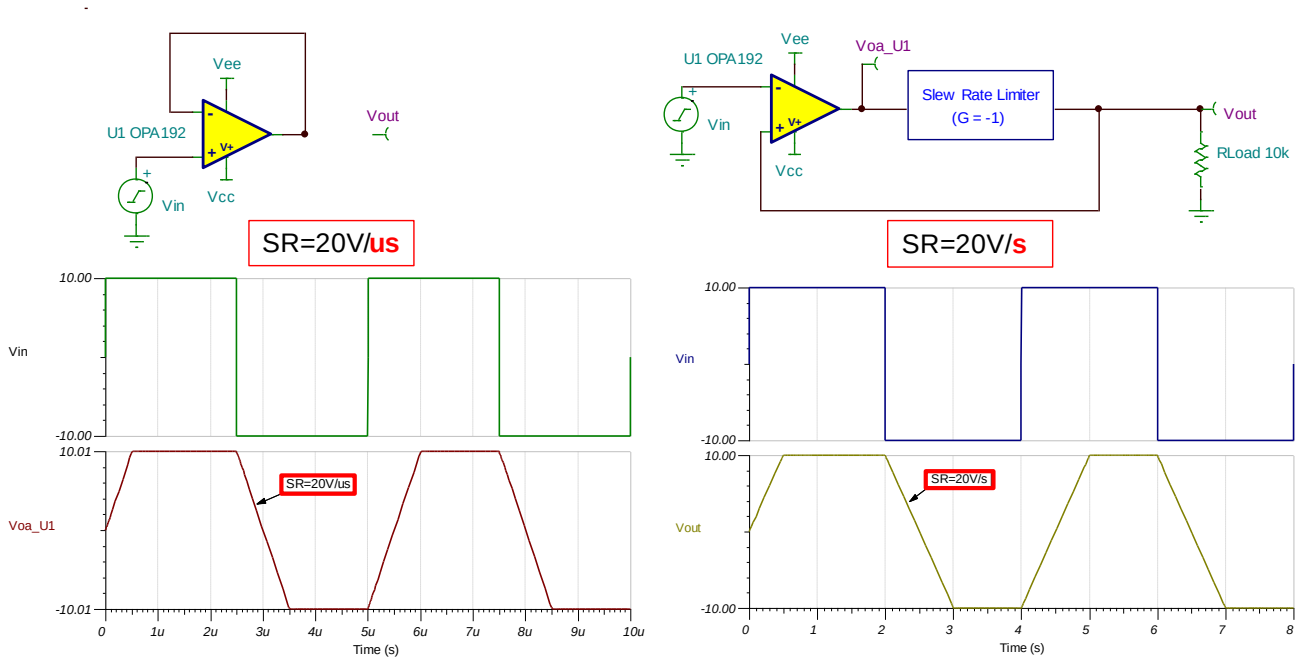


Figure 2: Slew Rate Limiter Concept

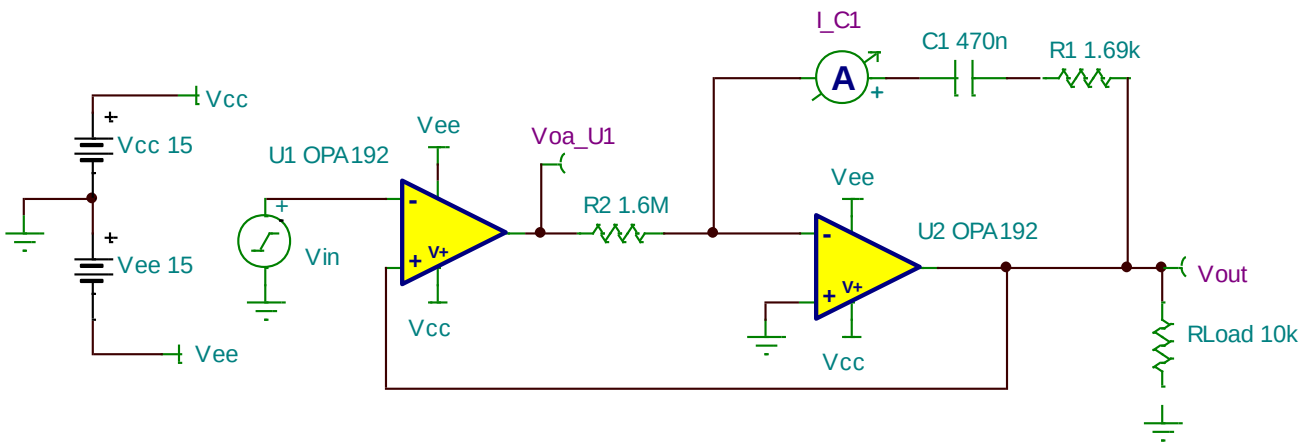


Figure 3 shows the full schematic for the design. The circuit uses one op amp, U2, inside the closed loop of a signal gain stage op amp, U1, to achieve slew rate control. U1 is the main op amp with closed loop feedback from Vout. Overall gain (Vout/Vin) is set to 1 since there is no feedback or input resistor around the gain setting amplifier, U1. Any small change in Vin will saturate the output of U1, due to U1's high open loop gain. Since the inverting input of U2 is at "virtual ground", the voltage across R2 is the saturation voltage, U1_Vsat, of U1's output, Voa_U1. I_C1 is the current through C1 and will be U1_Vsat/R2. Vout Slew rate is dV/dt=I_C1/C1 by re-arranging the standard capacitor equation of I=C*dV/dt. Regardless of input voltage, slew rate will always be the same. R1 is needed for stability compensation and is covered in detail in Appendix A. Note how the non-inverting input of this composite configuration is the inverting input of U1. This is because U2 inverts the output of U1 is fed back to the non-inverting input of U1 for "negative feedback."

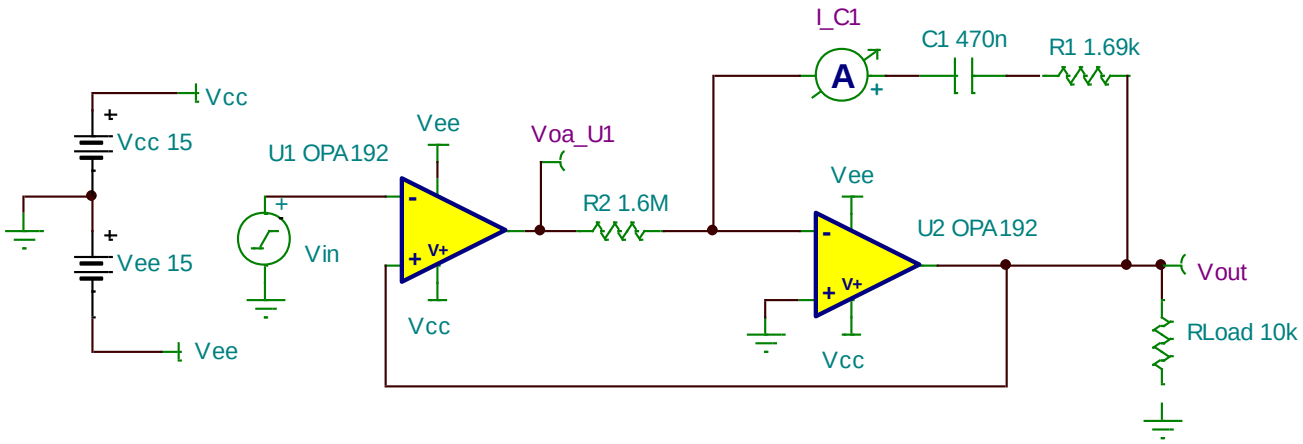


Figure 3: Complete Circuit Schematic

3 Component Selection

3.1 R2 and C1 Selection

Figure 4 contains the equations for programming the slew rate limiter. There are two controlling elements in the slew rate formula, I_C1 and C1. It can be seen from the table, in Figure 4, that the design trade-off is between the C1 value and IC_1. By keeping I_C1 low (<10μA) one can swing close to the supply rails of U1 and get a predictable charging/discharging current for C1. A standard capacitor value of 470nF yields a charging/discharging current of 9.4μA. These currents are programmed by R2, the saturation output voltage of U1, 10mV, and the power supply, +/-15V. The closest standard resistor value is chosen as 1.6MΩ.

SR=	20	V/s
I_C1	**C1**	**C1**
(A)	**(F)**	**std value**
1.0E-06	5.0E-08	47nF
1.0E-05	5.0E-07	470nF
1.0E-04	5.0E-06	4.7uF
1.0E-03	5.0E-05	47uF
1.0E-02	5.0E-04	470uF

Final Value Selection:

$$SR = 20\text{V/s}$$

$$SR = \frac{I\_C1}{C1}$$

$$20\frac{V}{s} = \frac{I\_C1}{470nF} \rightarrow I\_C1 = 9.4\mu A$$

$$I\_C1 = \frac{V\,supply - Vsat\_U1}{R2}$$

$$9.4\mu A = \frac{15V - 10mV}{R2} \rightarrow R2 = 1.5947M\Omega$$

Use R2 = 1.6MΩ (Standard Value)

Figure 4: R2 and C1 Selection

As can be seen in Figure 4 the accuracy of the slew rate is directly determined by the accuracy of R2, C1, Vsupply (Vcc or Vee), and Vsat_U1. A valid assumption is that Vsat_U1 does not change much and is a small contribution to the overall slew rate error. Figure 5 shows the slew rate accuracy for typical component and power supply tolerances. R1 will not affect the slew rate limiter accuracy as long as it is kept to a value that is less than R2/100. R1 is used for stability and is discussed in Appendix A.

Worst Case Min Slew Rate :

$$SR = \frac{\left(\frac{V\,supply - Vsat\_U1}{R2}\right)}{C1}$$

$$SR[min] = \frac{\left(\frac{14.25V - 10mV}{1.62M\Omega}\right)}{517nF} = 17\,\frac{V}{s}$$

Worst Case Max Slew Rate :

$$SR = \frac{\left(\frac{V\,supply - Vsat\_U1}{R2}\right)}{C1}$$

$$SR[max] = \frac{\left(\frac{15.75V - 10mV}{1.58M\Omega}\right)}{423nF} = 23.55\,\frac{V}{s}$$

Component	Tolerance (%)	Units	Min	Typical	Max
C1	10	F	4.23E-07	4.70E-07	5.17E-07
R2	1	Ω	1.58E+06	1.60E+06	1.62E+06
Vsupply	5	V	14.25	15	15.75

Figure 5: Min/Max Slew Rate Computation

3.2 Op Amp

Key considerations for the op amp U1 (Gain Stage) are:

1) Low saturation output voltage. Rail-to-rail output allows for accurate scaling of slew rate limiter.

2) Short overload recovery time. Output will be coming into and out of saturation while in slew rate limit. Short overload recovery time ensures minimal error and delay when reaching final voltage levels.

3) Slew rate = 10x-100x slew rate limiter value. To prevent any unnecessary delay on output from slewing up into saturation at beginning of slew rate limit.

4) Fast settling time. Allows for minimal delay to final value once slewing is finished.

5) Rail-to-rail input. Allows for expanded signal range in unity gain buffer configuration.

Key considerations for the op amp U2 (Slew Rate Limiter) are:

1) Low saturation output voltage. Rail-to-rail output allows for maximum signal swing on given supplies.

2) Slew rate = 10x-100x slew rate limiter value. To prevent any unnecessary delay on output from slewing up into saturation at beginning of slew rate limit.

3) Fast settling time. Allows for minimal delay to final value once slewing is finished.

4) Low input bias current. Allows for larger values of R1 without excessive offset voltage that can would minimize accuracy of voltage applied across R1 to get I_C1. Larger values of R1 means lower values of I_C1 which means smaller values for C1 for a given desired slew rate. Smaller values of C1 are easier to obtain in ceramic with good temperature coefficients and capacitance tolerances.

5) Output voltage swing vs. output current. Need to ensure that the current demands for charging/discharging C1 plus any load current out of U2 will still allow desired output voltage out of U2.

Based on key considerations for both U1 and U2, the OPA192 provides the desired characteristics as detailed in Table 1 and Figure 6.

Table 1: Op Amp Characteristics

PARAMETER (25C)	MIN	TYP	MAX	UNIT	COMMENTS
I_B Input Bias Current		+/-5	+/-20	pA	
V_{CM} Common Mode Voltage Range	(V-)-0.1		(V+)+0.1	V	
SR Slew Rate		20		V/us	
t_{OR} Overload Recovery Time		1		us	V_{IN}*G=(V+) or (V-)
V_O Output Voltage Swing to Rail	10	5		mV	No Load
I_{SC} Short-circuit Current		+/-60		mA	
V_S Specified Voltage Range	4.5		36	V	(V+) - (V-)
t_S Settling Time		1.4		us	To 0.001%, V_S=+/-18V, G=1, 10V step

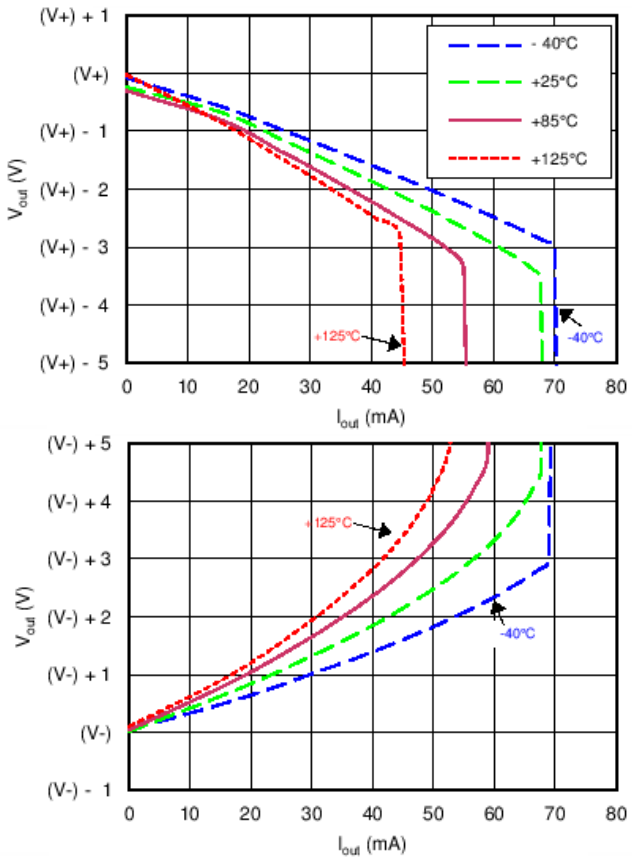


Figure 6: OPA192 Output Voltage vs. Output Current

Like most rail to rail input op amps, the OPA192 uses two different input stages in parallel, one P-Channel based and one N-Channel based, to achieve its wide input common mode range. The OPA192 input offset voltage is trimmed to a very low 5uV, typical value. As with all dual input stage topologies there is a small region of input common mode voltage where the input offset voltage will increase while both input pairs are engaged. This narrow transition region and its effects are shown in Figure 7. This region is approximately 1.5V below the positive supply voltage. For our slew rate limiter op amp, U2, this is not an issue since its input common mode voltage is zero (inverting gain configuration). U1, our input signal gain op amp, will only see 10V of input common mode on a +/-15V supply so it will not see this region in this application. However, if an application extends its input voltage range, in this overall composite buffer configuration, then one should consider the performance effects when transitioning through this VCM region.

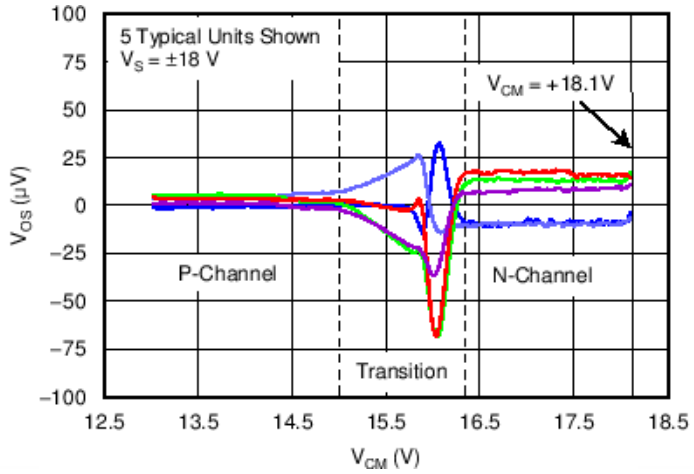


Figure 7: OPA192 Vos versus VCM

Most bipolar op amps, and some CMOS op amps, have differential input clamps, as shown in Figure 8. These back to back input diodes are used for input protection. Exceeding the turn-on threshold of these diodes, as in a pulse condition, can cause current to flow through the input protection diodes. If these diodes turn on, they take a long time to turn off, resulting in output settling issues and increased input bias currents. For our U1 op amp, a fast input step could create problems for an op amp with these input differential diodes. Depending upon the programmed slew rate of the slew rate limiter this could lead to long settling times and also, depending upon the input signal voltage source impedance, signal distortion. Fortunately the OPA192 does not have differential input diodes.

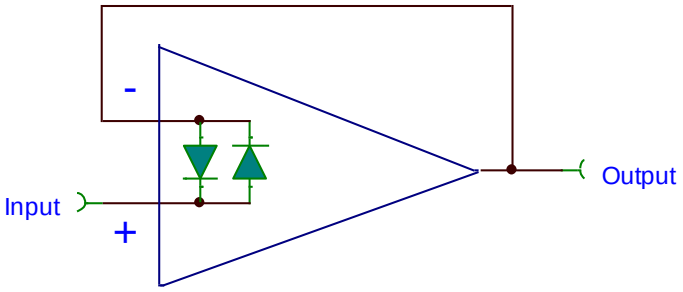


Figure 8: OPA192 Input *DOES NOT* have Differential Input Clamps

4 Simulation

The TINA-TITM test circuit of Figure 9 will be used to validate by simulation the performance of the slew rate limiter.

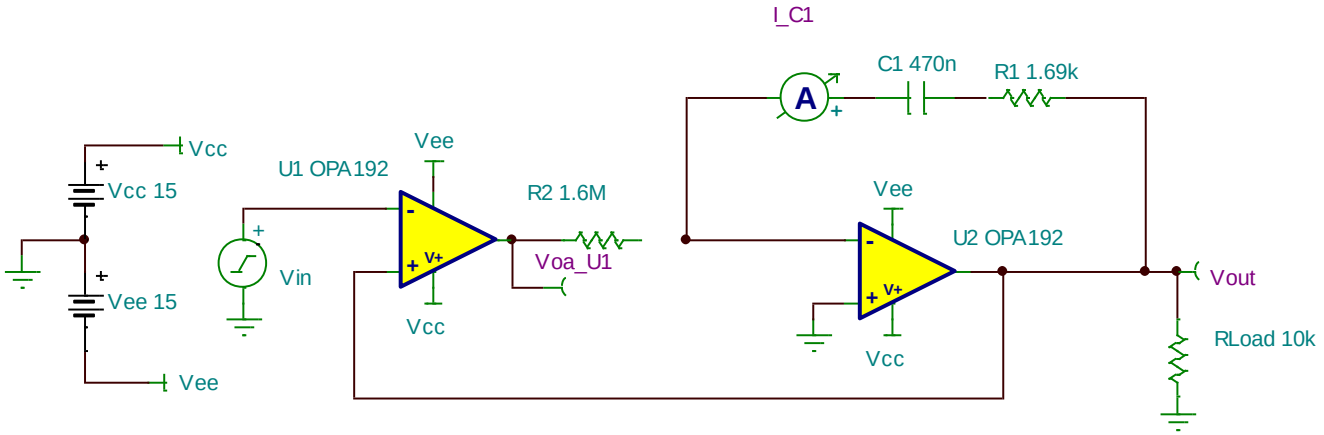


Figure 9: Slew Rate Limiter Test Circuit

Figure 10 shows a 19.94V/s slew rate for an input square wave of trise/tfall = 10ns.

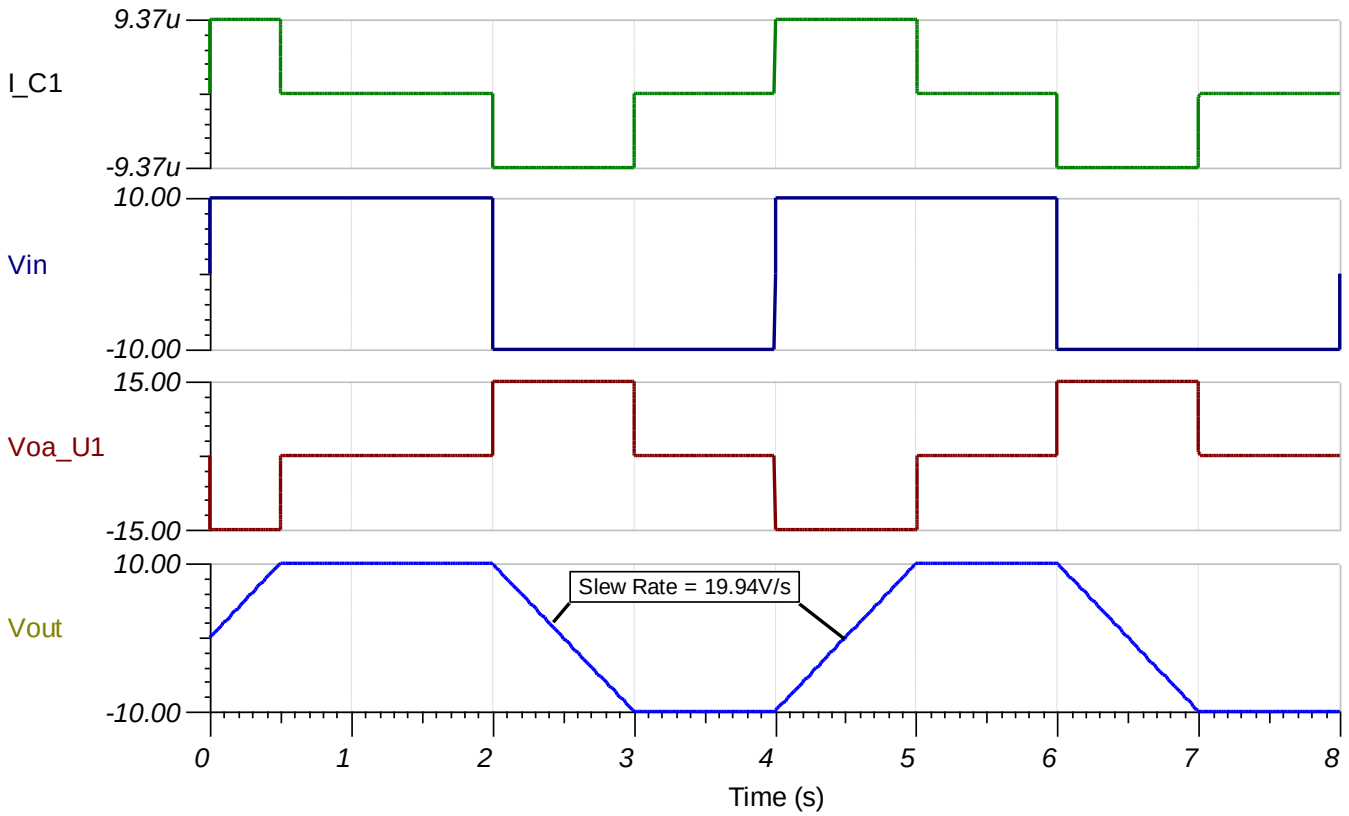


Figure 10: Slew Rate Limiter Response for trise/tfall = 10ns

Figure 11 shows a 20V/s slew rate for an input square wave of trise/tfall = 1s.

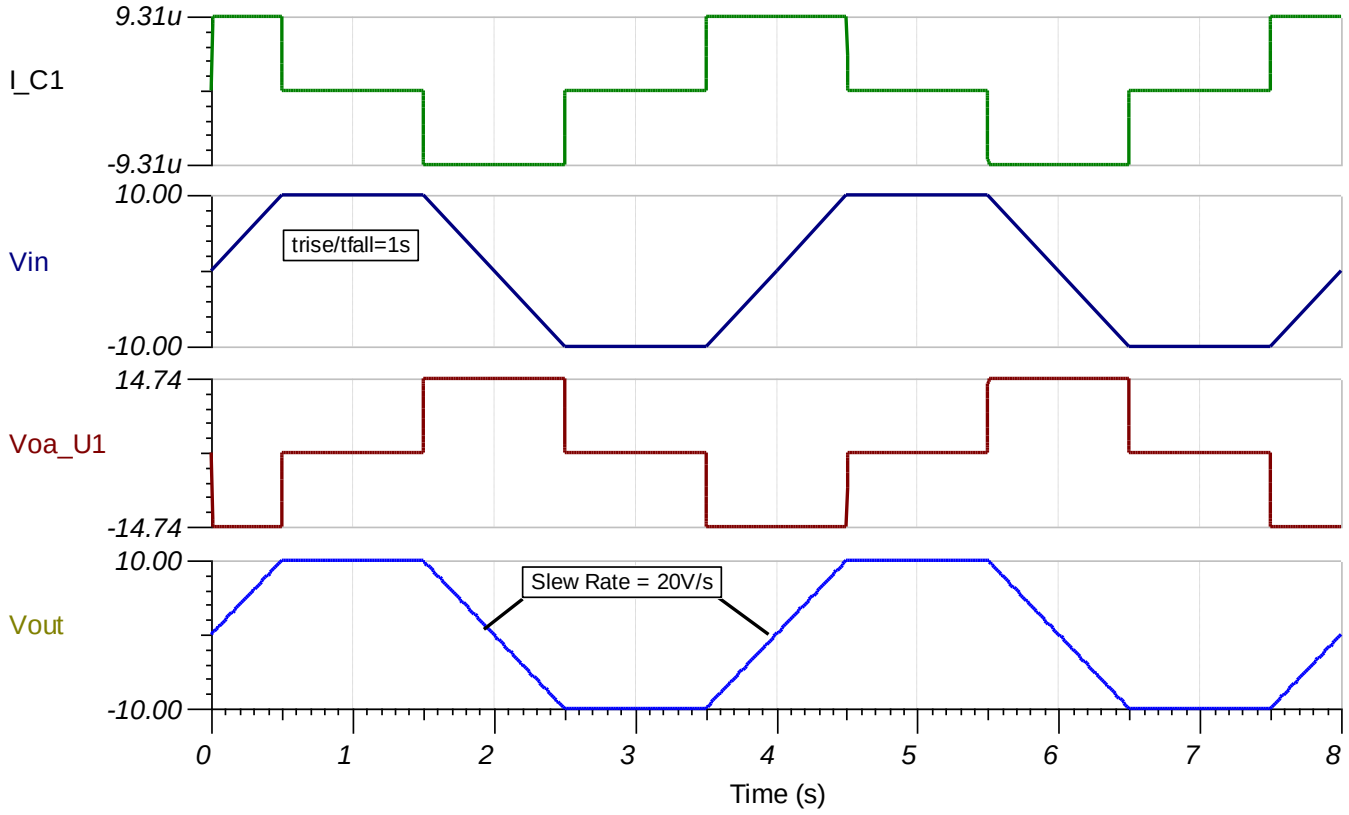


Figure 11: Slew Rate Limiter Response for trise/tfall = 1s

Figure 12 is the TINA-TI™ test circuit for worst case minimum slew rate limiter.

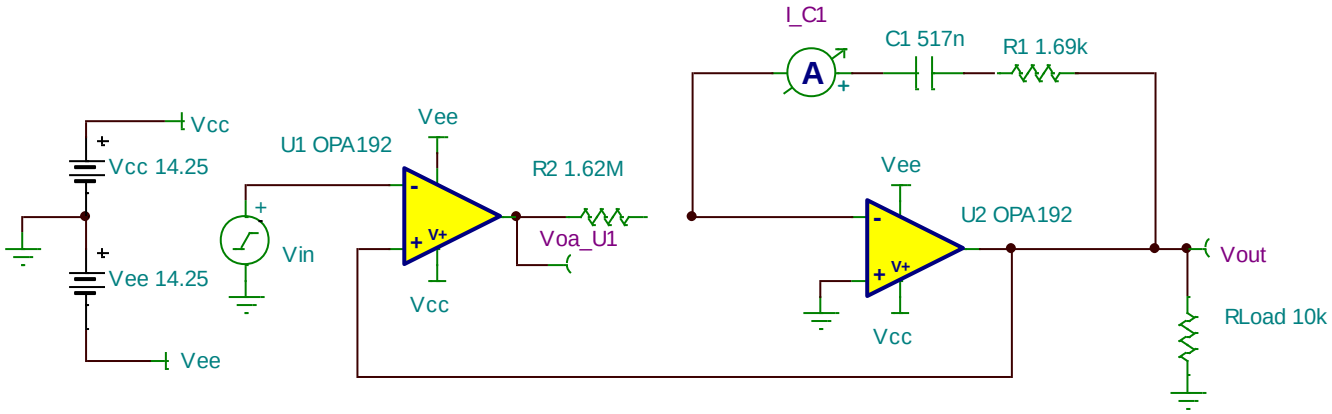


Figure 12: Worst Case Min Slew Rate Limiter Test Circuit

Figure 13 shows a 17V/s slew rate for worst case minimum slew rate limiter circuit values.

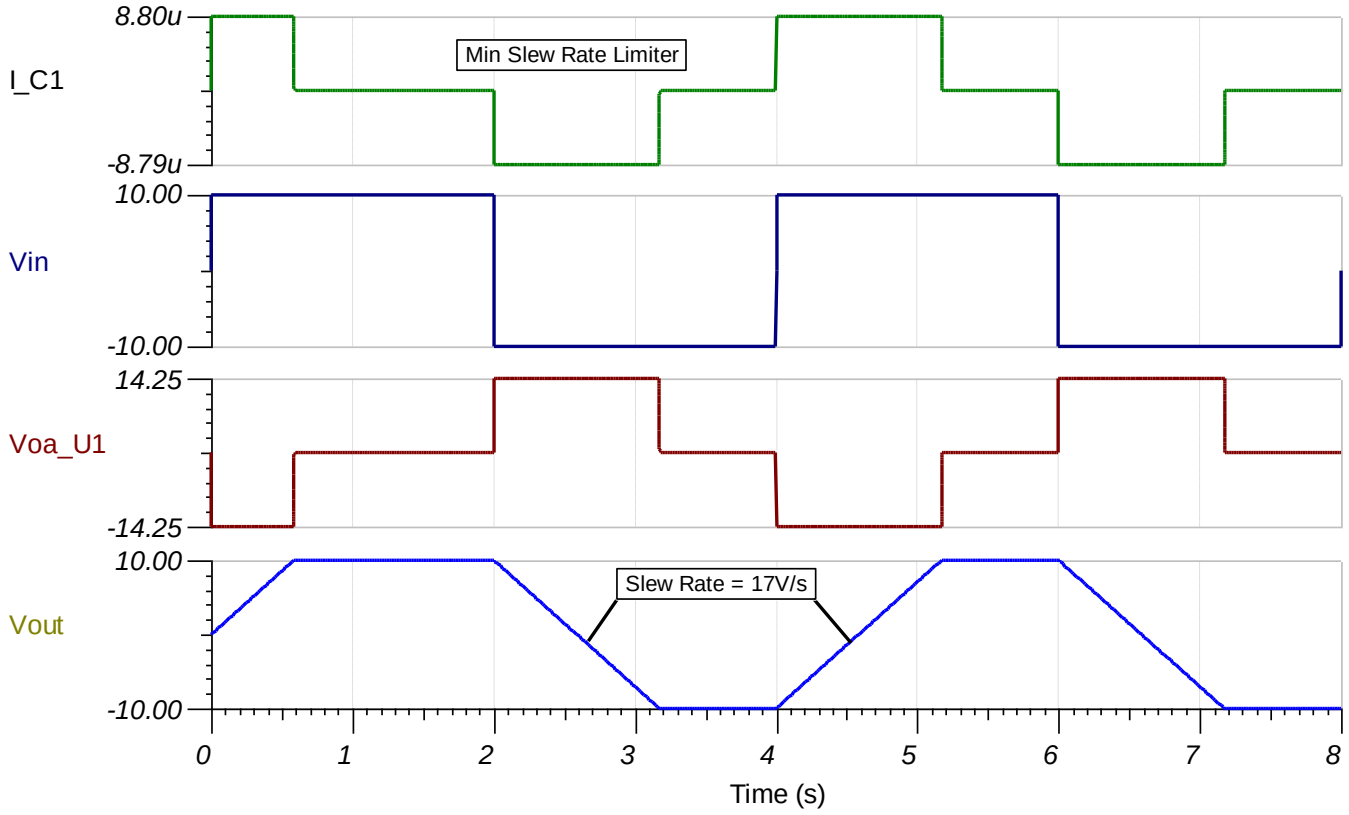


Figure 13: Worst Case Min Slew Rate Limiter Response

Figure 14 is the TINA-TI™ test circuit for worst case maximum slew rate limiter.

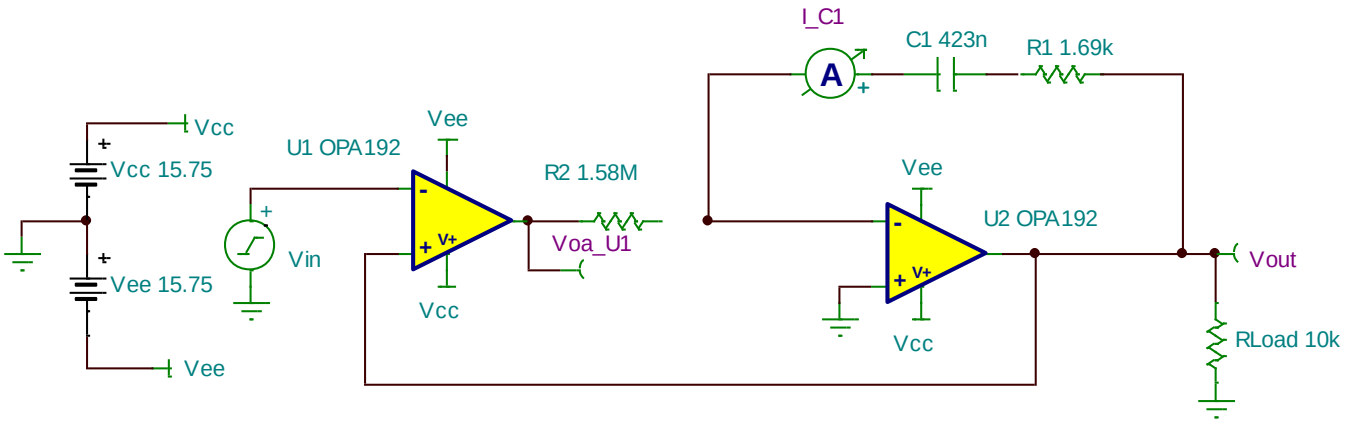


Figure 14: Worst Case Max Slew Rate Limiter Test Circuit

Figure 15 shows a 17V/μs slew rate for worst case maximum slew rate limiter circuit values.

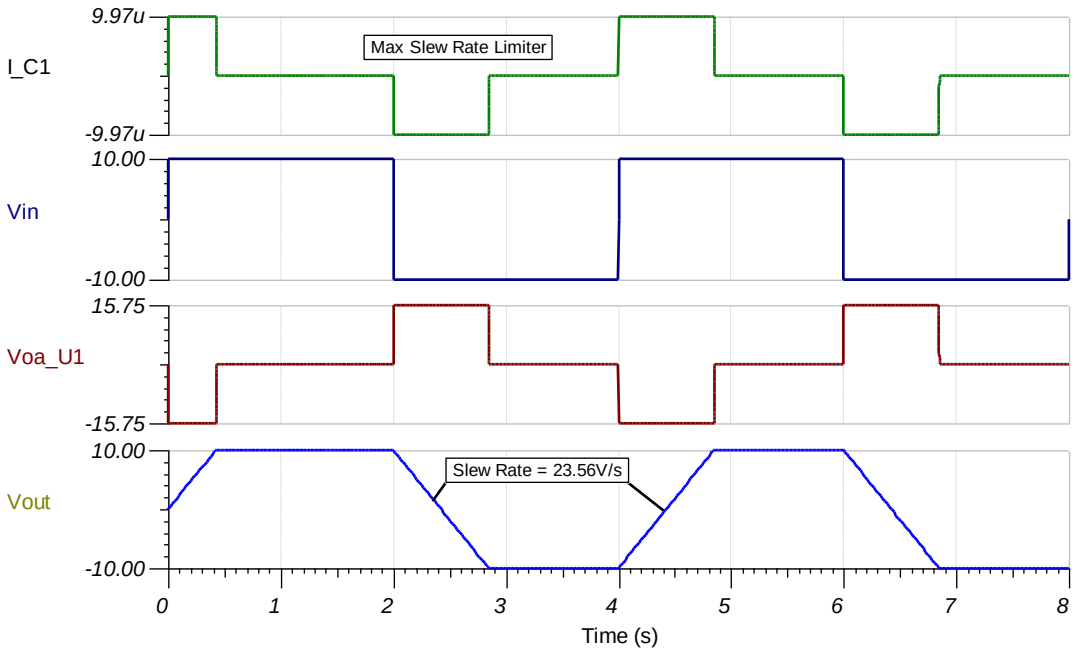


Figure 15: Worst Case Max Slew Rate Limiter Response

The test circuit of Figure 9 can also be used to show that our closed loop response of the composite amplifier is linear when it is not in the slew rate limit set by our op amp slew rate limiter. If we choose a frequency of 25mHz with an input amplitude of 10Vpp we will not be slew rate limited. We expect Vout to be a clean sinewave with gain of one times the input signal. In Figure 16 we see the results of such a simulation and indeed confirmation that our composite amplifier with the op amp slew rate limiter is a linear G=1 circuit when not in slew rate limit.

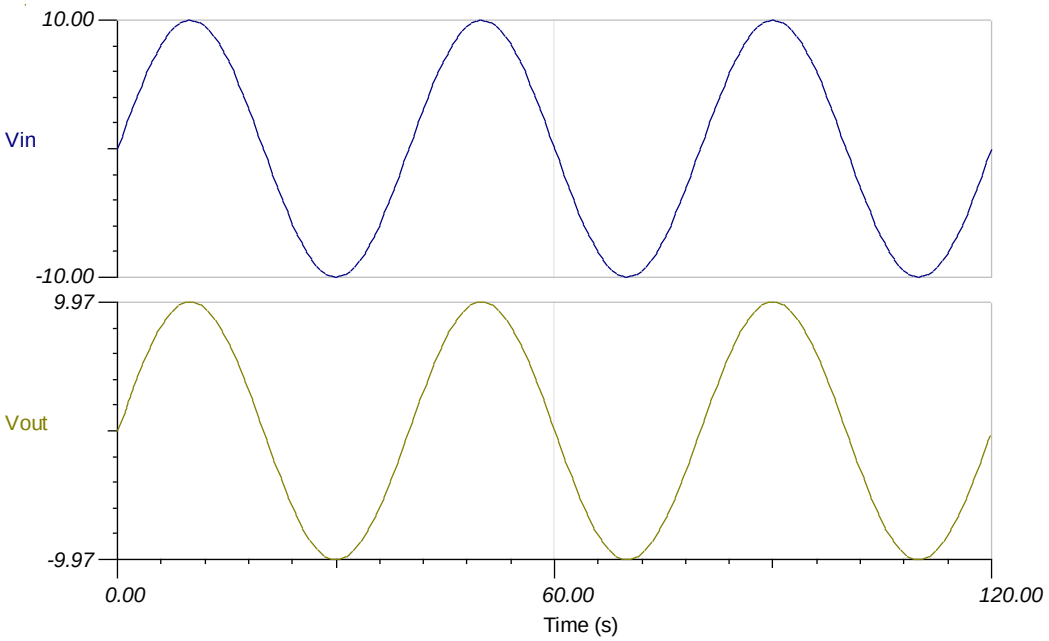
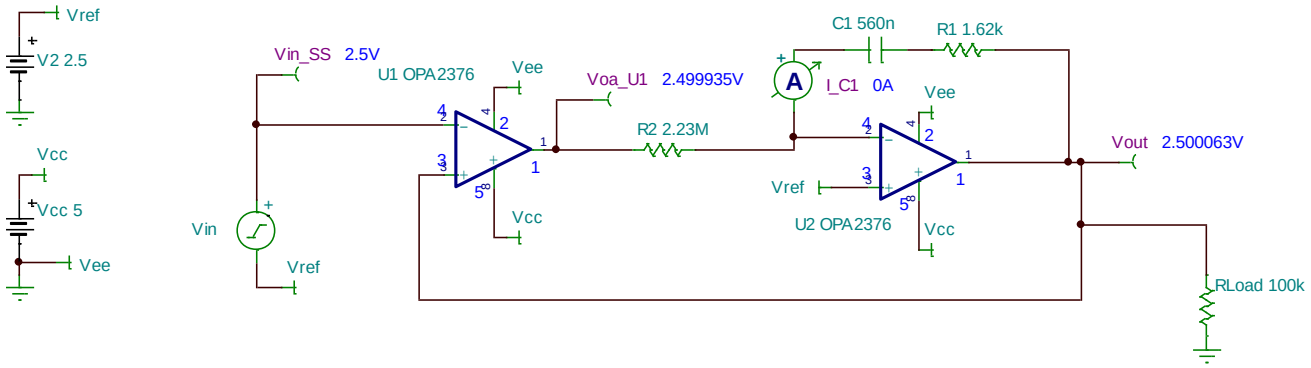


Figure 16: Linear Closed Loop Response at fin = 25mHz

5 Modifications

The slew rate limiter circuit can also be used in single supply applications as shown in Figure 17. There is a slight modification to the previously derived formula for the dual supply application. In many single supply applications there is a mid-supply reference point, Vref, to which the signal chain is referenced. In the circuit of Figure 17 this is the case. For this implementation the voltage swing out of U1, Voa_U1, will be positive and negative about the mid-supply point defined by Vref. In the previous dual supply application Vref=GND or 0V so there is no need to include it in the equations for slew rate computations. For this single supply application, using OPA2376 dual op amp, a 2V/s slew rate is achieved by setting C1=560nF and R2=2.23Mohm. With R1=1.62k a robust and stable circuit is designed. Stability analysis is the same for this single supply circuit as it was for the dual supply circuit (refer to Appendix A).



Final Value Selection:

$SR = 2V/s$

$$SR = \frac{I\_C1}{C1}$$

$$2\frac{V}{s} = \frac{I\_C1}{560nF} \rightarrow I\_C1 = 1.12\mu A$$

$$I\_C1 = \frac{(V\,supply - Vsat\_U1) - (Vref)}{R2}$$

$$1.12\mu A = \frac{(5V - 10mV) - 2.5V}{R2} \rightarrow R2 = 2.223M\Omega$$

Use R2 = 2.23MΩ (Standard Value)

Figure 17: Single Supply Application of the Op Amp Slew Rate Limiter

A large step transient analysis, shown in Figure 18, confirms that the single supply design yields the desired 2V/s slew rate.

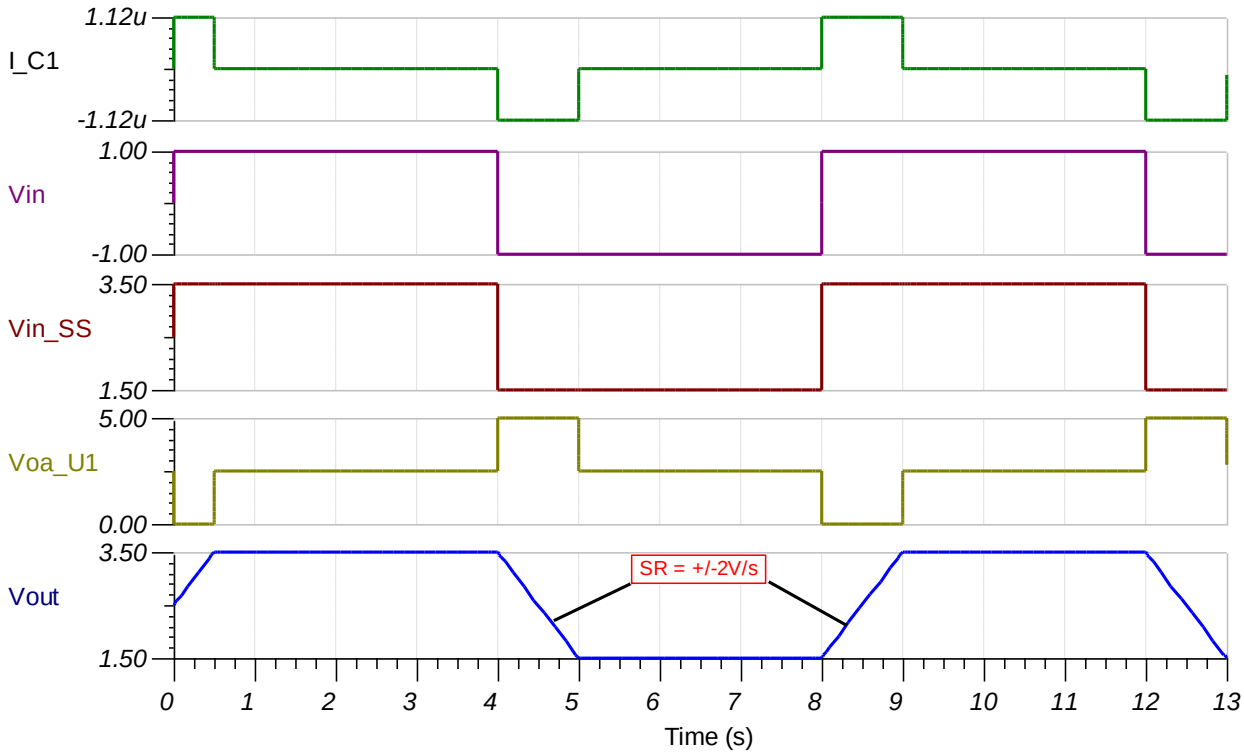


Figure 18: Single Supply Application Large Step Transient Results

6 About the Author

Tim Green is a Senior Analog Applications Engineer in Precision Analog Linear Applications at Texas Instruments Inc, Tucson Design Center. Tim has worked at Texas Instruments for over 8 years with roles as Strategic Marketing Engineer and Linear Applications Manager. His analysis and research into op amp open loop output impedance (Zo) and op amp stability have earned him the nickname “Wizard of Zo”, among his esteemed colleagues. His current focus is on optimizing op amp macromodels to match real silicon. He has over 31 years experience in brushless motor control, aircraft jet engine control, missile systems, power op amps, data acquisition systems, CCD cameras, power automotive audio, and analog/mixed signal semiconductors.

7 Acknowledgements & References

7.1 Acknowledgements

Special thanks to Thomas Kuehl, Senior Analog Applications Engineer, Texas Instruments, Tucson, Arizona, from whom the author stole this idea, with permission, to expand upon herein.

Appendix A.

A.1 Stability Analysis

A.2 U1 Stability Analysis with R1=0Ω

The slew rate limiter composite amplifier is designed for the desired overall slew rate, charging currents, and capacitor value, but must also be analyzed for stability. As can be seen in Figure A-1, the feedback for Vout, from Voa_U1, must pass through the closed loop transfer function of U2.The circuit shown in Figure A-1 will allow several key factors for stabilizing this composite amplifier to be analyzed. Loop gain analysis is an open loop ac analysis. LT is a short at dc and an open for any ac frequencies of interest. SPICE must compute a dc operating point before it performs an ac analysis. LT will allow SPICE to do this for dc and give us the open loop analysis we need during the ac Analysis. CT is an open for dc and a short for any ac frequencies of interest. Vtest is injected into the highest impedance side of LT, U1's +input (it makes no sense to drive an ac test signal into a low impedance). A complete walk all the way around the loop will result in reading loop gain at the lowest impedance side of LT, Vout. With this test circuit U1 Loop Gain, U1_Aol, and U1_1/β can be obtained. First analyze the circuit with R1=0ohms to enable the best choice of a value final for R1.

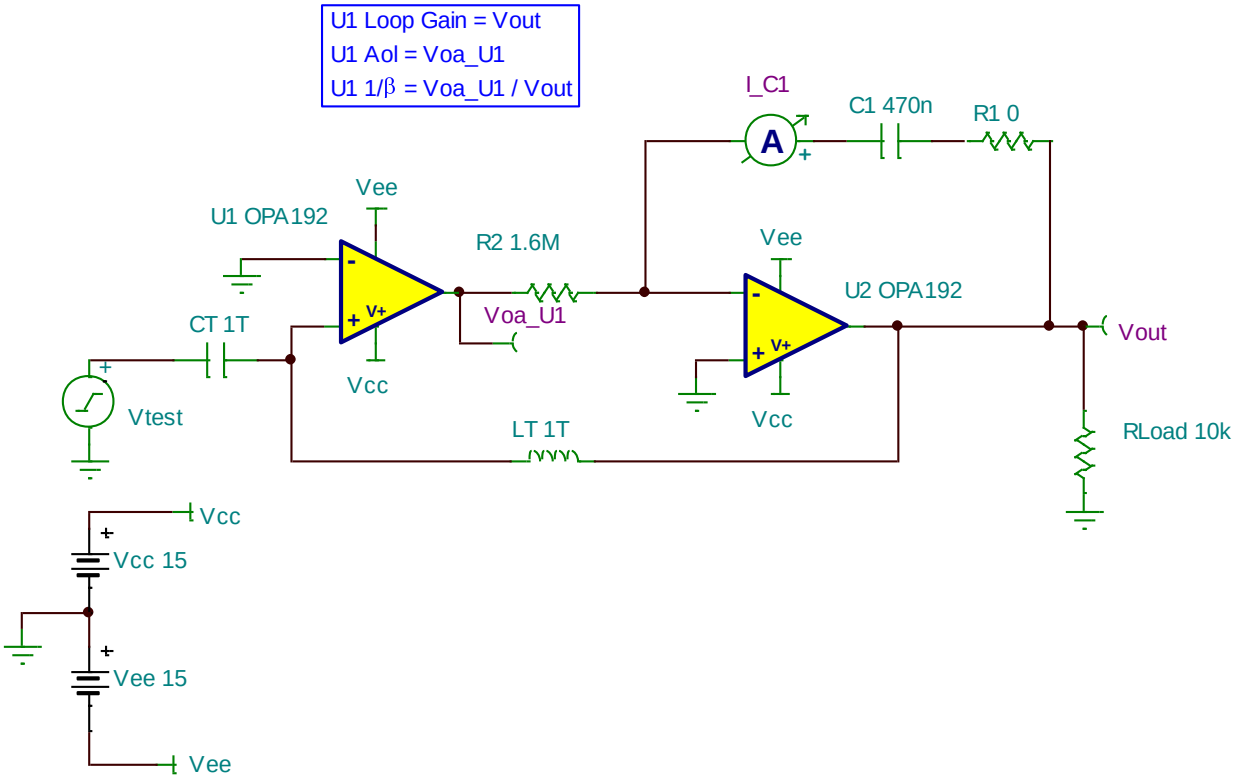


Figure A-1: U1 Stability Analysis Test Circuit with R1=0Ω

In Figure A-2 U1_Aol is plotted along with U1_1/β. At fcl, where U1_Al and U1_1/ β cross, loop gain goes to zero. For a stable op amp circuit, the rate-of-closure must be 20dB/decade. In this slide U1_Aol is -20dB/decade and U1_1/ β is +20dB/decade. The subtraction of these two slope results in -40dB/decade, or an unstable system. The sharp downward turn in the U1_1/ β plot in Figure A-2 can be ignored as this is a TINA-TI™ artifact of the math post-processing from ac analysis.

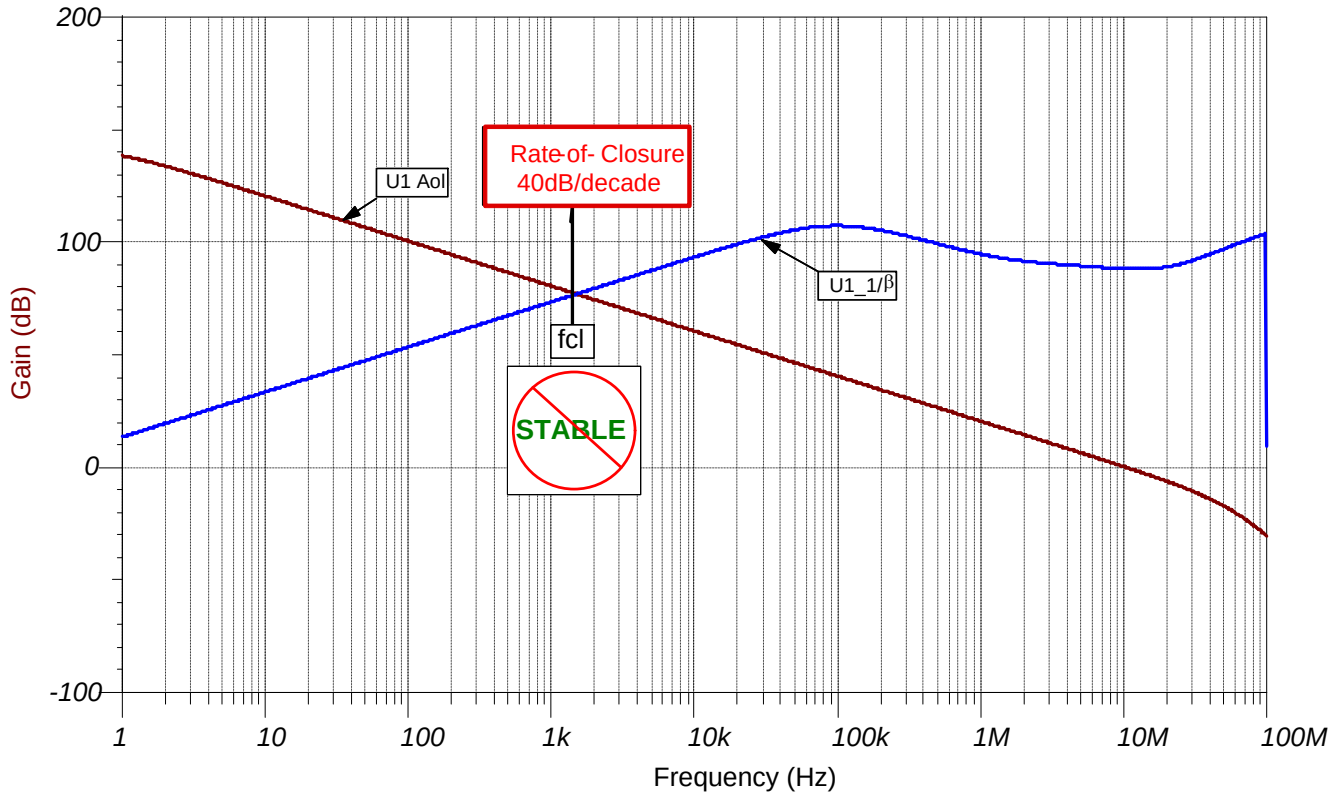


Figure A-2: U1_Aol and U1_1/β

A look at the loop gain plot, in Figure A-3, of the current circuit, shows at fcl, where loop gain goes to zero, the phase margin is almost zero (19 milli-degrees). Phase margin is how far the phase shift through the entire loop is away from 180 degrees. At least 45 degrees of phase margin is desired for a stable design.

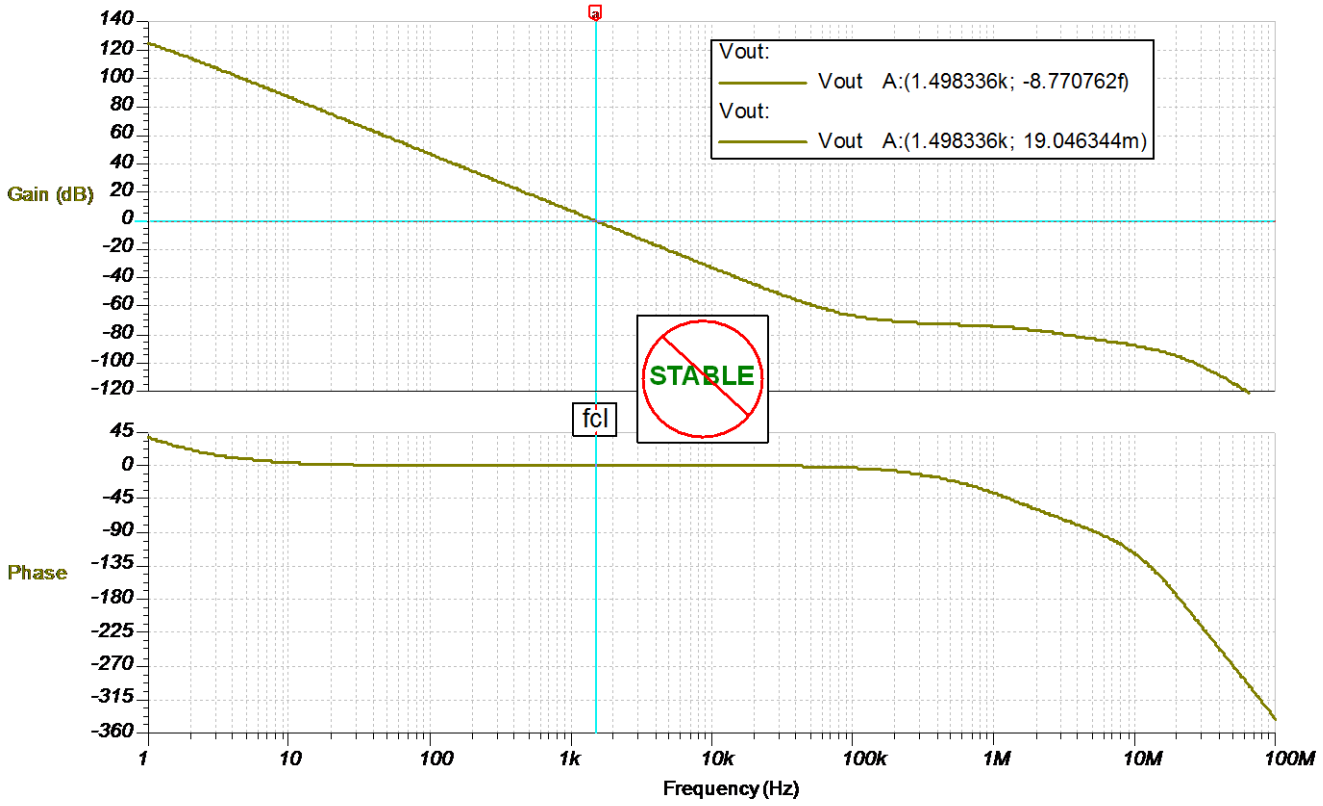


Figure A-3: U1 Loop Gain

The circuit shown in Figure A-4 will be used in a time domain or transient analysis to show that our current circuit is not stable. A small amplitude square wave of 100Hz will be injected into our composite amplifier in its closed loop configuration. We will look for overshoot and ringing as an indication of a marginally stable to unstable circuit.

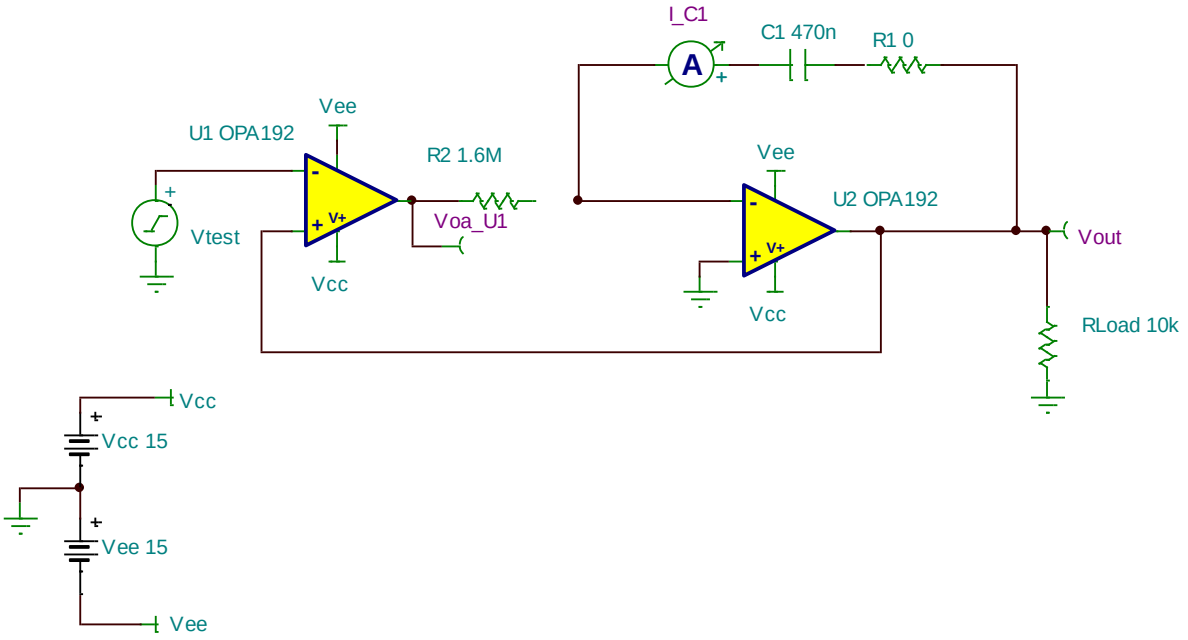


Figure A-4: Small Step Transient Analysis Test with R1=0Ω

From the TINA-TI™ SPICE Transient Analysis results in Figure A-5 there is undesired overshoot and ringing in the square wave test indicating a marginally stable to unstable circuit.

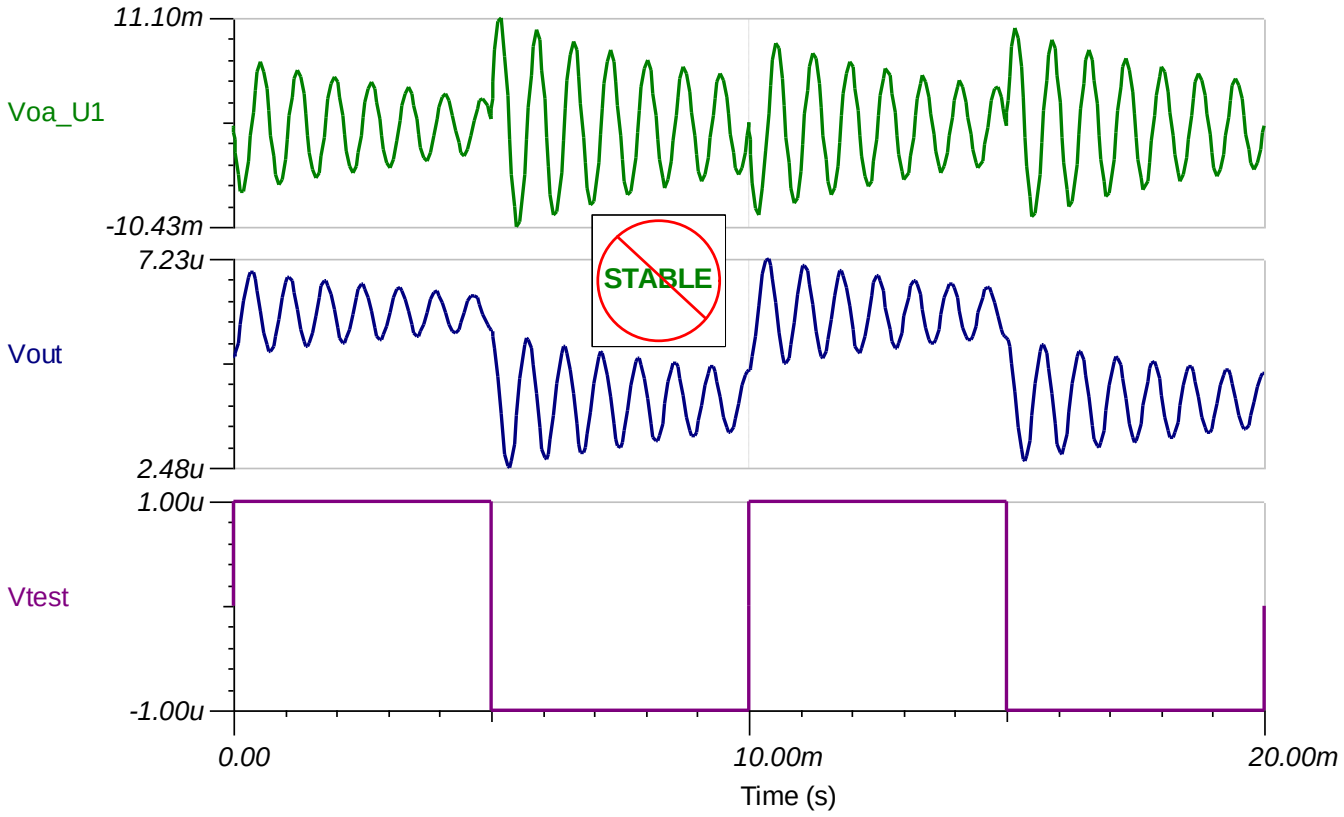


Figure A-5: Small Step Transient Analysis Results with R1=0Ω

A.3 U1 Stability Analysis with R1=1.69kΩ

From U1_Aol and U1_1/β plots a fix to this stability problem can be plotted. Modification of U1_1/ β, as shown in Figure A-6, will cause the intersection at U1_Aol to be a rate-of-closure that is 20dB/decade, at fcl, indicating a good stable circuit. Place fp1 in the U1_1/ β curve at least one decade away from fcl. This ensures that as Aol varies from lot-to-lot and over temperature it will never intersect the new U1_1/ β at 40dB/decade rate-of-closure. A good rule-of-thumb is that the Aol UGBW (Unity Gain Bandwidth) can be x½ or x2 its typical value, over process and temperature variations.

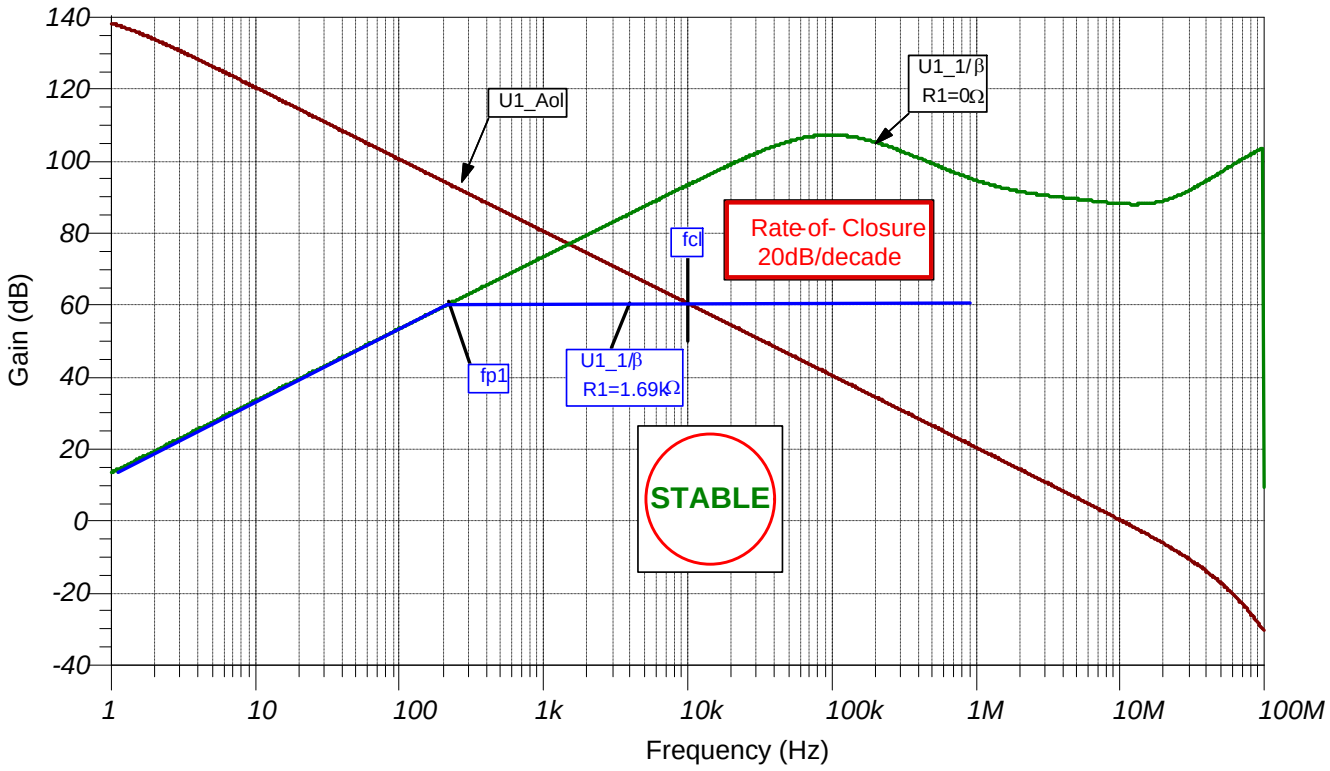
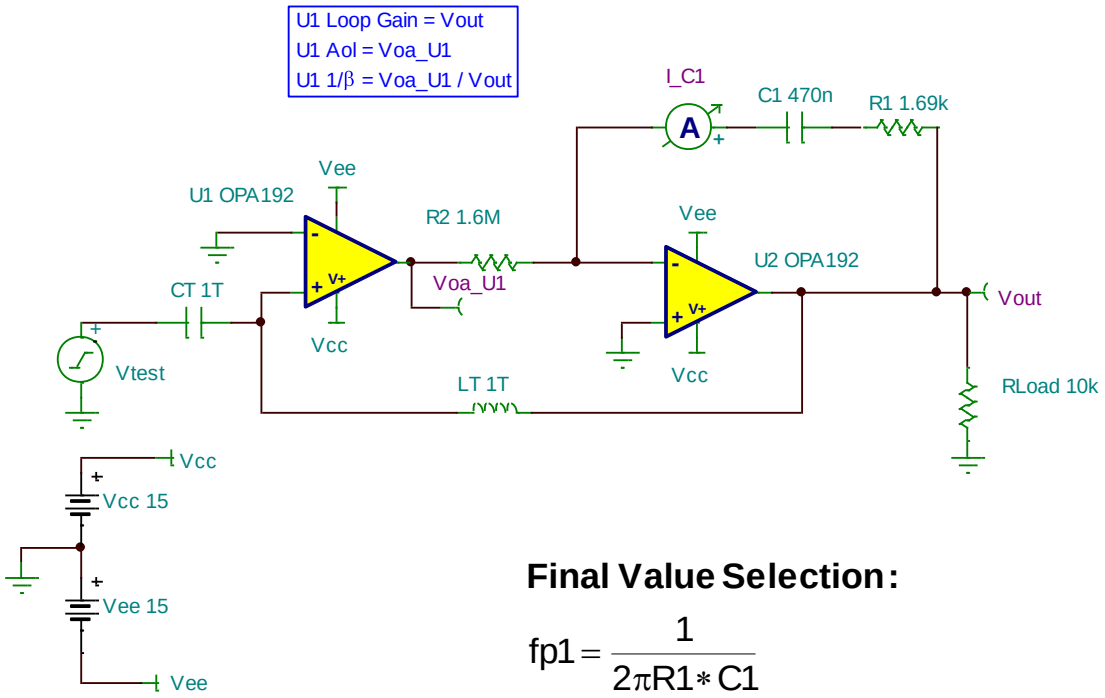


Figure A-6: Modify U1_1/β with R1=1.69kΩ

Based on the desired fp1 location in the U1_1/β plot, R1 can be computed as shown In Figure A-7. The test circuit in Figure A-7 will be used to confirm that U1_1/β is now designed for good stability.



Final Value Selection:

$$fp1 = \frac{1}{2\pi R1 * C1}$$

$$200Hz = \frac{1}{2\pi R1 * 470nF} \rightarrow R1 = 1.693k\Omega$$

Use R2 = 1.69kΩ (Standard Value)

Figure A-7: U1 Stability Analysis Test Circuit with R1=1.69kΩ

Results of the new U1_1/β on U1_Aol are shown in Figure A-8. There is the desired 20dB/decade rate-of-closure at fcl where loop gain will be zero.

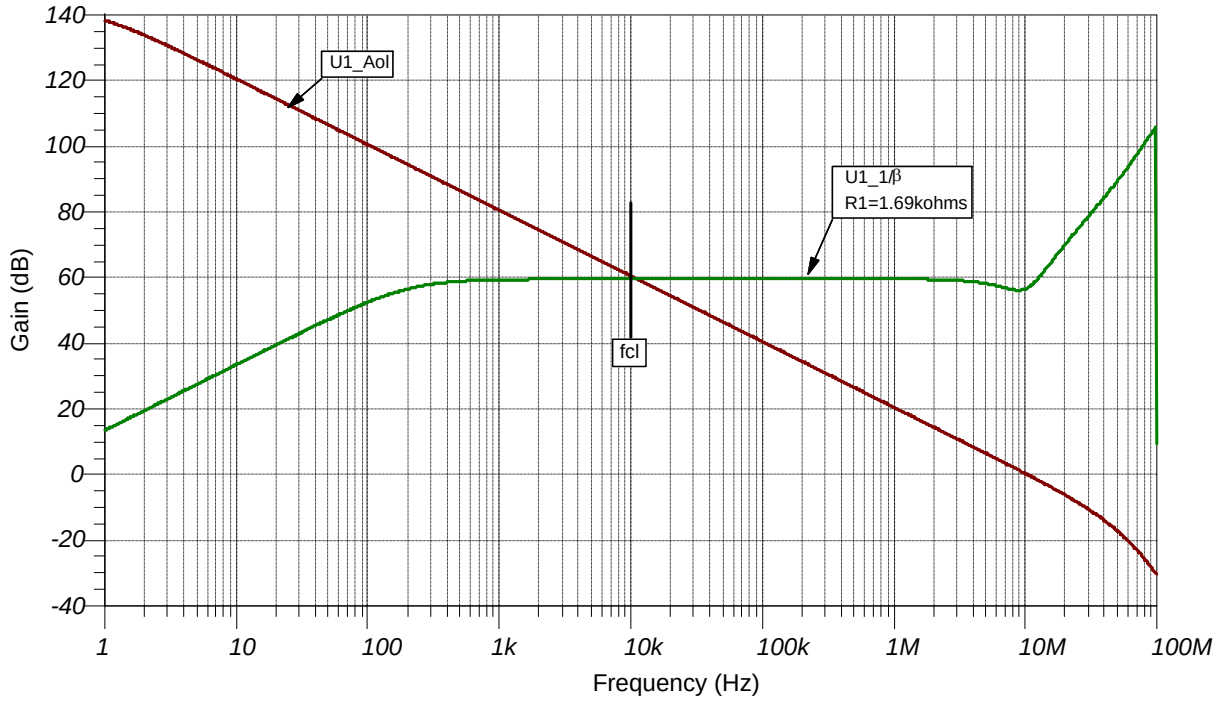


Figure A-8: U1 Stability Analysis Test Results with R1=1.69kΩ

A loop gain plot in Figure A-9, using the new value for R1 of 1.69kΩ, shows that at fcl, where loop gain goes to zero, there is over 88 degrees of phase margin. Note also that the loop gain phase plot never dips below zero degrees, and other slopes are +/45 degrees/decade (indicates no complex conjugate poles with sharp phase drop in narrow frequency band). And also note the loop gain phase dip to almost zero is at least a decade away from fcl. All of this predicts a good and stable design.

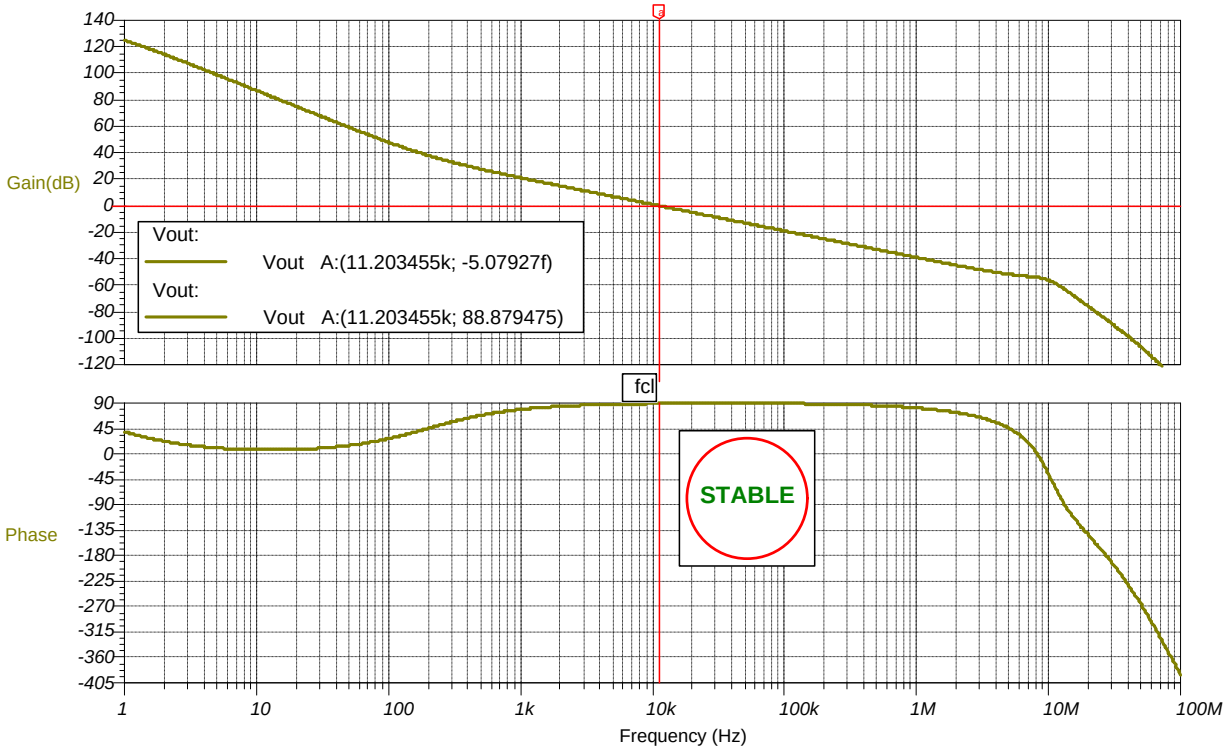


Figure A-9: U1 Loop Gain with R1=1.69kΩ

A.4 U2 Stability Analysis with R1=1.69kΩ

U1 has been compensated to be stable. A check must also be performed on U2 to ensure it is stable by loop gain analysis. The loop gain test circuit for U2 is shown in Figure A-10.

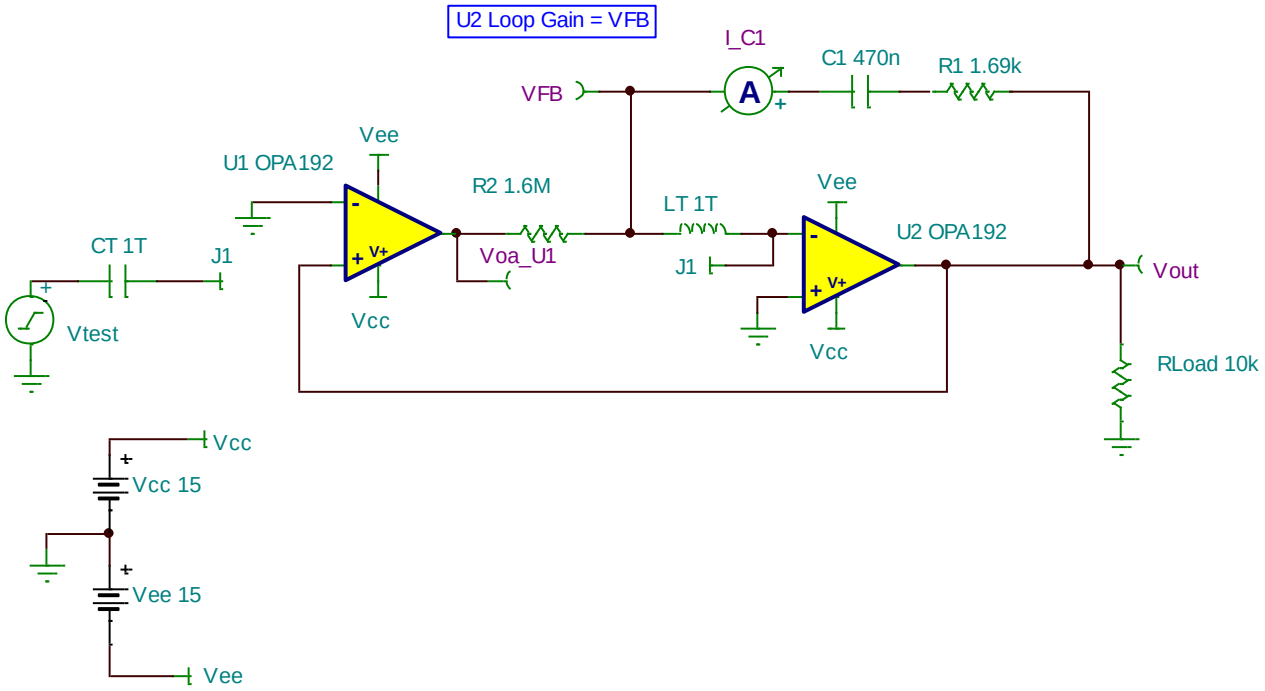


Figure A-10: U2 Stability Analysis Test Circuit with R1=1.69kΩ

The loop gain test results, in Figure A-11, for U2 show a good stable design with phase margin of 68 degrees at fcl. Also note loop gain phase shifts of only +/-45 degrees/decade. Loop gain phase shift never dips below 0 degrees and its lowest dip is at least a decade away from fcl. All of this predicts a stable composite design.

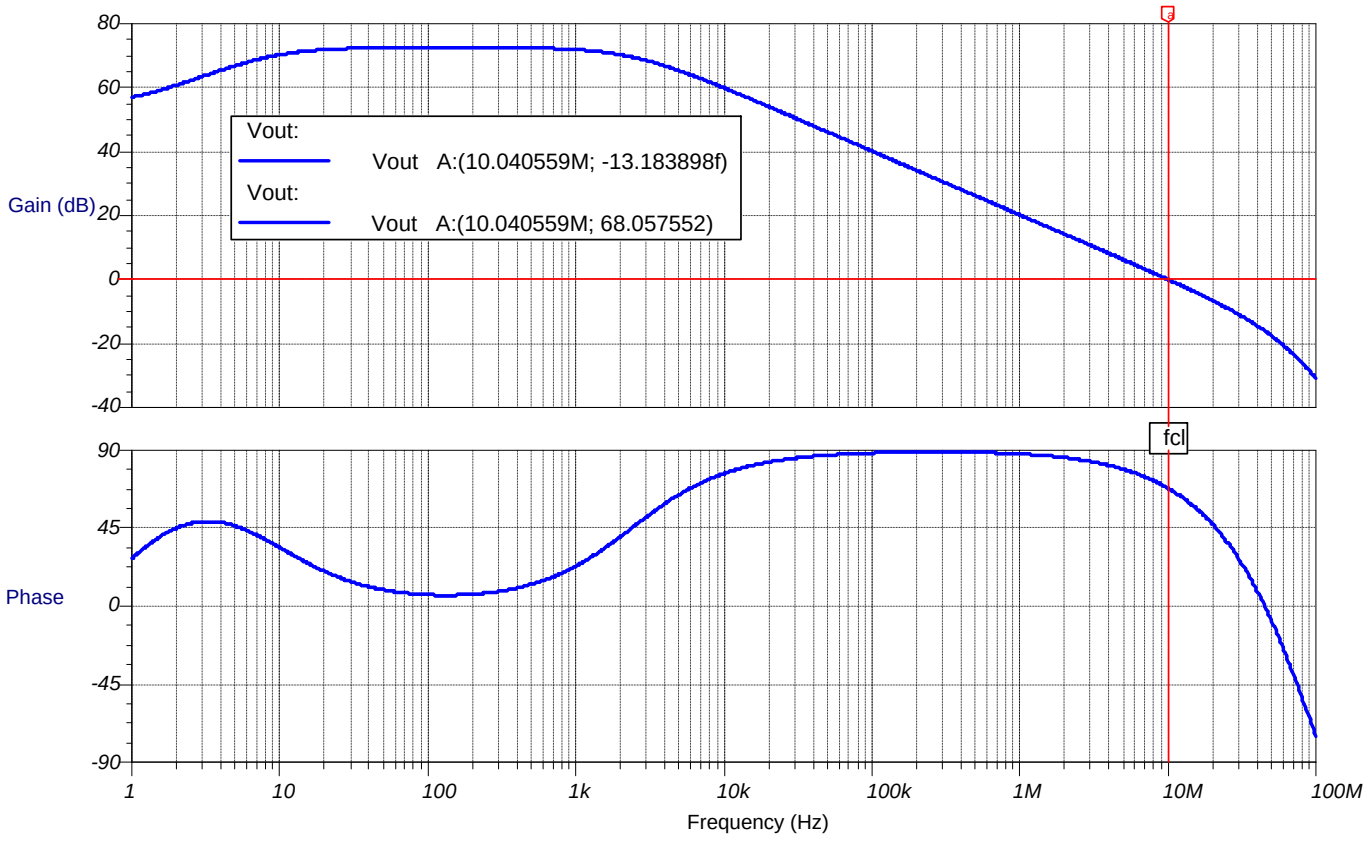


Figure A-11: U2 Loop Gain with R1=1.69kΩ

To double check the final stability compensation with R1=1.69kohms a transient analysis will be run using the circuit in Figure A-12, with a low amplitude peak-to-peak signal source, that uses a fast rise/fall time.

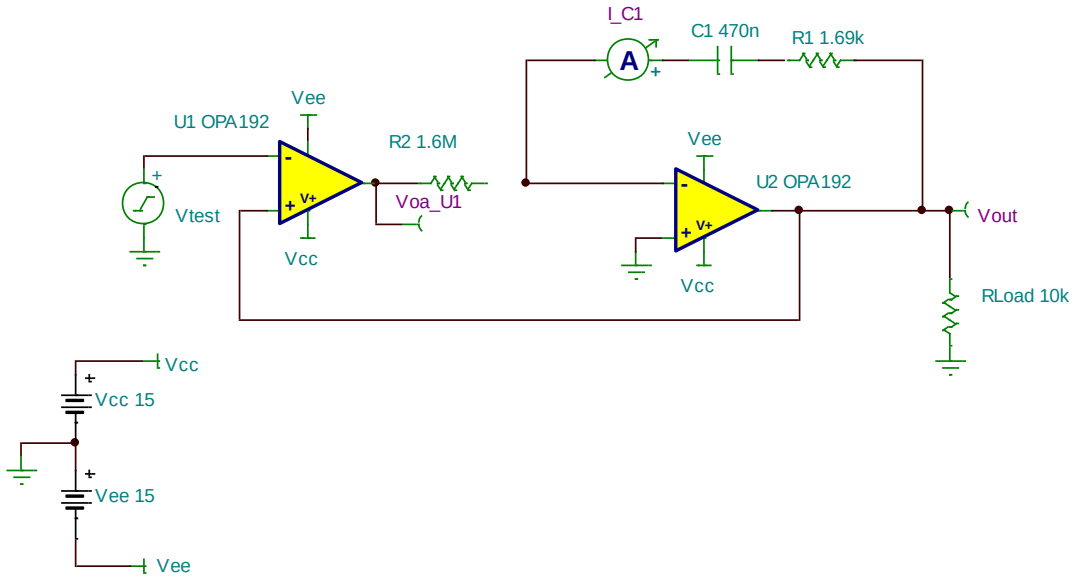


Figure A-12: Small Step Transient Analysis Test with R1=1.69kΩ

The results of the transient analysis, in Figure A-12, for R1=1.69kΩ, show no ringing or oscillations confirming that the entire design is now robust and stable. The voltage overshoot on Voa_U1 is not the traditional voltage overshoot followed by ringing used to determine open loop phase margin, based on a small amplitude closed loop transient. The voltage overshoot is caused by a step change of current as a result of closed loop feedback trying to keep up with an abrupt change in input signal.

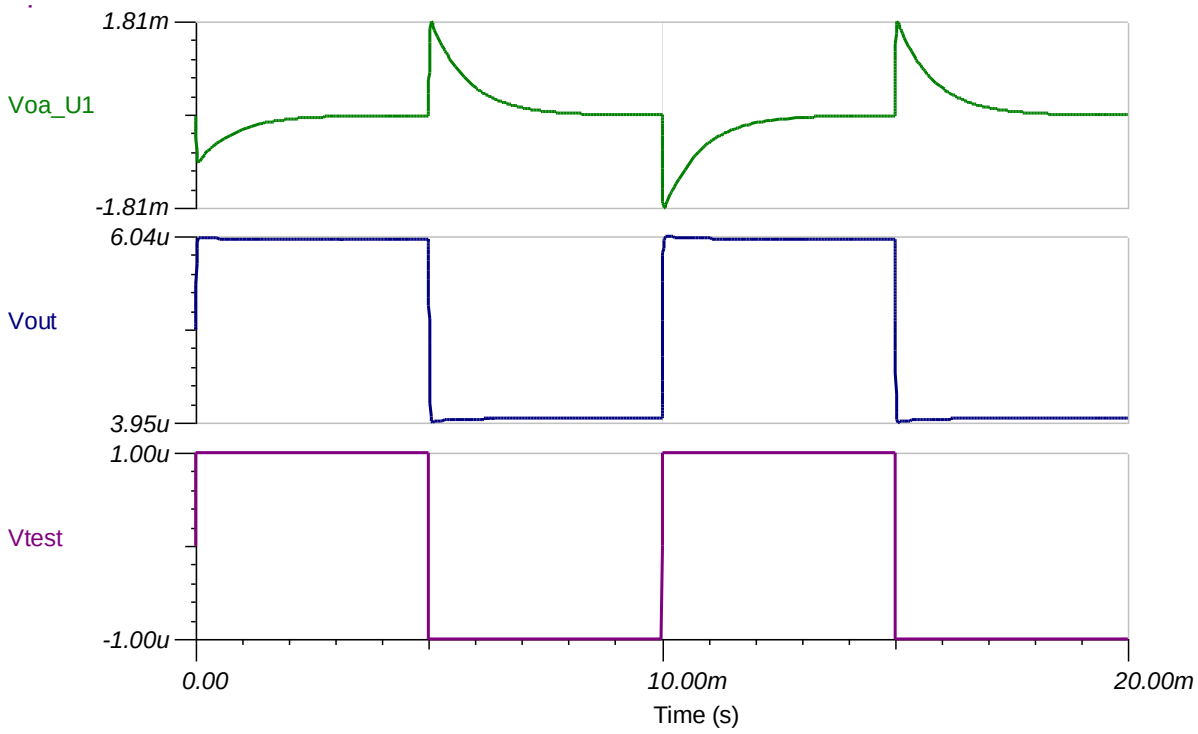


Figure A-12: Small Step Transient Analysis Results with R1=1.69kΩ

A.5 Closed Loop Response

From Figure A-6 the closed loop response of the composite amplifier can be predicted. In Figure A-13 Figure A-6 is repeated and, by inspection, U1_Aol crosses U1_1/β at fcl, where loop gain goes to zero. When loop gain goes to zero there is no way to correct for errors and the output of the composite amplifier will follow U1's Aol curve down at higher frequencies. This prediction is shown in Figure A-13 as "Closed Loop Vout/Vin".

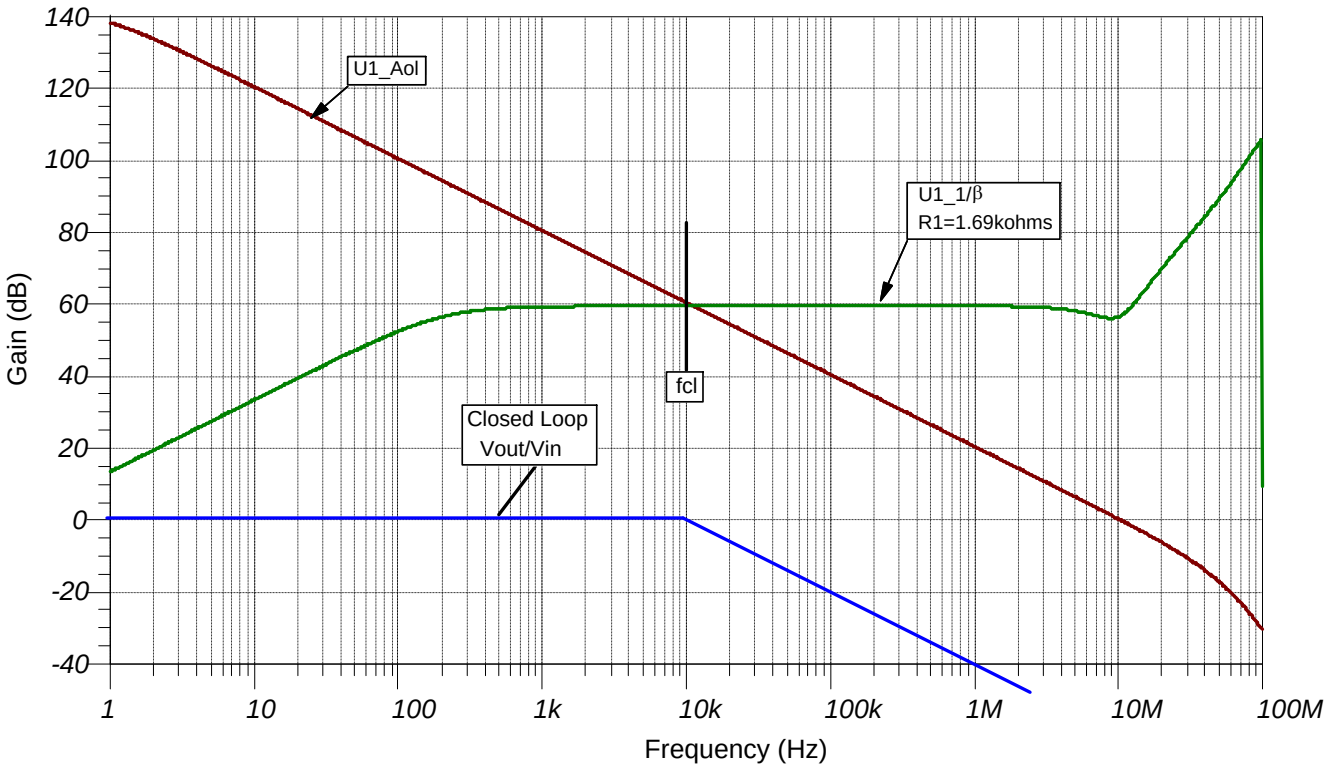


Figure A-13: Predict Overall Closed Loop Response

The circuit of Figure A-14 is used to test the closed loop ac response, Vout/Vin, of the complete composite amplifier

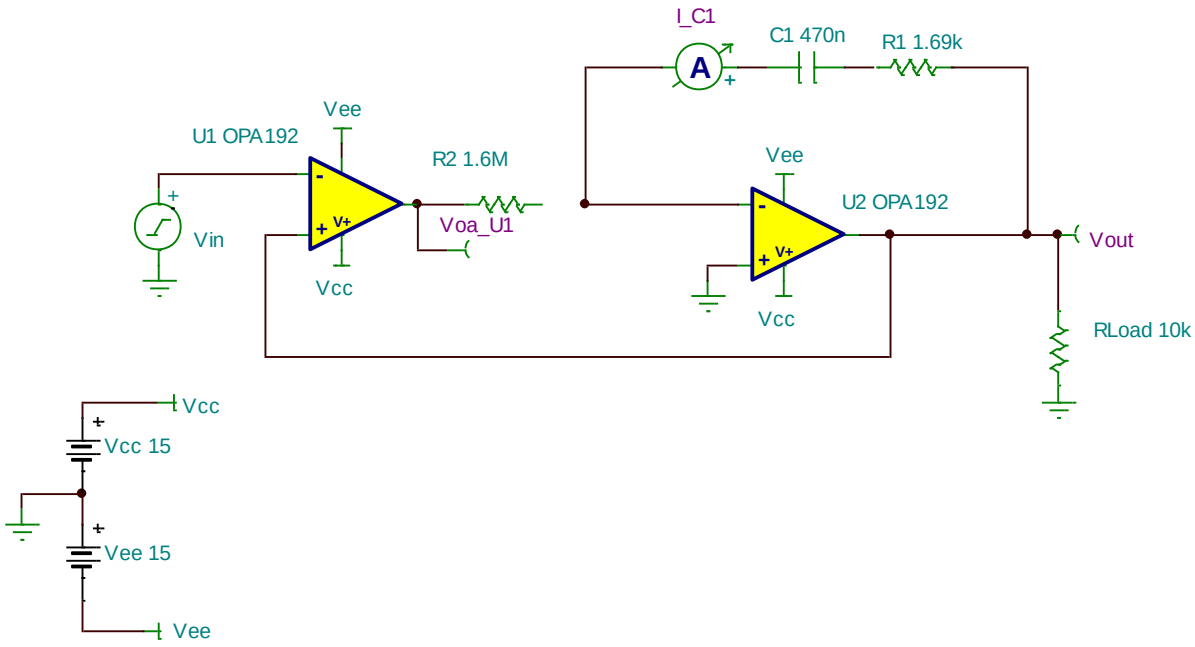


Figure A-14: Closed Loop Response Test Circuit

Figure A-15 shows the test results of the closed loop AC response, Vout/Vin, of the entire composite amplifier. A comparison of Figure A-15 to the prediction in Figure A-13 confirms that the closed loop AC response matches closely to predictions.

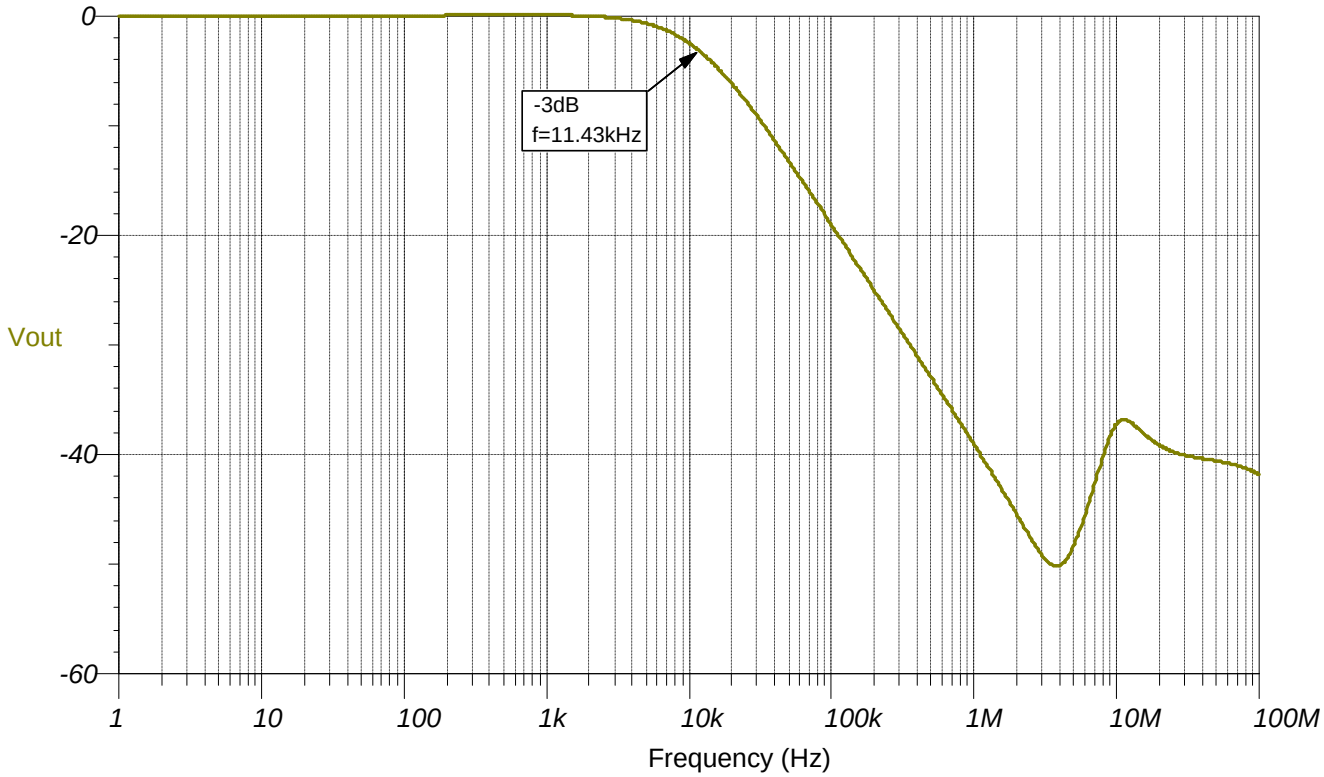


Figure A-15: Closed Loop

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