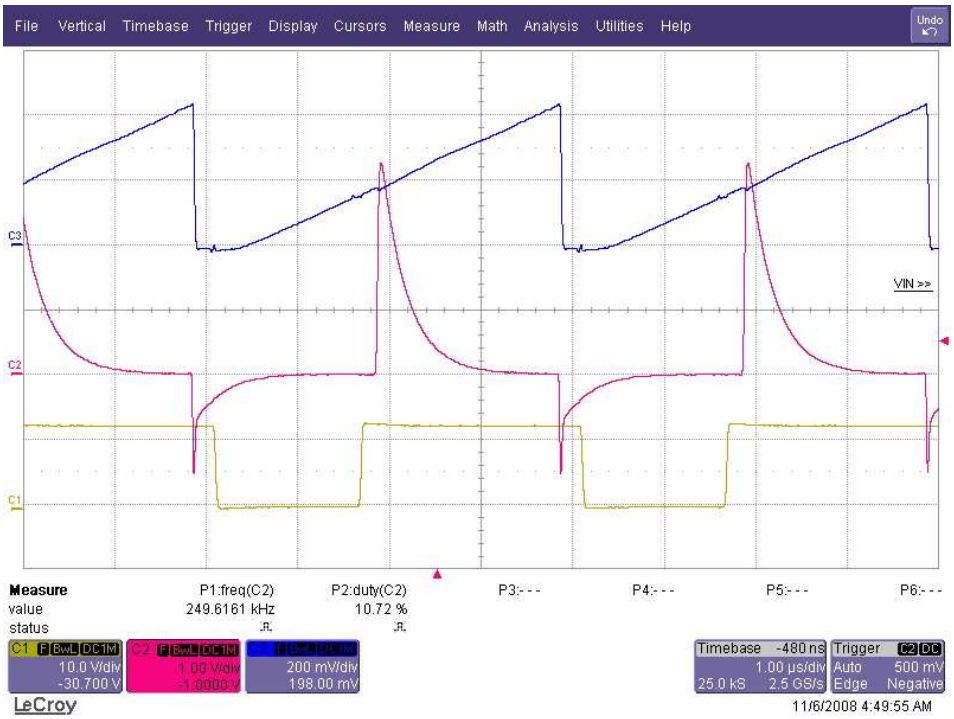
1 Main Waveforms

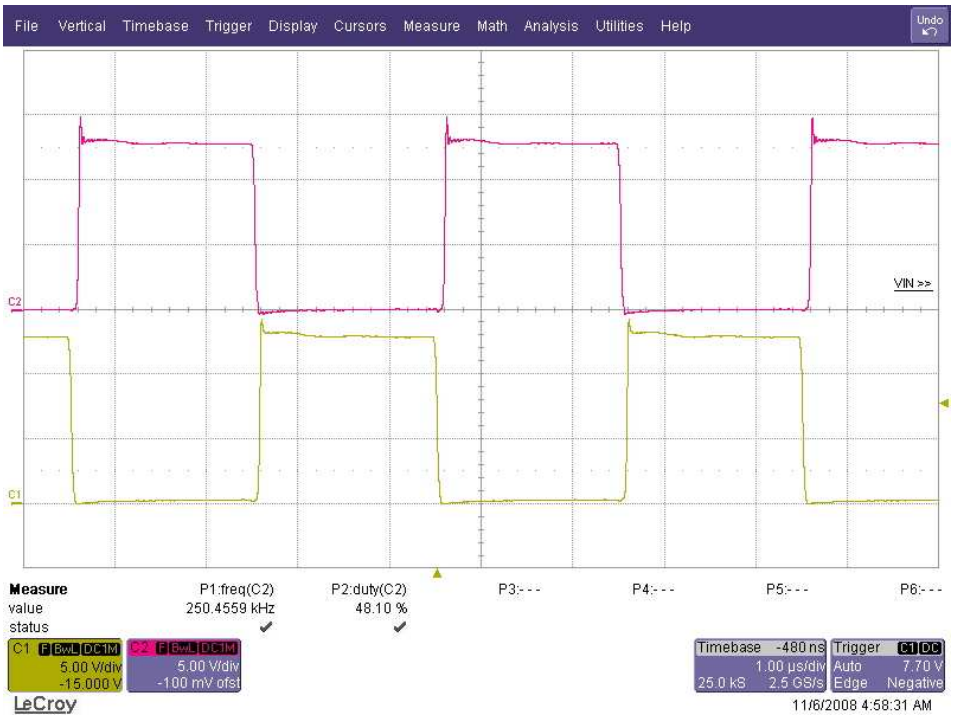


Synchronization Circuit 1: Out U3-TLC555D (C1), Gate of Q4 (C2), Synch_Master signal (C3)

Synchronization Circuit 2: Out U3-TLC555D (C1), Synch_Master signal (C3), Synch Slave (C4)

Current Sharing 1 (Iout<0.5A Vin=9V): VdsQ1, VdsQ2

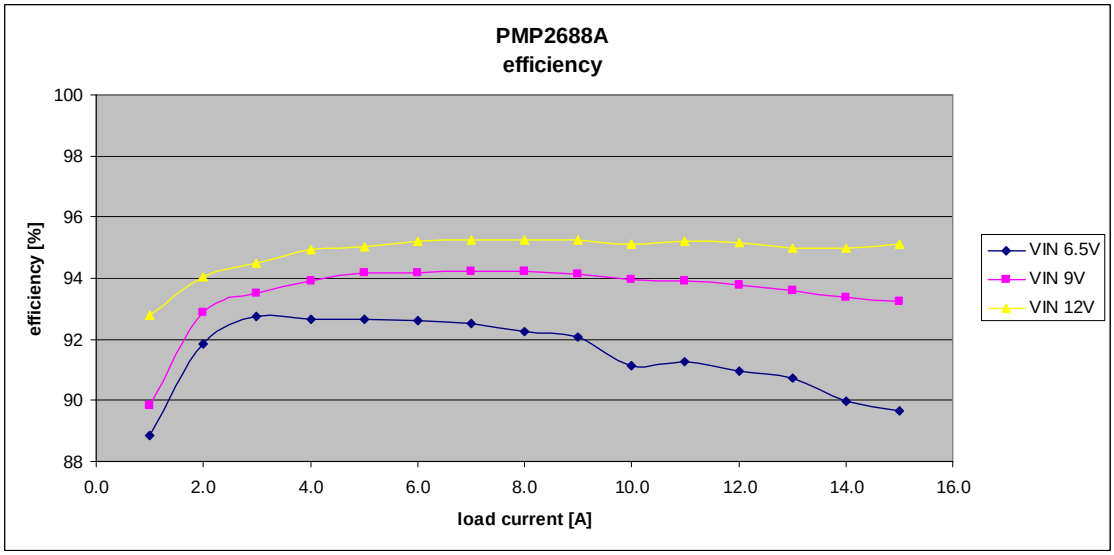
Current Sharing 2 (Iout<0.15A Vin=6.5V): VdsQ1 (C1), VdsQ2 (C2)



Current Sharing 3 (Iout=10A Vin=6.5V): VdsQ1 (C1), VdsQ2 (C2)

Current Sharing 4 (Vin=9V Iout=5A): CsenseQ1 (C1), Vsense Q2 (C2)

2 Efficiency and Load Regulation



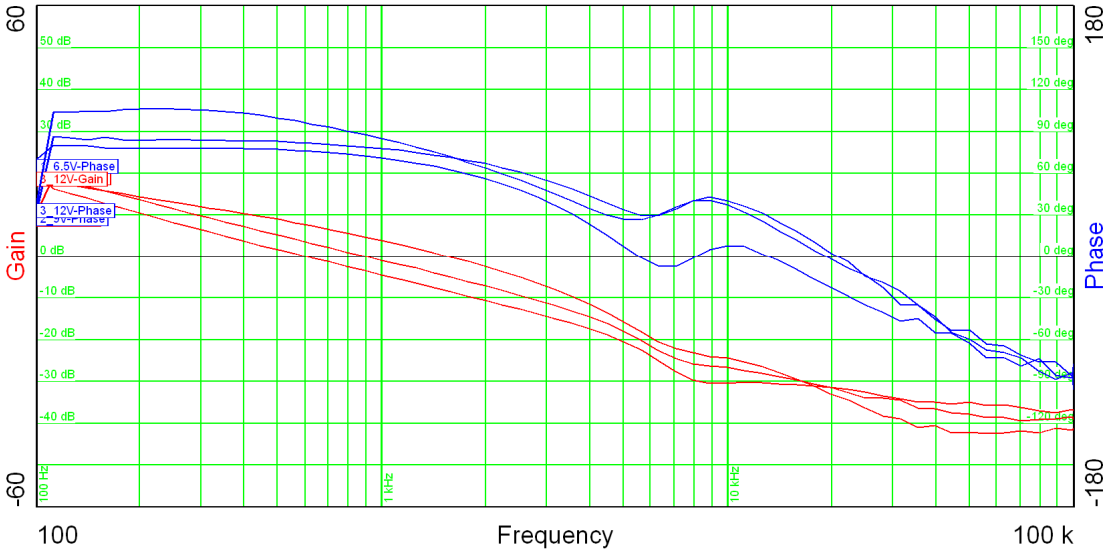
The following table shows the measured values:

voltage [V]	input current [A]	power [W]	voltage [V]	output current [A]	power [W]	efficiency [%]
6.50	2.14	13.91	12.36	1.00	12.36	88.9
6.50	4.14	26.91	12.36	2.00	24.72	91.9
6.50	6.15	39.98	12.36	3.00	37.08	92.8
6.50	8.21	53.37	12.36	4.00	49.44	92.6
6.50	10.26	66.69	12.36	5.00	61.80	92.7
6.50	12.32	80.08	12.36	6.00	74.16	92.6
6.50	14.39	93.54	12.36	7.00	86.52	92.5
6.50	16.49	107.19	12.36	8.00	98.88	92.3
6.50	18.60	120.90	12.37	9.00	111.33	92.1
6.50	20.88	135.72	12.37	10.00	123.70	91.1
6.50	22.94	149.11	12.37	11.00	136.07	91.3
6.50	25.11	163.22	12.37	12.00	148.44	90.9
6.50	27.28	177.27	12.37	13.00	160.81	90.7
6.48	29.74	192.63	12.38	14.00	173.32	90.0
6.47	32.03	207.11	12.38	15.00	185.70	89.7
9.00	1.53	13.77	12.37	1.00	12.37	89.8
9.00	2.96	26.64	12.37	2.00	24.74	92.9
9.00	4.41	39.69	12.37	3.00	37.11	93.5
9.00	5.85	52.65	12.36	4.00	49.44	93.9
9.00	7.29	65.61	12.36	5.00	61.80	94.2
9.00	8.75	78.75	12.36	6.00	74.16	94.2
9.00	10.21	91.89	12.37	7.00	86.59	94.2
9.00	11.67	105.03	12.37	8.00	98.96	94.2

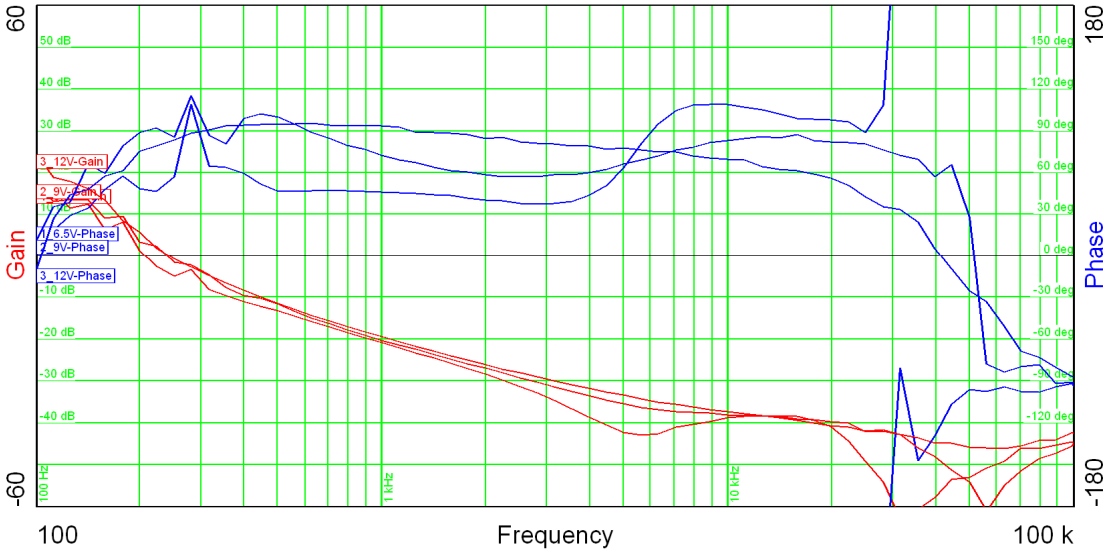
9.00	13.14	118.26	12.37	9.00	111.33	94.1
9.00	14.63	131.67	12.37	10.00	123.70	93.9
8.99	16.11	144.88	12.37	11.00	136.07	93.9
9.00	17.59	158.31	12.37	12.00	148.44	93.8
9.03	19.02	171.79	12.37	13.00	160.81	93.6
9.02	20.55	185.44	12.37	14.00	173.18	93.4
9.02	22.07	199.01	12.37	15.00	185.55	93.2
12.00	1.11	13.32	12.36	1.00	12.36	92.8
12.00	2.19	26.28	12.36	2.00	24.72	94.1
12.00	3.27	39.24	12.36	3.00	37.08	94.5
12.00	4.34	52.08	12.36	4.00	49.44	94.9
12.00	5.42	65.04	12.36	5.00	61.80	95.0
12.00	6.49	77.88	12.36	6.00	74.16	95.2
12.00	7.57	90.84	12.36	7.00	86.52	95.2
12.00	8.65	103.80	12.36	8.00	98.88	95.3
12.00	9.73	116.76	12.36	9.00	111.24	95.3
12.00	10.83	129.96	12.36	10.00	123.60	95.1
12.10	11.80	142.78	12.36	11.00	135.96	95.2
12.10	12.88	155.85	12.36	12.00	148.32	95.2
12.05	14.04	169.18	12.36	13.00	160.68	95.0
12.04	15.13	182.17	12.36	14.00	173.04	95.0
12.04	16.19	194.93	12.36	15.00	185.40	95.1

3 Control Loop Frequency Response

The figures below show the open loop response for 6.5V, 9V, 12V input voltage

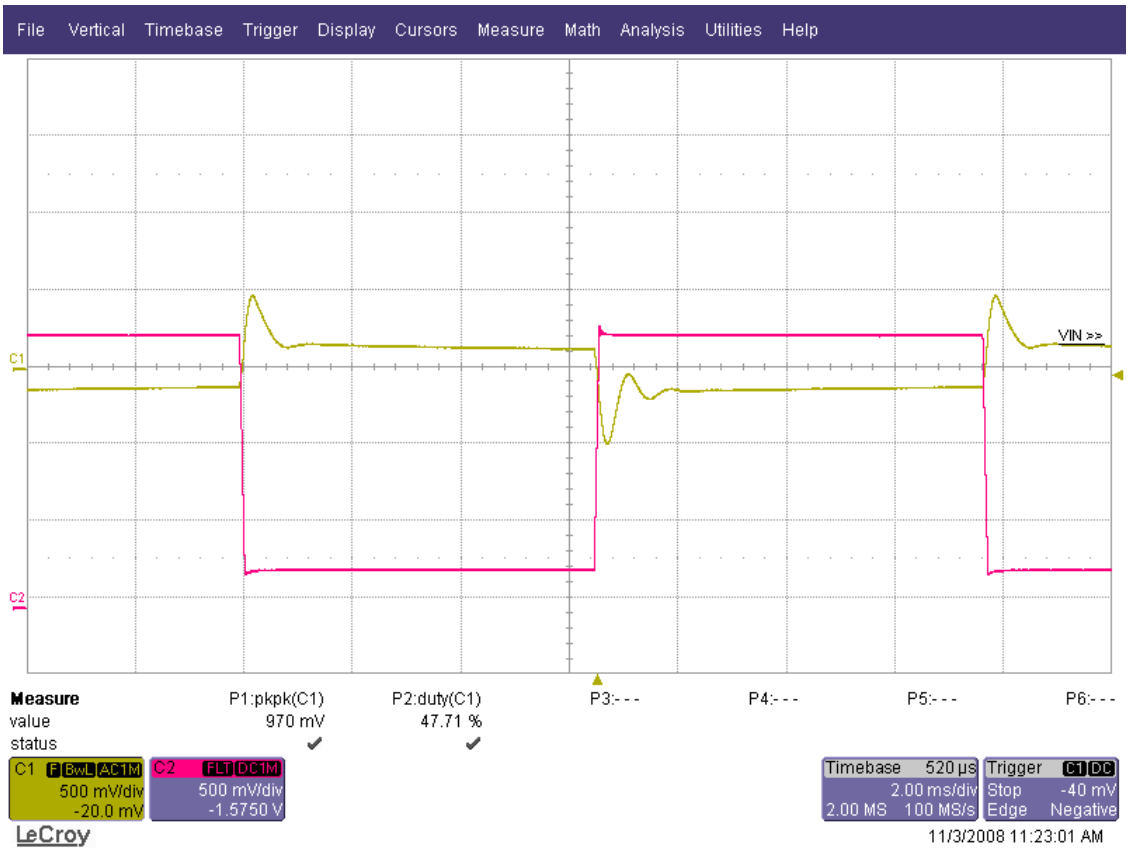


Vin=6.5V, Vin=9V, Vin=12V @ 15A Output



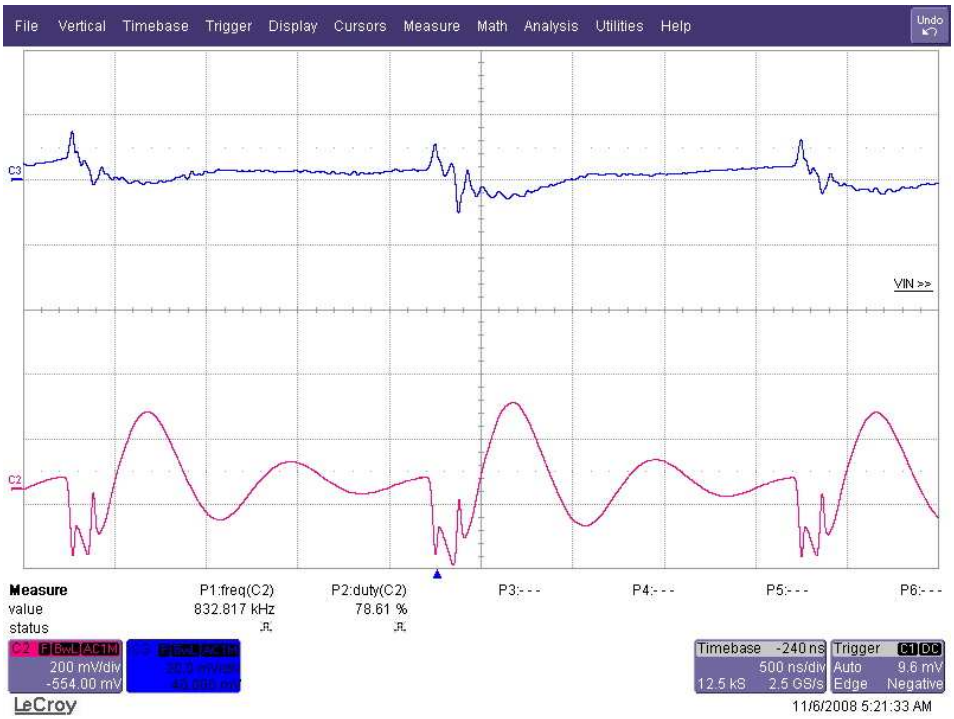
Vin=6.5V, Vin=9V, Vin=12V @ Discontinous Mode (no load)

4 Load Transients

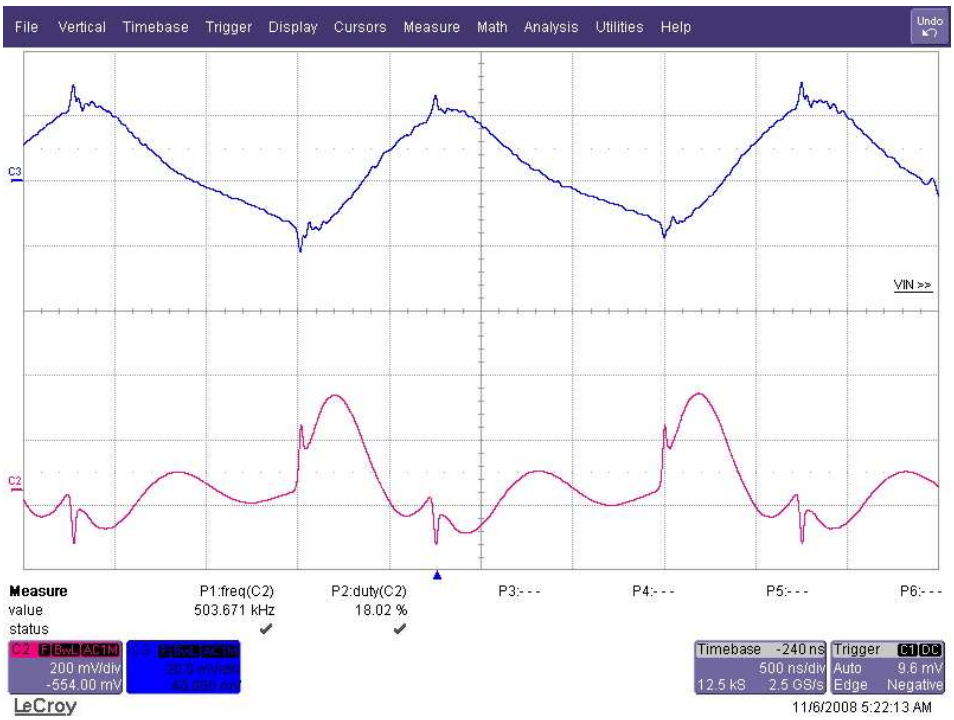


Vout (C1), Iout (C2, 10A/V current probe)

5 Output and Input Ripple Voltage



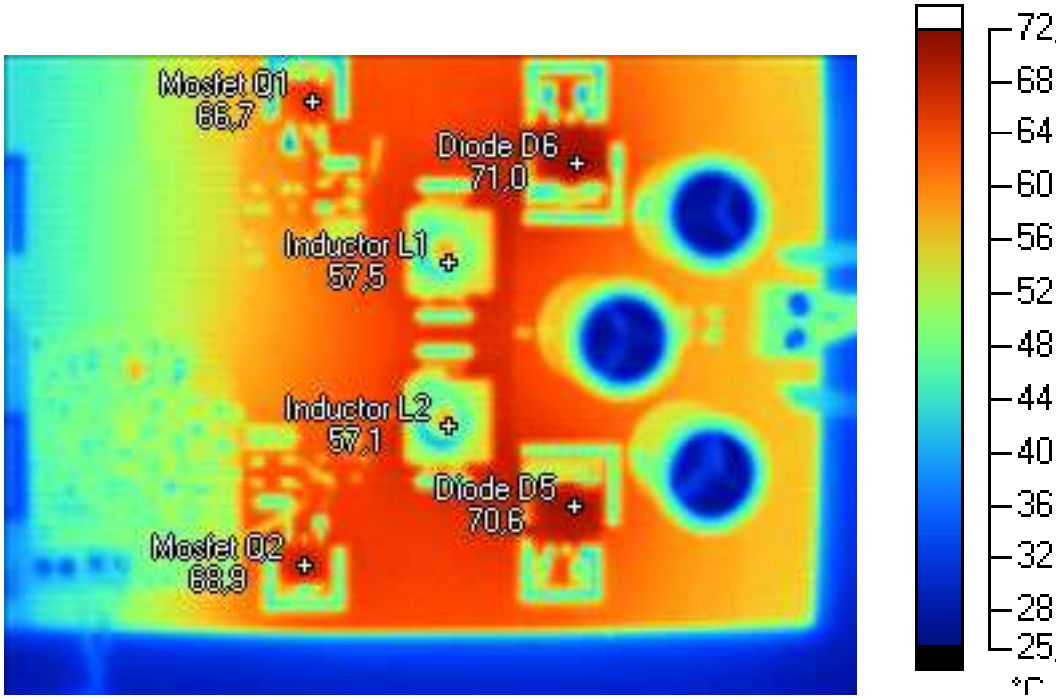
Input Voltage Ripple (C3), Output Voltage Ripple (C2) at full load 15A @ Vin=6.5V



Input Voltage Ripple (C3), Output Voltage Ripple (C2) at full load 15A @ Vin=9V

PMP2688RevA Test Results

Thermal Images



Output Power Continuous 10A Vin=6.5V

Markierungen

Beschriftung	Temperatur	Emissionsgrad	Hintergrund
Diode D6	71,0 °C	0,95	20,0 °C
Diode D5	70,6 °C	0,95	20,0 °C
Inductor L2	57,1 °C	0,95	20,0 °C
Mosfet Q2	68,9 °C	0,95	20,0 °C
Mosfet Q1	66,7 °C	0,95	20,0 °C
Inductor L1	57,5 °C	0,95	20,0 °C

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