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TI Designs – Precision: Verified Design

Single Supply Unipolar Multiplying DAC Reference Design

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Design Resources

Design Archive	All Design files
TINA-TI™	SPICE Simulator
DAC7811	Product Folder
REF5050	Product Folder
OPA376	Product Folder

Circuit Description

This multiplying DAC (MDAC) circuit outputs unipolar voltages from 0 V to 2.5 V. This design does not require dual supplies to realize a unipolar, positive output voltage. This design removes the need for a negative supply rail by applying a bias voltage to the output transimpedance stage.

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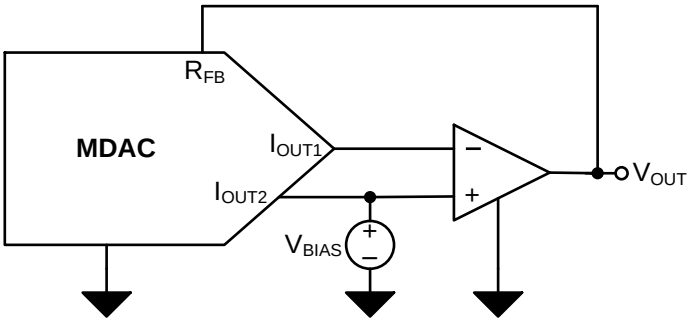

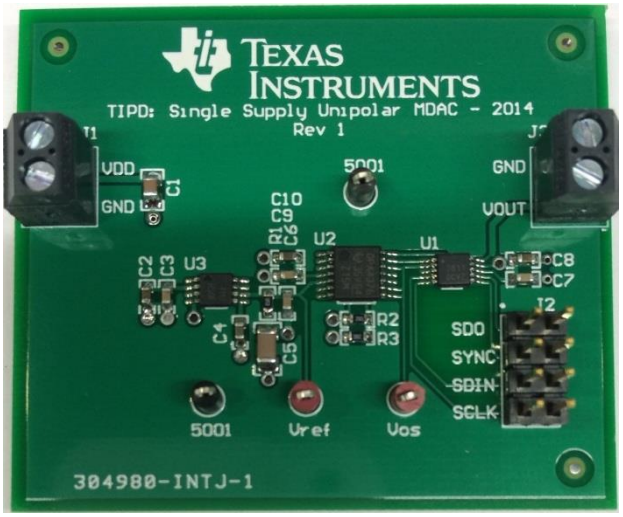

1 Design Summary

The design requirements are as follows:

- Supply Voltage: 5.5 V
- Input: 3-wire, 16-bit SPI
- Output: 0 - 2.5 V

The design goals and performance are summarized in Table 1. Figure 1 depicts the measured transfer function of the design.

Table 1 : Comparison of Design Goals, Simulation, and Measured Performance

	Goal	Simulated	Measured
Total Unadjusted Error (%FSR)	0.1%	0.0967%	0.0500%

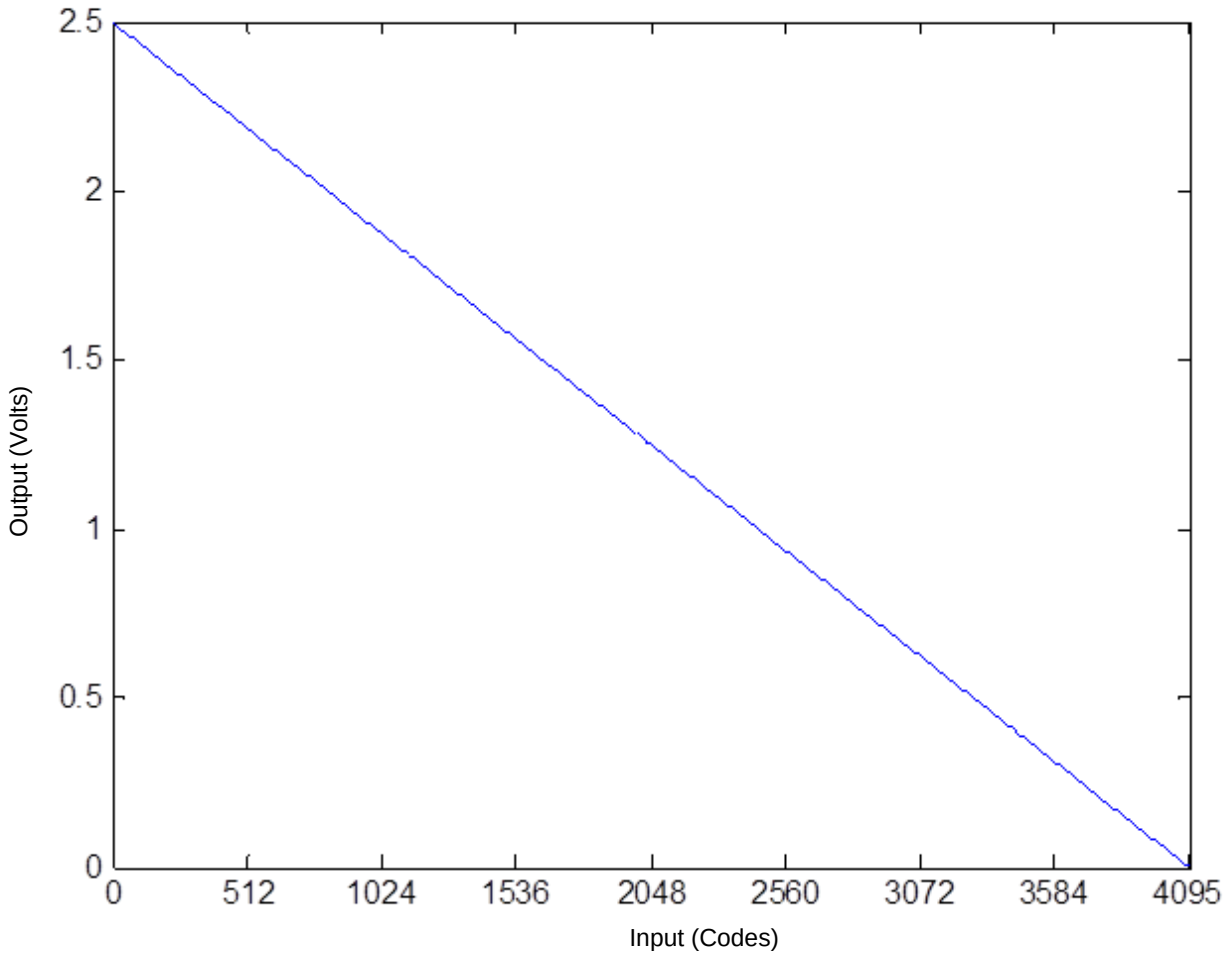

Figure 1: Measured Transfer Function

2 Theory of Operation

A multiplying DAC (MDAC) is a current output digital-to-analog converter. Typically the output current is converted into a voltage by including an op-amp in a transimpedance configuration at the MDAC current output terminal. The transimpedance stage creates an output voltage with opposite polarity to that of V_{REF} and subsequently requires dual supplies. This circuit removes the need of dual power supplies and uses a single supply to power the circuit.

A complete schematic for this design, including the reference voltage, voltage divider used to obtain the bias voltage, and the three buffers is shown in Figure 2.

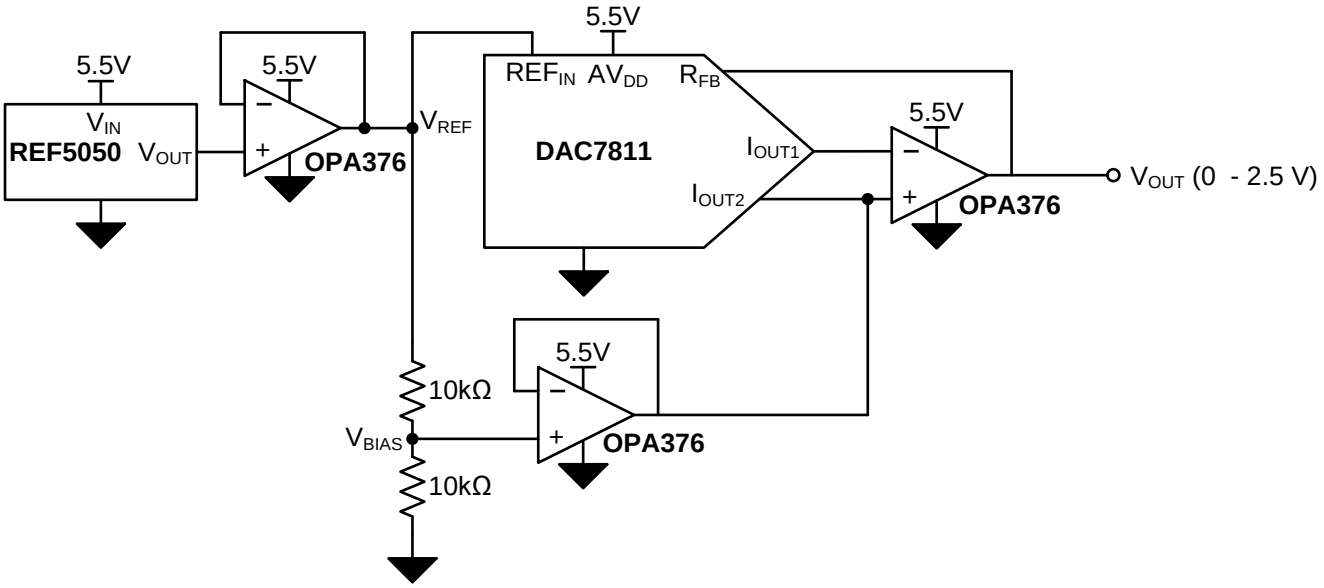

Figure 2: Complete Circuit Schematic

The transfer function from digital code to output voltage is shown in Equation (1).

$$V_{OUT}(Code) = V_{BIAS} - \frac{(V_{REF} - V_{BIAS})}{2^{bits}} * Code \quad (1)$$

2.1 Typical MDAC Configuration

A simplified illustration of the MDAC R-2R ladder architecture is shown in Figure 3. Each 2R leg of the ladder can either be connected to the I_{OUT1} or I_{OUT2} terminal. In normal operation the I_{OUT2} terminal of the MDAC is connected to the non-inverting input terminal of an op amp and ground, while the I_{OUT1} terminal is connected to the inverting input terminal and R_{FB}, as shown in Figure 3. Current flow out of I_{OUT1} develops a voltage across R_{FB}. Through negative feedback the op amp creates a voltage of equal magnitude but opposite polarity to the voltage across R_{FB} at its output to drive the non-inverting terminal to ground.

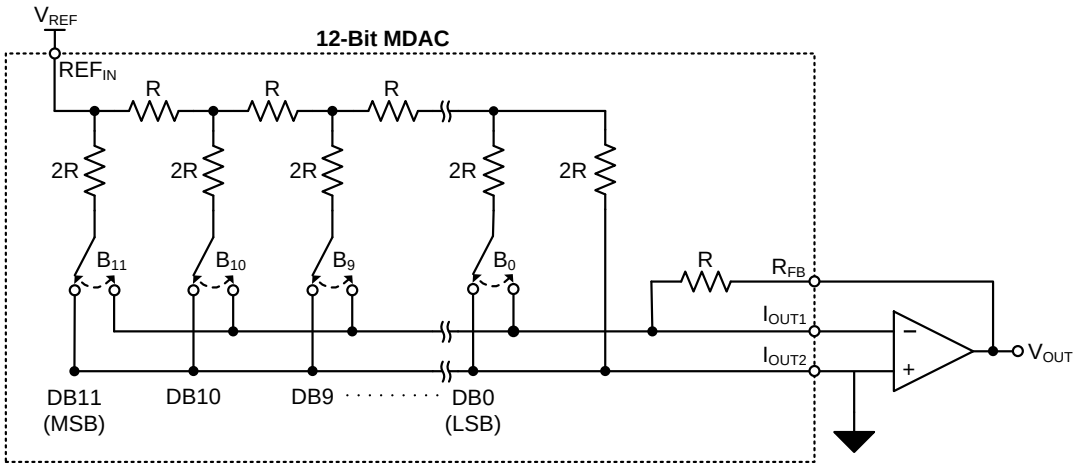

Figure 3: Typical MDAC Application

2.2 Modifications for Single-Supply Operation

In this design the I_{OUT2} terminal of the MDAC is connected to a 2.5 V bias voltage, V_{BIAS}, as shown in Figure 4, instead of ground as is shown in Figure 3. Biasing I_{OUT2} to 2.5 V instead of ground causes the transimpedance amplifier to drive I_{OUT1} to 2.5 V. For example, at zero-scale when all DAC switches are connected to the I_{OUT2} terminal, no current flows through R_{FB} developing 0 V at I_{OUT1}. The op amp will then produce 2.5 V at its output to drive I_{OUT1} to 2.5 V. At full-scale all DAC switches are connected to the I_{OUT1} terminal and full-scale current flows through R_{FB} developing 2.5 V at the non-inverting input terminal. The op amp produces 0V at its output to drive I_{OUT1} to 2.5 V. This behavior results in an output range from 2.5 V (zero-scale code) to 0 V (full-scale code).

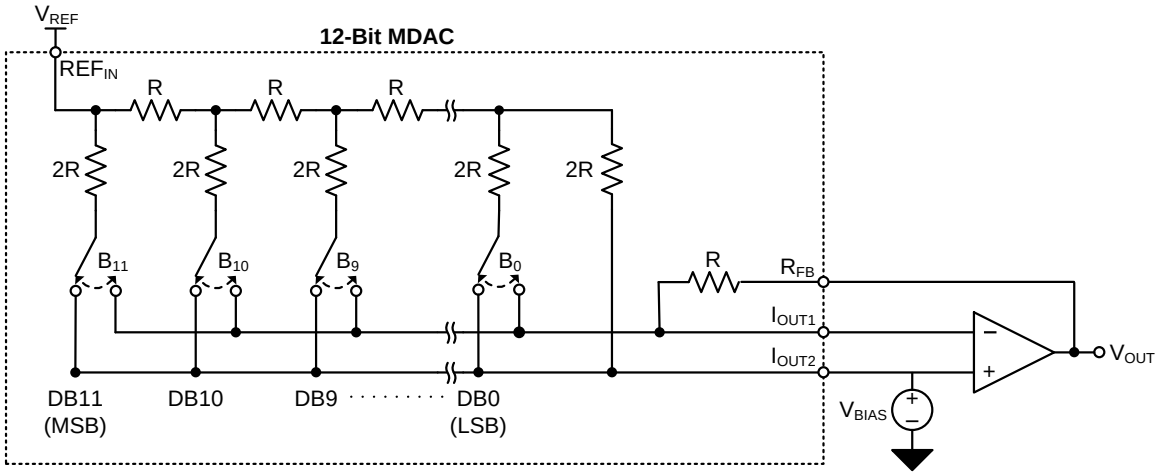

Figure 4: MDAC with offset voltage

2.3 Circuit Limitations

N-channel MOSFETs are used in the R-2R DAC ladder to construct the switches. Figure 5 shows a simplified diagram of the circuit used to create one of these switches, with the switch connected to I_{OUT2}.

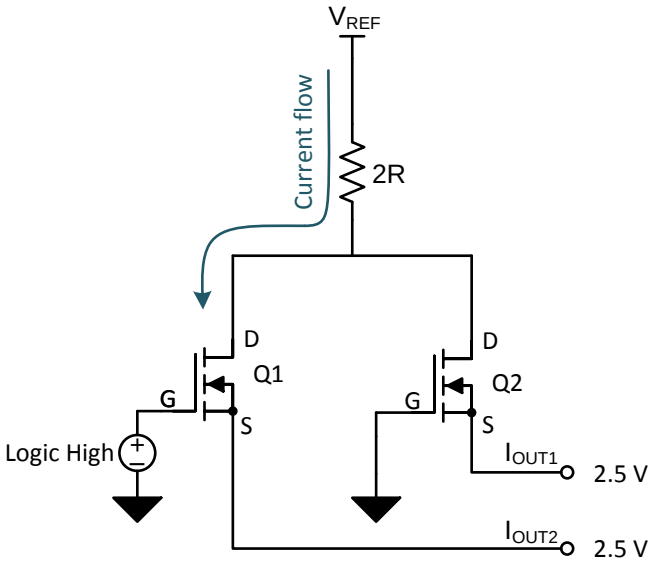

Figure 5: MOSFET Switch

There are two limitations that should be kept in mind when choosing the bias voltage in this design: ensuring that the digital block of the DAC can still control the DAC switches, and that the MOSFETs in the switches are biased appropriately to have matched on resistances, or R_{ON}, to maintain DAC linearity.

In order to ensure that the digital block of the DAC can still control the DAC switches, the V_{GS} voltage must be greater than the V_{TH} voltage of the switch MOSFETs. The logic high voltage applied by the digital block of the DAC to the gate of the MOSFETs in the switches should be approximately 2.0 V higher than the bias voltage applied at I_{OUT2} to ensure functionality over all operating conditions for a majority of DACs at the time of this writing.

In order to also maintain the DAC linearity, the V_{GS} voltage will need to be higher than 2.0 V. Mismatched impedances in the “2R” legs of the R-2R ladder create linearity errors at the DAC output. The 2R resistors are often trimmed to match one another and ideally the MOSFETs in each of the DAC switches is exposed to the same biasing scheme and therefore exhibit matched R_{ON}. In this design the transimpedance amplifier on the output of the MDAC forces I_{OUT1} and I_{OUT2} to the same potential which ensures the same source voltage on each MOSFET. All of the MOSFETs see the same drain voltage (V_{REF}) and the same gate voltage (the digital logic high voltage). To enhance R_{ON} matching, it is helpful to exceed the minimum V_{GS} voltage, 2.0 V, for the MOSFETs in the switches. For a majority of DACs, at the time of this writing, 2.7 V V_{GS} should be sufficient to maintain datasheet specified linearity over all operating conditions.

This design will use 5.5 V for V_{REF} to meet both of these conditions.

3 Component Selection

3.1 MDAC Selection

MDAC selection for this design is based on dc accuracy goals and the requirement of operating on a single-supply. Important parameters to consider for dc accuracy are gain error and linearity errors (INL and DNL). Since MDACs do not feature internal output amplifiers, they do not contribute offset error to the system output. In order to realize a design that operates on a single-supply the MDAC must provide external access to the I_{OUT2} node of the R-2R ladder.

The DAC7811 was chosen for this design because both I_{OUT1} and I_{OUT2} are accessible and it offers strong dc performance with gain error of ±0.05 %FSR and INL error of ±1 LSB.

3.2 Amplifier Selection

Three amplifiers must be selected in this design: one to buffer the reference voltage, one to buffer V_{BIAS} and another in the output transimpedance stage.

For the transimpedance amplifier, low input bias current and low input offset voltage are the most critical parameters to deliver dc accuracy. Input bias current will create a dc offset and input offset voltage will create an integral non-linearity error. For full details on the interaction of the transimpedance amplifier and the MDAC refer to TIPD137.

Similar dc concerns are applicable to the reference buffer and bias voltage buffer but input bias current is not as critical for these sections since they are driven by low-impedance sources that will not interact with input bias current to create substantial error. Input offset voltage is the primary consideration for amplifiers in this section.

The OPA4376 was chosen for this design because it delivers strong performance for both input bias current and input offset voltage in a quad-package that reduces PCB area and keeps cost low.

3.3 Passive Component Selection

The resistor divider network used to create the bias voltage of 2.5 V from the reference voltage contributes offset error to the system output and must use resistors with tight tolerance. In this design resistors with ±0.1% tolerance were chosen.

3.4 Reference

Reference initial accuracy in this design contributes to both offset and gain errors for the system output and is an important parameter for device selection. The REF5050 5 V reference was chosen for this design which delivers strong initial accuracy at 0.05%.

4 Simulation and Calculations

4.1 Error Calculation

According to the datasheet, the DAC7811 has an integral non-linearity (INL) of 1 LSB at 12 bits of resolution. The INL error is converted to % FSR by using Equation (**3**).

$$INL_{DAC}(\%FSR) = \frac{INL(LSB)}{2^{DAC\_RESOLUTION}} * 100 \quad (2)$$

$$INL_{DAC}(\%FSR) = \frac{1LSB}{2^{12}} * 100 = 0.024414\% \quad (3)$$

The gain error for DAC7811 is also obtained from the datasheet. The gain error is specified as full-scale gain error of ±5 mV with 10 V reference voltage. The gain error is converted in to % FSR by using Equation (**4**).

$$GainError_{DAC}(\%FSR) = \frac{GainError}{FullScaleRange} * 100\% = \frac{5mV}{10V} * 100\% = 0.05\% \quad (4)$$

In the transimpedance stage the input bias current of the operational amplifier interacts with the current output of the MDAC resulting in offset error at the voltage output of the transimpedance stage. This offset voltage is given by Equation (**5**). The OPA376 has input bias current of 0.2 pA and DAC7811 has feedback resistance of 10 kΩ.

$$OffsetError_{OPA}(Volts) = i_b * R_{FB} \quad (5)$$

$$OffsetError_{OPA}(Volts) = 0.2pA * 10k\Omega = 0.000000002V \quad (6)$$

$$OffsetError_{OPA}(\%FSR) = \frac{V_{OFFSET}}{FullScaleRange} * 100\% = \frac{0.000000002V}{2.5V} * 100\% = 0.00000004\% \quad (7)$$

The input offset voltage of the transimpedance amplifier is modulated by the R-2R DAC ladder and causes a linearity error. The linearity error can be calculated by multiplying the input offset voltage with the non-inverting gain of the output amplifier. The non-inverting gain is dependent on the DAC code, but an estimate of the maximum non-inverting gain applied to the amplifier by the R-2R ladder can be made using the approach outlined in TIPD137. The OPA376 has an input offset voltage of the 5 µV. Using the general guideline from TIPD137, the maximum non inverting gain is 2.4 V/V. Equations (**8**), (**9**) and (**10**) shows the calculations.

$$INL_{OPA}(Volts) = V_{OS} * non-inverting\_gain \quad (8)$$

$$INL_{OPA}(Volts) = 5\mu V * 2.4 = 0.000012V \quad (9)$$

$$INL_{OPA}(\%FSR) = \frac{INL_{OPA}(Volts)}{FullScaleRange} * 100\% = 0.00048\% \quad (10)$$

The buffers and resistor dividers from the reference source contribute additional errors to the system which were modeled using the TINA-TI schematic shown in Figure 6. The parameters of the buffers are modeled using the OPA4376 TINA-TI SPICE model and the effects of the resistor divider tolerance are modeled using Monte-Carlo analysis.

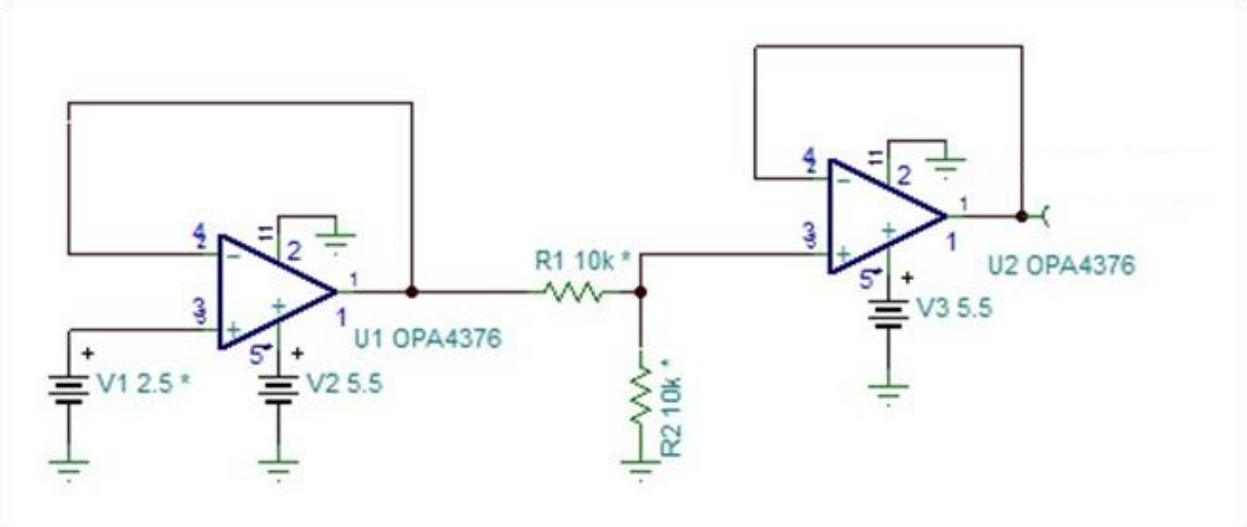

Figure 6: TINA-TI schematic to calculate offset error

The total unadjusted error (TUE) is obtained by computing the root square sum (RSS) of the error terms as shown in Equation (11).

$$TUE = \sqrt{INL_{DAC}{}^2 + INL_{OPA}{}^2 + GainError_{DAC}{}^2 + OffsetError_{OPA}{}^2 + OffsetError_{Divider}{}^2} \quad (11)$$

$$TUE = 0.063990912\% \quad (12)$$

All the calculations done above are computed by using an ideal reference of 5 V. To better understand of the overall system performance, the errors computed above are represented with four parameters, the INL error, gain error, offset error and the TUE. The INL error is obtained by the RSS of the DAC INL and the OPA INL error contributions. Similarly offset error is the RSS of the offset error contributions of the buffers and resistor divider. With an ideal reference voltage the DAC gain error is the only contributor to system gain error.

Table 2: System performance with ideal reference

Parameter	Calculated Value
V_{REF}	5 V
INL Error	0.02441%
Gain Error	0.05000%
Offset Error	0.03160%
TUE	0.06399%

The data sheet of the REF5050 indicates that it has initial accuracy of 0.05% @25ºC. Table 3 shows another set of calculated results that include the effects of reference accuracy on offset and gain error.

Table 3: System performance with non-ideal reference

Parameter	Calculated Value
V_{REF}	5 V±0.05%
INL Error	0.02441%
Gain Error	0.07250%
Offset Error	0.05914%
TUE	0.09670%

5 PCB Design

The PCB schematic and bill of materials can be found in the Appendix A.

5.1 PCB Layout

The PCB layout for top and bottom layers is shown in Figure 7 and Figure 8. In this design general PCB layout guidelines should be followed, including proper decoupling and adequate ground planes.

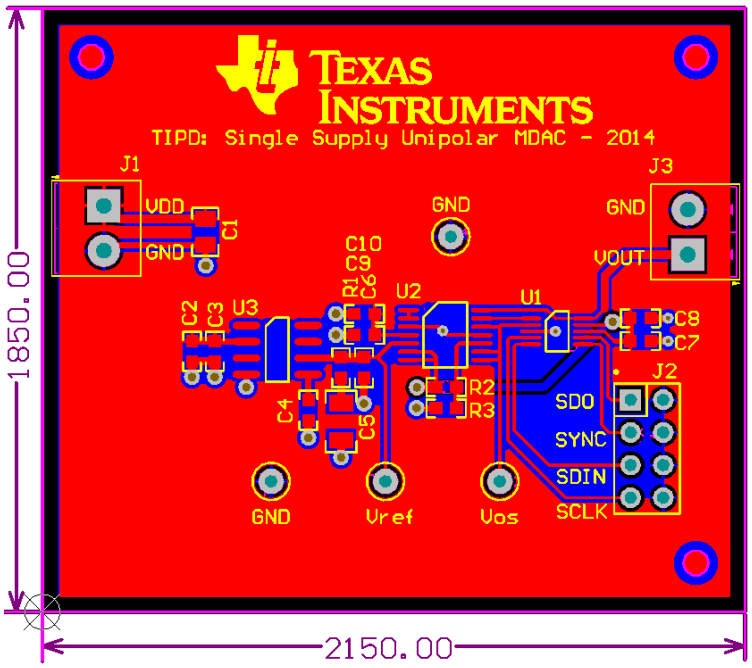

Figure 7: PCB Layout, Top Layer

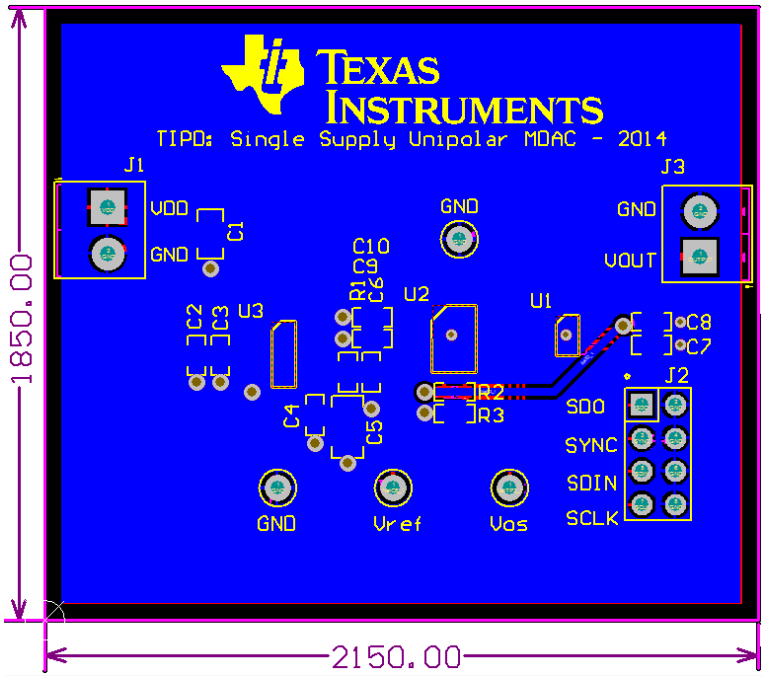

Figure 8: PCB Layout, Bottom Layer

6 Verification & Measured Performance

6.1 Transfer Function

The graph in Figure 9 is generated by applying input codes from 0 to 4095 to 10 boards and measuring the output voltage of each.

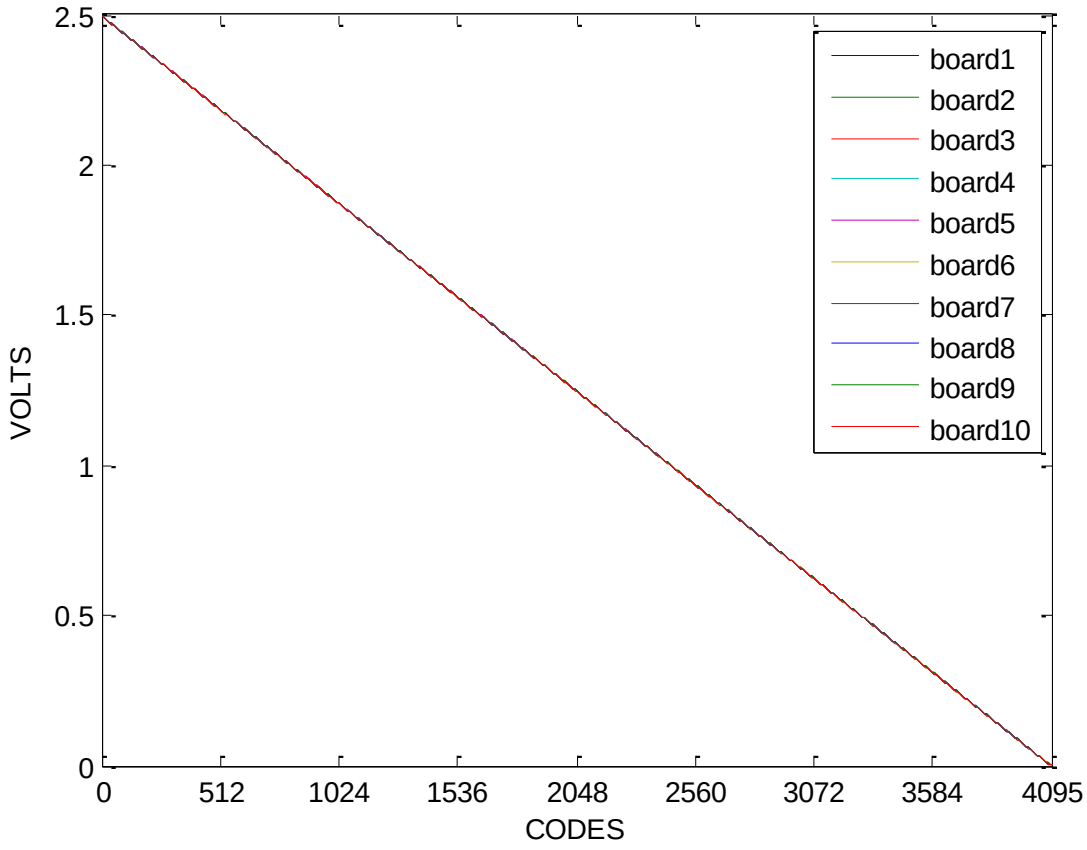

Figure 9: Measured transfer function

Figure 10 and Figure 11 show performance of the voltage output near the supply rails for the first 30 and last 45 DAC codes respectively. Recall that in this system the zero-scale output is the maximum voltage output and the full-scale output is the minimum voltage output. At zero-scale the output amplifier has enough head-room over the maximum voltage output to not exhibit any output voltage swing to rail limitation and therefore does not exhibit any degradation in linearity. Near full-scale, however, the output amplifier does not have enough foot-room to avoid output voltage swing to rail limitations and displays some non-linearity.

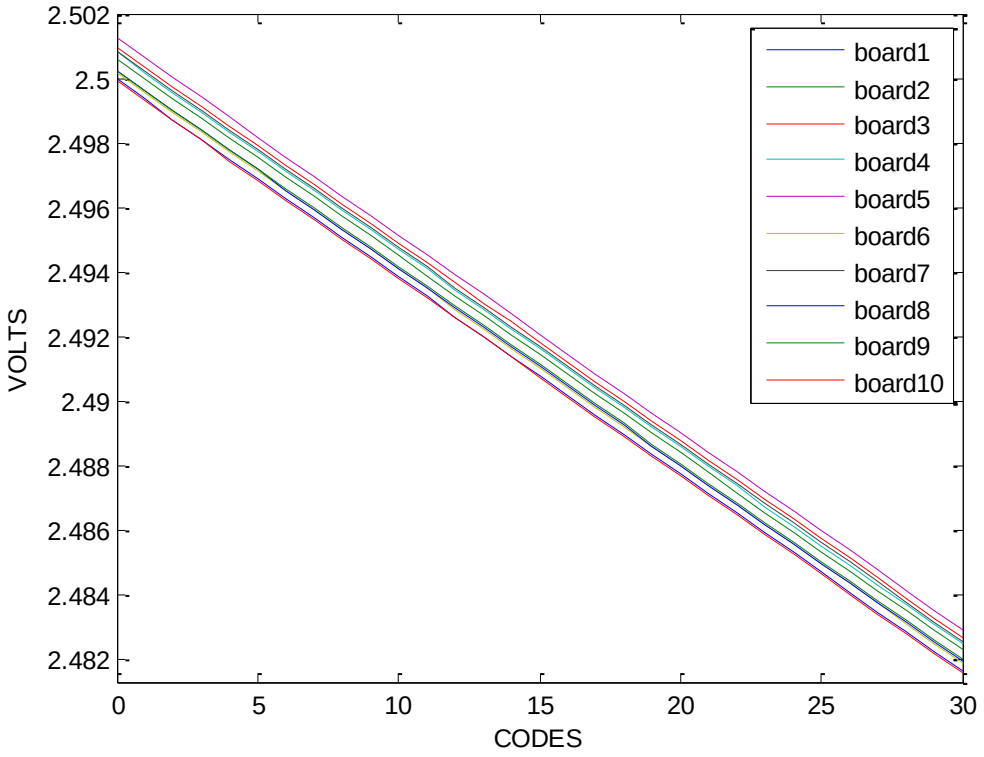

Figure 10: Voltage output for code 0 to 30

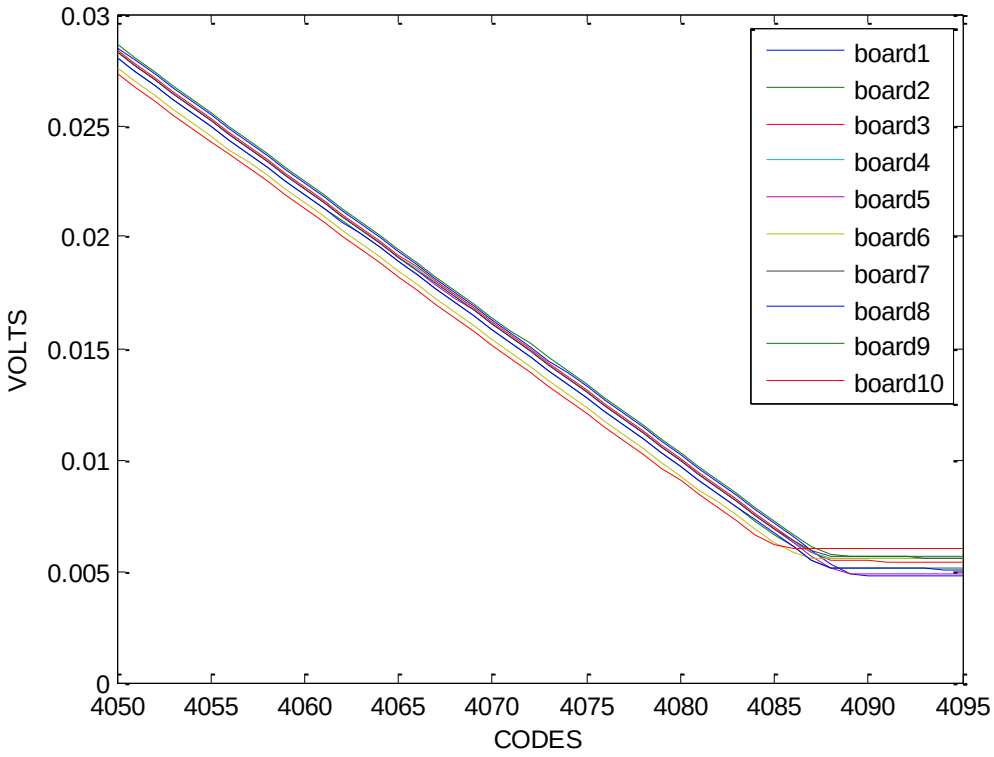

Figure 11: Output voltage for code 4050 to 4095

To better understand performance of the system the difference between the ideal output and the measured output voltage of the circuit in %FSR is graphed in Figure 12 The plot below represents data ranging from code 30 to 4050. The figure shows the absolute error (TUE) has a maximum value of about 0.05% FSR which is within the design constraints of (+-0.1%) TUE.

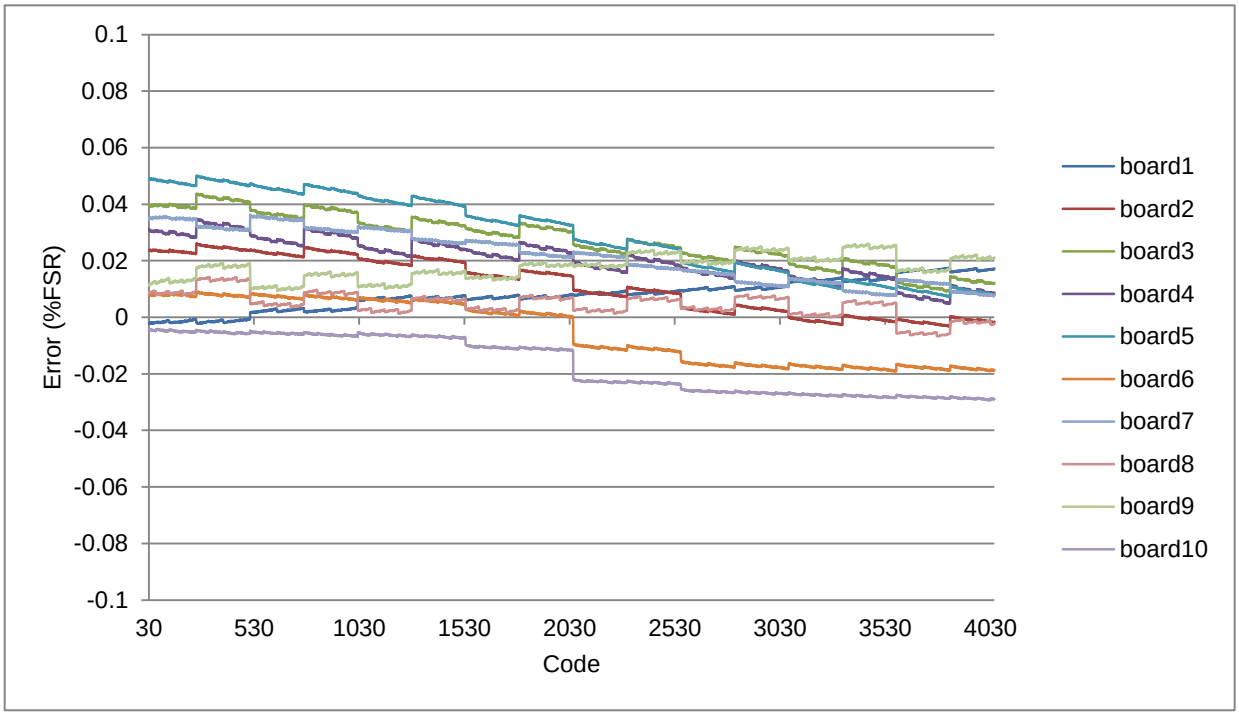

Figure 12: Absolute error (TUE) in %FSR

Table 4 below shows the minimum, maximum, and average measured results obtained on 10 boards. Offset, gain, and linearity error are measured using a two-point line of best fit at code 30 and 4050. TUE is measured against the absolute ideal output voltage.

Table 4: Measured Parametric Errors

Parameter	Minimum	Maximum	Average	Standard Deviation
Offset Error (%FSR)	-0.029123827	0.021269274	0.000221401	0.014914514
Gain Error (%FSR)	-0.019847514	0.04114075	0.017596324	0.018634120
INL Error (%FSR)	-0.007034199	0.007496817	-0.004581663	0.004350889
Measured TUE (%FSR)	-0.029358687	0.050078188	0.020028831	0.025894554

Table 5 compares worst-case measured results to the goals outlined at the beginning of this document and calculated performance.

Table 5: Calculated and Measured Error Values

Parameter	Calculated	Measured	Goal
Offset Error (%FSR)	0.0316	0.0291	n/a
Gain Error (%FSR)	0.0781	0.0411	n/a
INL Error (%FSR)	0.0244	0.0074	n/a
Measured TUE (%FSR)	0.0877	0.0500	0.1

Equations (**13**), (**14**), (**15**) and (**16**) are used to calculate the INL, offset error, gain error and total unadjusted error respectively from the measured results.

$$INL(i) = \sum_{j=0}^{i} DNL(j) \quad (13)$$

$$OffsetError = \frac{V_{out(LowCode)} - \left(\frac{V_{out(HighCode)} - V_{out(LowCode)}}{HighCode - LowCode} * LowCode \right)}{FullScaleRange} * 100 \quad (14)$$

$$GainError = \frac{LSB_{Measured} - LSB_{Ideal}}{LSB_{Ideal}} * 100\% \quad (15)$$

$$TUE = \frac{V_{out\_measured(code)} - V_{out\_ideal(code)}}{FullScaleRange} * 100 \quad (16)$$

7 Modifications

This design could be realized using a wide variety of reference solutions or operational amplifiers depending on the application's specific ac and dc performance requirements. DAC selection in this design, however, is limited to a small section of DACs that make both sides of the R-2R ladder available outside the package in such a way that they can be biased to a non-ground voltage. Table 6 lists alternative DACs that could be used in this design. For inquiries about DACs not in this list or for an updated list, please visit the TI E2E Community.

Table 6: Alternative MDACs

Device	Resolution (Bits)	Channels	Interface
DAC7811	12	1	SPI
DAC7821	12	1	Parallel
DAC7822	12	2	Parallel
DAC8820	16	1	Parallel

8 About the Authors

Kevin Duke is an applications engineer in the precision digital to analog converters group at Texas Instruments where he supports industrial and products and applications, Kevin received his BSEE from Texas Tech University in 2010.

Neeraj Gill was an analog applications rotation engineer at Texas Instruments. Neeraj received his BSEE from University of New Hampshire in 2011 and his Masters in Electrical Engineering, also from University of New Hampshire, in 2013.

Appendix A.

A.1 Electrical Schematic

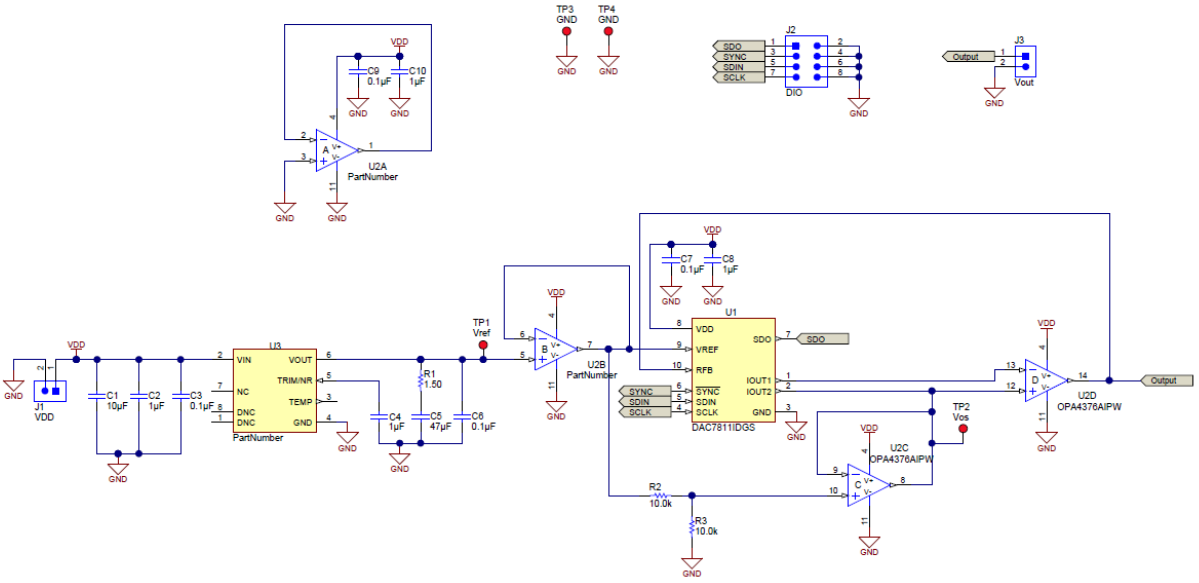

Figure A-1: Electrical Schematic

A.2 Bill of Materials

Texas Instruments

Bill of Materials

TI DESIGNS
TIPD157: Single Supply Unipolar MDAC

Item #	Quantity	Designator	Value	Description	Manufacturer	Manufacturer Part Number 1	Supplier Part Number 1
1	1	J2		Header, TH, 100mil, 4x2, Gold plated, 230 mil above insulator	Samtec	TSW-104-07-G-D	SAM1028-04-ND
2	2	R2, R3	10.0k	RES, 10.0k ohm, 0.1%, 0.1W, 0603	Susumu Co Ltd	RG1608P-103-B-T5	RG16P10.0KBCT-ND
3	1	U3		Low-Noise, Very Low Drift, Precision Voltage Reference, D0008A	Texas Instruments	REF5050ID	296-22212-5-ND
4	1	U2		Low-Noise, Low Quiescent Current, Precision Operational Amplifier e-trim™ Series, PW0014A	Texas Instruments	OPA4376AIPW	296-26288-5-ND
5	3	C6, C7, C9	0.1uF	CAP, CERM, 0.1uF, 25V, +/-10%, X7R, 0603	MuRata	GRM188R71E104KA01D	490-1524-1-ND
6	1	J1		Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	On-Shore Technology	ED555/2DS	ED1514-ND
7	1	J3		Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	On-Shore Technology	ED555/2DS	ED1514-ND
8	1	U1		12-Bit, Serial Input, Multiplying Digital-to-Analog Converter, DGS0010A	Texas Instruments	DAC7811IDGS	296-33261-5-ND
9	1	R1	1.5 ohm	RES, 1.50 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06031R50FKEA	541-1.50HHCT-ND
10	1	C5	47uF	CAP, CERM, 47uF, 25V, +/-20%, X5R, 1206	TDK	C3216X5R1E476M160AC	445-8047-1-ND
11	1	C1	10uF	CAP, CERM, 10uF, 25V, +/-10%, X5R, 0805	TDK	C2012X5R1E106K125AB	445-5984-1-ND
12	3	C2, C3, C4	1uF, 0.1uF, 1uF	CAP, CERM, 1uF, 16V, +/-10%, X5R, 0603, CAP, CERM, 0.1uF, 25V, +/-10%, X7R, 0603, CAP, CERM, 1uF, 16V, +/-10%, X5R, 0603	Kemet, MuRata, Kemet	C0603C105K4PACTU, GRM188R71E104KA01D , C0603C105K4PACTU	399-5090-1-ND, 490-1524-1-ND, 399-5090-1-ND
13	2	C8, C10	1uF	CAP, CERM, 1uF, 16V, +/-10%, X5R, 0603	Kemet	C0603C105K4PACTU	399-5090-1-ND
14	1	TP1	Red	Test Point, Miniature, Red, TH	Keystone	5000	5000K-ND
15	1	TP2	Red	Test Point, Miniature, Red, TH	Keystone	5000	5000K-ND
16	2	TP3, TP4	Red	Test Point, Miniature, Red, TH	Keystone	5000	5000K-ND
17	3	FID1, FID2, FID3		Fiducial mark. There is nothing to buy or mount.	N/A		

Figure A-2: Bill of Materials

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