TI Designs

24-V DC,10-A eFuse and Protection Circuit for Programmable Logic Controllers (PLC)

TI Designs

TI Designs provide the foundation that you need including methodology, testing and design files to quickly evaluate and customize the system. TI Designs help *you* accelerate your time to market.

Design Resources

TIDA-00233	Tool Folder Containing Design Files
LM5069-2	Product Folder
LM5050-1	Product Folder
CSD18532Q5B	Product Folder

TI E2E™ Community

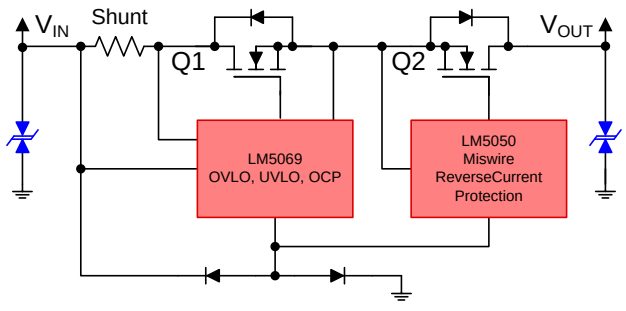
ASK Our Analog Experts
WEBENCH® Calculator Tools

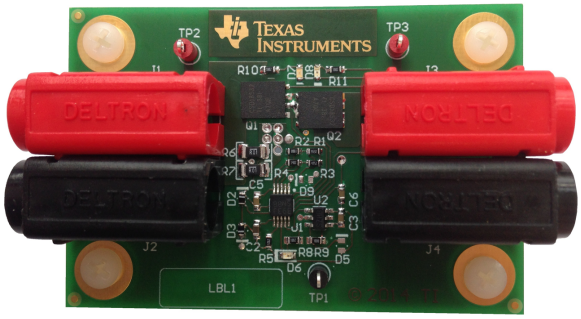
Design Features

- Protection
  - Configurable Undervoltage Lockout (UVLO) and Overvoltage Lockout (OVLO)
  - Overcurrent Protection (OCP)
  - Reverse Current protection
  - Reverse Polarity Protection
  - Miswire Protection
  - Surge Protection (IEC61000-4-5)
- Low Power Operation
  - 0.5-mA Quiescent Current
  - 99% Efficiency in Normal Operation

Featured Applications

- Programmable Logic Controller
  - Power Supply
  - CPU
  - I/O Module
- Distributed Control System (DCS)
- Motor Control
- Sensor Concentrators





1 System Description

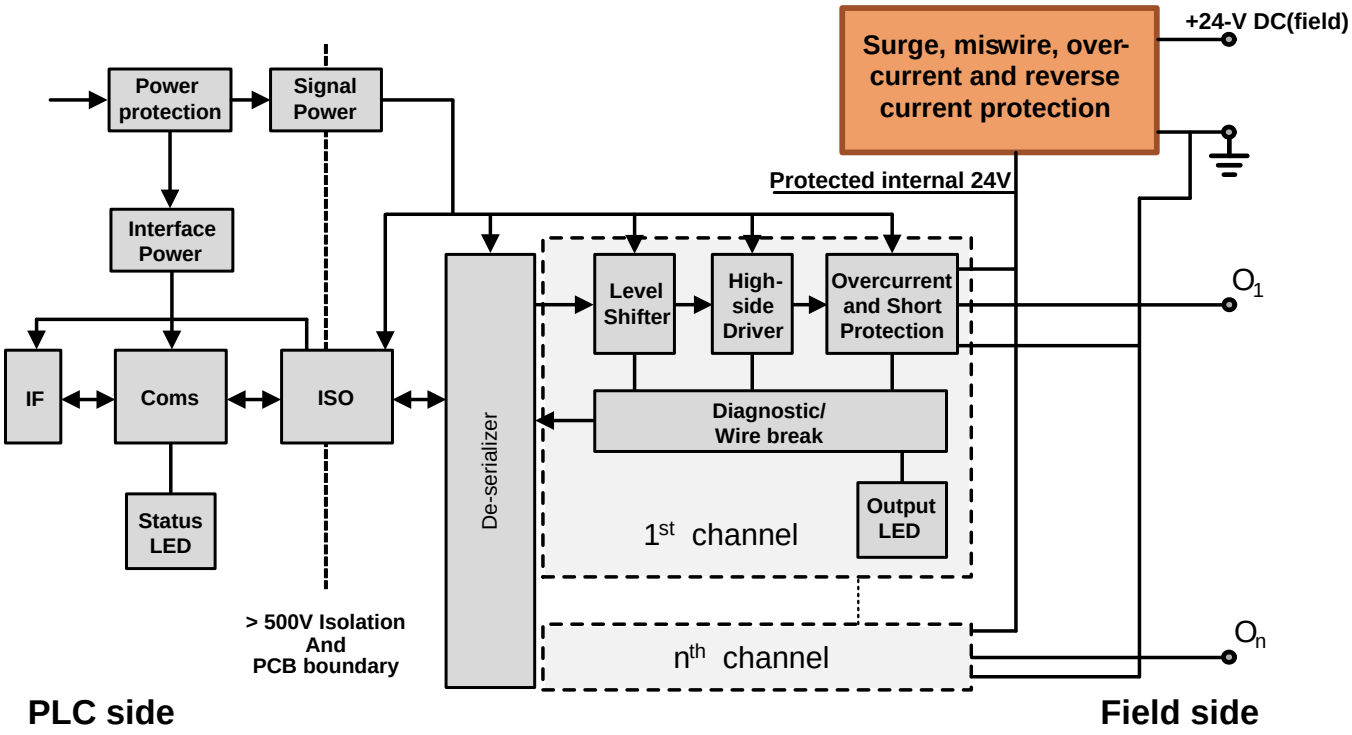


Figure 1. Use of This Design (Orange Block) in System Context (High Side Driver with 24-V Field Supply)

PLC or Distributed Control System (DCS) I/O modules connected to a field power supply capable of delivering stable 24-V DC at high power benefit from protection on the 24-V, field-input connectors. The reason that the PLC or DCS modules may benefit from protection is due to power-supply faults or miswiring. Power-supply faults or miswiring might damage the modules or cause the modules to not operate correctly. OVLO and UVLO protect integrated circuits (ICs) on the I/O module from voltages outside of the operating range which might permanently damage the modules, make the modules nonfunctional, or cause the modules to operate in an undesired region. An example of an undesired region is the linear region of MOSFETs, with large resulting power dissipation.

A field power supply is often connected to multiple I/O modules. A field power supply is capable of delivering more current than a single I/O module can handle. OCP limits the current from the power supply to the module so that the maximum current does not rise above what the board is designed for. OCP also acts as a short circuit protection (SCP) as the maximum current is limited to 10 A.

The design also acts as a smart diode with protection against reverse current. A reverse current could damage the field power supply and cause other ICs on the module to run hot or cause permanent damage. A Schottky diode is often used to provide protection against reverse current with the disadvantage that the forward-voltage drop causes a permanent power loss. At high currents, a permanent power loss becomes significant in normal operation mode. At 10 A, the forward loss with a Schottky diode is approximately 7 W. At 10 A, the forward loss with the smart diode function in this design is approximately 1 W.

If the field power supply is connected with reverse polarity (which is not unlikely as field power supplies are usually connected with screw terminals), ICs connected after connecting the power supply will not operate as desired and potentially receive permanent damage. The reverse polarity protection in this design will prevent the reverse power from getting into the module. If the field power supply is connected to an input or output of the module, the miswire protection breaks the path that might cause the current to flow from an input or output to the field supply input.

NOTE: Status LEDs on the board indicate input and output voltage.

2 Design Features

2.1 Specifications

Table 1. Specifications(1)

SYMBOL	PARAMETER	CONDITIONS	SPECIFICATION			UNIT
			MIN.	TYP.	MAX.	
V_{IN}	Input voltage	Normal operation	-33	24	33	V
I_Q	Quiescent current (2)	Normal operation	5	7.6	10	mA
V_{OVLO_DIS}	OVLO output disabled	V_{IN} increasing	-	32.5	33.0	V
V_{OVLO_EN}	OVLO output re-enabled	V_{IN} decreasing	29.9	30.5	-	V
t_{OVLO}	OVLO delay	V_{IN} increasing			50	µs
U_{UVLO_EN}	UVLO output enabled	V_{IN} increasing	-	12.4	12.64	V
U_{UVLO_DIS}	UVLO output disabled	V_{IN} decreasing	11.29	11.4	-	V
I_{OCP}	OCP	V_{IN} = 12 V to 30 V	-	10.3	11	A
t_{OCP}	OCP delay	$I_{IN} > I_{OCP}$			50	µsSpe
t_{SCP}	SCP delay	$I_{IN} > 2 \times I_{OCP}$			0.5	µs
I_{REV_POL}	Reverse polarity protection current	V_{IN} = -30 V or -10 V		0.1	1	µA
I_{MIS}	Miswire and reverse-current protection current	V_{IN} = 10 V, 12 V, or 30 V	2.0	2.2	3	mA
t_{REV}	Miswire and reverse-current protection delay			40	100	ns

(1) Ambient temperature T_A = 25°C
(2) Without indicator LEDs, the quiescent current is reduced by 2 x I_LED = 2 x 2.2 mA (Vin = 24 V) = 4.4 mA.

3 Block Diagram

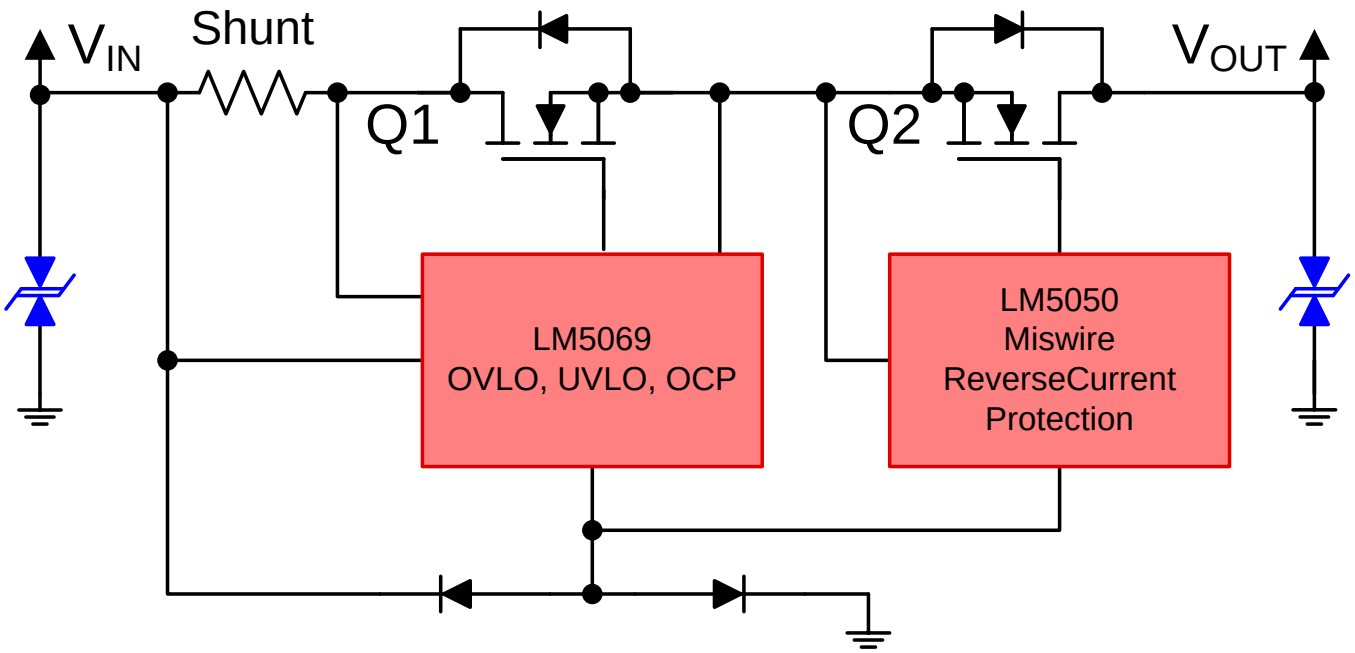


Figure 2. Simplified Block Diagram with the High Power Path between V_{IN} and V_{OUT}

4 Component Description

4.1 MOSFET Controllers

This design is using two MOSFET controllers to regulate the circuit's high power path. The LM5069-2 (U1) is a high voltage controller with OVLO, UVLO, and current sense capability over an external shunt resistor. OVLO and UVLO are set with external resistor dividers. The OCP is set with a shunt resistor in the high power path. The LM5069-2 is controlling MOSFET Q1.

The LM5050-1 (U2) is also a MOSFET controller, that with an external MOSFET (Q2), becomes and ideal diode. The ideal diode is used to protect the high power path from reverse current due to miswiring or reverse polarity.

4.2 MOSFET

Two CSD18532Q5B (Q1 and Q2), 60-V, 2.5-mΩ $R_{DS(on)}$ MOSFETs are used in the high power path, connected back-to-back, to control the current. The low $R_{DS(on)}$ helps reduce the power loss and heat dissipation.

5 Circuit Design and Component Selection

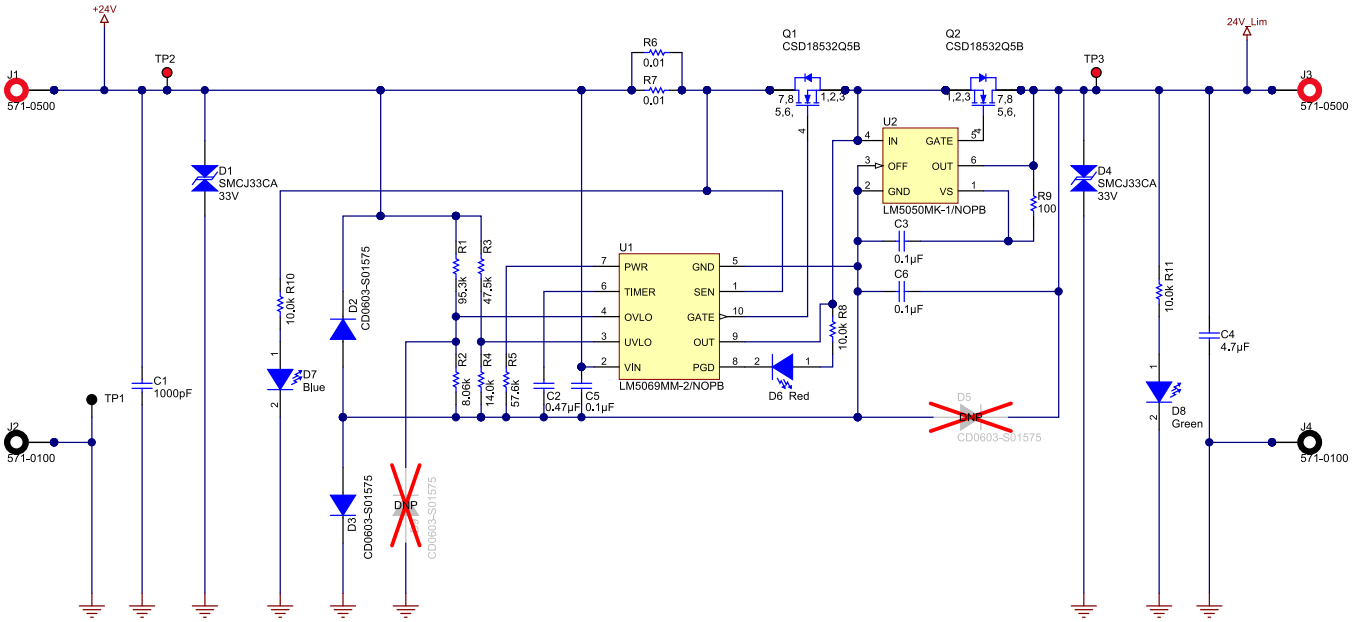


Figure 3. Circuit Schematics

5.1 UVLO and OVLO

From $V_{IN(MIN)}$ to V_{UVLO_EN}, the design blocks V_{IN} from reaching the output terminals (J3 and J4). From V_{UVLO_EN} to V_{OVLO_DIS}, the design passes V_{IN} to the output. From V_{OVLO_DIS} to $V_{IN(MAX)}$, the design blocks V_{IN} from reaching the output. For $V_{IN} < V_{IN(MIN)}$ or $V_{IN} > V_{IN(MAX)}$, the behavior is set by the TVS diodes (D1 and D4), which block surge voltages above the reverse standoff voltage V_R = 33 V.

Therefore, $V_{IN(MAX)}$ = 33 V.

UVLO and OVLO is performed by a function in U1. The resistor divider R1 and R2 is setting the threshold level for OVLO. The resistor divider R3 and R4 is setting the threshold for UVLO. Keeping both dividers separate enables different hysteresis settings for UVLO and OVLO. The resistor values are calculated with Equation 1 through Equation 4.

Once U1 detects a V_{IN} undervoltage or overvoltage condition, the output is turned off. Shifting load current on the output can lead to input-voltage variations in the supply voltage and trigger repeated lockout conditions. The hysteresis should be selected so that an input-voltage change due to output-current changes does not trigger a lockout. In this design, the overvoltage hysteresis, $V_{OV(HYS)}$ (V_{OVLO_DIS} - V_{OVLO_EN}) has been set to 2 V and the undervoltage hysteresis, $V_{UV(HYS)}$ (V_{UVLO_EN} - V_{UVLO_DIS}) has been set to 1 V.

UVLO and OVLO resistor divider equations are shown in Equation 1 through Equation 4:

$$R_1 = \frac{V_{OV(HYS)}}{21\mu A} \quad (1)$$

$$R_2 = \frac{2.5\,V \times R_1}{V_{OVLO\_DIS} - 2.5\,V} \quad (2)$$

$$R_3 = \frac{V_{UV(HYS)}}{21\,\mu A} \quad (3)$$

$$R_3 = \frac{V_{UV(HYS)}}{21\,\mu A} \quad (4)$$

If an overvoltage lockout condition is detected by U1, the gate of Q1 will be discharged with 2 mA. Using Q1's gate capacitance of 5.6 nF as the the turn off time, t_{OVLO} = 50 µs.

5.2 Overcurrent Protection (eFuse)

OCP is set by R6 and R7. If the voltage drop across the parallel resistors exceeds 55 mV, which equals 11 A in the high power path, U1 pulls the gate voltage of Q1 low. The t_{OCP} is measured to 50 µs. If the voltage drop exceeds 110 mV, which equals 22 A (2 × I_{OCP}, short circuit condition) in the high power path, t_{SCP} is 0.5 µs to prevent damage of Q1. C2 = 0.47 uF gives a 340-ms insertion time. Ambient conditions (for example, temperature and air flow) can vary depending on implementation. Therefore, a thermal analysis is needed to select C2 and R5. R5 = 57.6 kΩ with R6||R7 = 5 mΩ, which corresponds to 100-W power dissipation in Q1. See *LM5069 Positive High Voltage Hot Swap / Inrush Current Controller with Power Limiting*, Data Sheet LM5069-2 for selection information on selection of C2 and R5.

R6||R7 sets the over current protection, $I_{OCP(MAX)}$ = 11 A. R6||R7 are non-Kelvin type resistors without separate voltage sense pins which cause additional resistance in the layout so that $I_{OCP(TYP)}$ = 10.3 A.

5.3 Reverse Polarity Protection

If the input (J1 and J2) is connected to a power supply with reverse polarity, so that V_{IN} becomes negative, the design will block this voltage from reaching the output. The input current under this condition is specified by I_{REV_POL}. A negative V_{IN} will connect D2 with the GND pins of U1 and U2 to V_{IN}. As the V_{DD} pins of U1 and U2 are connected to the same potential, both devices remain unpowered and Q1 and Q2 remain in high-impedance state. At negative V_{IN} , the body diode of Q1 conducts the input voltage to the drain of Q2. The high impedance in Q2 is blocking the voltage from the output of the design.

5.4 Miswire and Reverse Current Protection

Miswire and reverse-current protection are implemented using U2 to measure the source-drain voltage drop of Q2. If the voltage drop is negative, the gate of Q2 is pulled low, preventing a reverse-current flow to the input. This function also prevents the charge from an external output capacitor to flow back into the power supply, eliminating adverse effects from an input-voltage drop. A short turnoff time is desired to reduce the capacitor discharge from this reverse current. In this design the turnoff time $t_{REV(MAX)}$ = 100 ns.

5.5 Surge Protection

Surge protection is implemented using multiple stages. The first level of protection is given by the TVS diode, D1. When tested at 0.5 kV over 2 Ω, the surge pulse reaches 250 A. In this case, the voltage across D1 will rise above 55 V, and an additional protection stage is activated. The high voltage across D1 is causing a current higher than 22 A through D4, which triggers the short-circuit protection described in Section 5.2. As t_{SCP} = 0.5 µs, Q1 will turn to a high-impedance state before the 8/20 us current pulse generates a voltage exceeding 45 V across D4. The designer may add a capacitor to the output of the design covering the power interrupt caused by the surge pulse.

6 Test Setup

6.1 UVLO and OVLO

Power Supply: Hewlett Packard E3631A triple-output DC power supply 0 V to 6V, 5 A and, 0 - ±25 V, 1A

Multimeter: Wavetek 23XT

J1 (red) of the DUT is connected to the positive terminal of the power supply and J2 (black) to the negative terminal. The negative supply is set to 10 V and the positive supply can be adjusted from 0 V to 25 V. For safety reasons, the current limit is set to 50 mA.

The overvoltage lockout thresholds (V_{OVLO_DIS} and V_{OVLO_EN}) are tested by increasing the positive supply from 20 V until D8 turns *off* and then decreasing the positive supply until D8 turns *on*.

The undervoltage lockout thresholds (V_{UVLO_DIS} and V_{UVLO_EN}) are tested by increasing the positive supply from 0 V until D8 turns *on* and then decreasing the positive supply until D8 turns *off*.

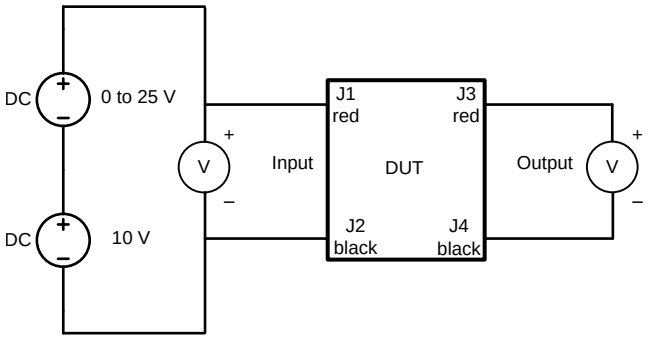


Figure 4. Measurement setup for over and under voltage lockout

6.2 Overcurrent Protection (eFuse)

Power Supply: Agilent 6574A 0 – 60V, 0-A to 35-A DC power supply

Electronic Load: Agilent 6060B 3-V to 60-V, 0-A to 60-A system DC electronic load

Multimeter: METRAHIT pro professional TRMS

J1 (red) of the DUT is connected to the positive terminal of the power supply and J2 (black) to negative terminal. In the first test V_{IN} = 12 V, and in the second test, V_{IN} = 30 V with the electronic load connected to J3 (red) and J4 (black). Under both test conditions, the load of the DUT is sequentially set to 2 A, 6 A, 8 A, and 10 A. The board temperature is monitored at each test point. At 10 A, the load current is slowly increased until the DUT turns off the output voltage.

WARNING

The operator has to take the usual precautions when handling high currents.

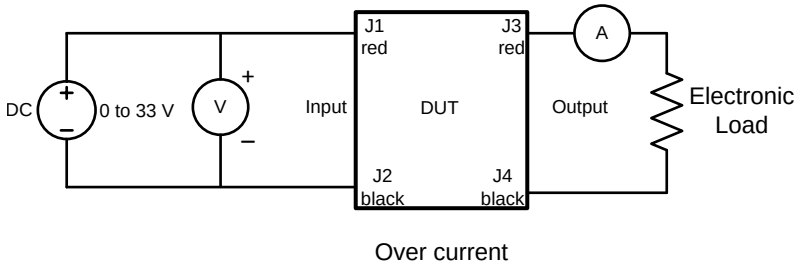


Figure 5. Measurement Setup for Circuit Breaker Function

6.3 Reverse Polarity Protection

Power Supply: Hewlett Packard E3631A triple-output DC power supply 0 V to 6V, 5 A and 0 - ±25 V, 1A

Multimeter: Wavetek 23XT

The DUT is connected to the ±25 V output of the power supply. J1 (red) is connected to the negative terminal of the power supply and J2 (black) is connected to the positive terminal. The negative supply is set to 10 V. The positive supply is set to 0 V, resulting in V_{IN} = -10 V. This process is repeated for V_{IN} = -30 V, with the positive supply set to 20 V. For safety reasons, the current limit is set to 50 mA.

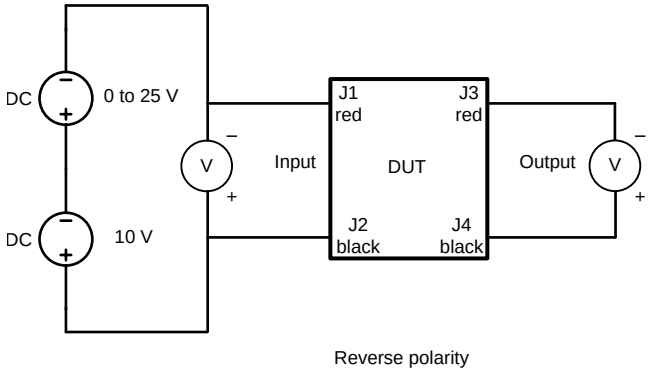


Figure 6. Measurement Setup for Reverse Polarity Current Measurement

6.4 Miswire and Reverse Current Protection

Power Supply: Hewlett Packard E3631A triple-output DC power supply 0 V to 6V, 5 A and, 0 - ±25 V, 1A

Multimeter: Wavetek 23XT

The DUT is connected to the ±25 V output of the power supply. J3 (red) is connected to the positive terminal of the power supply and J4 (black) is connected to the negative terminal. The negative supply is set to 10 V. The positive supply is set to 0 V, resulting in V_{IN} = 10 V. This process is repeated for V_{IN} = 30 V, with the positive supply set to 20 V. For safety reasons, the current limit is set to 50 mA.

I_{MIS} is measured with the multimeter (ampere meter) connected to J1 (red) and J2 (black).

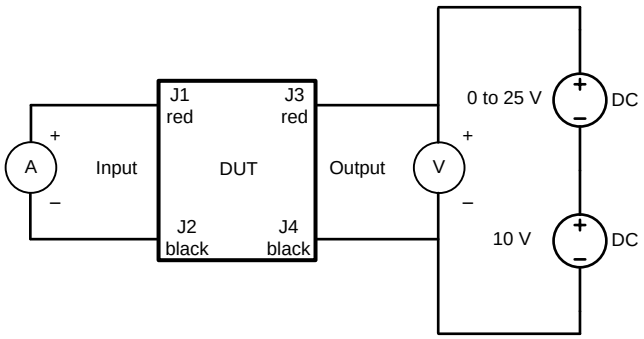


Figure 7. Measurement Setup for Miswire Protection Current Measurement

6.5 Surge Protection

EFT/Surge/ESD Generator: AMETEK, EM TEST UCS500N
Oscilloscope: Tektronix TPS2014B

The design is tested according to IEC61000-4-5 (1.2/50 µs, 2.0 Ω, 18 uF) ±0.5 kV surge specification. Compliance is confirmed in two separate tests.

6.5.1 Test 1: Power Supply Surge Test

V_{IN} = 28 V. The surge pulse is injected using a surge generator with coupling network as described in Figure 8. Test 1 is performed with 4 different loads: open circuit, I_L = 280 mA, 10A, and short circuit, connected to J3 (red) and J4 (black). The correct function of the design is first verified using a multimeter with a peak detector. A battery-powered oscilloscope is then connected in parallel with the load to record U_L. The surge pulse is applied 5 times at 0.5 kV and 5 times at -0.5 kV.

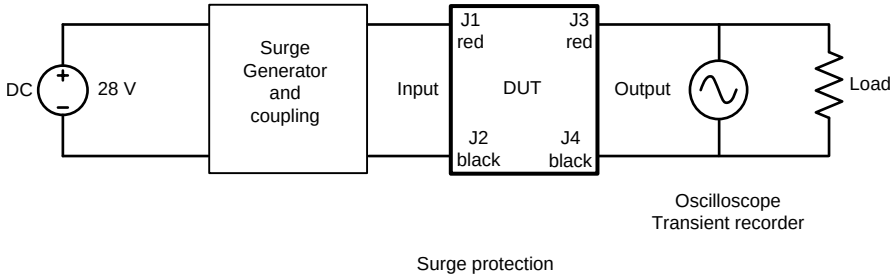


Figure 8. Measurement Setup for Surge Test

6.5.2 Test 2: Reverse Power Surge Test

The power supply is connected to J3 and J4 with a voltage set to 28 V. An oscilloscope is connected between J1 and J2 to record transients. The surge pulse is injected using a surge generator with coupling network to J3, as described in Figure 9.

To verify proper operation of the surge protection, Test 1 is repeated after Test 2 with the same DUT, to ensure Test 2 caused no derating.

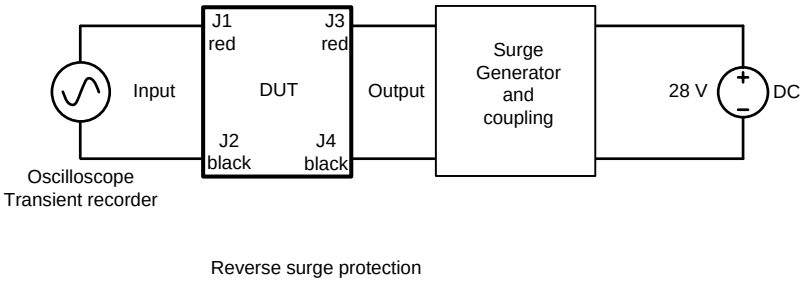


Figure 9. Measurement Setup for Reverse Power Surge Test

7 Test Results

7.1 Measurement Results

Table 2 shows the test results for normal operation and during surge conditions.

Table 2. Test Results Compared to Design Specification

SYMBOL	PARAMETER	CONDITIONS	SPECIFICATION			MEAS.	UNIT
			MIN.	TYP.	MAX.		
V_{IN}	Input voltage	Normal operation	-33	24	33		V
I_Q	Quiescent current(1)	Normal operation	5	7.6	10	7.6	mA
V_{OVLO_DIS}	OVLO output disabled	V_{IN} increasing	-	32.5	33.0	32.5	V
V_{OVLO_EN}	OVLO output re-enabled	V_{IN} decreasing	29.9	30.5	-	30.5	V
t_{OVLO}	OVLO delay	V_{IN} increasing			50	TBM	µs
U_{UVLO_EN}	UVLO output enabled	V_{IN} increasing	-	12.4	12.64	12.45	V
U_{UVLO_DIS}	UVLO output disabled	V_{IN} decreasing	11.29	11.4	-	11.49	V
I_{OCP}	OCP	V_{IN} = 12 V or 30 V	-	10.3	11	10.3	A
t_{OCP}	OCP delay	$I > I_{OCP}$			50	TBM	µs
t_{SCP}	SCP delay	$I > 2 \times I_{OCP}$			0.5	TBM	µs
I_{REV_POL}	Reverse polarity protection current	V_{IN} = -30 V or -10 V		0.1	1	0.1	µA
I_{MIS}	Miswire and reverse-current protection current	V_{IN} = 10 V, 12 V, or 30 V	2.0	2.2	3	2.2	mA
t_{REV}	Miswire and reverse-current protection delay			40	100	TBM	ns
V_{SURGE_pp}	Peak output voltage during surge	V_{IN} = 30 V+ 500 V surge	0.0		45		V

(1) Without indicator LEDs, the quiescent current is reduced by 2 x I_LED = 2 x 2.2 mA (Vin = 24 V) = 4.4 mA.

7.2 Surge Protection

Figure 10 through Figure 15 show the output voltage of the protection device at different load conditions during a surge pulse of 500 V. The device is effectively blocking all dangerous input voltages towards the load. The maximum output voltage exists during lightly loaded conditions. In that case, the output voltage reaches its maximum at 45 V before it shuts down for 250 ms. Also, a negative output voltage could be observed, which is low energy and results from capacitive coupling through MOSFETs Q1 and Q2.

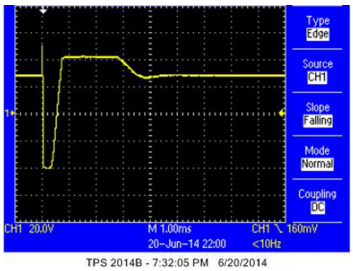


Figure 10. Output Voltage of the Protection Device during Surge at No Load

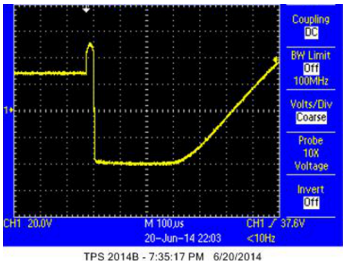


Figure 11. Zoom into the Waveform in Figure 10 at the Surge Location

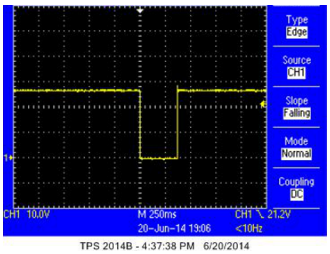


Figure 12. Output Voltage of the Protection Device during Surge at 100-Ω Load

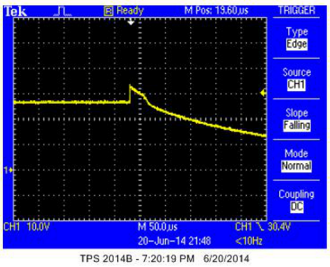


Figure 13. Zoom into Figure 12

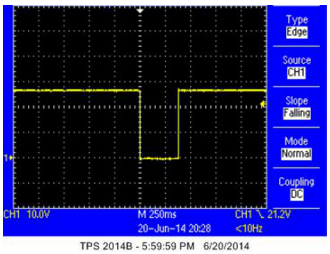


Figure 14. Output Voltage of the Protection Device during Surge at 15-Ω Load

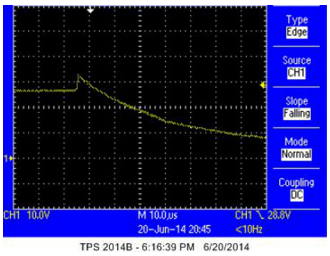


Figure 15. Zoom into Figure 14

8 Design Files

8.1 Schematics

To download the Schematics, see the design files at TIDA-00233.

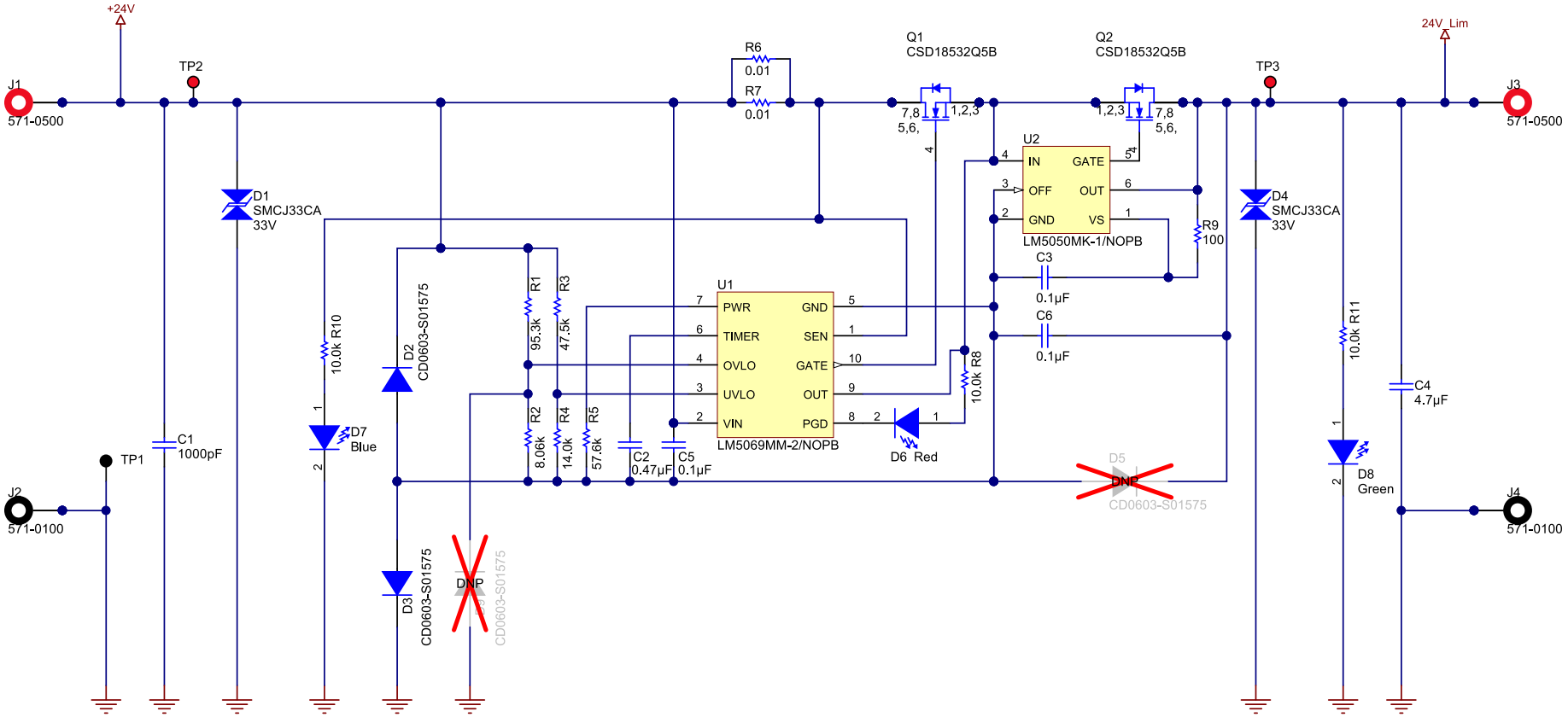


Figure 16. Schematics — Protection

8.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00233.

Table 3. BOM

DESIGNATOR	DESCRIPTION	MANUFACTURER	PARTNUMBER	QTY	SUPPLIER 1	SUPPLIER P/N 1	SUPPLIER 2	SUPPLIER P/N 2
C1	CAP, CERM, 1000pF, 100V, +/-5%, X7R, 0603	AVX	06031C102JAT2A	1	Digi-Key	478-3698-1-ND	Mouser	581-06031C102J
C2	CAP, CERM, 0.47uF, 50V, 10%, X5R, 0603	Taiyo Yuden	UMK107ABJ474KA-T	1	Digi-Key	587-3171-6-ND		
C3, C5, C6	CAP, CERM, 0.1uF, 100V, +/-10%, X7R, 0603	MuRata	GRM188R72A104KA35D	3	Digi-Key	490-3285-1-ND	Mouser	81-GRM188R72A104KA35
C4	CAP, CERM, 4.7uF, 100V, +/-10%, X7S, 1210	TDK	C3225X7S2A475K200AB	1	Digi-Key	445-6042-1-ND	Mouser	810-C3225X7S2A475K
D1, D4	Diode, TVS, Bi, 33V, 1500W, SMC	Littlefuse	SMCJ33CA	2	Digi-Key	SMCJ33CALFCT-ND	Mouser	576-SMCJ33CA
D2, D3, D5, D9	Diode, Switching, 100V, 0.15A, 0603 Diode	Bourns	CD0603-S01575	2	Digi-Key	CD0603-S01575CT-ND	Mouser	652-CD0603-S01575
D6	LED, Red, SMD	Lite-On	LTST-C190CKT	1	Digi-Key	160-1181-1-ND	Mouser	859-LTST-C190CKT
D7	LED, Blue, SMD	OSRAM	LB Q39G-L2N2-35-1	1	Digi-Key	475-2816-1-ND	Mouser	720-LBQ39GL2N2351
D8	LED, Green, SMD	Lite-On	LTST-C190KGKT	1	Digi-Key	160-1435-1-ND	Mouser	859-LTST-C190KGKT
H2, H5, H8, H11	Standoff, Hex, 0.5 in.L #4-40 Nylon	Keystone	1902C	4	Digi-Key	1902CK-ND		
H3, H6, H9, H12	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	B and F Fastener Supply	NY PMS 440 0025 PH	4	Digi-Key	H542-ND		
J1, J3	Standard Banana Jack, insulated, 10A, red	DEM Manufacturing	571-0500	2	Newark	30M0087	Mouser	164-6219
J2, J4	Standard Banana Jack, insulated, 10A, black	DEM Manufacturing	571-0100	2	Newark	45M6896	Mouser	164-6218
LBL1	Thermal Transfer Printable Labels, 0.650 in. W x 0.200 in. H	Brady	THT-14-423-10	1	Newark	97C5133	Farnell	2065596

Table 3. BOM (continued)

DESIGNATOR	DESCRIPTION	MANUFACTURER	PARTNUMBER	QTY	SUPPLIER 1	SUPPLIER P/N 1	SUPPLIER 2	SUPPLIER P/N 2
Q1, Q2	MOSFET, N-CH, 60V, 172A, SON 5x6mm	Texas Instruments	CSD18532Q5B	2	Digi-Key	296-35628-1-ND	Mouser	595-CSD18532Q5B
R1	RES, 95.3k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060395K3FKEA	1	Digi-Key	541-95.3KHCT-ND	Mouser	71-CRCW0603-95.3K-E3
R2	RES, 8.06k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06038K06FKEA	1	Digi-Key	541-8.06KHCT-ND	Mouser	71-CRCW0603-8.06K-E3
R3	RES, 47.5k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060347K5FKEA	1	Digi-Key	541-47.5KHCT-ND	Mouser	71-CRCW0603-47.5K-E3
R4	RES, 14.0k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060314K0FKEA	1	Digi-Key	541-14.0KHCT-ND	Mouser	71-CRCW0603-14K-E3
R5	RES, 56.0k ohm, 0.1%, 0.1W, 0603	Vishay-Dale	CRCW060357K6FKEA	1	Digi-Key	541-57.6KHCT-ND	Mouser	71-CRCW0603-57.6K-E3
R6, R7	RES, 0.01 ohm, 1%, 1W, 1206	Vishay-Dale	WSLP1206R0100FEA	2	Digi-Key	WSLP-.01CT-ND	Mouser	71-WSLP1206R0100FEA
R8, R10, R11	RES, 10.0k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060310K0FKEA	3	Digi-Key	541-10.0KHCT-ND	Mouser	71-CRCW0603-10K-E3
R9	RES, 100 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603100RFKEA	1	Digi-Key	541-100HCT-ND	Mouser	71-CRCW0603-100-E3
TP1	Test Point, Miniature, Black, TH	Keystone	5001	1	Digi-Key	5001K-ND		
TP2, TP3	Test Point, Miniature, Red, TH	Keystone	5000	2	Digi-Key	5000K-ND		
U1	Positive High Voltage Hot Swap / Inrush Current Controller	Texas Instruments	LM5069MM-2/NOPB	1	Digi-Key	LM5069MM-2/NOPBTR-ND		
U2	LM5050-1 High Side OR-ing FET Controller	Texas Instruments	LM5050MK-1/NOPB	1	Digi-Key	LM5050MK-1/NOPBTR-ND		

8.3 Layout Guidelines

To withstand the IEC61000-4-5 (1.2/50 µs) ±0.5 kV surge specification, the PCB layout needs special attention. The surge current is passed over the pads of D1 and D4. The trace width has to be at least 8 mm for longer traces in free air to support $I_{OCP(MAX)}$ = 11 A. As the 24-V pin of D1 has a short trace, D1 provides additional cooling area and the trace width is reduced to 6 mm. The other high power traces are laid out as copper areas.

Q1 and Q2 are cooled using PCB copper area. The PCB copper area size needs to be large enough to dissipate the heat over the design's operating temperature range. Q1 has a copper area of 1.2 cm^2 available on the top layer and 1.1 cm^2 on the bottom layer. Q2 has a copper area of 0.5 cm^2 available on the top layer and 1.8 cm^2 on the bottom layer.

R6||R7 are preferably resistors of Kelvin type, where the high power path uses separate connection pads in addition to the pads for the SENSE and V_{IN} pins of the U1. See Figure 17. To optimize the design for footprint, resistors of non-Kelvin type are used, which adds the R6||R7 pads' resistance so that $I_{OCP(TYP)}$ = 10.3 A.

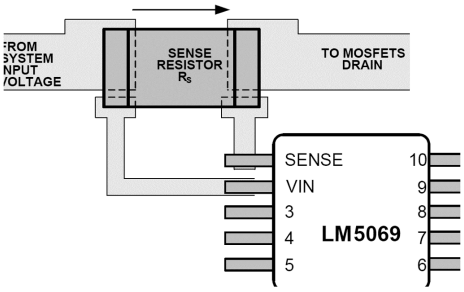


Figure 17. U1 SENSE and V_{IN} Pin Pad Connection using Resistors of Kelvin Type

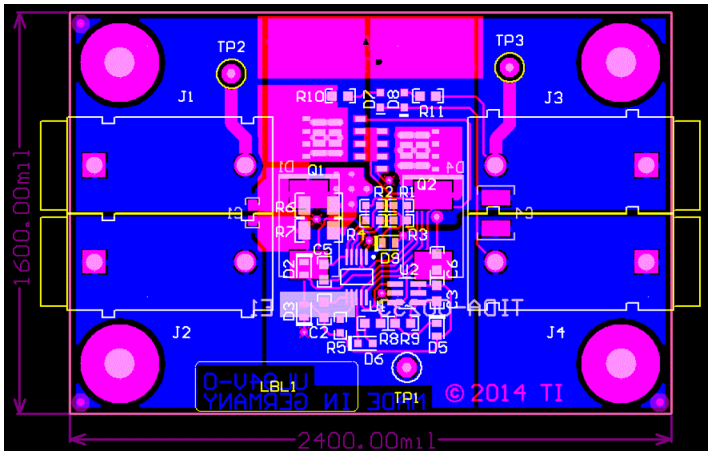


Figure 18. All Layers

8.4 Layer Plots

To download the layer plots, see the design files at TIDA-00233.

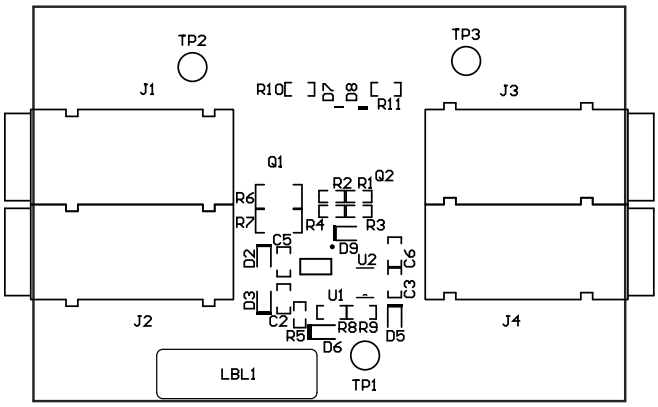


Figure 19. Top Silkscreen

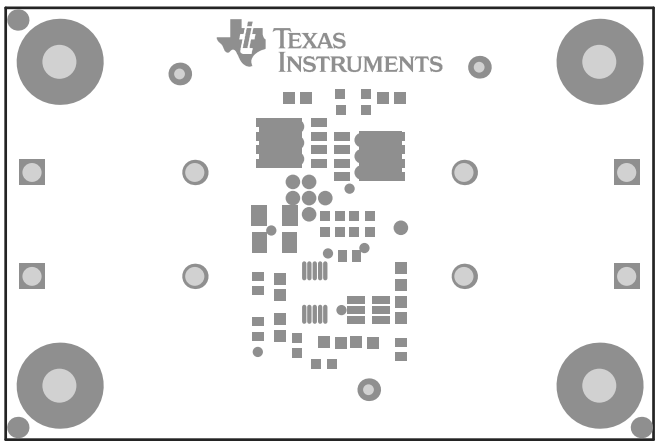


Figure 20. Top Solder Mask

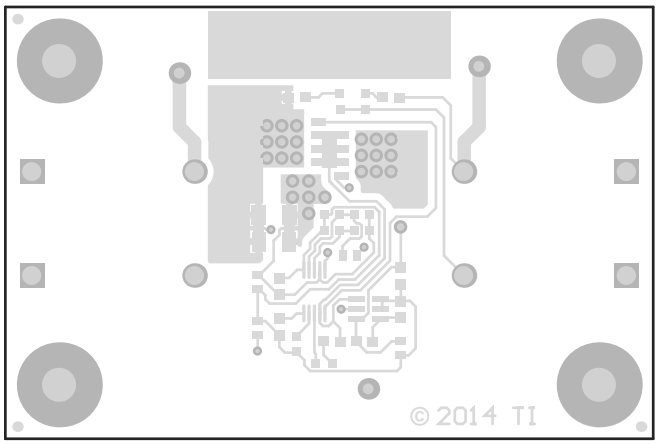


Figure 21. Top Layer

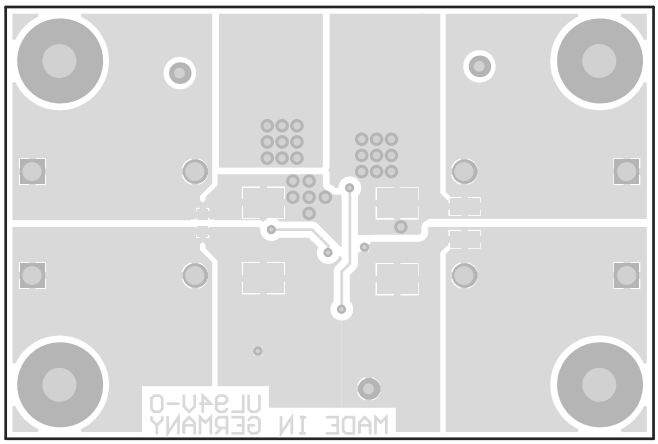


Figure 22. Bottom Layer

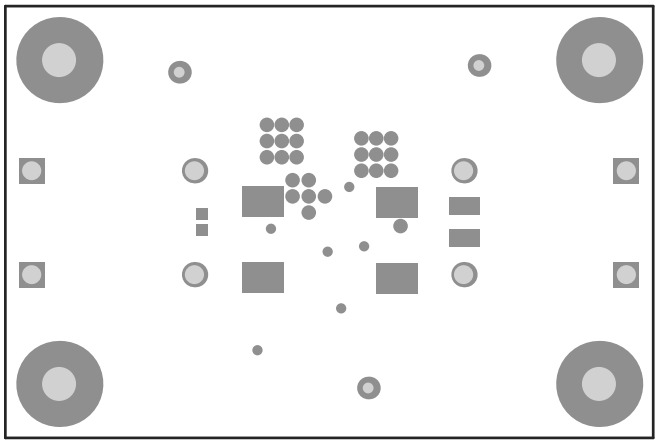


Figure 23. Bottom Solder Mask

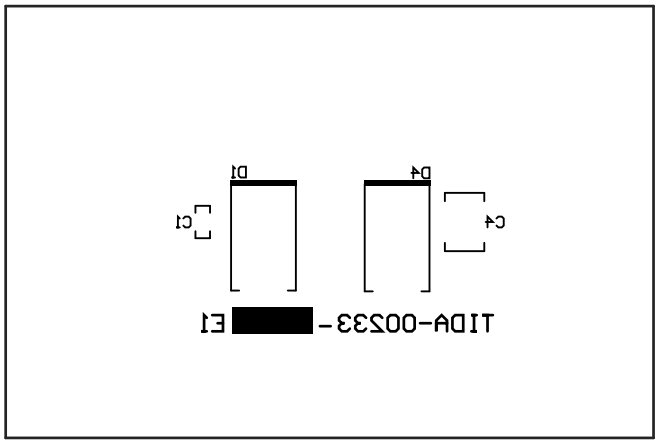
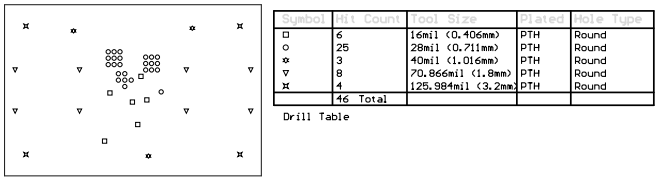


Figure 24. Bottom Silkscreen



Symbol	Hit Count	Tool Size	Plated	Hole Type
□	6	16mil (0.406mm)	PTH	Round
○	25	28mil (0.711mm)	PTH	Round
✡	3	40mil (1.016mm)	PTH	Round
▽	8	70.866mil (1.8mm)	PTH	Round
✖	4	125.984mil (3.2mm)	PTH	Round
	46 Total			

Drill Table

Figure 25. Drill Drawing

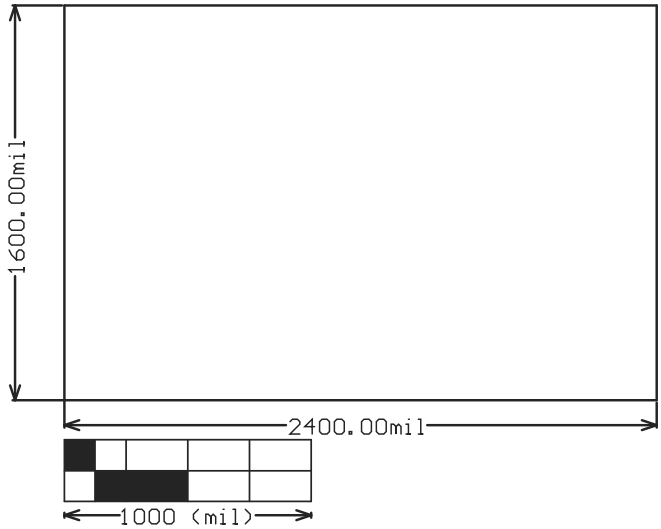


Figure 26. Board Dimensions

8.5 Altium Project

To download the Altium project files, see the design files at TIDA-00233.

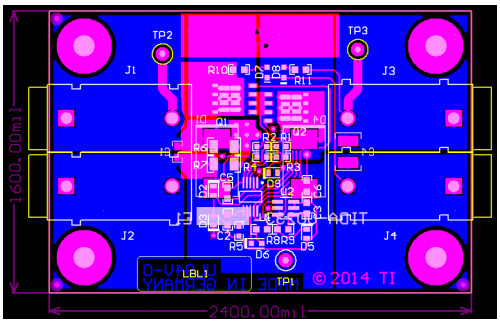


Figure 27. All Layers

8.6 Gerber Files

To download the Gerber files, see the design files at TIDA-00233

8.7 Assembly Drawings

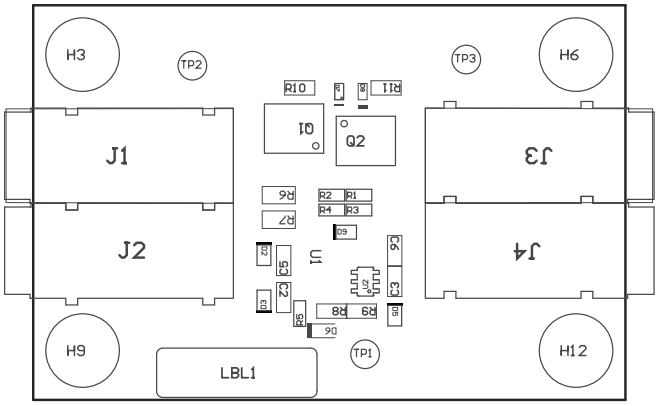


Figure 28. Top Assembly Drawing

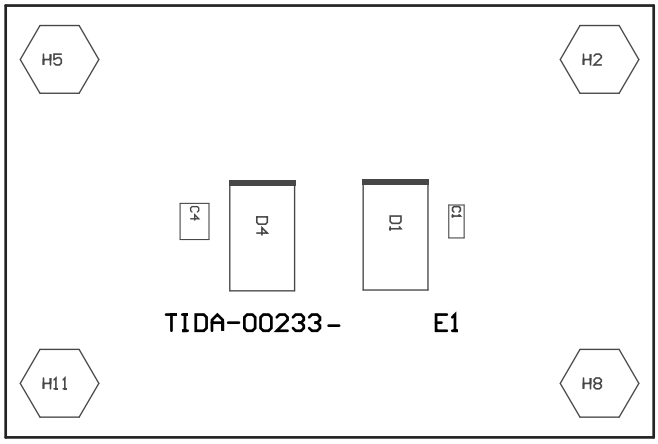


Figure 29. Bottom Assembly Drawing

8.8 Software Files

To download the software files, see the design files at TIDA-00233

9 References

1. *LM5050-1/LM5050-1-Q1 High Side OR-ing FET Controller*, Data Sheet LM5050-1
2. *LM5069 Positive High Voltage Hot Swap / Inrush Current Controller with Power Limiting*, Data Sheet LM5069-2

10 About the Author

INGOLF FRANK is a systems engineer in the Texas Instruments Industrial Automation Team, focusing on programmable logic controller I/O modules. Ingolf works across multiple product families and technologies to leverage the best solutions possible for system level application design. Ingolf earned his Electrical Engineering degree (Dipl. Ing. (FH)) in the field of information technology at the University of Applied Sciences Bielefeld, Germany in 1991.

HENRIK MANNESSON is a System Engineer at Texas Instruments Germany, in the Factory Automation and Control System Team. Henrik earned his Master of Science in Electrical Engineering (MSEE) from Lunds University of Technology (LTH), Lund, Sweden.

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ("TI") reference designs are solely intended to assist designers (“Buyers”) who are developing systems that incorporate TI semiconductor products (also referred to herein as “components”). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer’s systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. **TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.** TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED "AS IS". TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER’S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer’s safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have ***not*** been so designated is solely at Buyer's risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265