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Energy Buffering for Long-Life Battery Applications

Reference Guide & Test Report

CIRCUIT DESCRIPTION

Long Life Batteries like $LiSOCl_2$ chemistry in a bobbin type cell construction have a very high Specific energy (Wh/kg) but are unable to provide currents higher than e.g. 20mA. They furthermore suffer with reduced operation runtimes when higher currents are drawn.

This application concept shows a proven reference design for a combination of TPS62740 and a Super-Capacitor powered by a long life primary cell.

In this Reference Design, the Ultra-Low Quiescent Current Buck Converter TPS62740 charges a Supercapacitor to buffer energy for load peaks.

BENEFITS

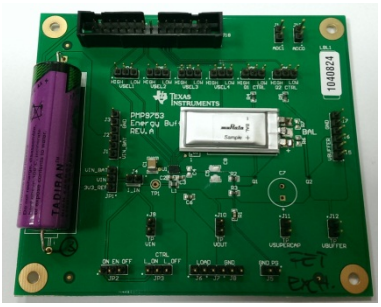
- Peak Power Assistance
- Energy Buffering
- Longer Battery Runtime
- >15 Years operating Runtime
- Efficient Super Capacitor Charging

APPLICATIONS

- Wireless Sensor Nodes
- Smart Flow Meter
- Heat Cost Allocator

LINKS

TPS62740 Product Page
TPS62740 Evaluation Module
Energy Buffering Application Note



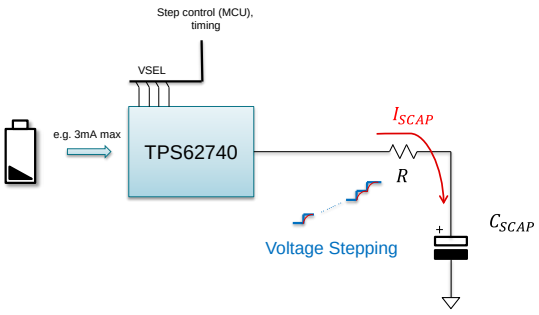


TABLE OF CONTENTS

LIST OF FIGURES

1 Introduction

Battery chemistries like the $LiSOCl_2$ type offer great benefits in terms of application runtime. They bring operation runtimes of 15 years and more to reality.

The technology, however, has a limited characteristic in terms of supporting higher loads.
Higher load pulses cannot be supported by the battery itself due to the internal impedance. As well, the higher the drawn current, the shorter the battery operation. Figure 1 shows, how different battery currents translates to different battery runtimes.

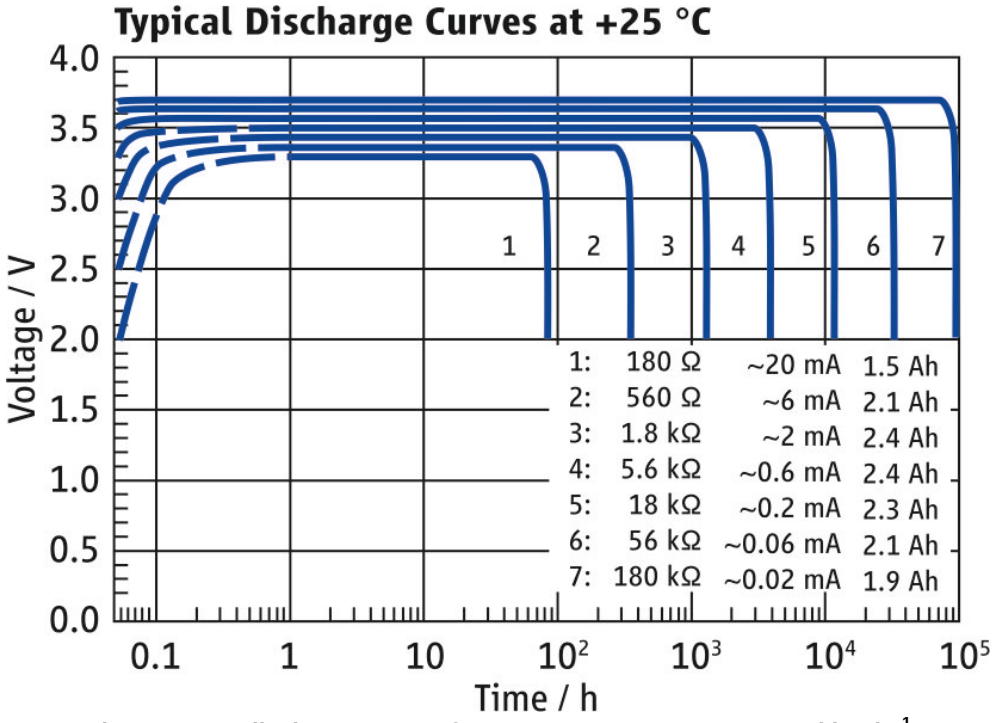


Figure 1: typ. discharge curve of a TADIRAN SL-360 over several loads [1]

To overcome these limitations, peak power assistance concepts have to be considered.
For example, a wireless Sensor node transmits its gathered data once a day to a base station. The data transmission requires 500mA for 200ms. This short power peak cannot be supported by the primary cell itself. The pulse needs to be buffered somewhere else.

[1] http://www.tadiranbatteries.de/pdf/lithium-thionyl-chloride-batteries/SL-360.pdf

2 Reference Design Description

This Reference Design shows an Energy Buffering Concept based on the TPS62740, a 360nA quiescent current buck converter, in combination with an EDLC (electric double layer capacitor) or a so called Supercapacitor.

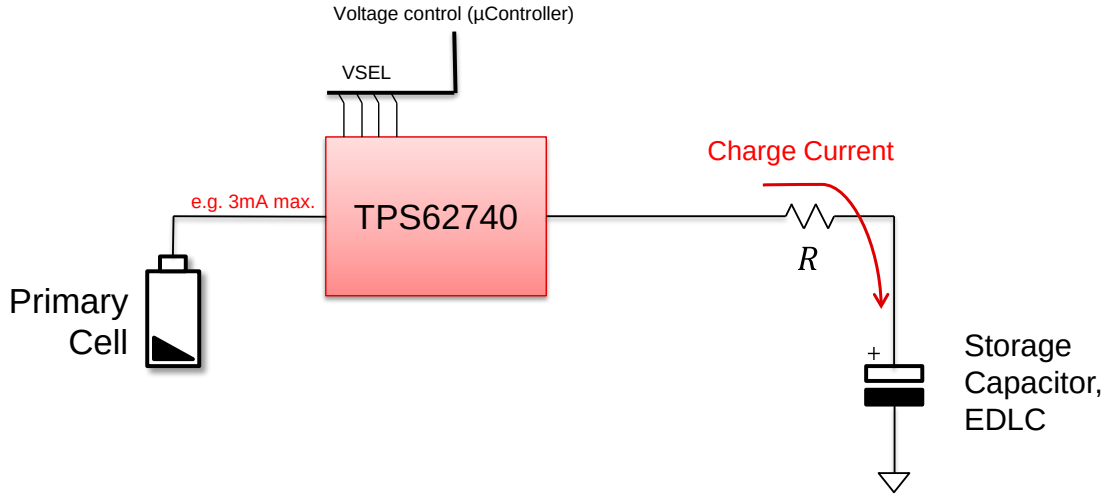


Figure 2: Simplified charging block diagram

The circuit uses a resistor at the output of the TPS62740 to limit the current into the Storage Capacitor as well as the battery current drawn from the primary cell. The resistor will be selected in a way to keep the load and thereby the battery current below a level, the primary battery can support. The TPS62740 features a digital input to adjust the output voltage by four VSEL Pins. During the charging of the EDLC, the output voltage can be stepped up in 100mV steps. This helps to minimize the power losses caused by the resistor.

In an application like a wireless sensor, the µController will be supplied from the output of the TPS62740 step-down converter. Therefore the voltage must stay above the µController minimum supply voltage (e.g. 1.9V). The maximum voltage of a single layer super-cap is typically 2.7V which leads to a usable capacitor voltage range of 1.9V to 2.7V

Figure 3 shows the basic flow of a recharge cycle.

Most of the time the voltage is kept at 1.9V to minimize the losses of the micro-controller and other leakage currents in the application (Phase 1). Prior a wireless data transmission, the capacitor is charged up to 2.7V (Phase 2). During transmission the stored energy in the capacitor can be extracted down to 1.9V (Phase 3).

For a more detailed description including component and parameter calculations, please see Application Report TIDU628.

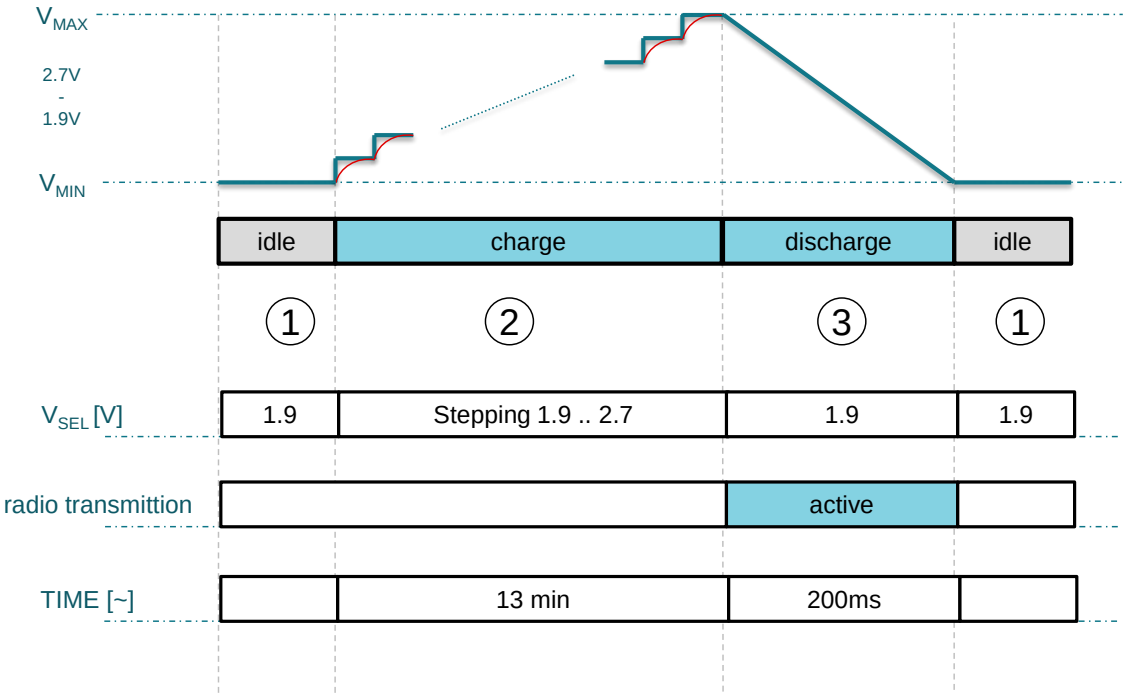


Figure 3: Recharge Cycle Sequencing

2.1 Detailed Block Diagram

Figure 4 below shows the Block Diagram of the Energy Buffering Reference Design. It consists of following main blocks:

- Primary Cell
- TPS62740 Buck Converter
- Current Limiting Resistor Network
- Storage Capacitor
- Connection to the µController

The $LiSoCl_2$ primary cell is directly connected to the TPS62740. The Buck Converter is controlled by the available µController in the Application. The MCU enables/disables the Buck Converter, adjusts the output voltage and enables the efficient charging as shown in Figure 3.
The output of the DC/DC Converter is connected to the current limiting resistor. Figure 4 shows two resistors, one resistor can be connected by a switch. This is designed to handle the start-up procedure which is necessary to pre-charge the EDLC to the minimum Voltage of 1.9V. To not exceed the maximum battery current, only the 300Ω resistor is used.
Once the Storage Capacitor is pre-charged, the switch is turned on and the current is limited by the combined resistance.

A load like a radio power amplifier can now be directly connected to the storage capacitor which does support larger peak currents to be drawn from it.

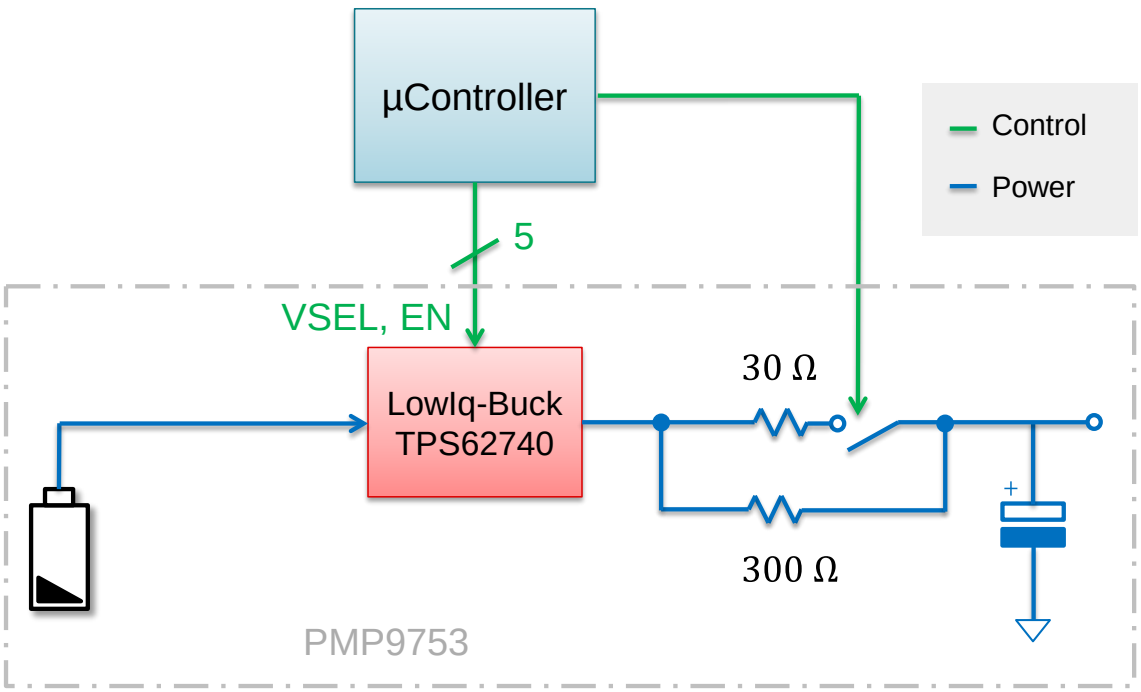


Figure 4: Reference design block diagram

2.2 Wireless Metering-Bus Circuit Definition

The measurement results presented in this document use the following typical use case: A Wireless-Metering-Bus (wM-Bus) data transmission with following parameters:

- Battery Voltage = 3.6V
- Maximum battery current = 3mA
- Transmission duration = 200ms
- Transmission power = 1000mW

The consideration is that the system uses a $LiSoCl_2$ primary battery. The primary cell is fresh and has a voltage of 3.6V. To make sure not to reduce the battery operation runtime, the battery current should not exceed 3mA during continuous operation.
It is only necessary to buffer the energy for one wM-Bus data transmission which requires 1000mW and has duration of maximum 200ms. To have enough margins, a 0.47F capacitor is used.
To achieve a system runtime of at least 15 years, the muRata EDLC DMF3Z5R5H474M3DTA0 is only charged up to 2.7V. Another benefit of keeping the voltage at this level is that there is no need for balancing which would add additional energy losses.

For more details around the calculation of the parameters and devices' values, please refer to Energy Buffering Application Report TIDU628.

2.3 Schematic

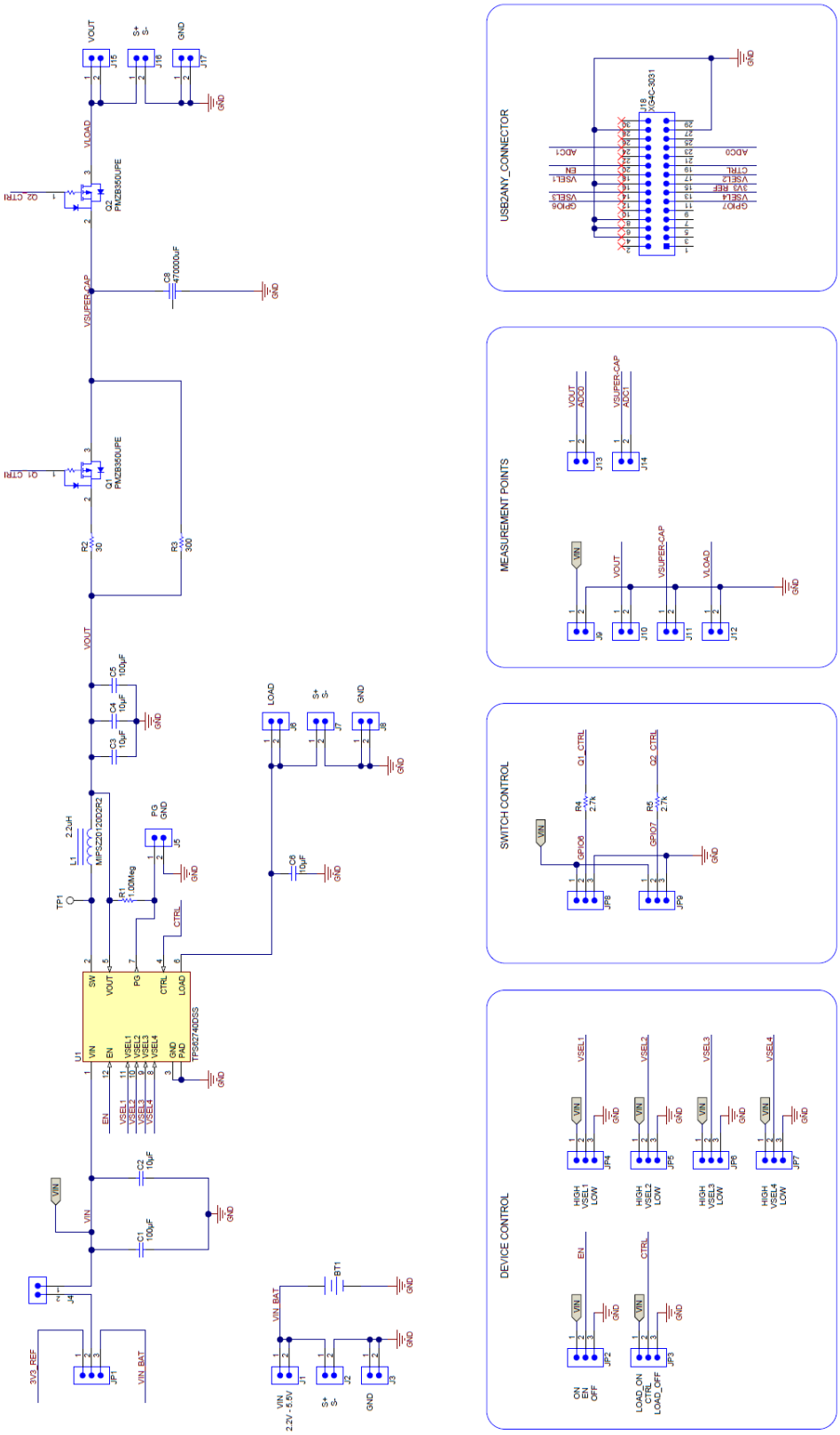


Figure 5: PMP9753 schematic

3 Measurement Results

Following Section shows the results of the start-up sequence where the EDLC is pre-charged to its minimum value. It also shows the results of the regular recharge cycle and the conversion efficiency for charging the capacitor.

3.1 Start-up behavior

Figure 6 shows the circuit configuration during start-up. For this scenario only the higher 300Ω resistor is used.
As the input current must not be higher than ~3.5mA during start-up, the corresponding output current has to be limited to 6.3mA. For the initial voltage step of 1.9V, the resistor value is chosen as 300Ω
For more detailed calculations, please refer to Energy Buffering Application Report TIDU628.

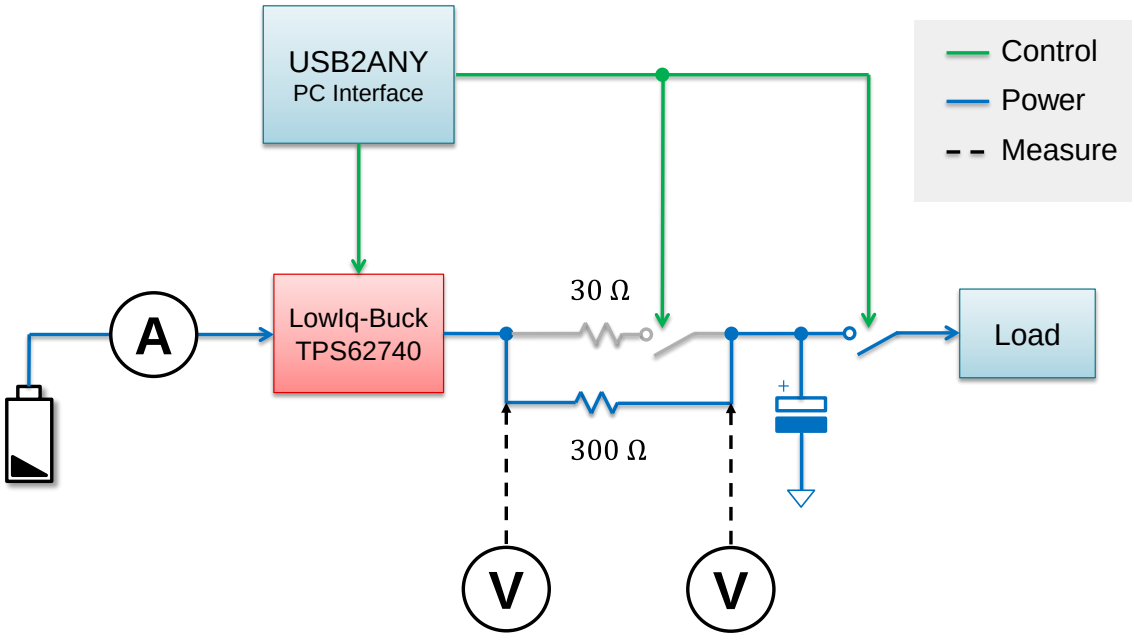


Figure 6: Start-up circuit configuration

Following graph shows the curves of the voltage across the EDLC and the battery current drawn. It shows that the battery current is limited to 3.7mA which corresponds to the calculated value above. This current is just flowing for the first time the application is powered up and it becomes smaller the higher the voltage at the storage capacitor is.

This sequence occurs at the very first initializing of the circuit. It just happens once in the whole lifetime of the application.

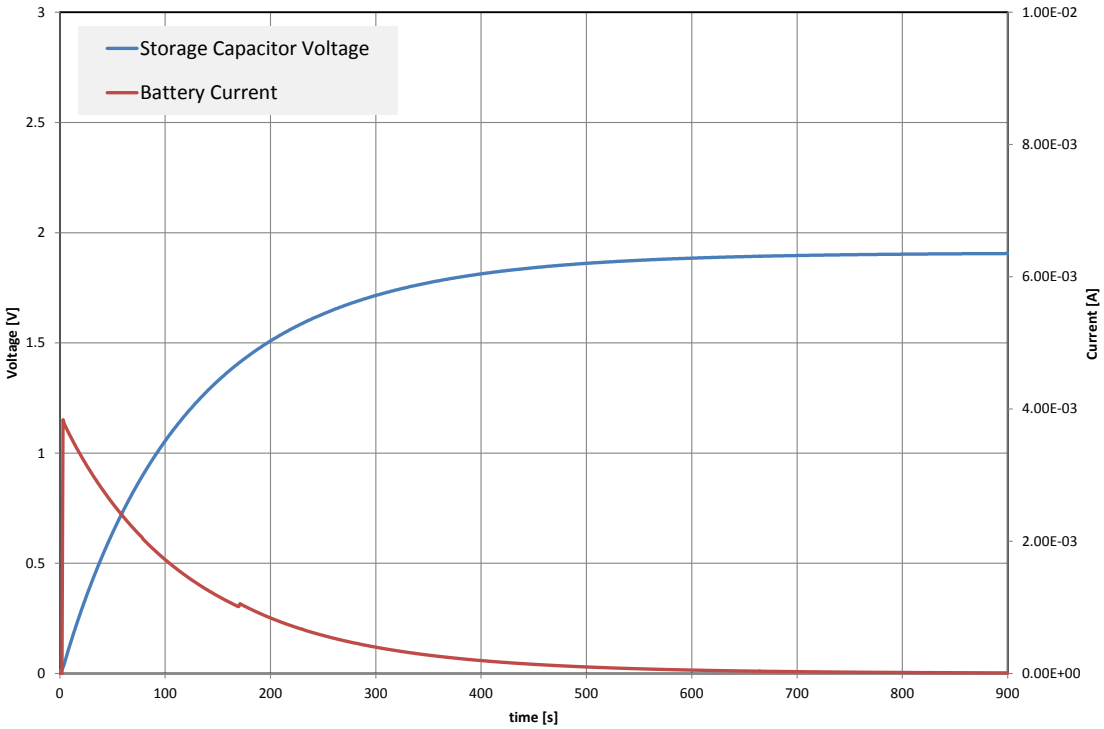


Figure 7: Battery current and capacitor voltage during pre-charge

3.2 Recharge Sequence Results

The block diagram in Figure 8 shows the measurement setup for the recharge sequence. This sequence is present prior every data transmission in the application.

The test sequence is controlled by TI's USB2ANY Interface and a LabVIEW program. The software controls the VSEL-Pins and adjusts the output voltage. This is how the sequencing in Figure 3 is implemented.
In a normal application this is controlled by the µController that is present.

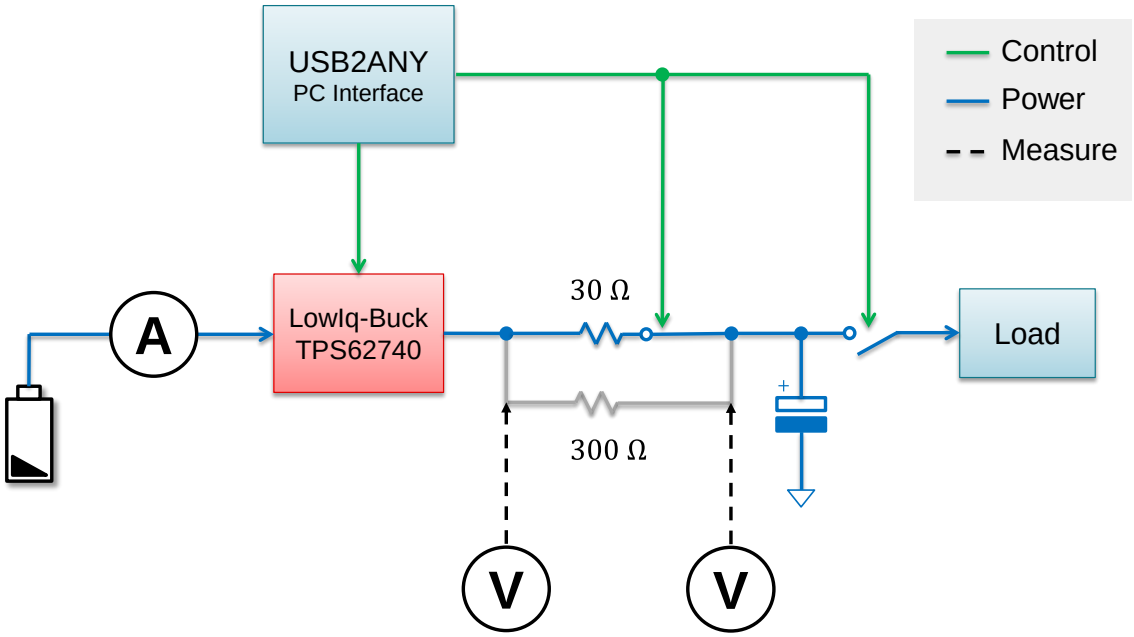


Figure 8: Diagram of the measurement setup

Figure 9 shows the waveforms in the application during a recharge cycle of the EDLC. In this sequence, the initial voltages at the storage capacitor as well as at the output of TPS62740 are at 1.9V.

Prior a wM-Bus data transmission, the capacitor is charged up by incrementing the TPS62740 output voltage in steps of 100mV.

Between the steps, the capacitor charges up to the next higher 100mV value. The current is limited by the resistor to its maximum value right after a step in the DC/DC converter's output voltage occurred and it decreases as expected in a RC-charge configuration. Once the capacitors voltage is at the level of the DC/DC converters output the next higher output voltage of the TPS62740 is selected. This way the voltage drop across the current limiting resistor will always be 100mV or below leading to reduced energy losses and highly efficient charging of the super-capacitor from 1.9V to 2.7V

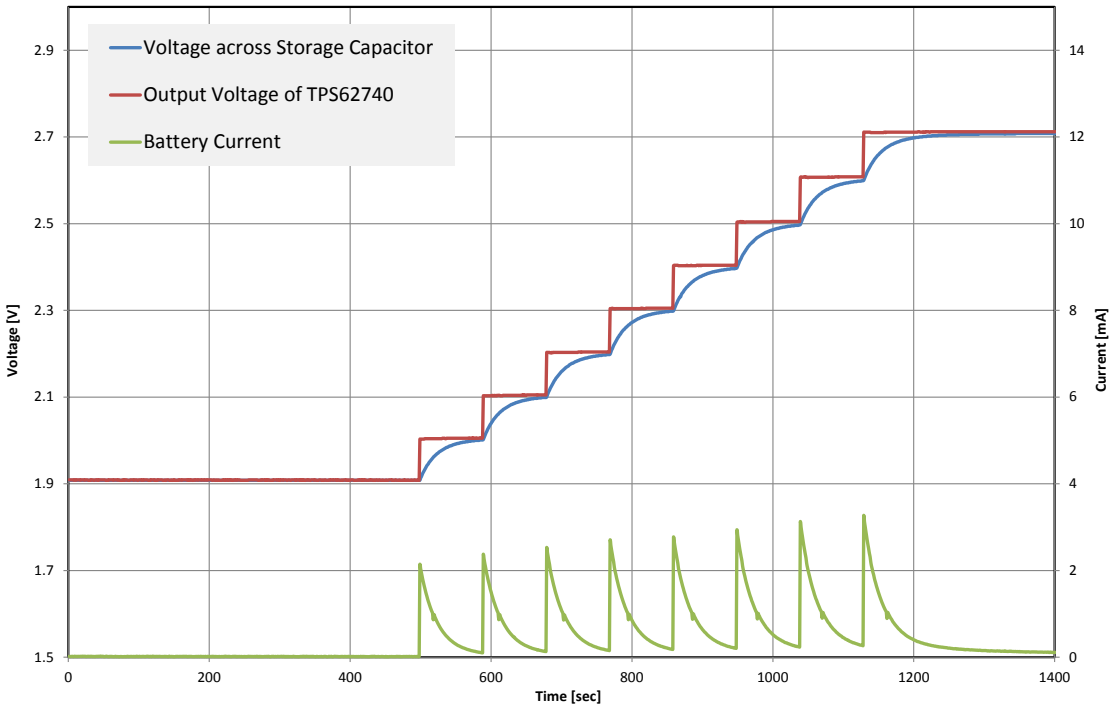


Figure 9: Charging waveforms

3.3 Recharge Conversion Efficiency Results

Figure 10 shows that the loss of the whole power conversion from the primary cell to the EDLC is split. It is the sum of the losses caused by the DC/DC Converter and the current limiting resistor.

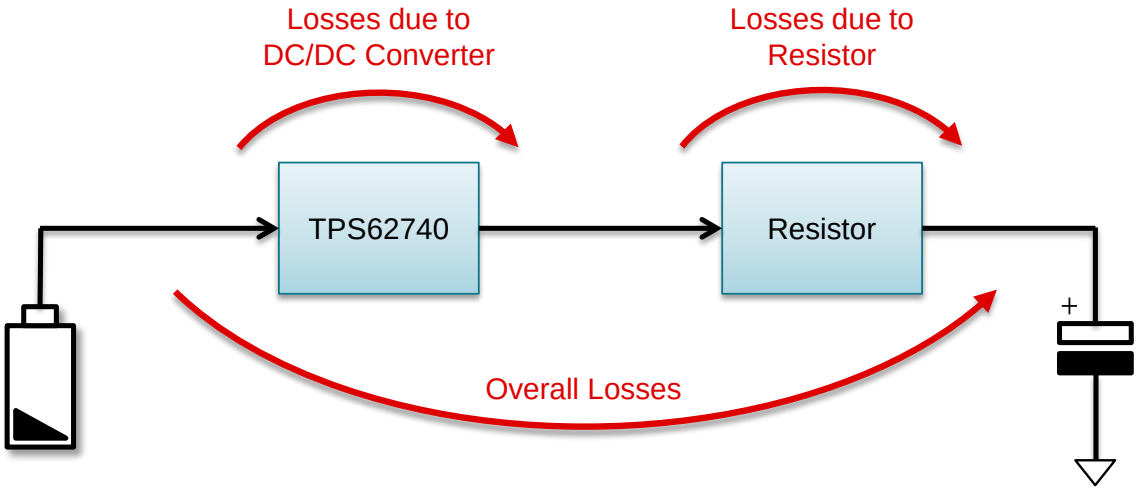


Figure 10: Conversion efficiency

The DC/DC Efficiency is found from Datasheet Curves. An excerpt is shown in Figure 11. Taking the curve, with an input voltage of 3.6V, the efficiency at 4.5mA of output current is ~91%. At this TPS62740 output current, the battery current is in the range of 2-3mA (Figure 9).

The highest losses are generated right after a new output voltage step, where the current through the resistor is the highest. For this case, the power loss is at its maximum.
Between two steps, the current decreases and therefore the resistor losses decrease as well. As shown in Figure 11, the Efficiency of the TPS62740 stays above 90% even down to 100µA.

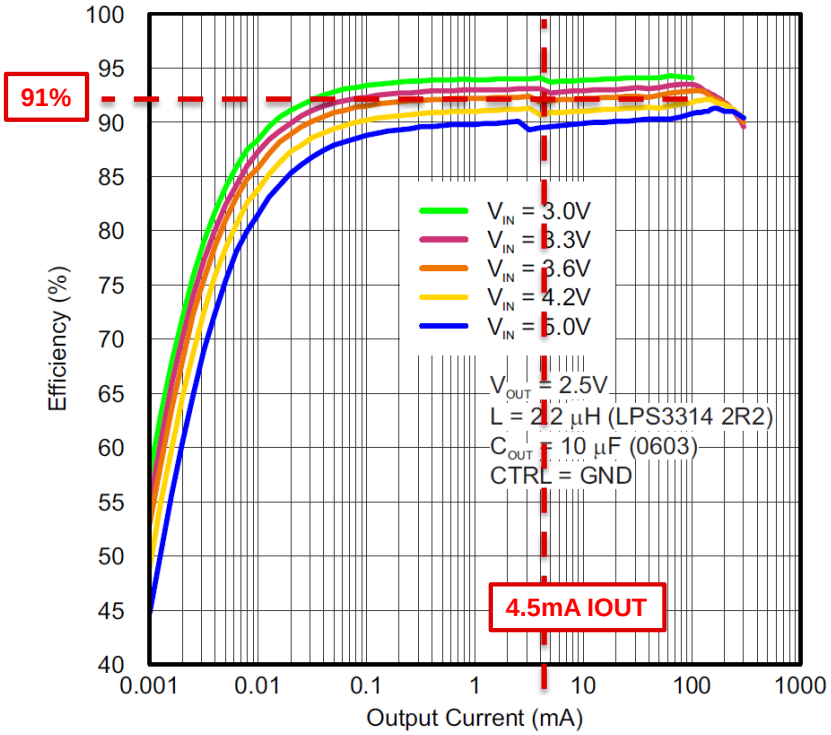


Figure 11:TPS62740: Efficiency vs. output current

The energy conversion efficiency is measured with the setup as shown in Figure 12.
The input power is taken by measuring the battery current multiplied by the battery voltage.
The energy stored in the capacitor is determined by the charging current through the resistor and the voltage across the capacitor.
Figure 13 shows the overall power losses for the conversion sequence. In Figure 14, the energy drawn from the battery and the one stored in the EDLC are monitored and put into perspective. It shows that the energy buffering concept show in this document has an conversion efficiency close to 90%.

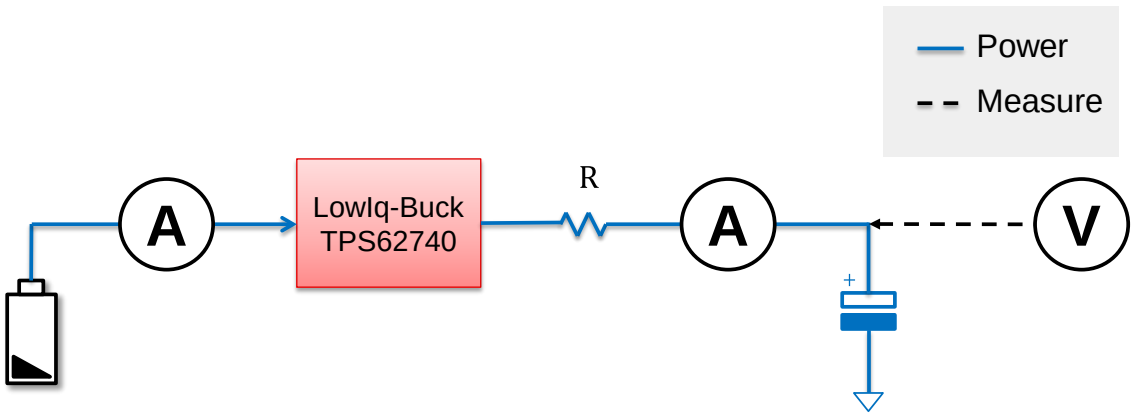


Figure 12: Energy conversion efficiency measurement setup

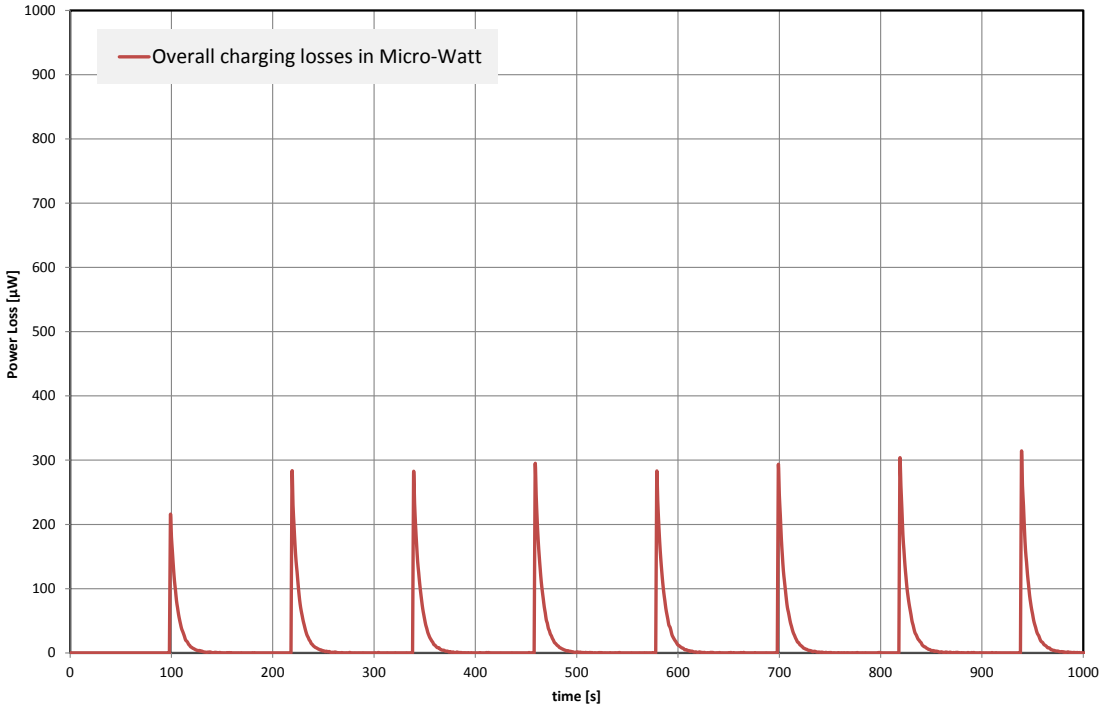


Figure 13: Overall charging power losses

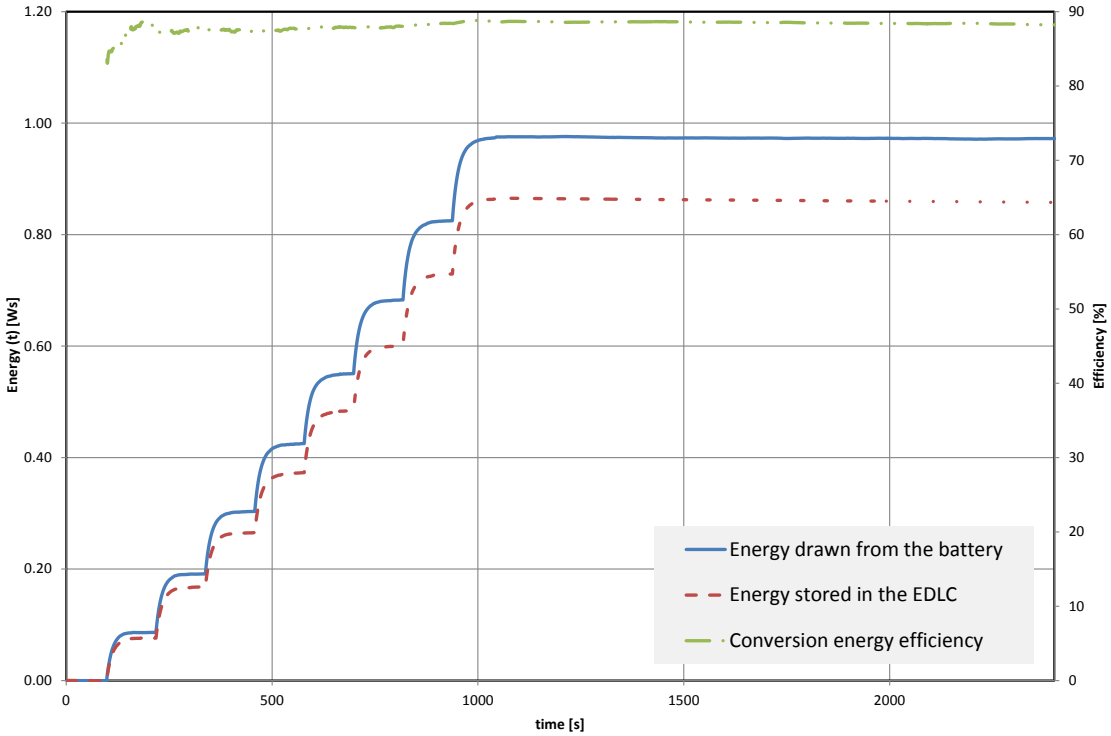


Figure 14: Energy conversion efficiency

4 Summary

Due to the characteristics of certain batteries, applications with ultra-long runtimes need new concepts for buffering energy.

Using an EDLC in combination the TPS62740 brings following main advantages:

- Single Cell Super Capacitor with a maximum voltage of below 3V can be used
- Storage Capacitors like muRata DMF series enable an application runtime of >15 years.
- Pulsed currents are decupled from batteries leading to more extractable energy
- Application runtimes are extended because of the high efficiency of the solution

The charging sequence can be implemented efficiently due to the digital output voltage selection feature of TPS62740.
This Buck Converter is designed to operate with a quiescent current of typical 360nA and is ideal for a direct connection to the battery and ultra-long runtimes.
Applications like a wireless sensor node can use the existing µController to handle the charging sequence of the EDLC.

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