TI Designs

Xilinx Virtex UltraScale MGT Power Supplies (PMP9408)

System Description

This TI Design demonstrates a proven design for the Multi-Gigabit Transceiver (MGT) power supply rails on the Xilinx Virtex UltraScale platform. It features +1.0V/24A output for the MGTAVCC, +1.2V/10A output for the MGTAVTT, and +1.8V/4A output for the MGTVCCAUX rails. This design is powered from a +5V input voltage and also provides power-up and power-down sequencing. This design aims for a controller + external FET solution to lower costs vs. an integrated solution.

Featured Applications

- FPGA

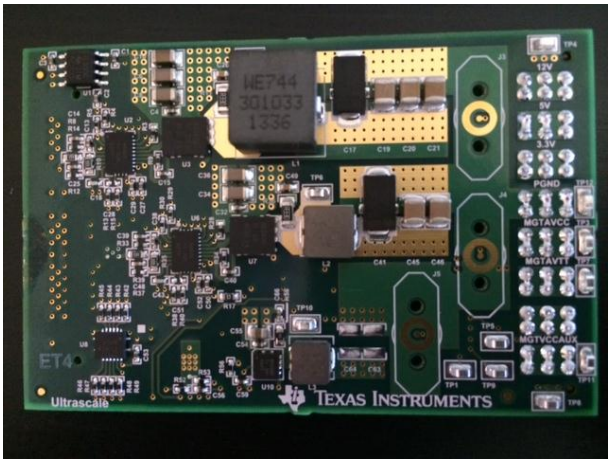
Design Resources

- Block Diagram and Schematic
- Test Data
- Gerber Files
- Design Files
- Bill of Materials

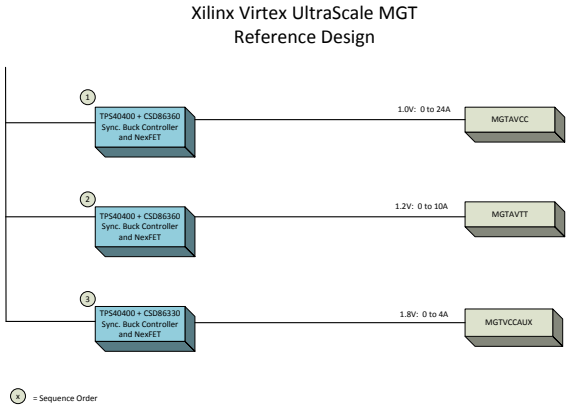
Design Features

- 5V Input Voltage
- Full power solution for MGT rails
  - +1.0V/24A MGTAVCC
  - +1.2V/10A MGTAVTT
  - +1.8V/4A MGTVCCAUX
- Power-up and power-down sequencing
- PMBUS compatible interface
- Selectable PMBUS address

Design Photo



Block Diagram



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Associated Part Numbers

Part Number	Part Description
TPS40400	Synchronous buck controller that operates from a nominal 3V to 20V supply. It is an analog PWM controller that allows programming and monitoring via the PMBus interface.
CSD86360Q5D	Synchronous buck NexFET power block MOSFET pair designed for applications offering high current, efficiency, and frequency capability with a 5V gate drive.
CSD86330Q3D	Synchronous buck NexFET power block MOSFET pair designed for applications offering high current, efficiency, and frequency capability with a 5V gate drive.
LM3880	Power sequencer that can control power up and power down of multiple power supplies using a precision enable pin and three output flags.
TS3A5017RGY	Dual single-pole quadruple-throw (4:1) analog switch designed to operate from 2.3 to 3.6V. This device can handle both digital and analog signals.

Design Considerations:

This design goal is to provide a power supply module to power MGT rails (MGTAVCC, MGTAVTT, MGTVCCAUX) on a Xilinx Virtex UltraScale platform and meet the current and voltage requirements. The solution is meant to fit into a 1.95" x 3.00" form factor and include all MGT rails and plug into a customer host characterization platform through mating connectors on the bottom layer. PMBUS, telemetry, sequencing, and low noise were all a requirement for this application.

MGTAVCC – The MGTAVCC rail required +1.0V/24A with +/-10mV output ripple and 3% tolerance on load transients.

1) TPS40400 was chosen since it's a voltage mode controller for lower output noise and also because of it's PMBUS and telemetry features. CSD86360 was chosen because of it's low Rdson and current ratings.

MGTAVTT – The MGTAVTT rail required +1.2V/10A with +/-10mV output ripple and 3% tolerance on load transients.

2) TPS40400 was chosen since it's a voltage mode controller for lower output noise and also because of it's PMBUS and telemetry features. CSD86360 was chosen because of it's low Rdson and current ratings.

MGTVCCAUX – The MGTVCCAUX rail required +1.8V/4A with +/-10mV output ripple and 3% tolerance on load transients.

3) TPS40400 was chosen since it's a voltage mode controller for lower output noise and also because of it's PMBUS and telemetry features. CSD86330 was chosen because of it's smaller 3mm x 3mm size, low Rdson, and current ratings.

Sequencing – Power-up and power-down sequencing was a requirement for this design.

1) A LM3880 was selected to provide 1-2-3 power-up and 3-2-1 power down sequencing.

PMBUS Address Selection – The TSA3A501RGY is a SP4T switch that gives four different options for PMBUS address for each of the rails. By configuring ALT_PMBUS_ADDR0 and ALT_PMBUS_ADDR1, the user can select between each of the four addresses.

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