Low noise linear regulator + DC/DC solution with excellent transient response

Test Report

1.1 Power Up

Power up testing was done with a dual output supply with a single output enable and is shown in Figure 1. The 5.0 V DC/DC rail (blue) powered up first followed by the 1.8 V rail LDO supply voltage (green). Power up testing was conducted at full load with the 1.5 V LDO loaded with a 0.5 Ω resistor and the 1.2V DC/DC output loaded with a 0.4 Ω resistor.

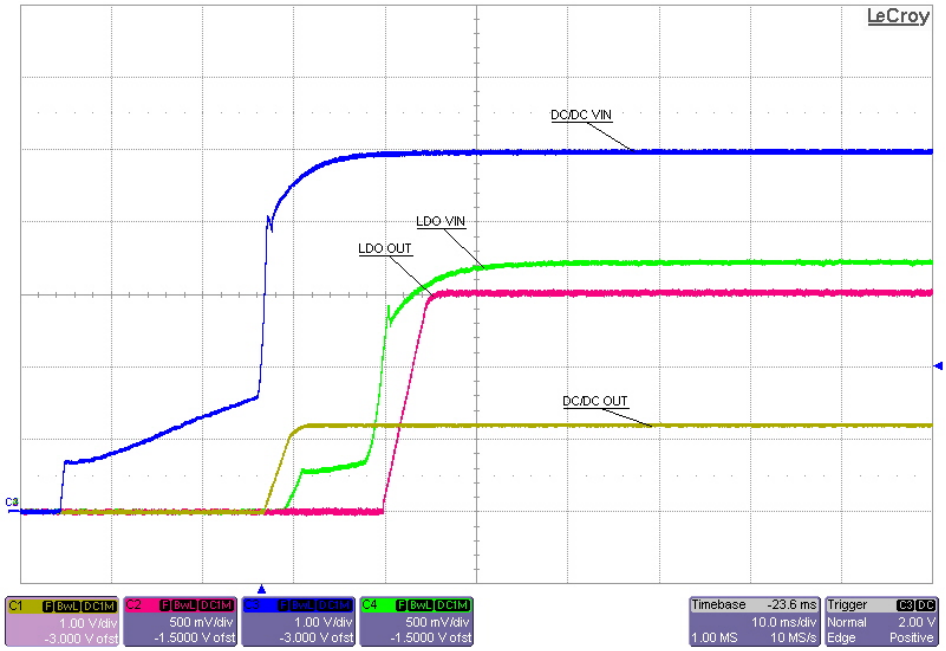

Figure 1. System Power Up

Even though the input supplies were not ideally behaved, the output voltages for both the DC/DC and LDO powered up in the correct sequence and exhibited a monotonic startup. The enable pin of the LDO was connected to the Power Good signal from the DC/DC so that the LDO would power up after the DC/DC even if the input supply sequence were reversed. The TPS54122 allows for the startup ramp rate of the DC/DC and LDO to be set independently by adjusting the external soft-start capacitor accordingly. For this design the startup time was set to approximately 5ms for both the 1.2 V DC/DC and 1.5 V LDO.

1.2 Power Down

The power down waveform was generated by disabling the input supply and is shown in Figure 2.

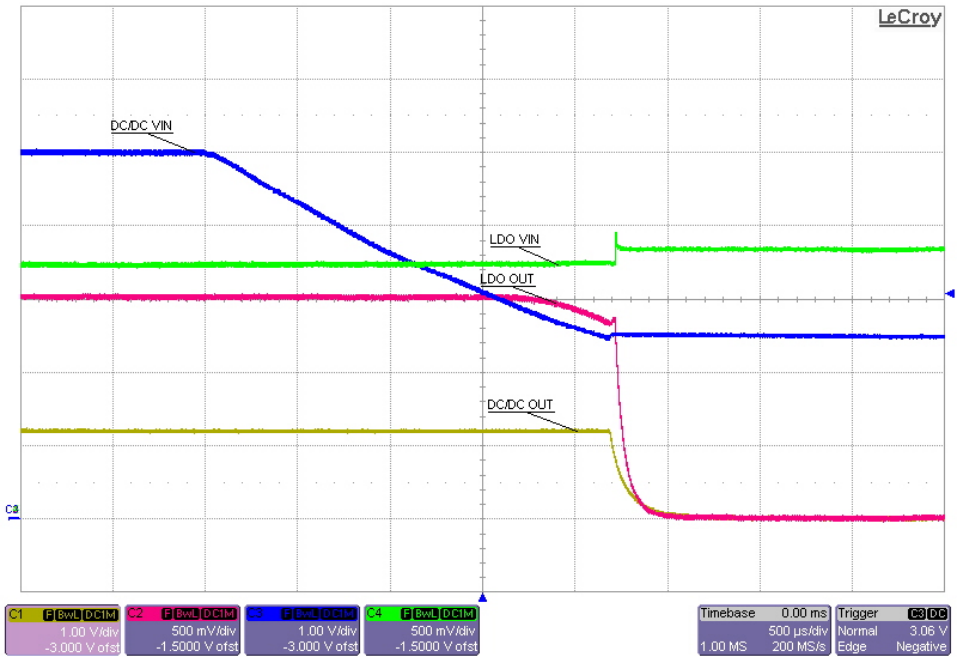

Figure 2. Power-Down behavior

The 5 V input to the DC/DC collapses first causing the DC/DC to turn off. When this occurs the DC/DC power good signal goes low disabling the LDO. On power down the LDO output starts to drop even when the DC/DC output is still functional. This droop in the LDO output occurs because the bias supply for the LDO is powered from the 5 V DC/DC input. As the 5 V supply starts to drop the LDO will enter bias supply dropout causing the output voltage to droop.

1.3 DC/DC Efficiency

Efficiency of the DC/DC convertor is shown in Figure 3. This efficiency curve was taken with a snubber RC circuit on the switch node. Slightly higher efficiency can be achieved without the snubber network provided switch node ringing is not a concern.

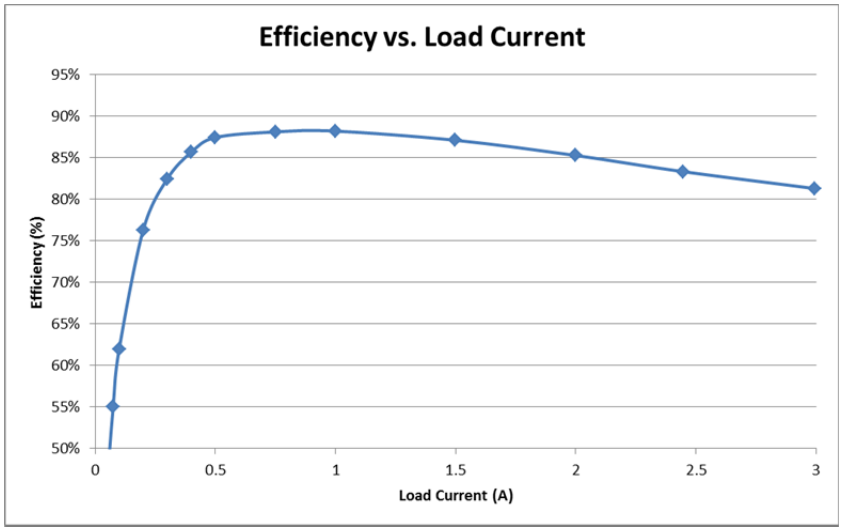

Figure 3. 1.2V DC/DC Output Efficiency

1.4 DC/DC Load Transient Response

The 1.2 V DC/DC output voltage transient response was tested with a load step of 300 mA to 3 A and is shown in Figure 4. The slew rate on the load step is approximately 1 A/µs.

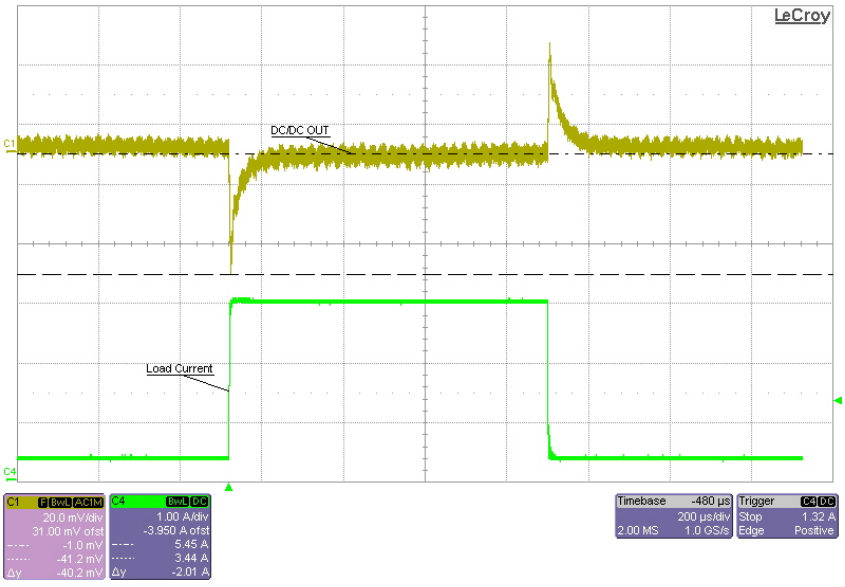

Figure 4. 1.2 V DC/DC Output Transient Response

The transient droop on the 1.2 V rail was approximately 40 mV or 3.33% of VOUT.

1.5 DC/DC Output Ripple and Switch Node

Both the output ripple and switch node waveforms are shown in Figure 5. The output ripple was measured with a scope probe GND adapter to minimize pick up of high frequency spikes that can otherwise be seen with improper grounding techniques.

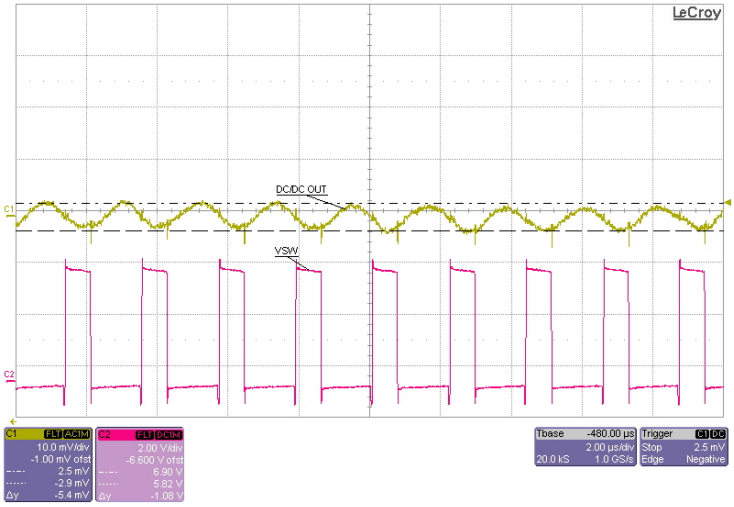

Figure 5. Output ripple and switch node.

The peak to peak ripple amplitude was measured to be approximately 5.5 mV. A snubber circuit on the switch node to VIN was used to minimize and switch node ringing that might be radiated to the output scope probe.

1.6 DC/DC Loop Gain

The loop gain(blue) and phase(red) are shown in Figure 6. The phase margin can be found by looking at the phase when the loop gain is equal to zero.

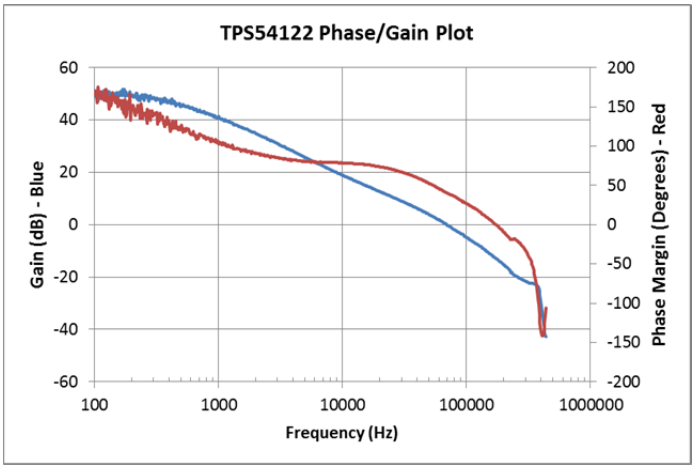

Figure 6. Loop gain and phase

For this design the higher phase margin was sacrificed to achieve a higher crossover frequency. The phase margin was measured to be 40 degrees with a crossover frequency of 69 kHz.

1.7 LDO Power Supply Ripple Rejection

Power supply ripple rejection measurements were taken on the LDO with VIN = 1.8 V and VOUT = 1.5 V. Data on PSRR was taken at both 3 A and 0.5 A and is shown in Figure 7.

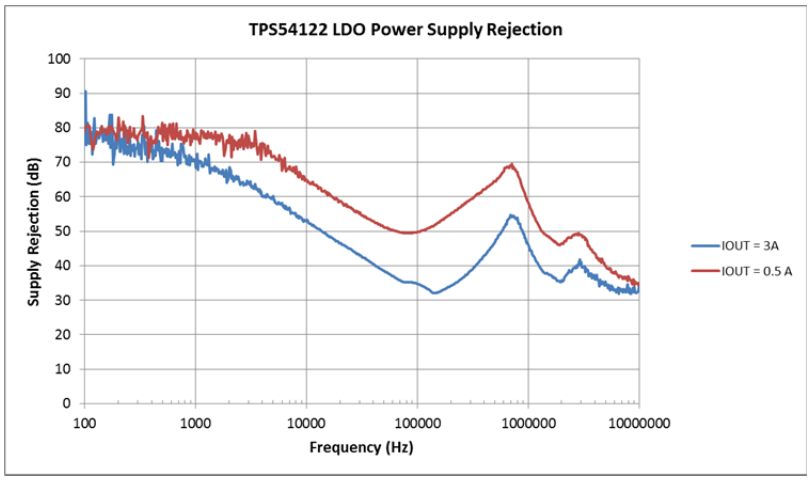

Figure 7. Power Supply Ripple Rejection

The output capacitors were selected to have a low impedance point at the switching frequency to achieve this highest ripple rejection. The two peaks in the PSRR curve occurring at 700 kHz and 2.8 MHz are due to the 47 μF and 10 μF output capacitors.

1.8 LDO Output Noise

Figure 8 shows the output spectral noise density of the LDO with the DC/DC convertor in operation.

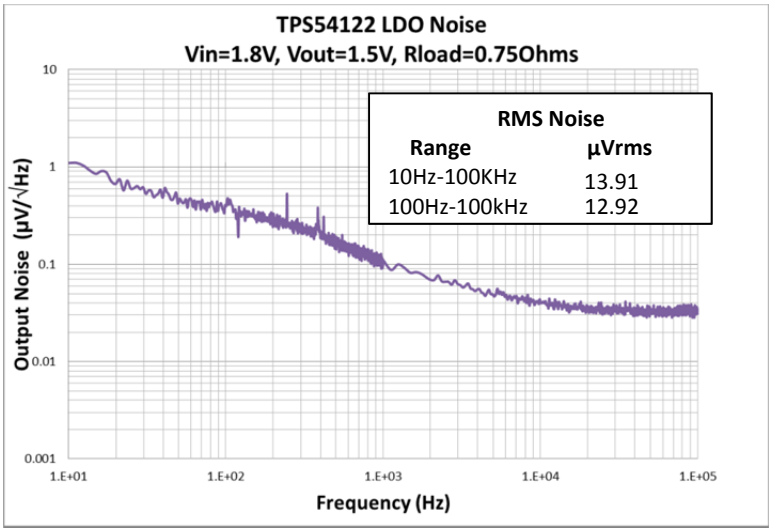

Figure 8. Output Spectral Noise Density (10 Hz to 100 kHz)

The RMS noise can be calculated from figure 8, yielding a noise of 14 μVRMS over the frequency range of 10 Hz to 100 kHz.

1.9 LDO Transient Response

The LDO transient response was measured with VIN = 1.8 V and VOUT = 1.5 V. The slew rate of the load step was approximately 1 A/μs. Since the input voltage is close to the output voltage a stiff input supply with good transient characteristics was used for this scope shot to avoid input supply transient droop affecting the LDO output transient response.

Figure 9. LDO transient response

As shown in Figure 9. , the LDO transient response droop was measured to be approximately 40 mV or 2.7% of VOUT.

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